FAIRCHILD SEMICONDUCTOR™

September 1986
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DM74ALS74A
Dual D Positive-Edge-Triggered Flip-Flop with Preset and Clear

General Description

The DM74ALS74A contains two independent positive edge-triggered flip-flops. Each flip-flop has individual D, clock, clear and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input D is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the HIGH or LOW level, the D input signal has no effect.

Asynchronous preset and clear inputs will set or clear Q output respectively upon the application of low level signal.

Features

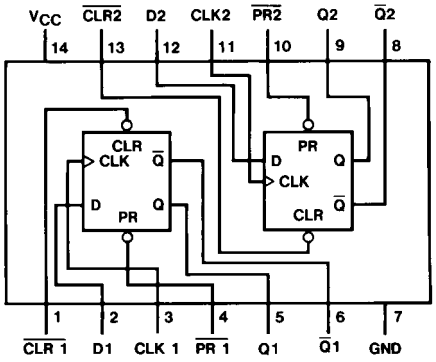
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and LS TTL counterpart
- Improved AC performance over LS74 at approximately half the power

Ordering Code:

Order Number	Package Number	Package Description
DM74ALS74AM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74ALS74ASJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74ALS74AN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

Inputs				Outputs	
$\overline{PR}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 1)	H (Note 1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

L = LOW State
H = HIGH State
X = Don't Care
↑ = Positive Edge Transition
Q_0 = Previous Condition of Q

Note 1: This condition is nonstable; it will not persist when preset and clear inputs return to their inactive (HIGH) level. The output levels in this condition are not guaranteed to meet the V_{OH} specification.

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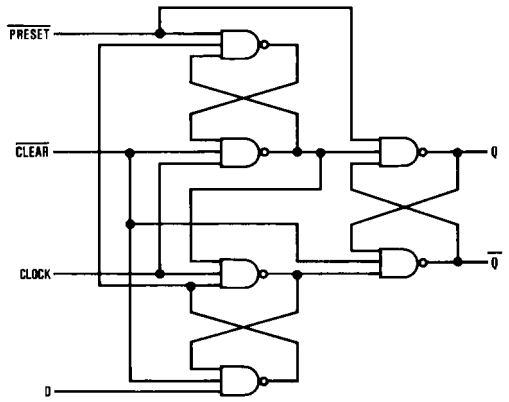
Logic Diagram



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Absolute Maximum Ratings(Note 2)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Typical θ_{JA}	
N Package	87.0°C/W
M Package	117.0°C/W

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	HIGH Level Input Voltage		2			V
V_{IL}	LOW Level Input Voltage				0.8	V
I_{OH}	HIGH Level Output Current				−0.4	mA
I_{OL}	LOW Level Output Current				8	mA
f_{CLK}	Clock Frequency		0		34	MHz
$t_{W(CLK)}$	Width of Clock Pulse	HIGH	14.5			ns
		LOW	14.5			ns
t_W	Pulse Width Preset & Clear	LOW	14.5			ns
t_{SU}	Data Setup Time	Data	15↑ (Note 3)			ns
		PRE or CLR Inactive	10↑ (Note 3)			
t_H	Data Hold Time		0↑ (Note 3)			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 3: The (↑) arrow indicates the positive edge of the Clock is used for reference.

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Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = −0.4 mA V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	LOW Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V	Clock, D			0.1	mA
			Preset, Clear			0.2	
I_{IH}	HIGH Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V	Clock, D			20	µA
			Preset, Clear			40	
I_{IL}	LOW Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V	Clock, D			−0.2	mA
			Preset, Clear (Note 5)			−0.4	
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V (Note 4)			2.4	4	mA

Note 4: I_{CC} is measured with D, CLK and PRESET grounded, then with D, CLK and CLEAR grounded.

Note 5: I_{IL} PRE and CLR pins not guaranteed to meet specifications with both PRE and CLK LOW.

Switching Characteristics

over recommended operating free air temperature range.

Parameter	Conditions	From	To	Min	Max	Units
f_{MAX}	V_{CC} = 4.5V to 5.5V			34		MHz
t_{PLH}	R_L = 500Ω	$\overline{\text{Preset}}$ or $\overline{\text{Clear}}$	Q or $\overline{Q}$	3	13	ns
t_{PHL}	C_L = 50 pF			5	15	ns
t_{PLH}		Clock	Q or $\overline{Q}$	5	16	ns
t_{PHL}				5	18	ns

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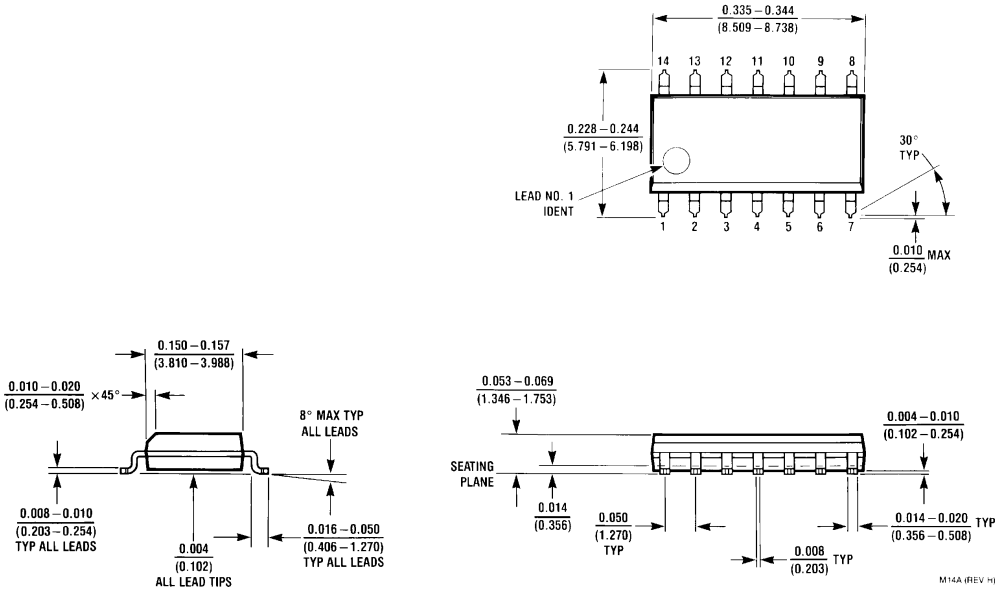
Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M14A

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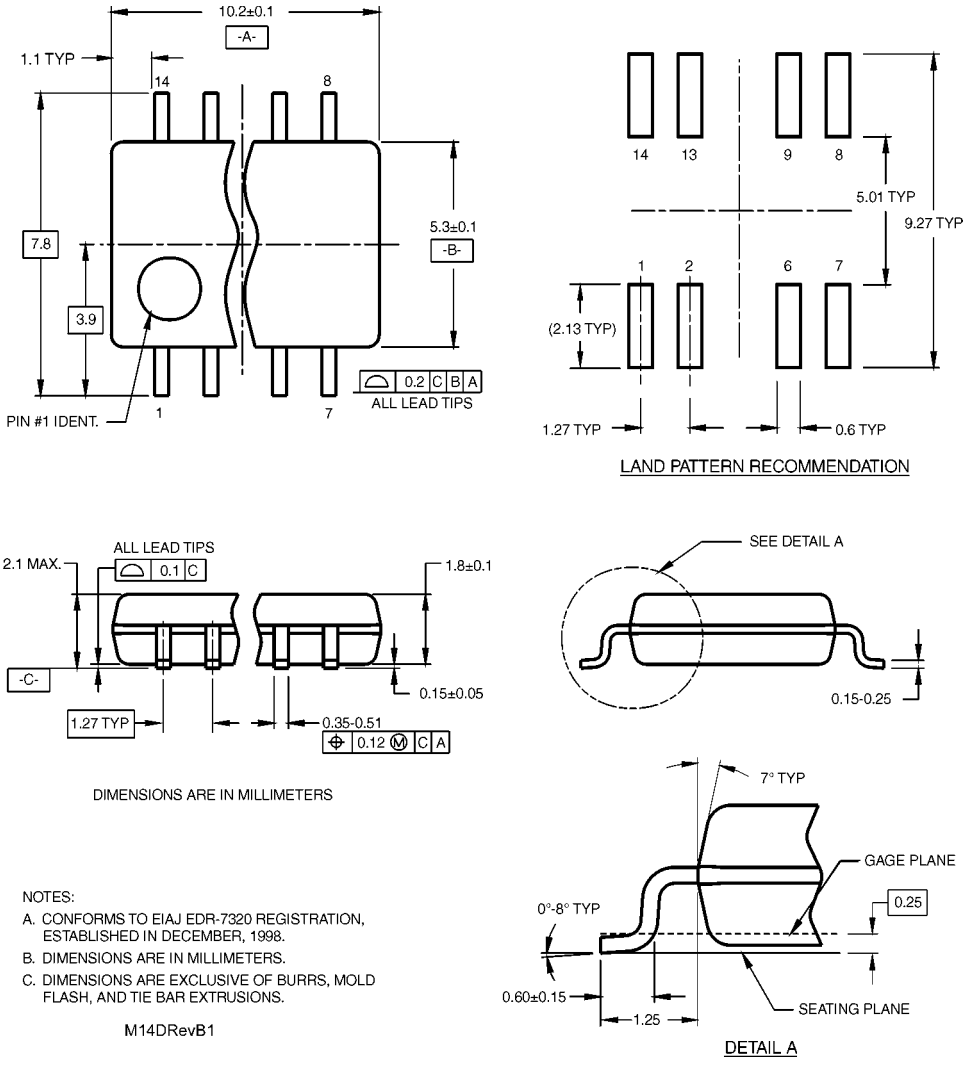
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

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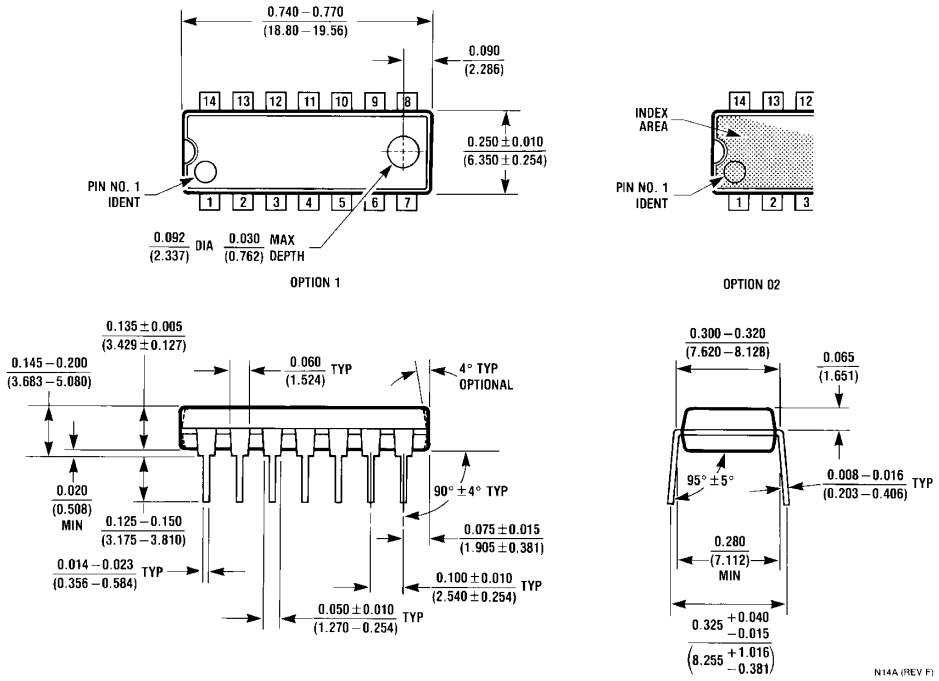
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

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