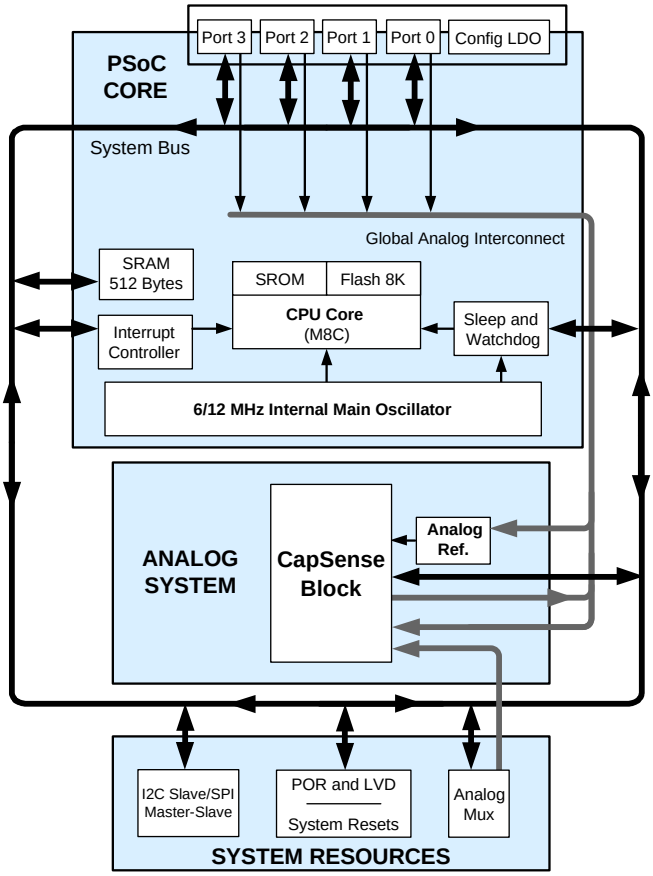
CY8C20234

Automotive PSoC® Programmable System-on-Chip

Features

- Automotive Electronics Council (AEC) Q100 qualified
- Low power CapSense® block
  - Configurable capacitive sensing elements
  - Supports combination of CapSense buttons, sliders, touch-pads, and proximity sensors
- Powerful Harvard-architecture processor
  - M8C processor speeds up to 12 MHz
  - Low power at high speed
  - Operating voltage: 3.0 V to 5.25 V
  - Automotive temperature range: –40 °C to +85 °C
- Flexible on-chip memory
  - 8 KB of flash program storage, 1000 erase/write cycles
  - 512 bytes of SRAM data storage
  - Partial flash updates
  - Flexible protection modes
  - In-system serial programming (ISSP)
- Complete development tools
  - Free development tool (PSoC Designer™)
  - Full featured, in-circuit emulator (ICE) and programmer
  - Full-speed emulation
  - Complex breakpoint structure
  - 128 KB trace memory
- Precision, programmable clocking
  - Internal ±5% 6-/12-MHz oscillator
  - Internal low-speed, low-power oscillator for watchdog and sleep functionality
- Programmable pin configurations
  - 20 mA sink on all general purpose I/Os (GPIOs)
  - Pull-up, high Z, open drain, or strong drive modes on all GPIOs
  - Up to 13 analog inputs on GPIOs
  - Configurable interrupt on all GPIOs
  - Selectable, regulated digital I/O on Port 1
    - 3.0 V, 2.4 V, and 1.8 V regulation available
    - Up to 5 mA source on Port 1 GPIOs
- Versatile analog mux
  - Common internal analog bus
  - Simultaneous connection of I/O combinations
  - Comparator noise immunity
- Additional system resources
  - Configurable communication speeds
    - I²C™ slave operation up to 400 kHz
    - SPI master or slave operation between 46.9 kHz and 12 MHz
  - Watchdog and sleep timers
  - Internal voltage reference
  - Integrated supervisory circuit

Logic Block Diagram



Contents

PSoC® Functional Overview

The PSoC family consists of many Programmable System-on-Chip with on-chip controller devices. These devices are designed to replace multiple traditional microcontroller unit (MCU)-based system components with one low cost single chip programmable component. A PSoC device includes configurable analog and digital blocks and programmable interconnect. This architecture enables the user to create customized peripheral configurations to match the requirements of each individual application. Additionally, a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The PSoC architecture for this device family, as shown in "Logic Block Diagram" on page 1, consists of three main areas: the PSoC core, the system resources, and the CapSense analog system. A common versatile bus enables connection between I/O and the analog system. Each CY8C20x34 PSoC device includes a dedicated CapSense block that provides sensing and scanning control circuitry for capacitive sensing applications. Depending on the PSoC package, up to 13 GPIOs are also included. The GPIOs provide access to the MCU and analog mux.

PSoC Core

The PSoC core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, internal main oscillator (IMO), and internal low-speed oscillator (ILO). The CPU core, called the M8C, is a powerful processor with speeds up to 12 MHz. The M8C is a two-MIPS, 8-bit Harvard-architecture microprocessor.

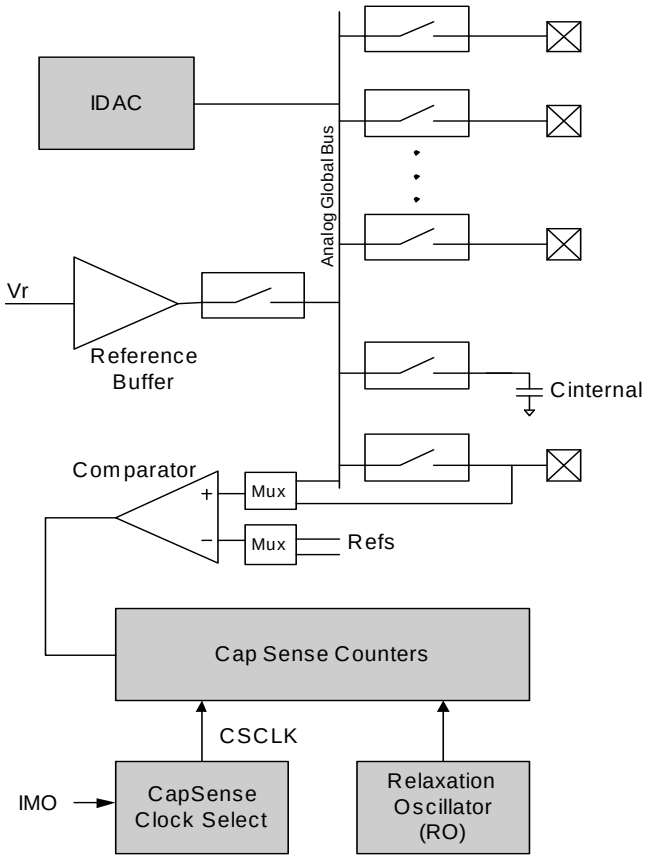
System resources provide additional capability such as a configurable I^2C slave, SPI slave, or SPI master communication interface and various system resets supported by the M8C.

The CapSense analog system consists of the CapSense® PSoC block and an internal analog reference. Together they support capacitive sensing of up to 13 inputs.

CapSense Analog System

The CapSense analog system contains the capacitive sensing hardware. Several hardware algorithms are supported. This hardware performs capacitive sensing and scanning without requiring external components. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled CapSense pins is completed quickly and easily across multiple ports.

Figure 1. Analog System Block Diagram



Analog Multiplexer System

The analog mux bus connects to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with the CapSense block comparator.

Switch control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Complex capacitive sensing interfaces such as sliders and touch pads
- Chip-wide mux that enables analog input from any I/O pin
- Crosspoint connection between any I/O pin combination

Additional System Resources

System resources provide additional capability useful for complete systems. Additional resources include low voltage detection (LVD) and power-on reset (POR). Brief statements describing the merits of each system resource are presented below.

- There is a digital module in CY8C20x34 devices that implements an I^2C slave, SPI slave, or SPI master interface.The I^2C slave mode provides 0 to 400 kHz communication over two wires. The SPI master and slave modes provide communication over three or four wires at frequencies of 46.9 kHz to 12 MHz (lower for a slower system clock).
- LVD interrupts signal the application of falling voltage levels, while the advanced POR circuit eliminates the need for a system supervisor.
- An internal voltage reference provides an absolute reference for capacitive sensing.
- The 3.0-V/2.4-V/1.8-V fixed output, low dropout regulator (LDO) provides regulation for I/Os. A register controlled bypass mode enables the user to disable the LDO.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, 4, or 0 digital blocks and 12, 6, 4, or 0 analog blocks. The following table lists the resources available for specific PSoC device groups. The device covered by this datasheet is shown in the highlighted row of the table.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66[1]	up to 64	4	16	up to 12	4	4	12	2 K	32 K
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4[2]	1 K	16 K
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K
CY8C24x94[1]	up to 56	1	4	up to 48	2	2	6	1 K	16 K
CY8C24x23A[1]	up to 24	1	4	up to 12	2	2	6	256	4 K
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K
CY8C22x45	up to 38	2	8	up to 38	0	4	6[2]	1 K	16 K
CY8C21x45	up to 24	1	4	up to 24	0	4	6[2]	512	8 K
CY8C21x34[1]	up to 28	1	4	up to 28	0	2	4[2]	512	8 K
CY8C21x23	up to 16	1	4	up to 8	0	2	4[2]	256	4 K
CY8C20x34[1]	up to 28	0	0	up to 28	0	0	3[2,3]	512	8 K
CY8C20xx6	up to 36	0	0	up to 36	0	0	3[2,3]	up to 2 K	up to 32 K

Notes
1. Automotive qualified devices available in this group.
2. Limited analog functionality.
3. Two analog blocks and one CapSense® block.

Getting Started

For in depth information, along with detailed programming details, see the *PSoC® Technical Reference Manual*.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Development Tools

PSoC Designer™ is the revolutionary Integrated Design Environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of pre-characterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This pre-populates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for a given application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality In-Circuit Emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24-MHz) operation.

Designing with PSoC Designer

The development process for the PSoC® device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is summarized in four steps:

1. Select User Modules.
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a pulse width modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Pinouts

This section describes, lists, and illustrates the automotive CY8C20x34 PSoC device pins and pinout configurations.

The automotive CY8C20x34 PSoC device is available in the packages listed and shown in the following tables. Every port pin (labeled with a “P”) is capable of digital I/O and can connect to the common analog bus. However, V_{SS}, V_{DD}, and XRES are not capable of digital I/O.

16-Pin Part Pinout

Figure 2. CY8C20234 16-Pin PSoC Device

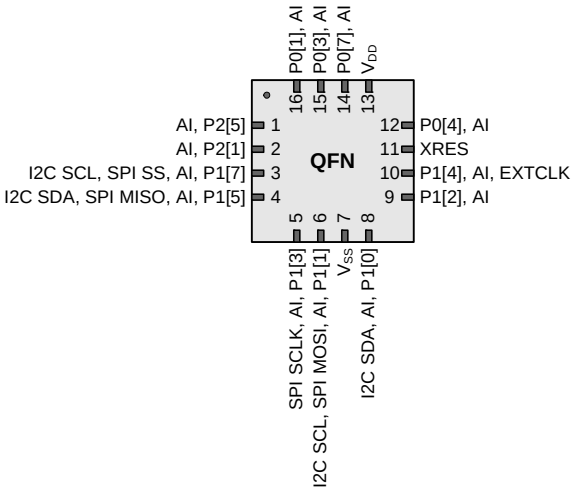


Table 2. Pin Definitions – CY8C20234 16-Pin (QFN)

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	
2	I/O	I	P2[1]	
3	I/OH	I	P1[7]	I^2C serial clock (SCL), SPI slave select (SS)
4	I/OH	I	P1[5]	I^2C serial data (SDA), SPI master-in-slave-out (MISO)
5	I/OH	I	P1[3]	SPI serial clock (SCLK)
6	I/OH	I	P1[1]	ISSP-SCLK[4], I^2C serial clock (SCL), SPI master-out-slave-in (MOSI)
7	Power		V_{SS}	Ground connection
8	I/OH	I	P1[0]	ISSP-SDATA[4], I^2C serial data (SDA)
9	I/OH	I	P1[2]	
10	I/OH	I	P1[4]	Optional external clock (EXTCLK) input
11	Input		XRES	Active high external reset with internal pull-down
12	I/O	I	P0[4]	
13	Power		V_{DD}	Supply voltage
14	I/O	I	P0[7]	
15	I/O	I	P0[3]	Integrating input
16	I/O	I	P0[1]	

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive

Note
4. These are the ISSP pins, that are not High Z after exiting a reset state. See the *PSoC Technical Reference Manual* for CY8C20x34 devices for details.

Electrical Specifications

This section presents the DC and AC electrical specifications of the automotive CY8C20x34 PSoC device. For the latest electrical specifications, check the most recent data sheet by visiting the web at http://www.cypress.com.

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100°C as specified, except where mentioned.

Refer to Table 11 on page 14 for the electrical specifications on the IMO using SLIMO mode.

Figure 3. Voltage versus CPU Frequency

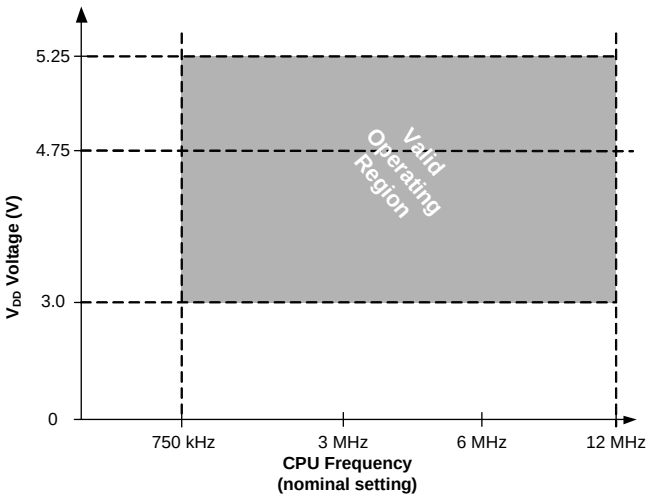
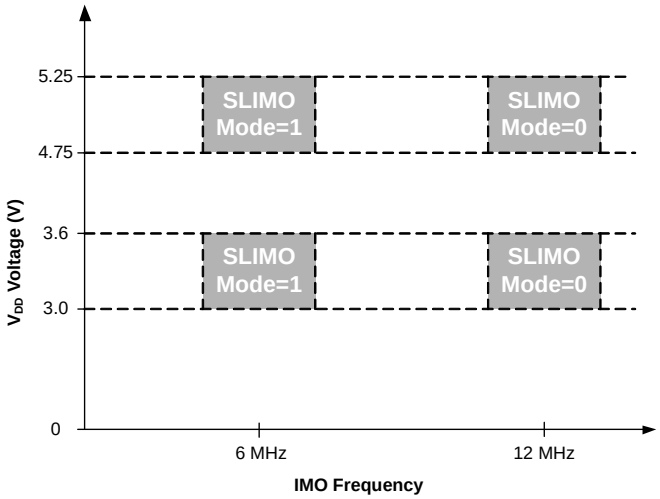


Figure 4. IMO Frequency Trim Options



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 3. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage temperature	-55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Time spent in storage at a temperature greater than 65 °C counts toward the $Flash_{DR}$ electrical specification in Table 10 on page 13.
$T_{BAKETEMP}$	Bake temperature	–	125	See package label	°C	
$t_{BAKETIME}$	Bake time	See package label	–	72	Hours	
T_A	Ambient temperature with power applied	–40	–	+85	°C	
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
V_{IOZ}	DC voltage applied to tri-state	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any port pin	–25	–	+50	mA	
ESD	Electrostatic discharge voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch-up current	–	–	200	mA	

Operating Temperature

Table 4. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient temperature	–40	–	+85	°C	
T_J	Junction temperature	–40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Table 19 on page 18. The user must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip Level Specifications

Table 5 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C. These are for design guidance only.

Table 5. DC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DD}	Supply voltage	3.0	–	5.25	V	See Table 8 on page 12.
I_{DD12}	Supply current, IMO = 12 MHz	–	1.5	2.5	mA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 12 MHz.
I_{DD6}	Supply current, IMO = 6 MHz	–	1	1.5	mA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 6 MHz
I_{SB}	Sleep (mode) current with POR, LVD, sleep timer, WDT, and ILO active.	–	2.8	5	µA	V_{DD} = 3.3 V, –40 °C ≤ T_A ≤ 85 °C

DC GPIO Specifications

Table 6 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C. These are for design guidance only.

Table 6. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
R_{PD}	Internal pull-down resistor on XRES pin	4	5.6	8	kΩ	
V_{OH1}	High output voltage Port 0, 2, or 3 pins	V_{DD} – 0.2	–	–	V	I_{OH} ≤ 10 µA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH2}	High output voltage Port 0, 2, or 3 pins	V_{DD} – 0.9	–	–	V	I_{OH} ≤ 1 mA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH3}	High output voltage Port 1 pins with LDO disabled	V_{DD} – 0.2	–	–	V	I_{OH} ≤ 10 µA, V_{DD} ≥ 3.0 V, maximum of 10 mA source current in all I/Os.
V_{OH4}	High output voltage Port 1 pins with LDO disabled	V_{DD} – 0.9	–	–	V	I_{OH} ≤ 5 mA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH5}	High output voltage Port 1 pins with 3.0-V LDO enabled	2.7	3.0	3.3	V	I_{OH} ≤ 10 µA, V_{DD} ≥ 3.1 V, maximum of 4 I/Os all sourcing 5 mA.
V_{OH6}	High output voltage Port 1 pins with 3.0-V LDO enabled	2.2	–	–	V	I_{OH} ≤ 5 mA, V_{DD} ≥ 3.1 V, maximum of 20 mA source current in all I/Os.
V_{OH7}	High output voltage Port 1 pins with 2.4-V LDO enabled	2.1	2.4	2.7	V	I_{OH} ≤ 10 µA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH8}	High output voltage Port 1 pins with 2.4-V LDO enabled	2.0	–	–	V	I_{OH} ≤ 200 µA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH9}	High output voltage Port 1 pins with 1.8-V LDO enabled	1.6	1.8	2.0	V	I_{OH} ≤ 10 µA 3.0 V ≤ V_{DD} ≤ 3.6 V 0°C ≤ T_A ≤ 85 °C Maximum of 20 mA source current in all I/Os.
V_{OH10}	High output voltage Port 1 pins with 1.8-V LDO enabled	1.5	–	–	V	I_{OH} ≤ 100 µA. 3.0 V ≤ V_{DD} ≤ 3.6 V. 0°C ≤ T_A ≤ 85 °C. Maximum of 20 mA source current in all I/Os.

Table 6. DC GPIO Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OL}	Low output voltage	–	–	0.75	V	$I_{OL} \le 20$ mA, $V_{DD} \ge 3.0$ V, maximum of 60 mA sink current on even port pins (for example, P0[4] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5]).
V_{IL}	Input low voltage	–	–	0.8	V	
V_{IH}	Input high voltage	2.0	–		V	
V_H	Input hysteresis voltage	–	140	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 μA
C_{IN}	Capacitive load on pins as input	0.5	1.7	5	pF	Package and pin dependent T_A = 25 °C
C_{OUT}	Capacitive load on pins as output	0.5	1.7	5	pF	Package and pin dependent T_A = 25 °C

DC Analog Mux Bus Specifications

Table 7 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C. These are for design guidance only.

Table 7. DC Analog Mux Bus Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{SW}	Switch resistance to common analog bus	–	–	450	Ω	

DC POR and LVD Specifications

Table 8 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C. These are for design guidance only.

Table 8. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} value for PPOR trip					V_{DD} must be greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from watchdog.
V_{PPOR0}	PORLEV[1:0] = 00b	–	2.36	2.40	V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	2.60	2.65	V	
V_{PPOR2}	PORLEV[1:0] = 10b	–	2.82	2.95	V	
	V_{DD} value for LVD trip					
V_{LVD0}	VM[2:0] = 000b	2.34	2.45	2.51[5]	V	
V_{LVD1}	VM[2:0] = 001b	2.54	2.71	2.78[6]	V	
V_{LVD2}	VM[2:0] = 010b	2.75	2.92	2.99[7]	V	
V_{LVD3}	VM[2:0] = 011b	2.85	3.02	3.09	V	
V_{LVD4}	VM[2:0] = 100b	2.96	3.13	3.20	V	
V_{LVD5}	VM[2:0] = 101b	–	–	–	V	
V_{LVD6}	VM[2:0] = 110b	–	–	–	V	
V_{LVD7}	VM[2:0] = 111b	4.44	4.73	4.93	V	

Notes
5. Always greater than 50 mV above V_{PPOR} (PORLEV = 00) for falling supply.
6. Always greater than 50 mV above V_{PPOR} (PORLEV = 01) for falling supply.
7. Always greater than 50 mV above V_{PPOR} (PORLEV = 10) for falling supply.

DC Analog Reference Specifications

Table 9 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C. These are for design guidance only.

Table 9. DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
BG	Bandgap reference voltage	1.274	1.30	1.326	V	

DC Programming Specifications

Table 10 lists the guaranteed minimum and maximum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C. These are for design guidance only. Flash Endurance and Retention specifications with the use of the EEPROM User Module are valid only within the range: 25 °C ± 20 °C during the Flash Write operation. Refer to the EEPROM User Module data sheet instructions for EEPROM Flash Write requirements outside of the 25 °C ± 20 °C temperature window.

Table 10. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify	3.0	3.1	3.2	V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operation	3.0	–	5.25	V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply current during programming or verify	–	5	25	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.2	–	–	V	
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output low voltage during programming or verify	–	–	0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash endurance (per block)[8]	1,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash endurance (total)[9]	128,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash data retention	10	–	–	Years	

Notes
8. The erase/write cycle limit per block ($Flash_{ENPB}$) is only guaranteed if the device operates within one voltage range. Voltage ranges are 3.0 V to 3.6 V and 4.75 V to 5.25 V.
9. The maximum total number of allowed erase/write cycles is the minimum $Flash_{ENPB}$ value multiplied by the number of flash blocks in the device.

AC Electrical Characteristics

AC Chip Level Specifications

Table 11 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C. These are for design guidance only.

Table 11. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{CPU1}	CPU frequency	0.71	–	12.6	MHz	12 MHz only for SLIMO Mode = 0
F_{32K1}	ILO frequency	15	32	64	kHz	This specification applies when the ILO has been trimmed.
F_{32KU}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C processor starts to execute, the ILO is not trimmed.
F_{IMO12}	IMO frequency for 12 MHz	11.4	12	12.6	MHz	Trimmed using factory trim values. See Figure 4 on page 9, SLIMO Mode = 0.
F_{IMO6}	IMO frequency for 6 MHz	5.5	6.0	6.5	MHz	Trimmed using factory trim values. See Figure 4 on page 9, SLIMO Mode = 1.
DC_{IMO}	IMO duty cycle	40	50	60	%	
DC_{ILO}	ILO duty cycle	20	50	80	%	
t_{XRST}	External reset pulse width	10	–	–	µs	
$SR_{POWERUP}$	Power supply slew rate	–	–	250	V/ms	V_{DD} slew rate during power-up.
$t_{POWERUP}$	Time between end of POR state and CPU code execution	–	16	100	ms	Power-up from 0 V.
t_{JIT_IMO} [10]	12 MHz IMO cycle-to-cycle jitter (RMS)	–	200	1600	ps	
	12 MHz IMO long-term N cycle-to-cycle jitter (RMS)	–	600	1400	ps	N = 32
	12 MHz IMO period jitter (RMS)	–	100	900	ps	

Note
10. Refer to Cypress Jitter Specifications Application Note – AN5054 at http://www.cypress.com for more information.

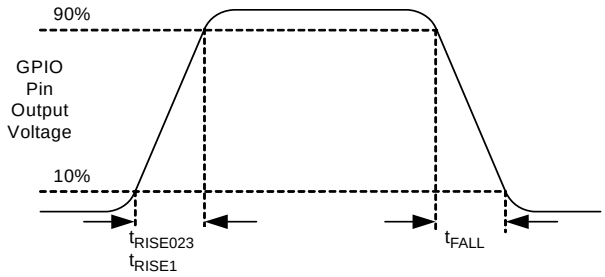
AC GPIO Specifications

Table 12 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C. These are for design guidance only.

Table 12. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	6.30	MHz	Normal strong mode, Port 1.
$t_{RISE023}$	Rise time, strong mode, Cload = 50 pF Ports 0, 2, 3	15	–	80	ns	V_{DD} = 3.0 V to 3.6 V and 4.75 V to 5.25 V, 10% - 90%
t_{RISE1}	Rise time, strong mode, Cload = 50 pF Port 1	10	–	50	ns	V_{DD} = 3.0 V to 3.6 V, 10% - 90%
t_{FALL}	Fall time, strong mode, Cload = 50 pF all Ports	10	–	50	ns	V_{DD} = 3.0 V to 3.6 V and 4.75 V to 5.25 V, 10% - 90%

Figure 5. GPIO Timing Diagram



AC Comparator Specifications

Table 13 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C. These are for design guidance only.

Table 13. AC Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{COMP}	Comparator response time, 50 mV overdrive	– –	– –	100 200	ns ns	V_{DD} > 3.6 V 3.0 V ≤ V_{DD} ≤ 3.6 V

AC External Clock Specifications

Table 14 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40°C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C. These are for design guidance only.

Table 14. AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.750	–	12.6	MHz	
–	High period	38	–	5300	ns	
–	Low period	38	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

AC Programming Specifications

Table 15 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40°C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C. These are for design guidance only.

Table 15. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RSCLK}	Rise time of SCLK	1	–	20	ns	
t_{FSCLK}	Fall time of SCLK	1	–	20	ns	
t_{SSCLK}	Data setup time to falling edge of SCLK	40	–	–	ns	
t_{HSCLK}	Data hold time from falling edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
t_{ERASEB}	Flash erase time (block)	–	10	40	ms	
t_{WRITE}	Flash block write time	–	40	160	ms	
t_{DSCLK}	Data out delay from falling edge of SCLK	–	–	45	ns	V_{DD} > 3.6 V
t_{DSCLK3}	Data out delay from falling edge of SCLK	–	–	50	ns	3.0 V ≤ V_{DD} ≤ 3.6 V
t_{PRGH}	Total flash block program time (t_{ERASEB} + t_{WRITE}), hot	–	–	100	ms	T_J ≥ 0 °C
t_{PRGC}	Total flash block program time (t_{ERASEB} + t_{WRITE}), cold	–	–	200	ms	T_J < 0 °C

AC SPI Specifications

Table 16 and Table 17 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C. These are for design guidance only.

Table 16. SPI Master AC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes
F_{SCLK}	SCLK clock frequency	–	–	12.6	MHz	
DC_{SCLK}	SCLK duty cycle	–	50	–	%	
t_{SETUP}	MISO to SCLK setup time	40	–	–	ns	
t_{HOLD}	SCLK to MISO hold time	40	–	–	ns	
t_{OUT_VAL}	SCLK to MOSI valid time	–	–	40	ns	
t_{OUT_H}	MOSI high time	40	–	–	ns	

Table 17. SPI Slave AC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes
F_{SCLK}	SCLK clock frequency	–	–	4	MHz	
t_{LOW}	SCLK low time	39.6	–	–	ns	
t_{HIGH}	SCLK high time	39.6	–	–	ns	
t_{SETUP}	MOSI to SCLK setup time	30	–	–	ns	
t_{HOLD}	SCLK to MOSI hold time	50	–	–	ns	
t_{SS_MISO}	SS low to MISO valid	–	–	153	ns	
t_{SCLK_MISO}	SCLK to MISO valid	–	–	125	ns	
t_{SS_HIGH}	SS high time	50	–	–	ns	
t_{SS_SCLK}	Time from SS low to first SCLK	$2/F_{SCLK}$	–	–	ns	
t_{SCLK_SS}	Time from last SCLK to SS high	$2/F_{SCLK}$	–	–	ns	

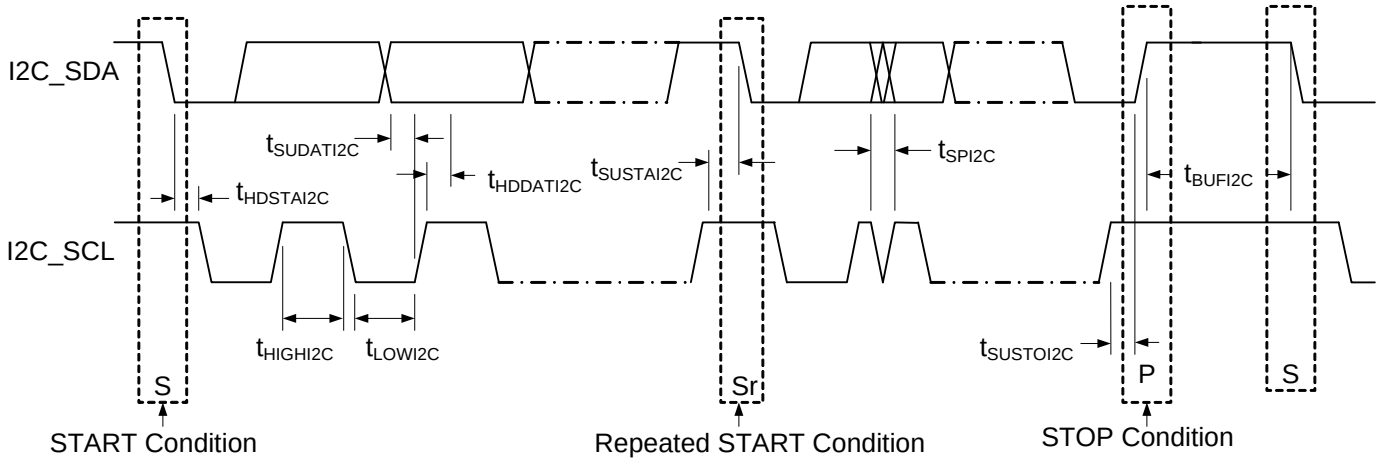
AC I²C Specifications

Table 18 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V or 3.3 V at 25 °C. These are for design guidance only.

Table 18. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL clock frequency	0	100[11]	0	400[11]	kHz
$t_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	–	0.6	–	µs
t_{LOWI2C}	LOW period of the SCL clock	4.7	–	1.3	–	µs
$t_{HIGHI2C}$	HIGH period of the SCL clock	4.0	–	0.6	–	µs
$t_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs
$t_{HDDATI2C}$	Data hold time	0	–	0	–	µs
$t_{SUDATI2C}$	Data setup time	250	–	100[12]	–	ns
$t_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	0.6	–	µs
t_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs
t_{SPI2C}	Pulse width of spikes are suppressed by the input filter	–	–	0	50	ns

Figure 6. Definition for Timing for Fast/Standard Mode on the I²C Bus



Notes

11. F_{SCLI2C} is derived from SysClk of the PSoC. This specification assumes that SysClk is operating at 12 MHz, nominal. If SysClk is at a lower frequency, then the F_{SCLI2C} specification adjusts accordingly.
12. A Fast-Mode I²C-bus device can be used in a Standard-Mode I²C-bus system, but the requirement $t_{SUDATI2C}$ ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{rmax} + $t_{SUDATI2C}$ = 1000 + 250 = 1250 ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

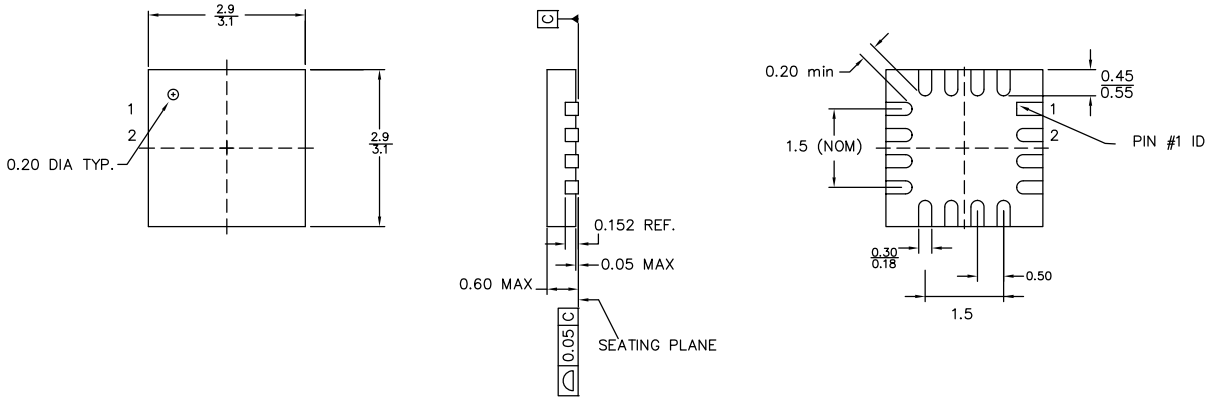
Packaging Information

This section illustrates the packaging specifications for the automotive CY8C20x34 PSoC device along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at http://www.cypress.com.

For information on the preferred dimensions for mounting QFN packages, see the application note “Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages” available at http://www.amkor.com.

Figure 7. 16-Pin (3 × 3 × 0.60 mm) QFN (Sawn)



PART NO.	DESCRIPTION
LG16A	LEAD–FREE
LD16A	STANDARD

NOTES:

1. JEDEC # MO–220
2. Package Weight: 0.014g
3. DIMENSIONS IN MM, MIN / MAX

001-09116 *F

Thermal Impedances

Table 19 illustrates the minimum solder reflow peak temperature to achieve good solderability.

Table 19. Thermal Impedances Per Package

Package	Typical θ_{JA} [12]
16-pin QFN	46 °C/W

Solder Reflow Specifications

Table 20 shows the solder reflow temperature limits that must not be exceeded.

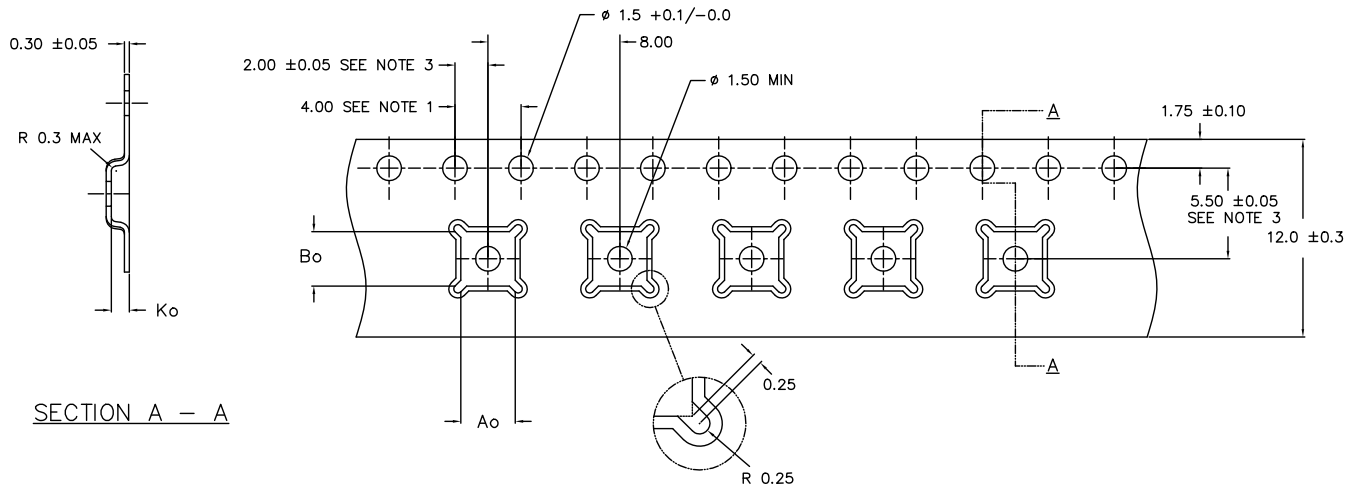
Table 20. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
16-pin QFN	260 °C	30 seconds

Note
12. $T_J = T_A + \text{Power} \times \theta_{JA}$

Tape and Reel Information

Figure 8. 16-Pin QFN Carrier Tape Drawing



Ao = 3.30
Bo = 3.30
Ko = 0.9

ALL DIMENSIONS ARE IN MILLIMETERS

NOTES:

1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

001-11785 **

Table 21. Tape and Reel Specifications

Package	Cover Tape Width (mm)	Hub Size (inches)	Minimum Leading Empty Pockets	Minimum Trailing Empty Pockets	Standard Full Reel Quantity
16-Pin QFN	9.2	7	63	38	2500

Development Tool Selection

This section presents the development tools available for the automotive CY8C20x34 family.

Software

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is available free of charge at http://www.cypress.com and includes a free C compiler.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer or PSoC Express. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com.

Development Kits

All development kits can be purchased from the Cypress Online Store. The online store also has the most up to date information on kit contents, descriptions, and availability.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. PSoC Designer also supports the advance emulation features. The kit includes:

- ICE-Cube Unit
- 28-Pin PDIP Emulation Pod for CY8C29466-24PXI
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Samples (two)
- PSoC Designer Software CD
- ISSP Cable
- MiniEval Socket Programming and Evaluation board
- Backward Compatibility Cable (for connecting to legacy Pods)
- Universal 110/220 Power Supply (12 V)
- European Plug Adapter
- USB 2.0 Cable
- Getting Started Guide
- Development Kit Registration form

CY3280-BK1

The CY3280-BK1 Universal CapSense Control Kit is designed for easy prototyping and debug of CapSense designs with pre defined control circuitry and plug-in hardware. The kit comes with a control boards for CY8C20x34 and CY8C21x34 devices as well as a breadboard module and a button(5)/slider module.

Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store. The online store also has the most up to date information on kit contents, descriptions, and availability.

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, an RS-232 port, and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3210-20X34 Evaluation Pod (EvalPod)

PSoC EvalPods are pods that connect to the ICE In-Circuit Emulator (CY3215-DK kit) to allow debugging capability. They can also function as a standalone device without debugging capability. The EvalPod has a 28-pin DIP footprint on the bottom for easy connection to development kits or other hardware. The top of the EvalPod has prototyping headers for easy connection to the device's pins. CY3210-20X34 provides evaluation of the CY8C20x34 PSoC device family.

Device Programmers

All device programmers are purchased from the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit allows a user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note CY3207ISSP needs special software and is not compatible with PSoC Programmer. This software is free and can be downloaded from http://www.cypress.com. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240 V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

Accessories (Emulation and Programming)

Table 22. Emulation and Programming Accessories

Part Number	Pin Package	Pod Kit [13]	Foot Kit [14]	Prototyping Module	Adapter [15]
CY8C20234-12LKXA	16-pin QFN	–	–	CY3210-20X34	–

Notes
13. Pod kit contains an emulation pod, a flex-cable (connects the pod to the ICE), two feet, and device samples.
14. Foot kit includes surface mount feet that is soldered to the target PCB.
15. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters is found at http://www.emulation.com.

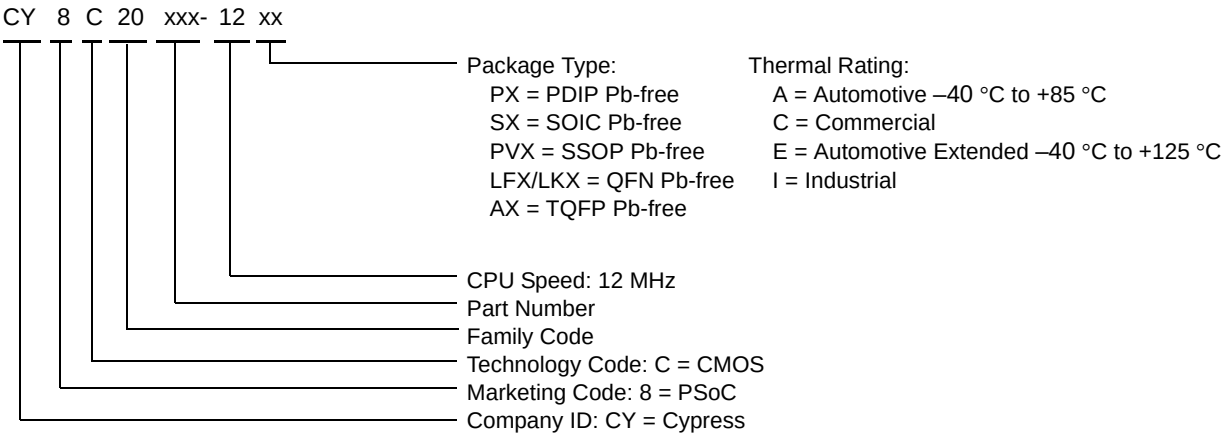
Ordering Information

Table 23 lists the automotive CY8C20x34 PSoC device key package features and ordering codes.

Table 23. PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	Digital Blocks	CapSense Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
16-pin (3 × 3 × 0.6 mm) QFN, sawn	CY8C20234-12LKXA	8 K	512	0	1	13	13	0	Yes
16-pin (3 × 3 × 0.6 mm) QFN, sawn (tape and reel)	CY8C20234-12LKXAT	8 K	512	0	1	13	13	0	Yes

Ordering Code Definitions



Reference Information

Acronyms

Table 24 lists the acronyms that are used in this document.

Table 24. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	LVD	low voltage detect
ADC	analog-to-digital converter	MCU	microcontroller unit
AEC	Automotive Electronics Council	MIPS	million instructions per second
API	application programming interface	PCB	printed circuit board
CMOS	complementary metal oxide semiconductor	PDIP	plastic dual inline package
CPU	central processing unit	PGA	programmable gain amplifier
DAC	digital-to-analog converter	POR	power-on reset
DC	direct current	PPOR	precision (POR)
EEPROM	electrically erasable programmable read-only memory	PSoC®	Programmable System-on-Chip
GPIO	general-purpose I/O	PWM	pulse-width modulator
I/O	input/output	QFN	quad flat no leads
ICE	in-circuit emulator	RMS	root mean square
IDE	integrated development environment	SLIMO	slow IMO
ILO	internal low-speed oscillator	SPI	serial peripheral interface
IMO	internal main oscillator	SRAM	static random-access memory
ISSP	in-system serial programming	SROM	supervisory read-only memory
LCD	liquid crystal display	USB	universal serial bus
LDO	low dropout regulator	WDT	watchdog timer
LED	light-emitting diode	XRES	external reset

Reference Documents

PSoC® CY8C20x34 and PSoC® CY8C20x24 Technical Reference Manual (TRM) (001-13033)

Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 (001-14503)

Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages – available at http://www.amkor.com.

Document Conventions

Units of Measure

Table 25 lists the units of measures.

Table 25. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	mV	millivolt
KB	1024 bytes	nA	nanoampere
kHz	kilohertz	ns	nanosecond
kΩ	kilohm	Ω	ohm
MHz	megahertz	%	percent
µA	microampere	pF	picofarad
µs	microsecond	ps	picosecond
mA	milliampere	V	volt
mm	millimeter	W	watt
ms	millisecond		

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimals.

Glossary

active high	1. A logic signal having its asserted state as the logic 1 state. 2. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
API (Application Programming Interface)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.
bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.

Glossary (continued)

block	1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.
buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.
bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows the user to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.
duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.

Glossary (continued)

emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.
external reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
flash	An electrically programmable and erasable, non-volatile technology that provides users with the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is off.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5 V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows users to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls below a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the ***slave device.***

Glossary (continued)

microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.
modulator	A device that imposes a signal on a carrier.
noise	1. A disturbance that affects a signal and that may distort the information carried by the signal. 2. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
phase-locked loop (PLL)	An electronic circuit that controls an ***oscillator*** so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
power on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is below a pre-set level. This is one type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurand
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.

Glossary (continued)

settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.
shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device allowing users to store and retrieve data at a high rate of speed. The term static is used because, after a value has been loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***API (Application Programming Interface)*** for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning "voltage drain." The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning "voltage source." The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

Document History Page

Document Title: CY8C20234 Automotive PSoC® Programmable System-on-Chip Document Number: 001-54650				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2743436	MASJ/AESA	07/24/09	New data sheet.
*A	2799448	BTK	11/05/09	Updated Features section. Updated text of PSoC Functional Overview section. Updated Getting Started section. Made corrections and minor text edits to Pinouts section. Changed the name of some sections to improve consistency. Added clarifying comments to some electrical specifications. Fixed all AC specifications to conform to a ±5% IMO accuracy. Made other miscellaneous minor text edits. Deleted some non-applicable or redundant information. Improved and edited content in Development Tool Selection section. Improved the bookmark structure. Changed $Flash_{ENT}$, F_{OSCEXT}, T_{ERASEB}, and T_{WRITE} electrical specifications according to MASJ input. Added and slightly modified the expanded SPI AC specifications from 001-05356 Rev *I. Added a table of contents.
*B	2822792	BTK/AESA	12/07/2009	Added T_{PRGH}, T_{PRGC}, F_{32KU}, DC_{ILO}, and $T_{POWERUP}$ electrical specifications. Updated the footnotes for Table 10, “DC Programming Specifications,” on page 13. Added maximum values and updated typical values for T_{ERASEB} and T_{WRITE} electrical specifications. Replaced T_{RAMP} electrical specification with $SR_{POWERUP}$ electrical specification. Changed F_{IMO6} electrical specification to have an 8.33% accuracy instead of 5%. Added “Contents” on page 2.
*C	2888007	NJF	03/30/2010	Updated Cypress website links. Updated CapSense Analog System. Removed PSoC Designer 4.4 reference in PSoC Designer Software Subsystems. Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters in Absolute Maximum Ratings. Removed DC Low Power Comparator Specifications, AC Analog Mux Bus Specifications, and AC Low Power Comparator Specifications. Updated Packaging Information. Added Solder Reflow Peak Temperature. Removed Third Party Tools and Build a PSoC Emulator into Your Board. Updated links in Sales, Solutions, and Legal Information.
*D	3043236	ARVM	09/30/10	Under section “AC Comparator Amplifier Specifications”, the caption for spec table changed from “AC Operational Amplifier Specifications” to “AC Comparator Specifications”. Also the section heading changed to AC Comparator specifications.
*E	3272879	BTK/NJF	06/10/11	Updated I^2C timing diagram to improve clarity. Added V_{DDP}, V_{DDLV}, and V_{DDHV} electrical specifications to give more information for programming the device. Updated solder reflow temperature specifications to give more clarity. Updated the jitter specifications. Added PSoC Device Characteristics table. Updated the F_{32KU} electrical specification. Added R_{PD} electrical specification. Updated note for the T_{STG} electrical specification to add more clarity. Updated Units of Measure, Acronyms, Glossary, and References sections. Added Tape and Reel Specifications section.
*F	3638596	BVI	06/06/2012	Updated F_{SCLK} parameter in the Table 17, “SPI Slave AC Specifications,” on page 16. Changed t_{OUT_HIGH} to t_{OUT_H} in Table 16, “SPI Master AC Specifications,” on page 16 Updated package drawing spec 001-09116 to *F revision.

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PSoC 1 | PSoC 3 | PSoC 5