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REVISION HISTORY

11/15—Rev. A to Rev. B

Changes to V_{DD}/V_{SS} Parameter, Table 2	5
Updated Outline Dimensions	19

1/13—Rev. 0 to Rev. A

Changes to RESET/ V_L Pin Description Column, Table 9	11
Changes to Power-On Reset Section.....	19
Updated Outline Dimensions	20

10/09—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

$V_{DD} = 15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, $V_L = 2.7\text{ V}$ to 5.5 V , $GND = 0\text{ V}$, unless otherwise noted.

Table 1.

Parameter	+25°C	–40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{SS} to V_{DD}	V	
On Resistance (R_{ON})	9.5			Ω typ	$V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$, $V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$; see Figure 23
	11.5	14	16	Ω max	
On-Resistance Match Between Channels (ΔR_{ON})	0.55			Ω typ	$V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$, $V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$
	1	1.5	1.7	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	1.6			Ω typ	$V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$, $V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$
	1.9	2.15	2.3	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.05			nA typ	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ $V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$; see Figure 24
	± 0.15	± 1	± 2	nA max	
Drain Off Leakage, I_D (Off)	± 0.05			nA typ	$V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$; see Figure 24
	± 0.15	± 1	± 2	nA max	
Channel On Leakage, I_D , I_S (On)	± 0.1			nA typ	$V_S = V_D = \pm 10\text{ V}$; see Figure 25
	± 0.3	± 2	± 4	nA max	
DIGITAL INPUTS					
Input High Voltage (V_{INH})			2.0	V min	
Input Low Voltage (V_{INL})			0.8	V max	
Input Current	± 0.001			μA typ	$V_{IN} = V_{GND}$ or V_L
			± 0.1	μA max	
Digital Input Capacitance (C_{IN})	4			pF typ	
LOGIC OUTPUTS (SDO)					
Output Low Voltage (V_{OL}) ¹			0.4	V max	$I_{SINK} = 3\text{ mA}$
			0.6	V max	$I_{SINK} = 6\text{ mA}$
High Impedance Leakage Current	0.001			μA typ	
			± 1	μA max	
High Impedance Output Capacitance ¹	4			pF typ	
DYNAMIC CHARACTERISTICS¹					
t_{ON}	75			ns typ	$R_L = 100\ \Omega$, $C_L = 35\text{ pF}$
	93	110	120	ns max	$V_S = 10\text{ V}$; see Figure 30
t_{OFF}	25			ns typ	$R_L = 100\ \Omega$, $C_L = 35\text{ pF}$
	35	35	35	ns max	$V_S = 10\text{ V}$; see Figure 30
Charge Injection	10			pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 31
Off Isolation	–73			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 26
Channel-to-Channel Crosstalk	–75			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 27
Total Harmonic Distortion (THD + N)	0.05			% typ	$R_L = 110\ \Omega$, 15 V p-p , $f = 20\text{ Hz}$ to 20 kHz ; see Figure 29
–3 dB Bandwidth	256			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 28
Insertion Loss	0.55			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 28
C_D , C_S (Off)	8			pF typ	$f = 1\text{ MHz}$
C_D , C_S (On)	32			pF typ	$f = 1\text{ MHz}$

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$
I_{DD}	0.001		1	$\mu\text{A typ}$ $\mu\text{A max}$	Digital inputs = 0 V or V_L
I_L Inactive	0.3		1	$\mu\text{A typ}$ $\mu\text{A max}$	Digital inputs = 0 V or V_L
I_L Active at 30 MHz	0.26			mA typ mA max	Digital inputs toggle between 0 V and V_L
I_L Active at 50 MHz	0.42	0.3	0.35	mA typ mA max	Digital inputs toggle between 0 V and V_L
I_{SS}	0.001	0.5	0.55	$\mu\text{A typ}$ $\mu\text{A max}$	Digital inputs = 0 V or V_L
V_{DD}/V_{SS}			1 $\pm 4.5/\pm 16.5$	V min/max	

¹ Guaranteed by design, not subject to production test.

12 V SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $V_L = 2.7\text{ V}$ to 5.5 V , $\text{GND} = 0\text{ V}$, unless otherwise noted.

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V_{DD}	V	
On Resistance (R_{ON})	18			Ω typ	$V_{DD} = 10.8\text{ V}$, $V_{SS} = 0\text{ V}$; $V_S = 0\text{ V}$ to 10 V , $I_S = -10\text{ mA}$; see Figure 23
On-Resistance Match Between Channels (ΔR_{ON})	21.5 0.55	26	28.5	Ω max Ω typ	$V_{DD} = 10.8\text{ V}$, $V_{SS} = 0\text{ V}$; $V_S = 0\text{ V}$ to 10 V , $I_S = -10\text{ mA}$
On-Resistance Flatness ($R_{FLAT(ON)}$)	1.2 5	1.6	1.8	Ω max Ω typ	$V_{DD} = 10.8\text{ V}$, $V_{SS} = 0\text{ V}$; $V_S = 0\text{ V}$ to 10 V , $I_S = -10\text{ mA}$
	6	6.9	7.3	Ω max	
LEAKAGE CURRENTS					$V_{DD} = 10.8\text{ V}$
Source Off Leakage, I_S (Off)	± 0.02 ± 0.15	± 1	± 2	nA typ nA max	$V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$; see Figure 24
Drain Off Leakage, I_D (Off)	± 0.02 ± 0.15	± 1	± 2	nA typ nA max	$V_S = 1\text{ V}/10\text{ V}$, $V_D = 10\text{ V}/1\text{ V}$; see Figure 24
Channel On Leakage, I_D , I_S (On)	± 0.05 ± 0.3	± 1 ± 2	± 2 ± 4	nA typ nA max	$V_S = V_D = 1\text{ V}$ or 10 V ; see Figure 25
DIGITAL INPUTS					
Input High Voltage (V_{INH})			2.0	V min	
Input Low Voltage (V_{INL})			0.8	V max	
Input Current	± 0.001		± 0.1	$\mu\text{A typ}$ $\mu\text{A max}$	$V_{IN} = V_{GND}$ or V_L
Digital Input Capacitance (C_{IN})	4			pF typ	
LOGIC OUTPUTS (SDO)					
Output Low Voltage (V_{OL}) ¹			0.4 0.6	V max V max	$I_{SINK} = 3\text{ mA}$ $I_{SINK} = 6\text{ mA}$
High Impedance Leakage Current			± 1	$\mu\text{A max}$	
High Impedance Output Capacitance ¹	4			pF typ	

Parameter	+25°C	–40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
DYNAMIC CHARACTERISTICS¹					
t _{ON}	145			ns typ	R _L = 100 Ω, C _L = 35 pF
	185	220	240	ns max	V _S = 8 V; see Figure 30
t _{OFF}	35			ns typ	R _L = 100 Ω, C _L = 35 pF
	45	46	46	ns max	V _S = 8 V; see Figure 30
Charge Injection	8			pC typ	V _S = 6 V, R _S = 0 Ω, C _L = 1 nF; see Figure 31
Off Isolation	–70			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 26
Channel-to-Channel Crosstalk	–75			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 27
–3 dB Bandwidth	240			MHz typ	R _L = 50 Ω, C _L = 5 pF; see Figure 28
Insertion Loss	1.15			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 28
C _D , C _S (Off)	12			pF typ	f = 1 MHz
C _D , C _S (On)	33			pF typ	f = 1 MHz
POWER REQUIREMENTS					
I _{DD}	0.001			μA typ	V _{DD} = +13.2 V
			1	μA max	Digital inputs = 0 V or V _L
I _L Inactive	0.3			μA typ	Digital inputs = 0 V or V _L
			1	μA max	
I _L Active at 30 MHz	0.26			mA typ	Digital inputs toggle between 0 V and V _L
		0.3	0.35	mA max	
I _L Active at 50 MHz	0.42			mA typ	Digital inputs toggle between 0 V and V _L
		0.5	0.55	mA max	
I _{SS}	0.001			μA typ	Digital inputs = 0 V or V _L
			1	μA max	
V _{DD} /V _{SS}			5/16.5	V min/max	

¹ Guaranteed by design, not subject to production test.

±5 V DUAL SUPPLY

$V_{DD} = +5\text{ V} \pm 10\%$, $V_{SS} = -5\text{ V} \pm 10\%$, $V_L = 2.7\text{ V}$ to V_{DD} , $GND = 0\text{ V}$, unless otherwise noted.

Table 3.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analogue Signal Range			V_{SS} to V_{DD}	V	
On Resistance (R_{ON})	21			Ω typ	$V_{DD} = +4.5\text{ V}$, $V_{SS} = -4.5\text{ V}$, $V_S = \pm 4.5\text{ V}$, $I_S = -10\text{ mA}$; see Figure 23
	25	29	32	Ω max	
On-Resistance Match Between Channels (ΔR_{ON})	0.6			Ω typ	$V_{DD} = +4.5\text{ V}$, $V_{SS} = -4.5\text{ V}$, $V_S = \pm 4.5\text{ V}$, $I_S = -10\text{ mA}$
	1.3	1.7	1.9	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	5.2			Ω typ	$V_{DD} = +4.5\text{ V}$, $V_{SS} = -4.5\text{ V}$, $V_S = \pm 4.5\text{ V}$;
	6.4	7.3	7.6	Ω max	$I_S = -10\text{ mA}$
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.02			nA typ	$V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$
	± 0.15	± 1	± 2	nA max	$V_S = \pm 4.5\text{ V}$, $V_D = \mp 4.5\text{ V}$; see Figure 24
Drain Off Leakage, I_D (Off)	± 0.02			nA typ	$V_S = \pm 4.5\text{ V}$, $V_D = \mp 4.5\text{ V}$; see Figure 24
	± 0.15	± 1	± 2	nA max	
Channel On Leakage, I_D , I_S (On)	± 0.05			nA typ	$V_S = V_D = \pm 4.5\text{ V}$; see Figure 25
	± 0.3	± 2	± 4	nA max	
DIGITAL INPUTS					
Input High Voltage (V_{INH})			2.0	V min	
Input Low Voltage (V_{INL})			0.8	V max	
Input Current	± 0.001			μA typ	$V_{IN} = V_{GND}$ or V_L
			± 0.1	μA max	
Digital Input Capacitance (C_{IN})	4			pF typ	
LOGIC OUTPUTS (SDO)					
Output Low Voltage (V_{OL}) ¹			0.4	V max	$I_{SINK} = 3\text{ mA}$
			0.6	V max	$I_{SINK} = 6\text{ mA}$
High Impedance Leakage Current			± 1	μA max	
High Impedance Output Capacitance ¹	4			pF typ	
DYNAMIC CHARACTERISTICS¹					
t_{ON}	190			ns typ	$R_L = 100\ \Omega$, $C_L = 35\text{ pF}$
	250	290	320	ns max	$V_S = 3\text{ V}$; see Figure 30
t_{OFF}	45			ns typ	$R_L = 100\ \Omega$, $C_L = 35\text{ pF}$
	60	65	70	ns max	$V_S = 3\text{ V}$; see Figure 30
Charge Injection	7			pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 31
Off Isolation	−70			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 26
Channel-to-Channel Crosstalk	−75			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 27
Total Harmonic Distortion (THD + N)	0.14			% typ	$R_L = 110\ \Omega$, 5 V p-p, $f = 20\text{ Hz}$ to 20 kHz ; see Figure 29
−3 dB Bandwidth	256			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 28
Insertion Loss	1			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 28
C_D , C_S (Off)	11			pF typ	$f = 1\text{ MHz}$
C_D , C_S (On)	35			pF typ	$f = 1\text{ MHz}$

Parameter	+25°C	–40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					$V_{DD} = +5.5\text{ V}$, $V_{SS} = -5.5\text{ V}$
I_{DD}	0.001		1	$\mu\text{A typ}$ $\mu\text{A max}$	Digital inputs = 0 V or V_L
I_L Inactive	0.3		1	$\mu\text{A typ}$ $\mu\text{A max}$	Digital inputs = 0 V or V_L
I_L Active at 30 MHz	0.26	0.3	0.35	mA typ mA max	Digital inputs toggle between 0 V and V_L
I_L Active at 50 MHz	0.42	0.5	0.55	mA typ mA max	Digital inputs toggle between 0 V and V_L
I_{SS}	0.001		1	$\mu\text{A typ}$ $\mu\text{A max}$	Digital inputs = 0 V or V_L
V_{DD}/V_{SS}			$\pm 4.5/\pm 16.5$	V min/max	

¹ Guaranteed by design, not subject to production test.

CONTINUOUS CURRENT PER CHANNEL

Guaranteed by design, not subject to production test.

Table 4. Eight Channels On

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT PER CHANNEL					
$\pm 15\text{ V}$ Dual Supply					$V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$
24-Lead TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$)	67	46	31	mA max	
24-Lead LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$)	121	75	42	mA max	
12 V Single Supply					$V_{DD} = 10.8\text{ V}$, $V_{SS} = 0\text{ V}$
24-Lead TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$)	64	44	30	mA max	
24-Lead LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$)	115	72	41	mA max	
$\pm 5\text{ V}$ Dual Supply					$V_{DD} = +4.5\text{ V}$, $V_{SS} = -4.5\text{ V}$
24-Lead TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$)	48	35	22	mA max	
24-Lead LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$)	86	57	36	mA max	

Guaranteed by design and characterization, not production tested.

Table 5. One Channel On

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT PER CHANNEL					
$\pm 15\text{ V}$ Dual Supply					$V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$
24-Lead TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$)	169	97	48	mA max	
24-Lead LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$)	295	139	55	mA max	
12 V Single Supply					$V_{DD} = 10.8\text{ V}$, $V_{SS} = 0\text{ V}$
24-Lead TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$)	161	93	47	mA max	
24-Lead LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$)	281	135	54	mA max	
$\pm 5\text{ V}$ Dual Supply					$V_{DD} = +4.5\text{ V}$, $V_{SS} = -4.5\text{ V}$
24-Lead TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$)	122	76	43	mA max	
24-Lead LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$)	214	114	51	mA max	

TIMING CHARACTERISTICS

All input signals are specified with $t_R = t_F = 1 \text{ ns/V}$ (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$ (see Figure 2). $V_{DD} = 4.5 \text{ V}$ to 16.5 V ; $V_{SS} = -16.5 \text{ V}$ to 0 V ; $V_L = 2.7 \text{ V}$ to 5.5 V or V_{DD} (whichever is less); $GND = 0 \text{ V}$; all specifications T_{MIN} to T_{MAX} , unless otherwise noted. Guaranteed by design and characterization, not production tested.

Table 6.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Conditions/Comments
t_1^1	20	ns min	SCLK cycle time
t_2	9	ns min	SCLK high time
t_3	9	ns min	SCLK low time
t_4	5	ns min	$\overline{\text{SYNC}}$ to SCLK active edge setup time
t_5	5	ns min	Data setup time
t_6	5	ns min	Data hold time
t_7	5	ns min	SCLK active edge to $\overline{\text{SYNC}}$ rising edge
t_8	15	ns min	Minimum $\overline{\text{SYNC}}$ high time
t_9	5	ns min	$\overline{\text{SYNC}}$ rising edge to next SCLK active edge ignored
t_{10}	5	ns min	SCLK active edge to $\overline{\text{SYNC}}$ falling edge ignored
t_{11}^2	40	ns max	SCLK rising edge to SDO valid
t_{12}	15	ns min	Minimum RESET pulse width

¹ Maximum SCLK frequency is 50 MHz at $V_{DD} = 4.5 \text{ V}$ to 16.5 V ; $V_{SS} = -16.5 \text{ V}$ to 0 V ; $V_L = 2.7 \text{ V}$ to 5.5 V or V_{DD} (whichever is less); $GND = 0 \text{ V}$.

² Measured with the 1 k Ω pull-up resistor to V_L and 20 pF load. t_{11} determines the maximum SCLK frequency in daisy-chain mode.

Timing Diagrams

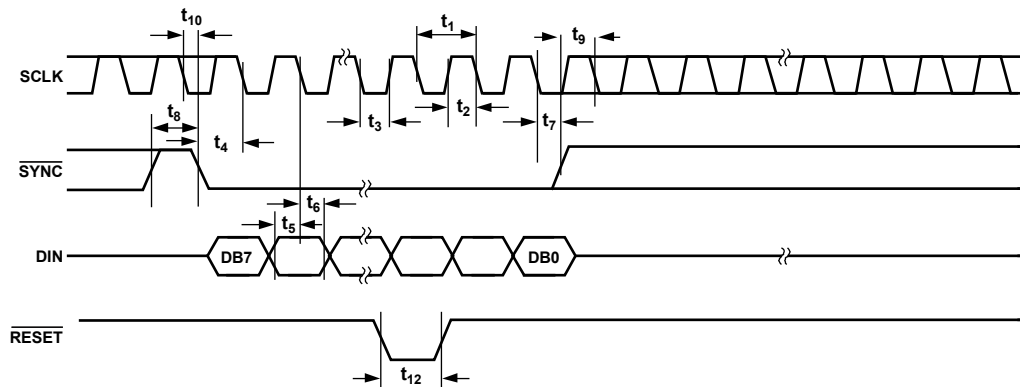


Figure 2. Serial Write Operation

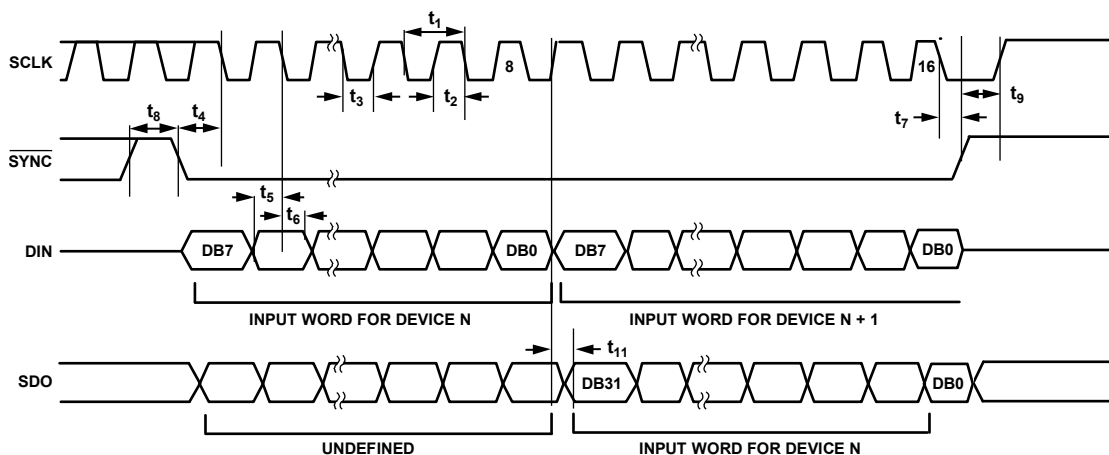


Figure 3. Daisy-Chain Timing Diagram

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 7.

Parameter	Rating
V_{DD} to V_{SS}	35 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
V_L to GND	−0.3 V to +7 V
Analog Inputs ¹	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs ¹	GND − 0.3 V to $V_L + 0.3\text{ V}$ or 30 mA, whichever occurs first
Continuous Current, Sx or Dx Pins	Table 4 specifications + 15%
Peak Current, Sx or Dx (Pulsed at 1 ms, 10% Duty Cycle Maximum)	
TSSOP Package	300 mA
LFCSP Package	400 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Reflow Soldering Peak Temperature, Pb free	260°C
Time at Peak Temperature	10 sec to 40 sec

¹ Overvoltages at the analog and digital inputs are clamped by internal diodes. Limit the current to the maximum ratings given.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating may be applied at any one time.

THERMAL RESISTANCE

Table 8. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
24-Lead TSSOP ¹	112.6	50	°C/W
24-Lead LFCSP ²	30.4		°C/W

¹ 4-layer board.

² 4-layer board and exposed paddle soldered to V_{SS} .

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

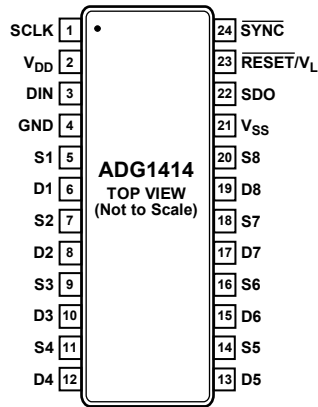
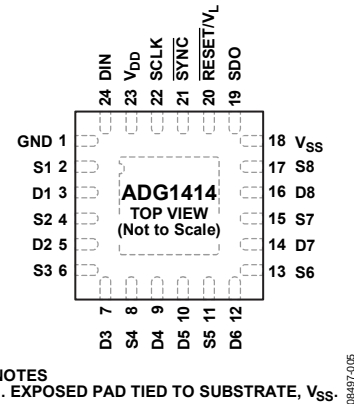


Figure 4. TSSOP Pin Configuration



NOTES
1. EXPOSED PAD TIED TO SUBSTRATE, V_{SS} .

Table 9. Pin Function Descriptions

Pin No.		Mnemonic	Description
TSSOP	LFCSP		
1	22	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz.
2	23	V_{DD}	Most Positive Power Supply Potential.
3	24	DIN	Serial Data Input. This device has an 8-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
4	1	GND	Ground (0 V) Reference.
5	2	S1	Source Terminal 1. This pin can be an input or an output.
6	3	D1	Drain Terminal 1. This pin can be an input or an output.
7	4	S2	Source Terminal 2. This pin can be an input or an output.
8	5	D2	Drain Terminal 2. This pin can be an input or an output.
9	6	S3	Source Terminal 3. This pin can be an input or an output.
10	7	D3	Drain Terminal 3. This pin can be an input or an output.
11	8	S4	Source Terminal 4. This pin can be an input or an output.
12	9	D4	Drain Terminal 4. This pin can be an input or an output.
13	10	D5	Drain Terminal 5. This pin can be an input or an output.
14	11	S5	Source Terminal 5. This pin can be an input or an output.
15	12	D6	Drain Terminal 6. This pin can be an input or an output.
16	13	S6	Source Terminal 6. This pin can be an input or an output.
17	14	D7	Drain Terminal 7. This pin can be an input or an output.
18	15	S7	Source Terminal 7. This pin can be an input or an output.
19	16	D8	Drain Terminal 8. This pin can be an input or an output.
20	17	S8	Source Terminal 8. This pin can be an input or an output.
21	18	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, it can be connected to ground.
22	19	SDO	Serial Data Output. This pin can be used for daisy-chaining a number of these devices together or for reading back the data in the shift register for diagnostic purposes. The serial data is transferred on the rising edge of SCLK and is valid on the falling edge of the clock. Pull this open-drain output to the supply with an external resistor.
23	20	$\overline{\text{RESET}}/V_L$	$\overline{\text{RESET}}$ /Logic Power Supply Input (V_L). Under normal operation, drive the $\overline{\text{RESET}}/V_L$ pin with a 2.7 V to 5 V supply. Pull the pin low (<0.8 V) for a short period of time (15 ns is sufficient) to complete a hardware reset. All switches are opened, and the appropriate registers are cleared to 0. When using the $\overline{\text{RESET}}/V_L$ pin to complete a hardware reset, all other SPI pins (SYNC, SCLK, and DIN) must be driven low.

Pin No.		Mnemonic	Description
TSSOP	LFCSP		
24	21	<u>SYNC</u>	Active Low Control Input. This is the frame synchronization signal for the input data. When <u>SYNC</u> goes low, it powers on the SCLK and DIN buffers and enables the input shift register. Data is transferred in on the falling edges of the following clocks. Taking <u>SYNC</u> high updates the switch condition.
N/A ¹	EP	Exposed Pad	Exposed Pad. Exposed pad tied to the substrate, V _{SS} .

¹ N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

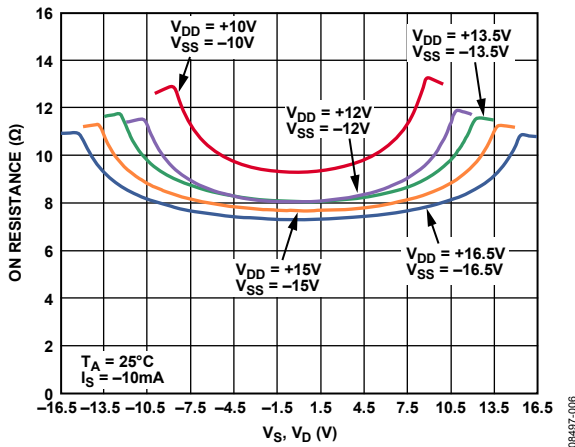


Figure 6. On Resistance as a Function of V_D (V_S), Dual Supply ($V_{DD} = 10\text{ V}$ to 16.5 V and $V_{SS} = -10\text{ V}$ to -16.5 V)

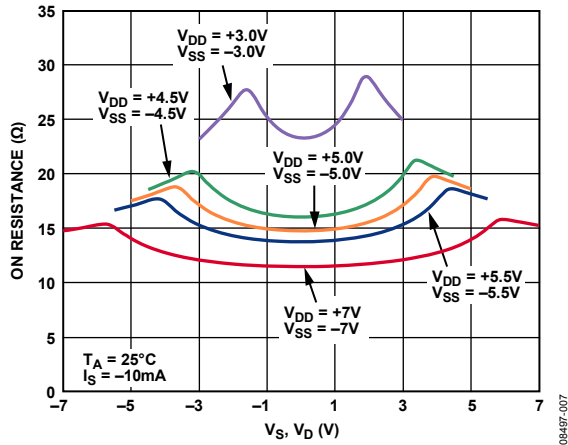


Figure 7. On Resistance as a Function of V_D (V_S), Dual Supply ($V_{DD} = 3.0\text{ V}$ to 7 V and $V_{SS} = -3.0\text{ V}$ to -7 V)

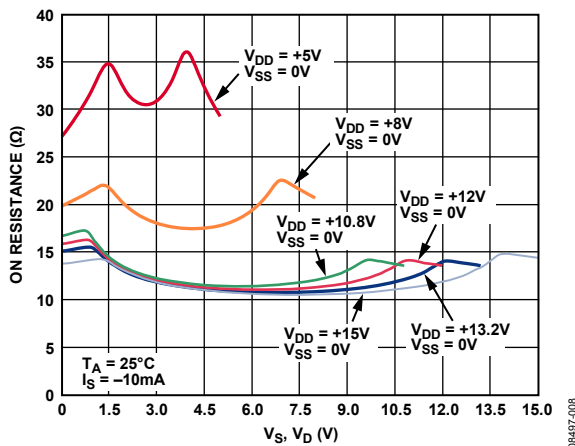


Figure 8. On Resistance as a Function of V_D (V_S), Single Supply

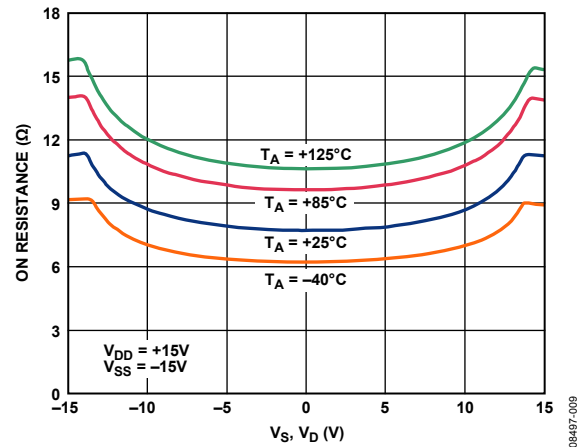


Figure 9. On Resistance as a Function of V_D (V_S), for Different Temperatures, $\pm 15\text{ V}$ Dual Supply

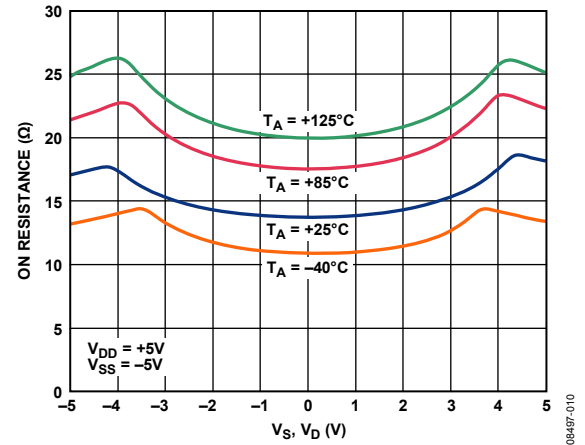


Figure 10. On Resistance as a Function of V_D (V_S), for Different Temperatures, $\pm 5\text{ V}$ Dual Supply

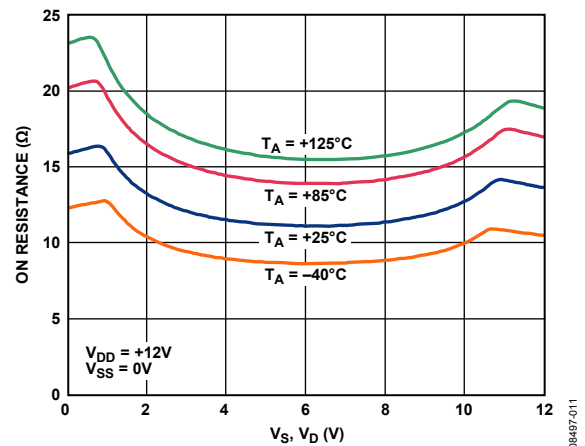


Figure 11. On Resistance as a Function of V_D (V_S), for Different Temperatures, 12 V Single Supply

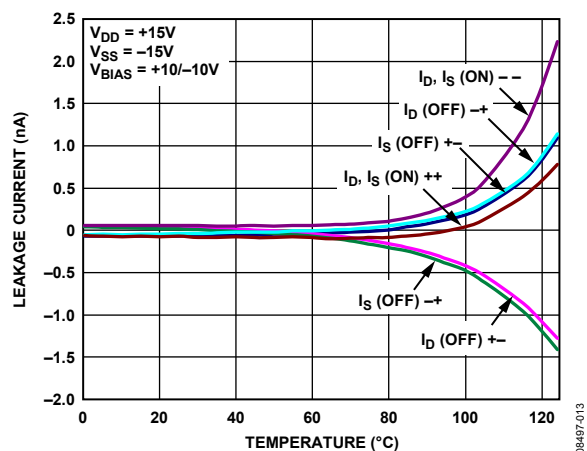
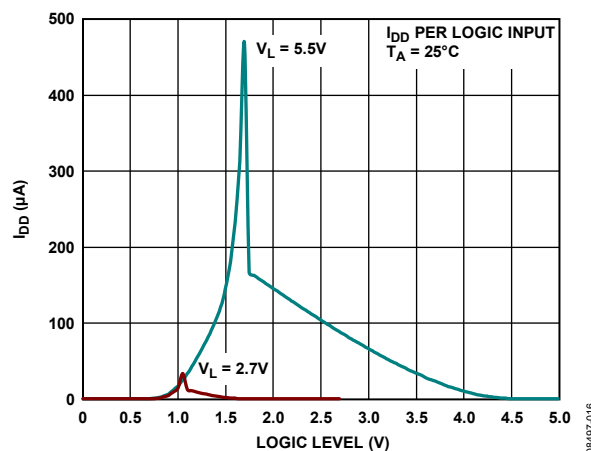
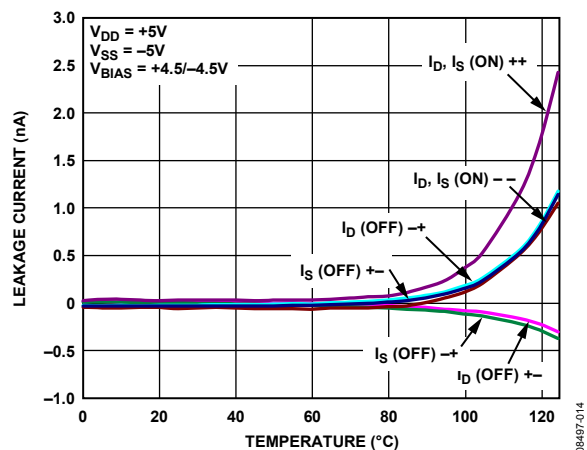
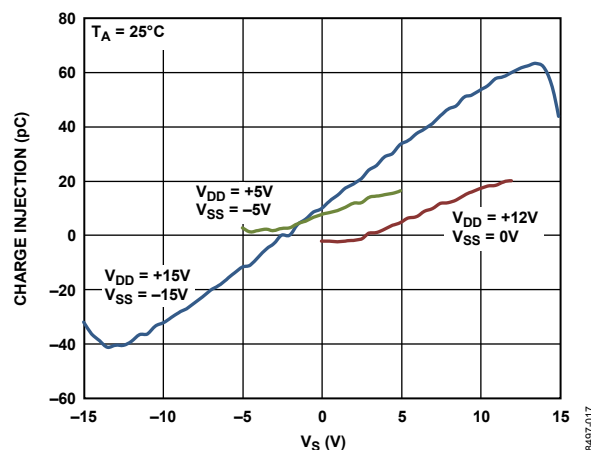
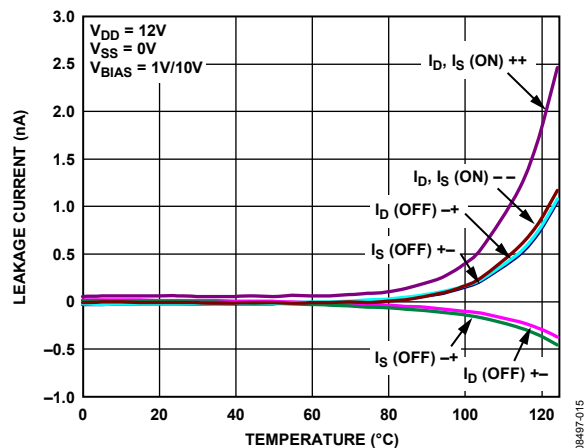
Figure 12. Leakage Current as a Function of Temperature, ± 15 V Dual SupplyFigure 15. I_{DD} vs. Logic LevelFigure 13. Leakage Current as a Function of Temperature, ± 5 V Dual SupplyFigure 16. Charge Injection vs. Source Voltage (V_S)

Figure 14. Leakage Current as a Function of Temperature, 12 V Single Supply

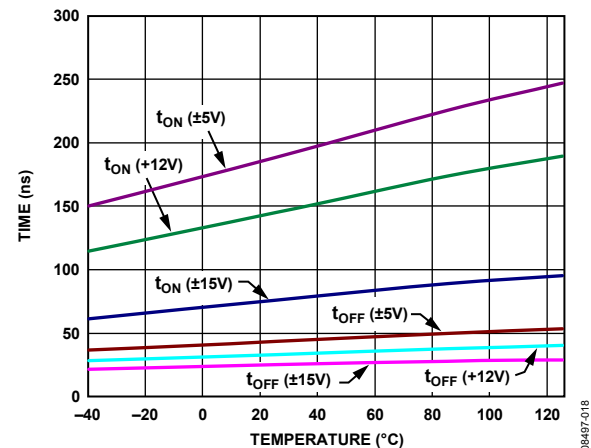


Figure 17. Transition Time vs. Temperature

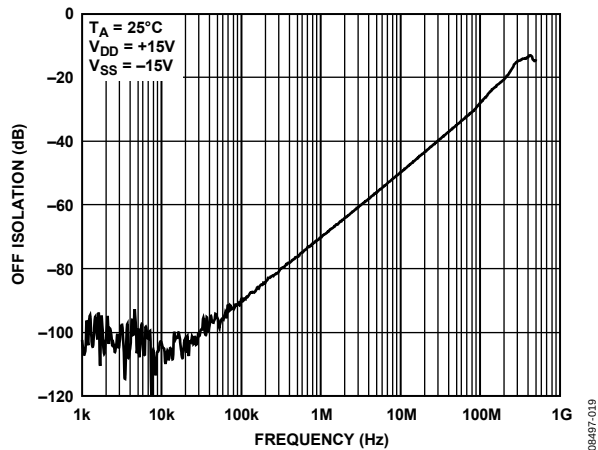


Figure 18. Off Isolation vs. Frequency

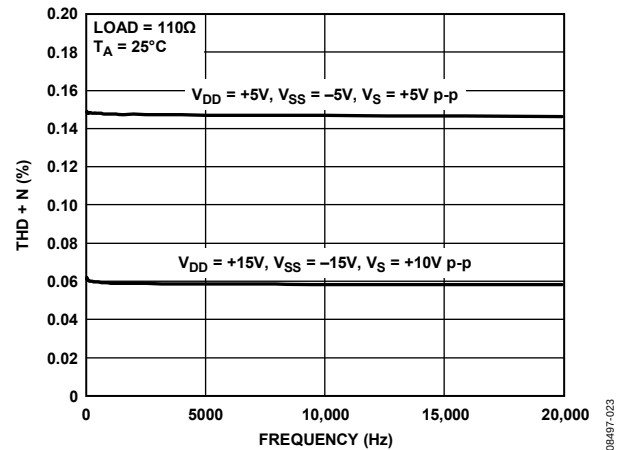
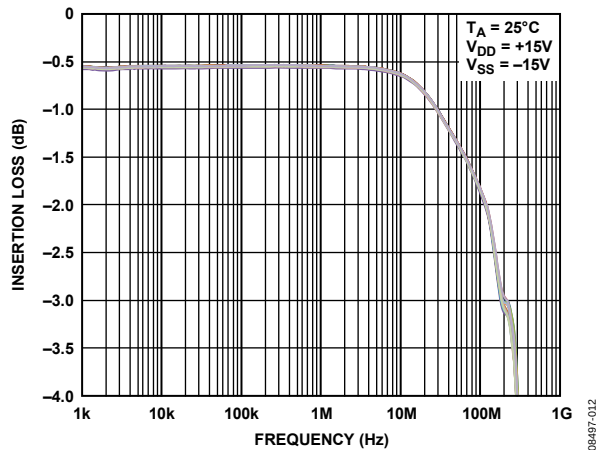
Figure 21. THD + N vs. Frequency, ± 15 V Dual Supply

Figure 19. On Response vs. Frequency

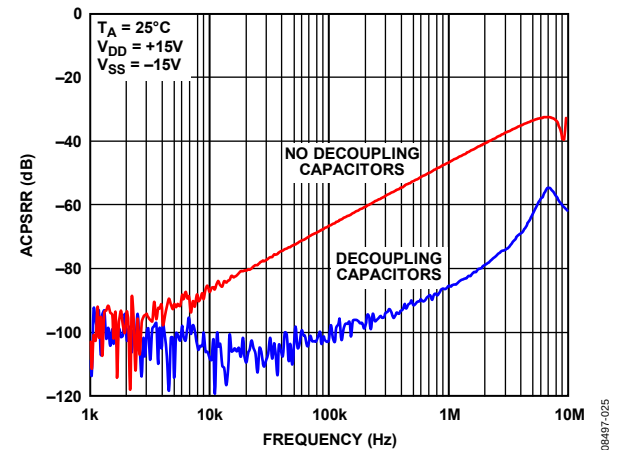


Figure 22. ACPSRR vs. Frequency

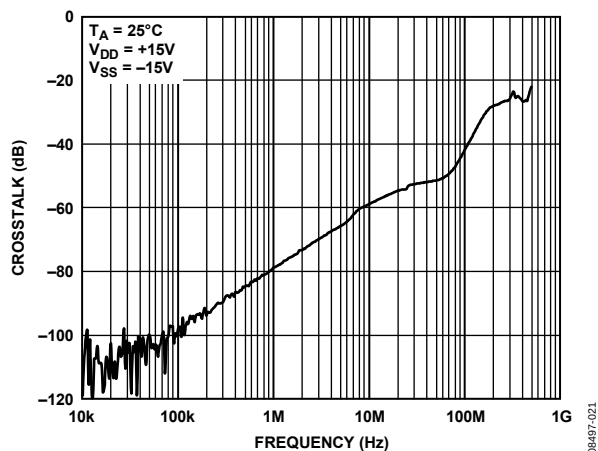
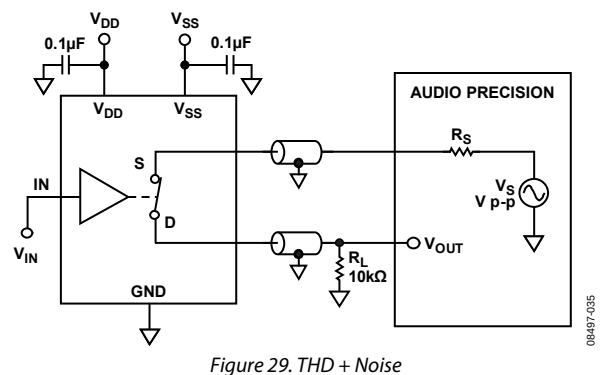
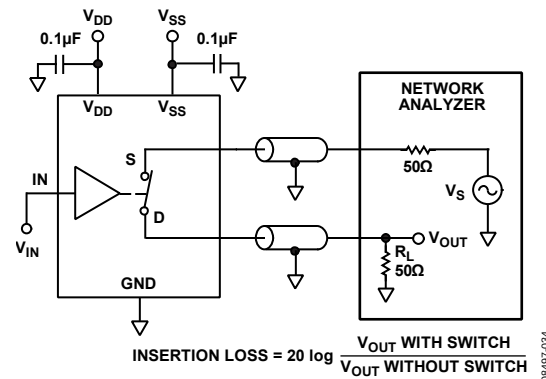
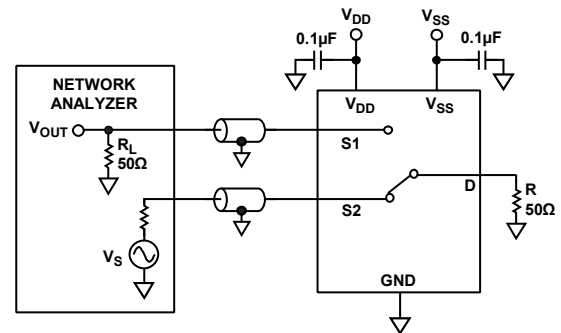
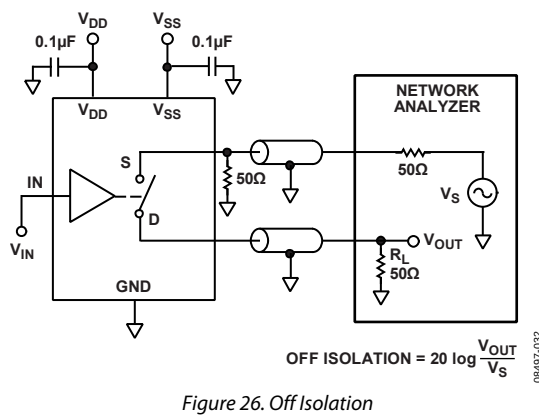
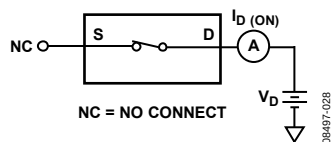
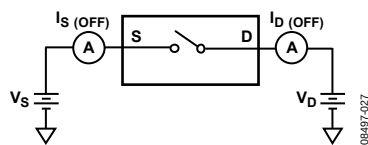
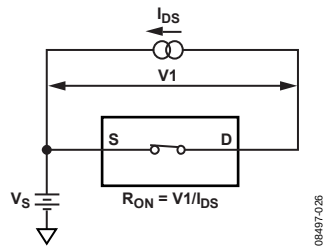
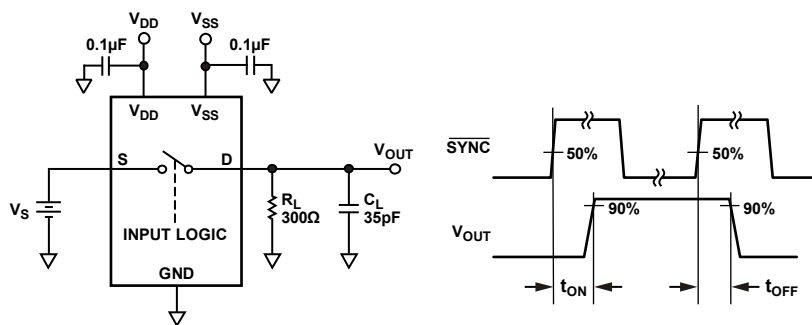


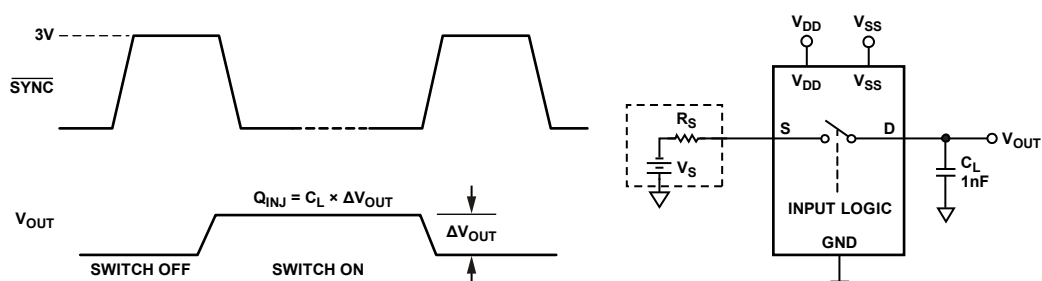
Figure 20. Crosstalk vs. Frequency

TEST CIRCUITS





08497-029



08497-031

TERMINOLOGY

I_{DD}

The positive supply current.

I_{SS}

The negative supply current.

V_D (V_S)

The analog voltage on Terminal Dx or Terminal Sx.

R_{ON}

The ohmic resistance between Terminal Dx and Terminal Sx.

ΔR_{ON}

The difference between the R_{ON} of any two channels.

R_{FLAT} (ON)

Flatness is defined as the difference between the maximum and minimum value of on resistance, as measured over the specified analog signal range.

I_S (Off)

The source leakage current with the switch off.

I_D (Off)

The drain leakage current with the switch off.

I_D, I_S (On)

The channel leakage current with the switch on.

V_{INL}

The maximum input voltage for Logic 0.

V_{INH}

The minimum input voltage for Logic 1.

I_{INL} (I_{INH})

The input current of the digital input.

C_S (Off)

The off switch source capacitance, measured with reference to ground.

C_D (Off)

The off switch drain capacitance, measured with reference to ground.

C_D, C_S (On)

The on switch capacitance, measured with reference to ground.

C_{IN}

The digital input capacitance.

t_{ON}

The delay between applying the digital control input and the output switching on. See Figure 30.

t_{OFF}

The delay between applying the digital control input and the output switching off. See Figure 30.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth

The frequency at which the output is attenuated by 3 dB.

On Response

The frequency response of the on switch.

Insertion Loss

The loss due to the on resistance of the switch.

THD + N

The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

AC Power Supply Rejection Ratio (ACPSRR)

A measure of the ability of a device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the ACPSRR.

THEORY OF OPERATION

The **ADG1414** is a set of serially controlled, octal SPST switches. Each of the eight bits of the 8-bit write corresponds to one switch of the device. A Logic 1 in the particular bit position turns the switch on, whereas a Logic 0 turns the switch off. Because an individual bit independently controls each switch, this independence provides the option of having any, all, or none of the switches turned on.

SERIAL INTERFACE

The **ADG1414** has a 3-wire serial interface ($\overline{\text{SYNC}}$, SCLK, and DIN pins) that is compatible with SPI, QSPI, and MICROWIRE interface standards, as well as most DSPs. See Figure 2 for a timing diagram of a typical write sequence.

The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low, which enables the input shift register. Data from the DIN line is clocked into the 8-bit input shift register on the falling edge of SCLK. The serial clock frequency can be as high as 50 MHz, making the **ADG1414** compatible with high speed DSPs.

Data can be written to the shift register in more or less than eight bits. In each case, the shift register retains the last eight bits that were written. When all eight bits have been written into the shift register, the $\overline{\text{SYNC}}$ line is brought high again. The switches are updated with the new configuration, and the input shift register is disabled. With $\overline{\text{SYNC}}$ held high, the input shift register is disabled; therefore, further data or noise on the DIN line has no effect on the shift register.

Data appears on the SDO pin on the rising edge of SCLK suitable for daisy chaining or readback, delayed by eight bits.

INPUT SHIFT REGISTER

The input shift register is eight bits wide (see Table 10). Each bit controls one switch. These data bits are transferred to the switch register on the rising edge of $\overline{\text{SYNC}}$.

Table 10. **ADG1414 Input Shift Register Bit Map¹**

MSB				LSB			
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
S8	S7	S6	S5	S4	S3	S2	S1

¹ Logic 0 = switch off, and Logic 1 = switch on.

POWER-ON RESET

The **ADG1414** contains a power-on reset circuit. On power-up of the device, all switches are in the off condition and the internal shift register is filled with zeros and remains so until a valid write takes place.

The device also has a $\overline{\text{RESET}}/\text{V}_\text{L}$ pin. Under normal operation, drive the $\overline{\text{RESET}}/\text{V}_\text{L}$ pin with a 2.7 V to 5 V supply and pull the pin low for short period of time (15 ns is sufficient) to complete the hardware reset.

When using the $\overline{\text{RESET}}/\text{V}_\text{L}$ pin to do a hardware reset, drive all other SPI pins ($\overline{\text{SYNC}}$, SCLK, and DIN) low. This is to prevent current flow due to ESD protection diodes on the V_L pin to the SPI pins.

When the $\overline{\text{RESET}}/\text{V}_\text{L}$ pin is low, all switches are off and the appropriate registers are cleared to 0.

DAISY CHAINING

For systems that contain several switches, the SDO pin can be used to daisy-chain several devices together. The SDO pin can also be used for diagnostic purposes and provide serial readback, wherein the user can read back the switch contents.

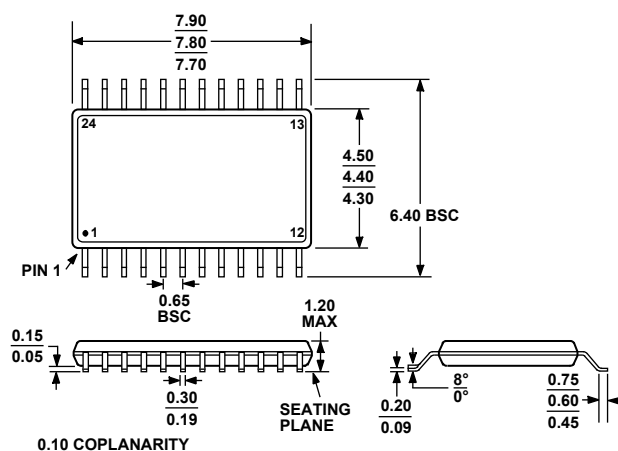
SDO is an open-drain output that must be pulled to the V_L supply with an external resistor.

The SCLK is continuously applied to the input shift register when $\overline{\text{SYNC}}$ is low. If more than eight clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge. By connecting this line to the DIN input on the next device in the chain, a multiswitch interface is constructed. Each device in the system requires eight clock pulses; therefore, the total number of clock cycles must equal 8N, where N is the total number of devices in the chain.

When the serial transfer to all devices is complete, $\overline{\text{SYNC}}$ is taken high. This prevents any further data from being clocked into the input shift register.

The serial clock can be a continuous or a gated clock. A continuous SCLK source can be used only if $\overline{\text{SYNC}}$ can be held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and $\overline{\text{SYNC}}$ must be taken high after the final clock to latch the data. Gated clock mode reduces power consumption by reducing the active clock time.

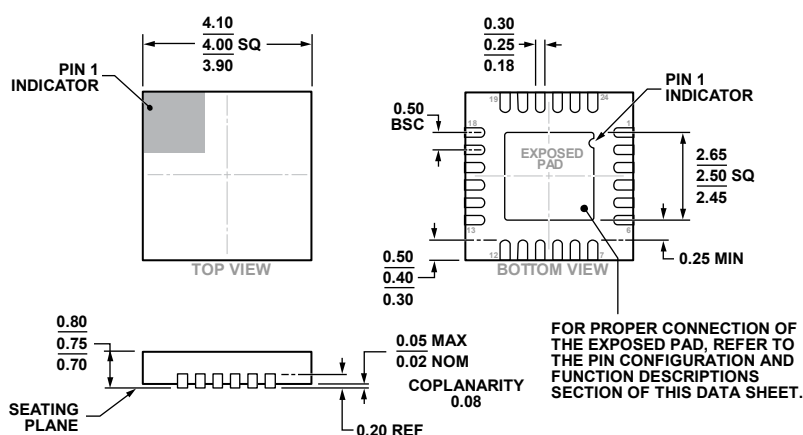
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AD

Figure 32. 24-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-24)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD.

Figure 33. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-24-7)

Dimensions shown in millimeters

03-11-2013-A

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADG1414BRUZ	−40°C to +125°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
ADG1414BRUZ-REEL7	−40°C to +125°C	24-Lead Thin Shrink Small Outline Package [TSSOP]	RU-24
ADG1414BCPZ-REEL7	−40°C to +125°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-7

¹ Z = RoHS Compliant Part.