TABLE OF CONTENTS

REVISION HISTORY

5/2016—Rev. 0 to Rev. A

Change CP-8-2 to CP-8-13 ... Throughout
Changes to Figure 1 ... 1
Changes to Figure 4 ... 6
Updated Outline Dimensions ... 19
Changes to Ordering Guide ... 19

10/2005—Revision 0: Initial Version

SPECIFICATIONS

V_S = ±12 V, T_A = 25°C, R_L = 1 kΩ, $\overline{DIS}$ = high, C_L = 3 pF, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +2, V_O = 0.2 V p-p, differential	34	38		MHz
	G = +2, V_O = 40 V p-p, differential	6.5	7.2		MHz
Overdrive Recovery Time	V_{S+} + 0.5 V to V_{S-} − 0.5 V; +recovery/−recovery		180/330		ns
Slew Rate	$V_{O, dm}$ = 2 V step		260		V/µs
	$V_{O, dm}$ = 40 V step		730		V/µs
Settling Time to 0.01%	$V_{O, dm}$ = 40 V step		580		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion	f_C = 5 kHz, V_O = 40 V p-p, R_L = 2 kΩ, HD2/HD3		−116/−109		dBc
	f_C = 100 kHz, V_O = 40 V p-p, R_L = 2 kΩ, HD2/HD3		−99/−100		dBc
Differential Output Voltage Noise	f = 100 kHz		12		nV/√Hz
Input Current Noise	f = 100 kHz		1.4		pA/√Hz
DC PERFORMANCE					
Differential Output Offset Voltage			0.35	1.1	mV
Differential Output Offset Voltage Drift			14		µV/°C
Input Bias Current			1.8	3.5	µA
Gain			2		V/V
Gain Error			−0.05		%
Gain Error Drift			0.0002		%/°C
INPUT CHARACTERISTICS					
Input Resistance			11		MΩ
Input Capacitance			1		pF
Input Voltage Range			±10.7		V
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Each single-ended output, R_L = 1 kΩ	±10.65	±10.7		V
DC Output Current			40		mA
Capacitive Load Drive	30% overshoot		20		pF
POWER SUPPLY					
Operating Range		5		26	V
Quiescent Current			9.4	10.1	mA
Quiescent Current (Disabled)			1.5	2.0	mA
Power Supply Rejection Ratio (PSRR)					
−PSRR			−89	−80	dB
+PSRR			−91	−83	dB
DISABLE					
$\overline{DIS}$ Input Voltage Threshold	Disabled		≤ −11		V
	Enabled		≥ −9		V
Turn-Off Time			160		µs
Turn-On Time			78		ns
$\overline{DIS}$ Bias Current					
Enabled	$\overline{DIS}$ = −9 V		114		µA
Disabled	$\overline{DIS}$ = −11 V		−125		µA

V_S = ±5 V, T_A = 25°C, R_L = 1 kΩ, $\overline{DIS}$ = high, C_L = 3 pF, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +2, V_O = 0.2 V p-p, differential	36	40.5		MHz
	G = +2, V_O = 12 V p-p, differential	6.5	13.5		MHz
Overdrive Recovery Time	+Recovery/−Recovery		200/670		ns
Slew Rate	$V_{O, dm}$ = 2 V step		220		V/µs
	$V_{O, dm}$ = 12 V step		350		V/µs
Settling Time to 0.01%	$V_{O, dm}$ = 12 V step		200		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion	f_C = 5 kHz, V_O = 12 V p-p, R_L = 2 kΩ, HD2/HD3		−102/−108		dBc
	f_C = 100 kHz, V_O = 12 V p-p, R_L = 2 kΩ, HD2/HD3		−101/−98		dBc
Differential Output Voltage Noise	f = 100 kHz		12		nV/√Hz
Input Current Noise	f = 100 kHz		1.4		pA/√Hz
DC PERFORMANCE					
Differential Output Offset Voltage			0.4	1.2	mV
Differential Output Offset Voltage Drift			12		µV/°C
Input Bias Current			2.0	3.5	µA
Gain			2		V/V
Gain Error			−0.05		%
Gain Error Drift			0.0002		%/°C
INPUT CHARACTERISTICS					
Input Resistance			11		MΩ
Input Capacitance			1		pF
Input Voltage Range			±3.6		V
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Each single-ended output, R_L = 1 kΩ	±3.55	±3.6		V
DC Output Current			40		mA
Capacitive Load Drive	30% overshoot		20		pF
POWER SUPPLY					
Operating Range		5		26	V
Quiescent Current			7.0	7.6	mA
Quiescent Current (Disabled)			0.7	1.6	mA
Power Supply Rejection Ratio (PSRR)					
−PSRR			−93	−82	dB
+PSRR			−91	−83	dB
DISABLE					
$\overline{DIS}$ Input Voltage	Disabled		≤ −4		V
	Enabled		≥ −2		V
Turn-Off Time			160		µs
Turn-On Time			78		ns
$\overline{DIS}$ Bias Current					
Enabled	$\overline{DIS}$ = −2 V		41		µA
Disabled	$\overline{DIS}$ = −4 V		49		µA

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	26 V
Power Dissipation	See Figure 3
Storage Temperature Range	–65°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for a device soldered in the circuit board with its exposed paddle soldered to a pad on the PCB surface that is thermally connected to a copper plane, with zero airflow.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC with EP on 4-Layer Board	79	25	°C/W
8-Lead LFCSP with EP on 4-Layer Board	81	17	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the ADA4922-1 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4922-1. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The power dissipated due to the load drive depends upon the particular application. For each output, the power due to load drive is calculated by multiplying the load current by the associated voltage drop across the device. The power dissipated due to all of the loads is equal to the sum of the power dissipation due to each individual load. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}. The exposed paddle on the underside of the package must be soldered to a pad on the PCB surface that is thermally connected to a copper plane to achieve the specified θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the packages vs. the ambient temperature for the 8-lead SOIC (79°C/W) and for the 8-lead LFCSP (81°C/W) on a JEDEC standard 4-layer board, each with its underside paddle soldered to a pad that is thermally connected to a PCB plane. θ_{JA} values are approximations.

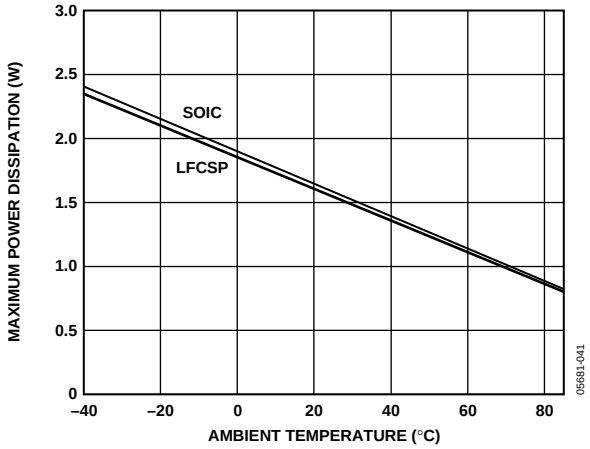


Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

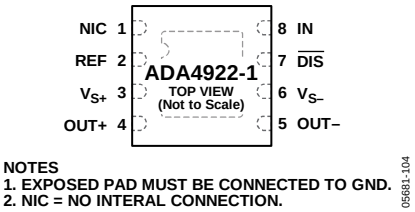


Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NIC	No Internal Connection
2	REF	Reference Voltage for Single-Ended Input Signal
3	V_{S+}	Positive Power Supply
4	OUT+	Noninverting Side of Differential Output
5	OUT−	Inverting Side of Differential Output
6	V_{S-}	Negative Power Supply
7	$\overline{DIS}$	Disable
8	IN	Single-Ended Signal Input

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, V_S = ±12 V, $R_{L, dm}$ = 1 kΩ, REF = 0 V, $\overline{DIS}$ = high, T_A = 25°C.

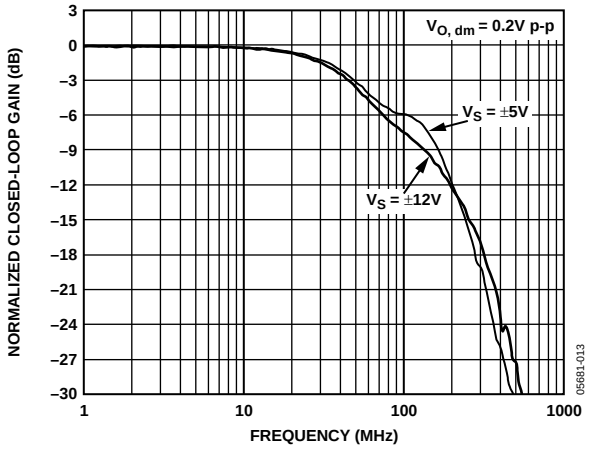


Figure 5. Small Signal Frequency Response for Various Power Supplies

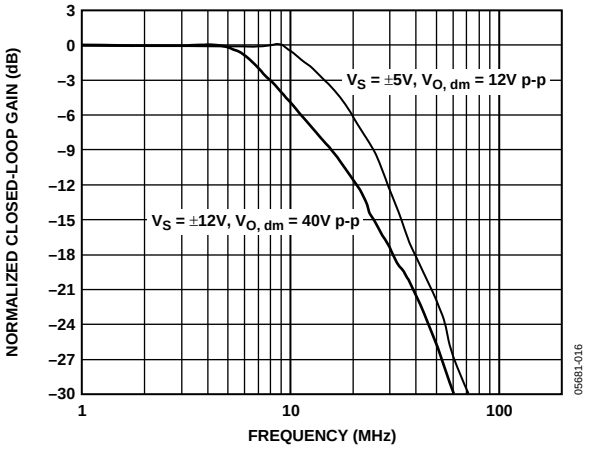


Figure 8. Large Signal Frequency Response for Various Power Supplies

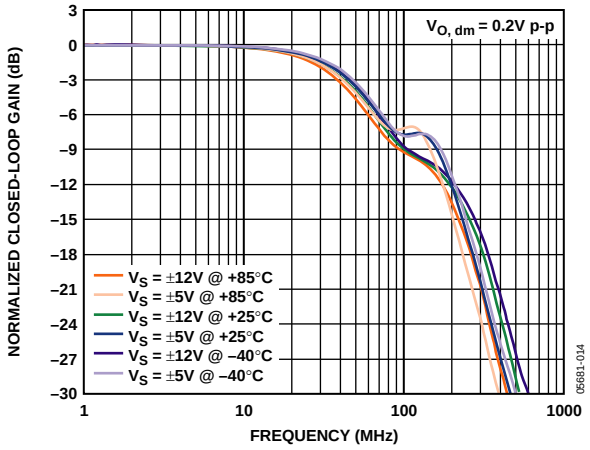


Figure 6. Small Signal Frequency Response for Various Temperatures and Supplies

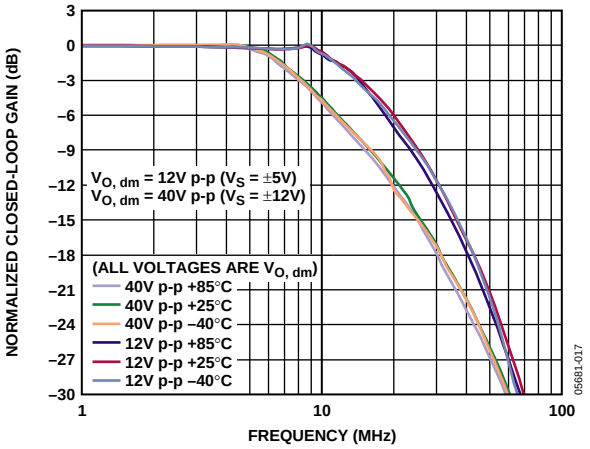


Figure 9. Large Signal Frequency Response at Various Temperatures and Supplies

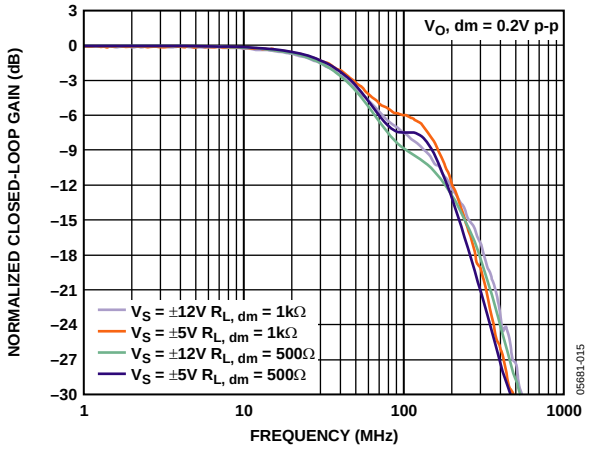


Figure 7. Small Signal Frequency Response for Various Resistive Loads and Supplies

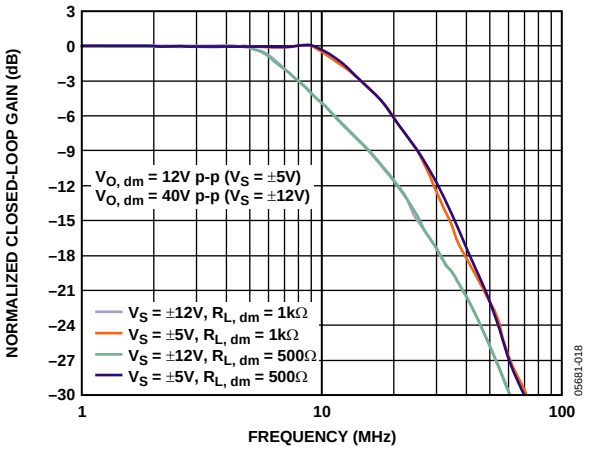


Figure 10. Large Signal Frequency Response for Various Resistive Loads and Supplies

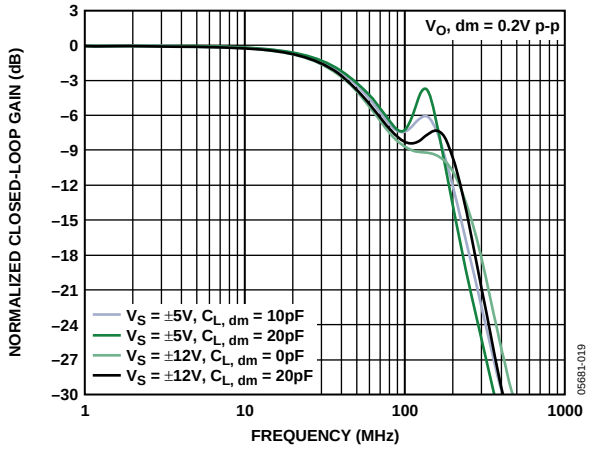


Figure 11. Small Signal Frequency Response for Various Capacitive Loads

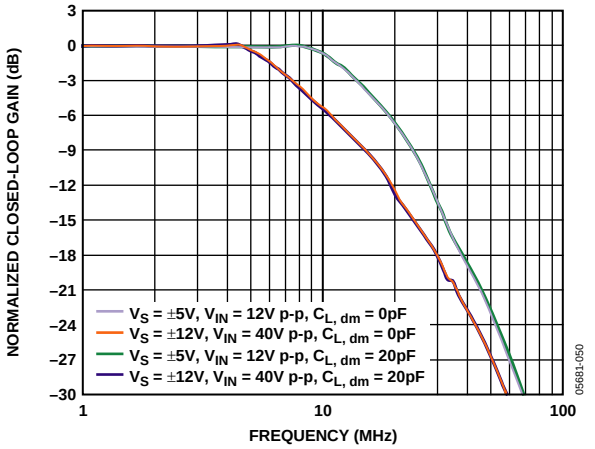


Figure 14. Large Signal Frequency Response for Various Capacitive Loads

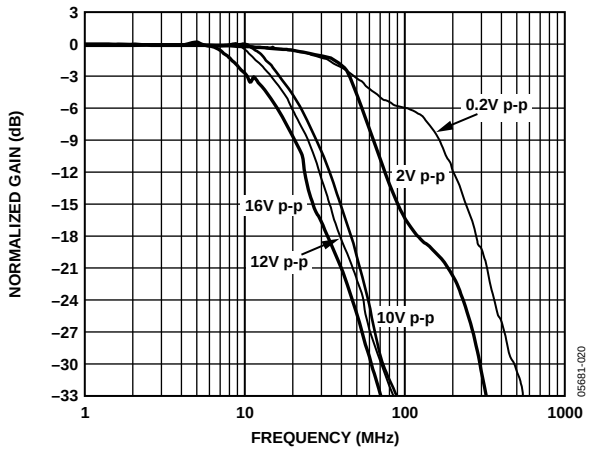


Figure 12. Frequency Response for Various Output Amplitudes, V_S = ±5 V

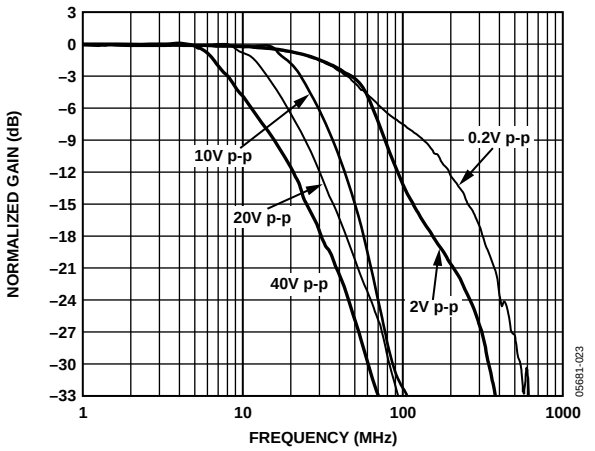


Figure 15. Frequency Response for Various Output Amplitudes, V_S = ±12 V

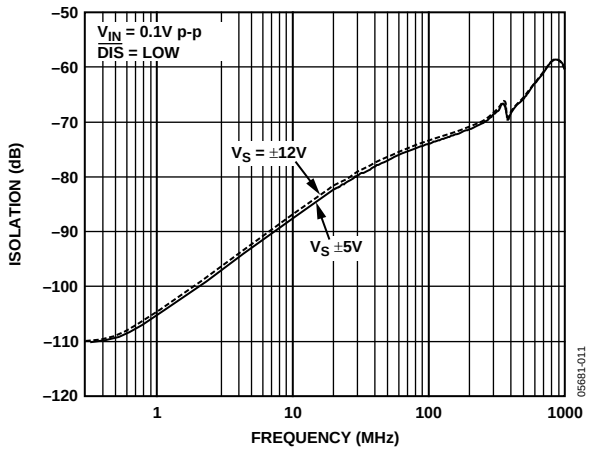


Figure 13. Isolation vs. Frequency—Disabled

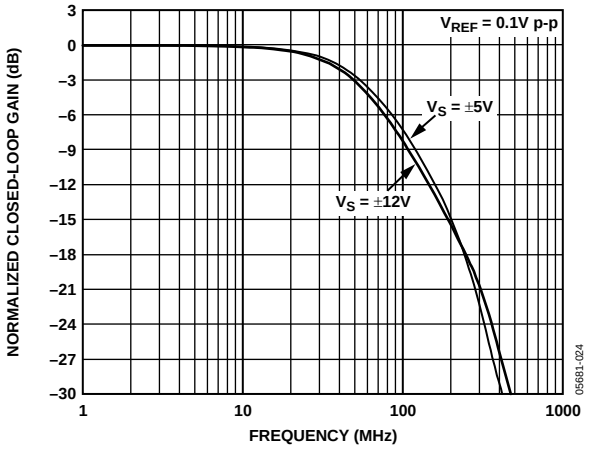


Figure 16. REF Small Signal Frequency Response for Various Power Supplies

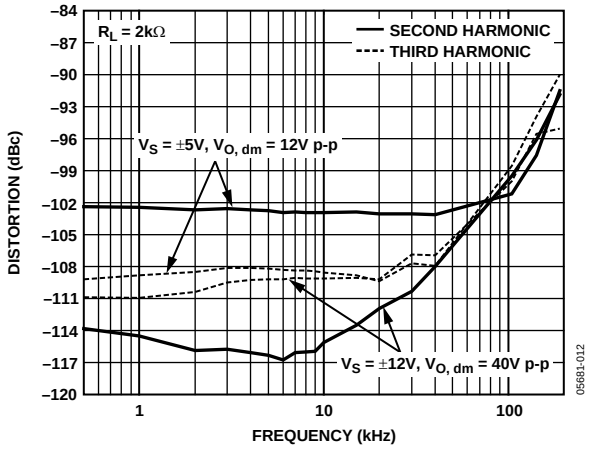


Figure 17. Harmonic Distortion for Various Power Supplies

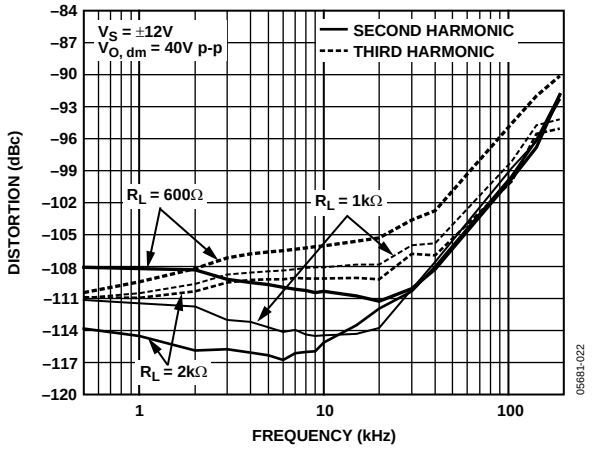


Figure 20. Harmonic Distortion for Various Loads

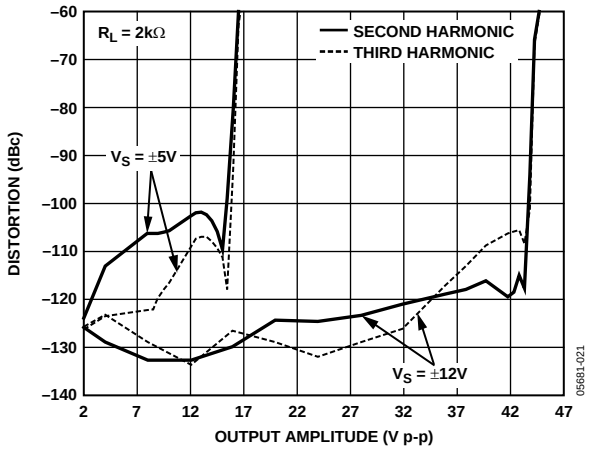


Figure 18. Harmonic Distortion vs. Output Amplitude and Supply Voltage (f = 10 kHz)

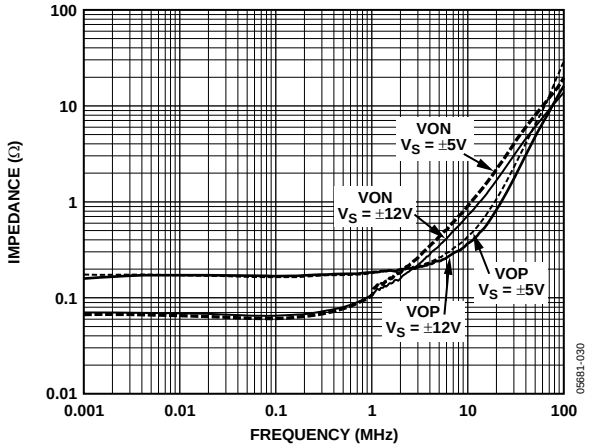


Figure 21. Single-Ended Output Impedance vs. Frequency and Supplies

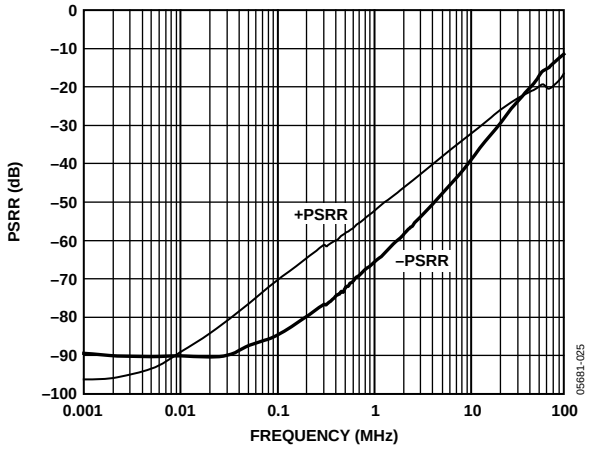


Figure 19. PSRR vs. Frequency

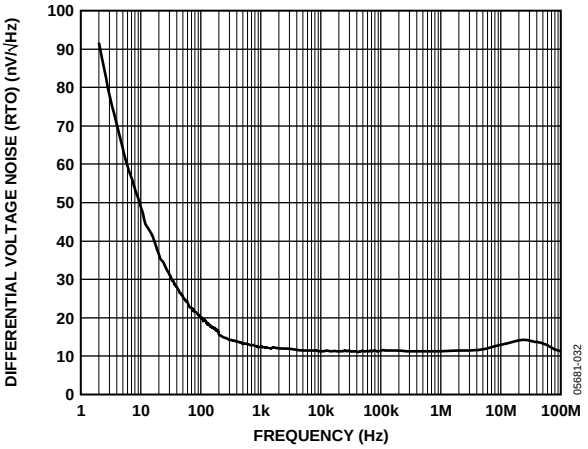


Figure 22. Differential Output Noise vs. Frequency

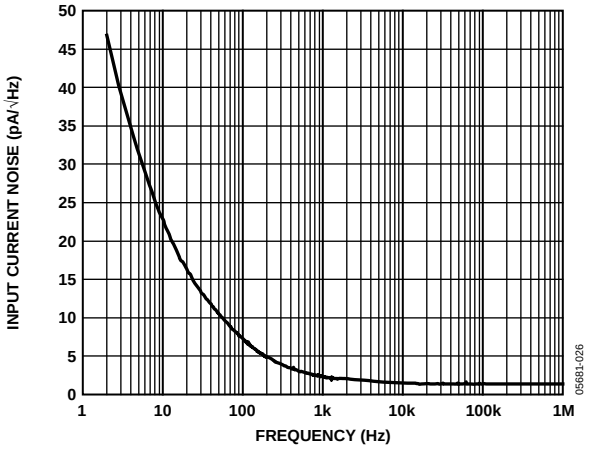


Figure 25. Input Current Noise vs. Frequency

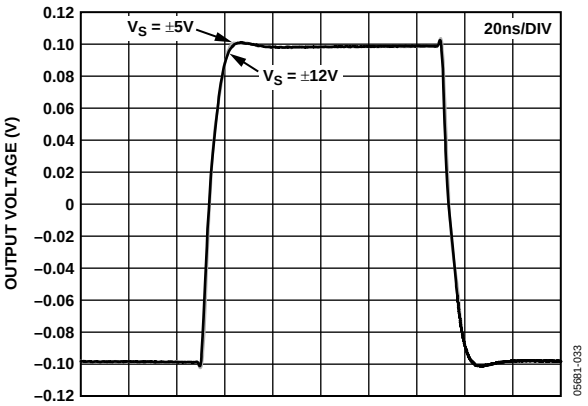


Figure 23. Small Signal Transient Response for Various Power Supplies

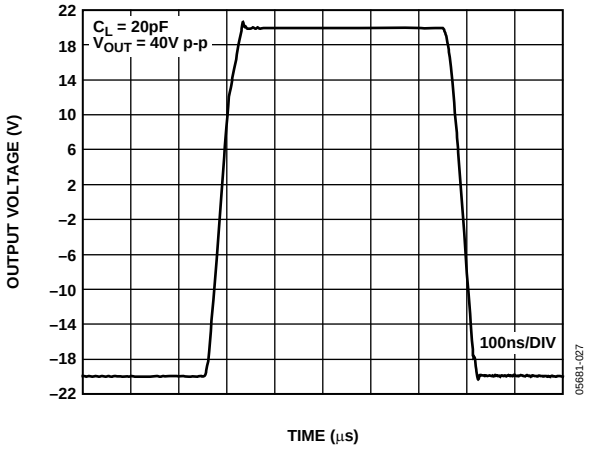


Figure 26. Large Signal Transient Response for Various Power Supplies

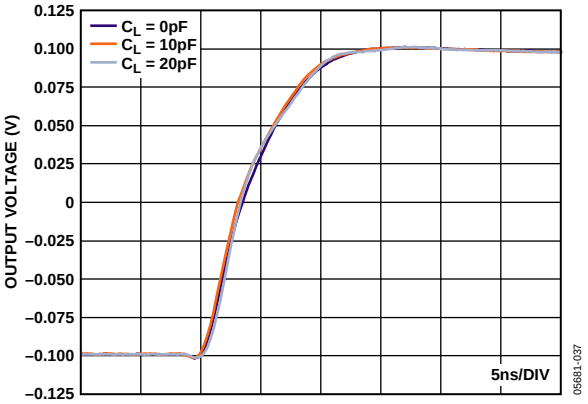


Figure 24. Small Signal Transient Response for Various Capacitive Loads

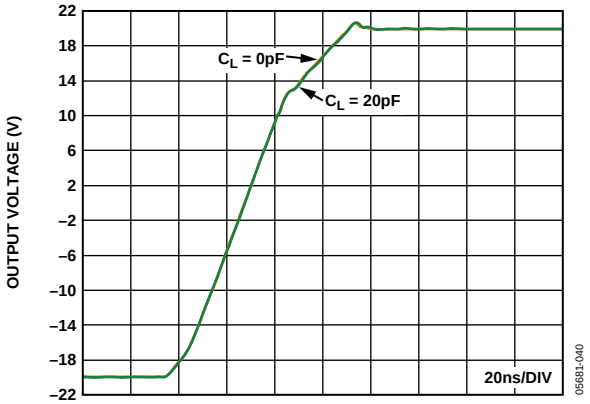


Figure 27. Large Signal Transient Response for Various Capacitive Loads

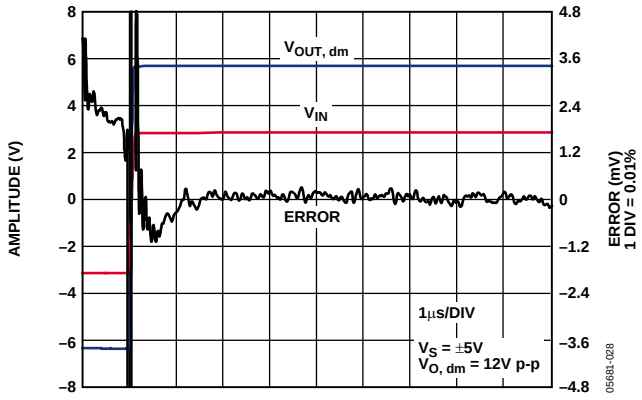


Figure 28. Settling Time, $V_S = \pm 5$ V

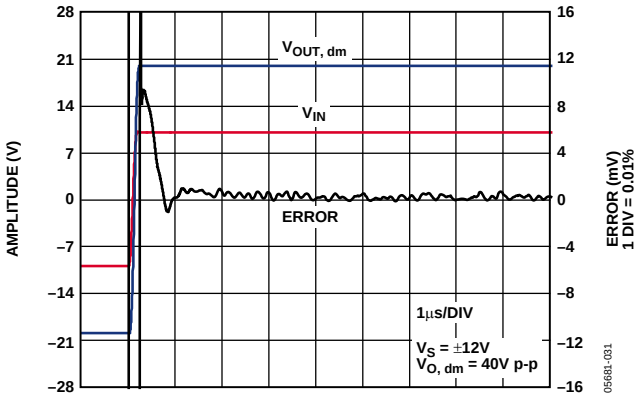


Figure 31. Settling Time, $V_S = \pm 12$ V

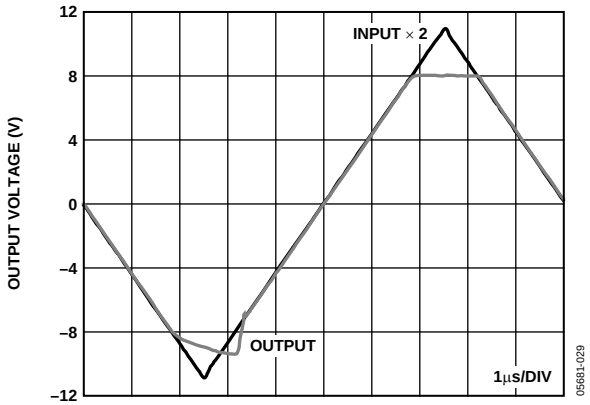


Figure 29. Input Overdrive Recovery, $V_S = \pm 5$ V

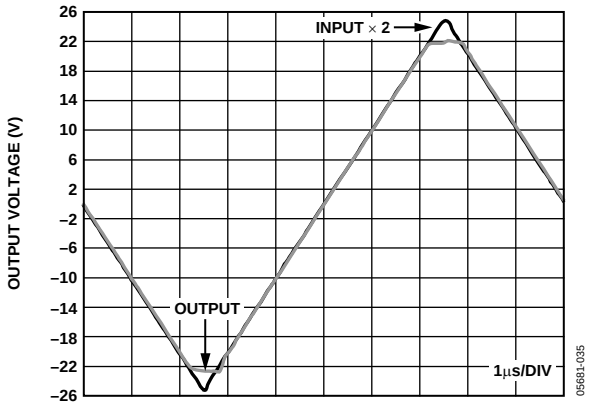


Figure 32. Input Overdrive Recovery, $V_S = \pm 12$ V

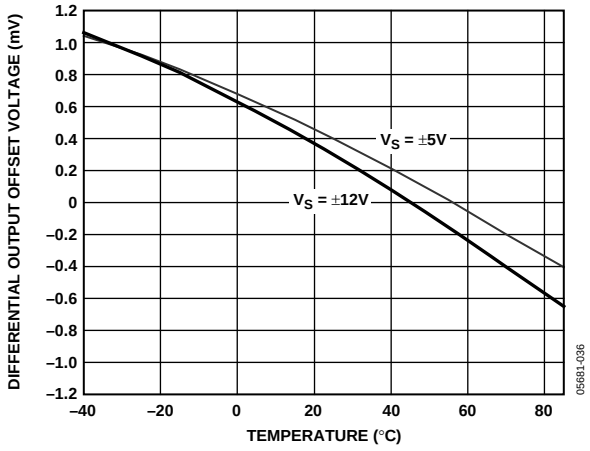


Figure 30. Differential Output Offset Voltage vs. Temperature

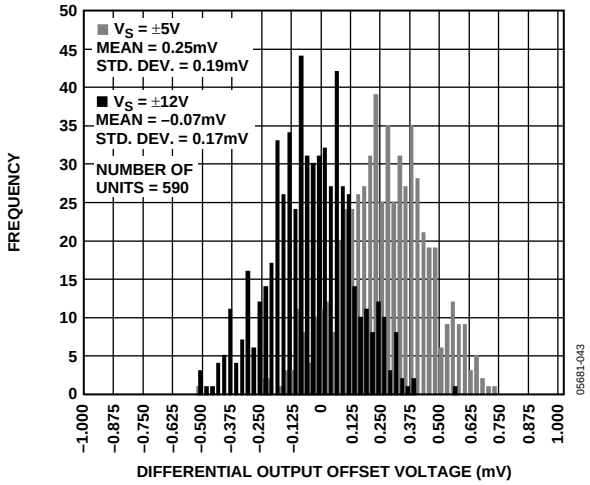


Figure 33. Differential Output Offset Voltage Distribution

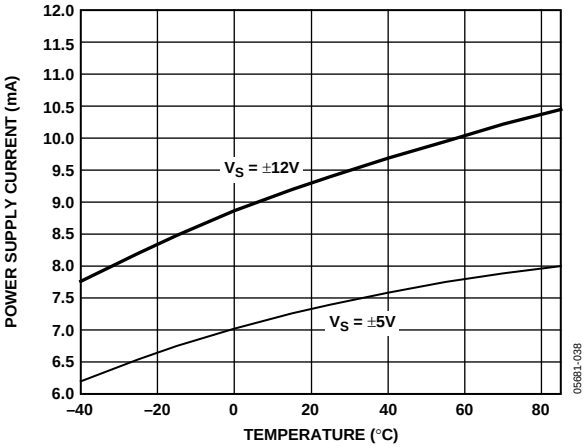


Figure 34. Power Supply Current vs. Temperature

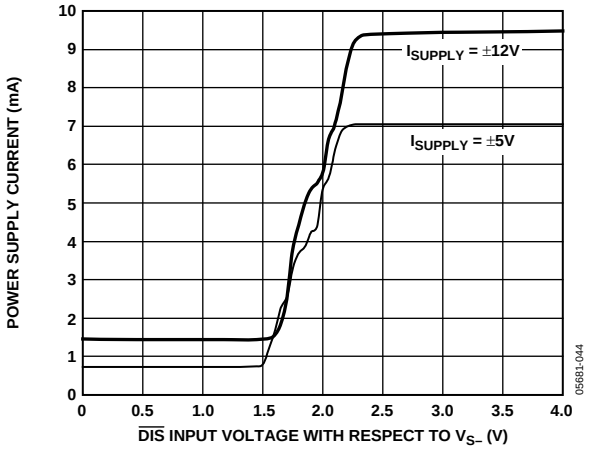


Figure 37. Power Supply Current vs. Disable Input Voltage

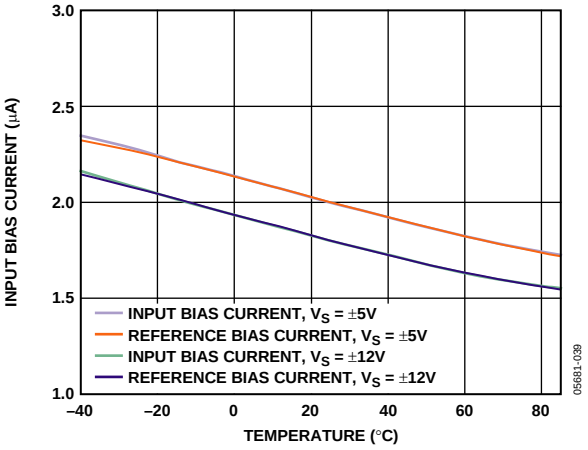


Figure 35. Input Bias Current vs. Temperature

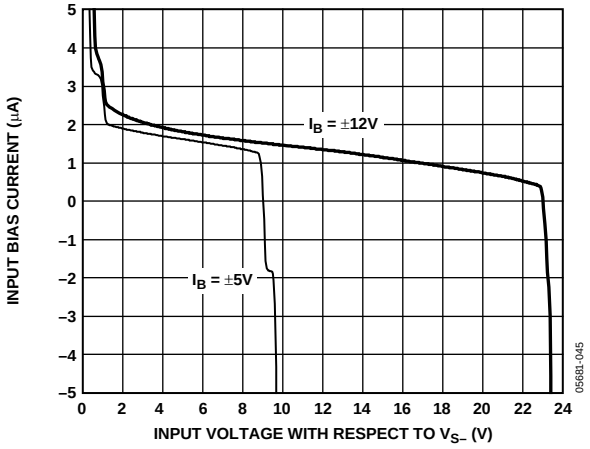


Figure 38. Input Bias Current vs. Input Voltage

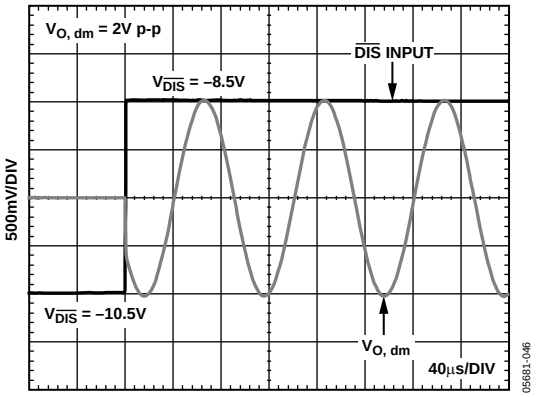


Figure 36. Disable Turn-On Time

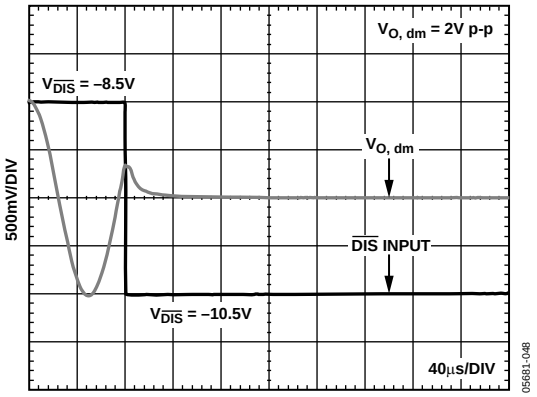


Figure 39. Disable Turn-Off Time

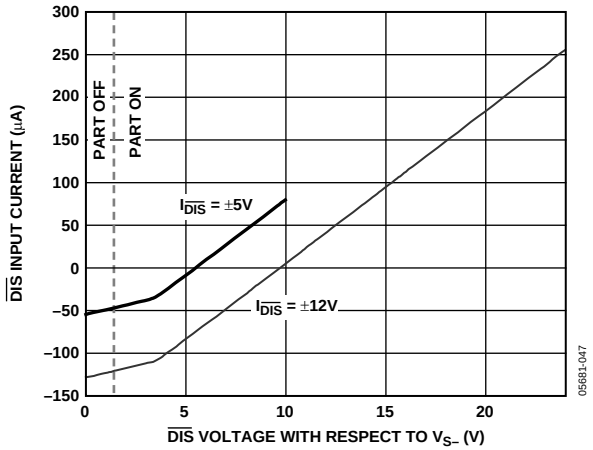


Figure 40. Disable Current vs. Disable Voltage

THEORY OF OPERATION

The ADA4922-1 is dual amplifier that has been optimized to drive a differential ADC from a single-ended input source with a minimum number of external components (see Figure 41).

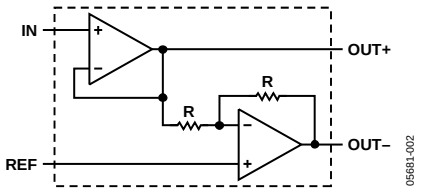


Figure 41. Functional Diagram

The differential output voltage is defined as

$$V_{O,\,dm} = V_{OUT+} - V_{OUT-} \quad (1)$$

Each amplifier in Figure 41 is identical, and the value of Resistor R is set at 600 Ω, yielding an optimal trade-off between output differential noise, internal power dissipation, and overall system linearity. For basic operation, the REF input is tied to the midswing level of the input signal, which is often midsupply. The input signal (referenced to REF) produces a differential output signal with an overall gain of +2. Figure 42 shows typical operation on ±12 V supplies with the source referenced to 0 V and the REF pin tied to 0 V.

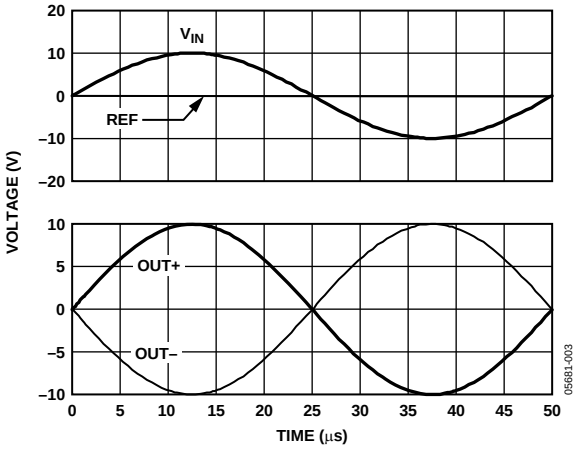


Figure 42. Typical Input/Output Response—Centered Reference

If an application uses an input midswing voltage other than midsupply, the REF pin needs to be offset to the input midswing level to obtain outputs that do not exhibit a differential offset (see Figure 43). If the voltage applied to the REF pin is different from the midswing level of the input signal, a dc offset is created between outputs V_{OUT+} and V_{OUT-}. Figure 44 illustrates this condition when the input signal is referenced to a positive level, and the REF pin is connected to 0 V.

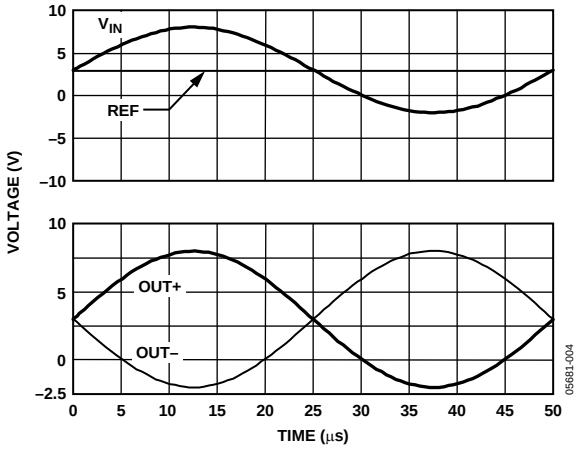


Figure 43. Typical Input/Output Response—Equal Input/Reference

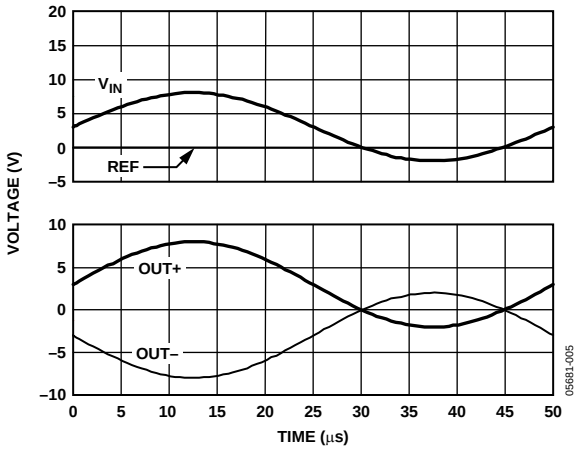


Figure 44. Typical Input/Output Response—Unequal Input/Reference

A more detailed view of the amplifier is shown in Figure 45. Each amplifier is a 2-stage design that uses an input H-Bridge followed by a rail-to-rail output stage (see Figure 46).

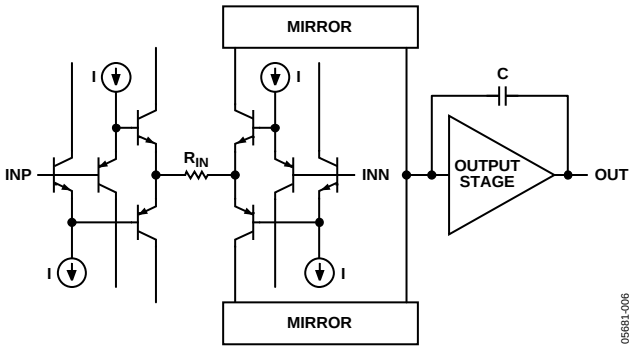


Figure 45. Internal Amplifier Architecture

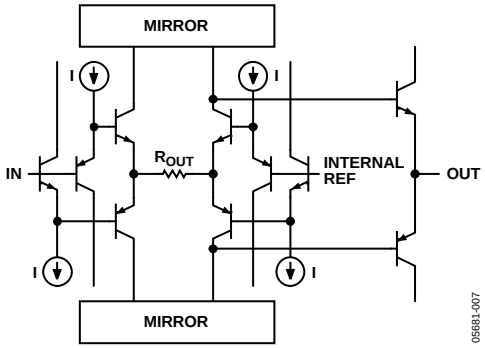


Figure 46. Output Stage Architecture

Figure 47 illustrates the open-loop gain and phase relationships of each amplifier in the ADA4922-1.

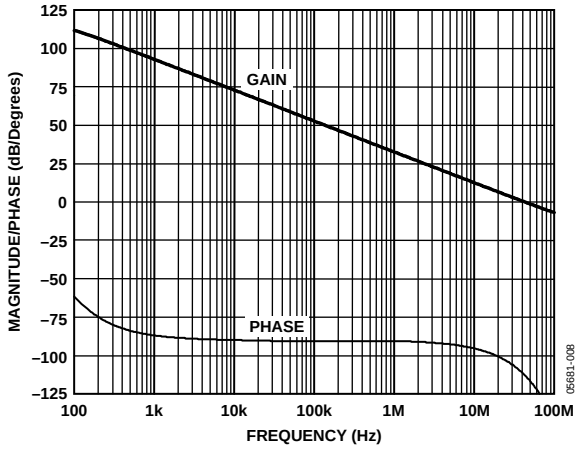


Figure 47. Amplifier Gain/Phase Relationship

The architecture used in the ADA4922-1 results in excellent SNR and distortion performance when compared to other differential amplifiers.

One of the more subtle points of operation arises when the two amplifiers are used to generate the differential outputs. Because the differential outputs are derived from a follower amplifier and an inverting amplifier, they have different noise gains and, therefore, different closed-loop bandwidths. For frequencies up to 1 MHz, the bandwidth difference between outputs causes little difference in the overall differential output performance. However, because the bandwidth is the sum of both amplifiers, the 3 dB point of the inverting amplifier defines the overall differential 3 dB corner (see Figure 48).

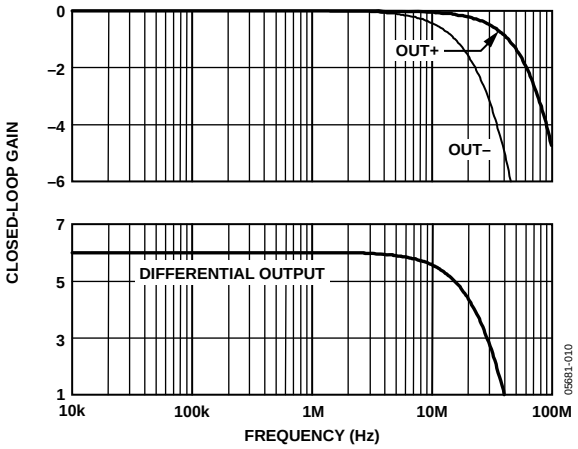


Figure 48. Closed-Loop AC Gain (Differential Outputs)

Small delay and gain errors exist between the two outputs because the inverting output is derived from the noninverting output through an inverting amplifier. The gain error is due to imperfect matching of the inverting amplifier gain and feedback resistors, as well as differences in the transfer functions of the two amplifiers, as illustrated in Figure 48. The delay error is due to the delay through the inverting amplifier relative to the noninverting amplifier output. The delay produces a reduction in differential gain because the two outputs are not exactly 180° out of phase. Both of these errors combine to produce an overall gain error because the outputs are completely balanced. This error is very small at the frequencies involved in most ADA4922-1 applications.

APPLICATIONS INFORMATION

The ADA4922-1 is a fixed-gain, single-ended-to-differential voltage amplifier, optimized for driving high resolution ADCs in high voltage applications. There are no gain adjustments available to the user.

ADA4922-1 DIFFERENTIAL OUTPUT NOISE MODEL

The principal noise sources in a typical ADA4922-1 application circuit are shown in Figure 49.

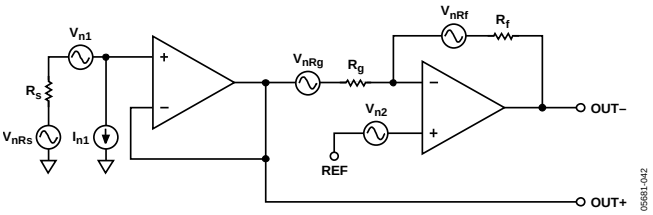


Figure 49. ADA4922-1 Differential Output Noise Model

Using the traditional approach, a noise source is applied in series with one of the inputs of each op amp to model input-referred voltage noise. The input current noise that matters the most is present at the input pin. The output voltage noise due to this noise current depends on the source resistance feeding the input, as well as the downstream gain in the amplifier. Resistor noise is modeled by placing a noise voltage source in series with a noiseless resistor. R_f and R_g are both 600 Ω and therefore have the same noise voltage density.

At room temperature,

$$V_{nRg} = V_{nRf} = \sqrt{4\text{ kT}(600\ \Omega)} \approx 3.2\text{ nV}/\sqrt{\text{Hz}} \quad (2)$$

The noise at OUT+ is due to the input-referred current and voltage noise sources of the noninverting amplifier and the noise of the source resistance, all reflected to the output with a noise gain of 1, and is equal to:

$$\textit{Voltage Noise @ OUT+: } V_{n1} + R_S(I_{n1}) + V_{nRs} \quad (3)$$

where R_S is the source resistance feeding the input, and V_{nRs} is the source resistance noise.

The noise at OUT– originates from a number of sources:

$$\textit{Voltage Noise @ OUT– due to } V_{n1}\text{: } V_{n1}\left(\frac{-R_f}{R_g}\right) = -V_{n1} \quad (4)$$

$$\textit{Voltage Noise @ OUT– due to } I_{n1}\text{: } R_S(I_{n1})\left(\frac{-R_f}{R_g}\right) = -R_S(I_{n1}) \quad (5)$$

$$\textit{Voltage Noise @ OUT– due to } R_S\text{: } V_{nRs}\left(\frac{-R_f}{R_g}\right) = -V_{nRs} \quad (6)$$

$$\textit{Voltage Noise @ OUT– due to } V_{nRg}\text{: } V_{nRg}\left(\frac{-R_f}{R_g}\right) = -V_{nRg} \quad (7)$$

$$\textit{Voltage Noise @ OUT– due to } V_{nRf}\text{: } V_{nRF} \quad (8)$$

$$\textit{Voltage Noise @ OUT– due to } V_{n2}\text{: } V_{n2}\left(1+\frac{R_f}{R_g}\right) = 2V_{n2} \quad (9)$$

When looking at OUT– by itself, the contributing noise sources are uncorrelated, and therefore, the total output noise is calculated as the root-sum-square (rss) of the individual contributors. When looking at the differential output noise, the noise contributors are uncorrelated except for three, V_{n1}, $R_S(I_{n1})$, and V_{nRs}, which are common noise sources for both outputs. It can be seen from the previous results that the output noise due to V_{n1}, $R_S(I_{n1})$, and V_{nRs} each appear at OUT+ with a gain of +1 and at OUT– with a gain of –1. This produces a gain of 2 for each of these three sources at the differential output.

The total differential output noise density is calculated as

$$V_{on,\,dm} = \sqrt{\left(2\left(V_n + R_s(1.4\text{ pA}/\sqrt{\text{Hz}}) + V_{nRs}\right)\right)^2 + 2\left(3.2\text{ nV}/\sqrt{\text{Hz}}\right)^2 + 4V_n^2} \quad (10)$$

where $V_{n1} = V_{n2} \equiv V_n = 3.9\text{ nV}/\sqrt{\text{Hz}}$; the input referred voltage noise of each amplifier is the same.

The output noise due to the amplifier alone is calculated by setting R_S and V_{nRs} equal to zero. In this case:

$$V_{on,\,dm} = 12\text{ nV}/\sqrt{\text{Hz}} \quad (11)$$

Clearly, the output noise is not balanced between the outputs, but this is not an issue in most applications.

USING THE REF PIN

The REF pin sets the output baseline in the inverting path and is used as a reference for the input signal. In most applications, the REF pin is set to the input signal midswing level, which in many cases is also midsupply. For bipolar signals and power supplies, REF is generally set to ground. In single-supply applications, setting REF to the input signal midswing level provides optimal output dynamic range performance with minimum differential offset. Note that the REF input only affects the inverting signal path, or OUT–.

Most applications require a differential output signal with the same dc common-mode level on each output. It is possible for the signal measured across OUT+ and OUT– to have a common-mode voltage that is of the desired level but has different dc levels at both outputs. Typically, this situation is avoided, because it wastes the output dynamic range of the amplifier.

Defining V_{IN} as the voltage applied to the input pin, the equations that govern the two signal paths are given in Equation 12 and Equation 13.

$$V_{OUT+} = +V_{IN} \quad (12)$$

$$V_{OUT-} = -V_{IN} + 2(REF) \quad (13)$$

When the REF voltage is set to the midswing level of the input signal, the two output signals fall directly on top of each other with minimal offset. Setting the REF voltage elsewhere results in an offset between the two outputs. This effect is illustrated in the Theory of Operation section.

The best use of the REF pin can be further illustrated by considering a single-supply example that uses a 10 V dc power supply and has an input signal that varies between 2 V and 7 V. This is a case where the midswing level of the input signal is not at midsupply but is at 4.5 V. By setting the REF input to 4.5 V and neglecting offsets, Equation 12 and Equation 13 are used to calculate the results. When the input signal is at its midpoint of 4.5 V, V_{OUT+} is at 4.5 V, as is V_{OUT-}. This can be considered as a type of baseline state where the differential output voltage is zero. When the input increases to 7 V, V_{OUT+} tracks the input to 7 V and V_{OUT-} decreases to 2 V. This can be viewed as a positive peak signal where the differential output voltage equals 5 V. When the input signal decreases to 2 V, V_{OUT+} again tracks to 2 V, and V_{OUT-} increases to 7 V. This can be viewed as a negative peak signal where the differential output voltage equals −5 V. The resulting differential output voltage is 10 V p-p.

The previous discussion exposes how the single-ended-to-differential gain of 2 is achieved.

INTERNAL FEEDBACK NETWORK POWER DISSIPATION

While traditional op amps do not have on-chip feedback elements, the ADA4922-1 contains two on-chip 600 Ω resistors that comprise an internal feedback loop. The power dissipated in these resistors must be included in the overall power dissipation calculations for the device. Under certain circumstances, the power dissipated in these resistors could be considerably more than the quiescent current of the device. For example, on ±12 V supplies with the REF pin tied to ground and OUT– at 9 V dc, each 600 Ω resistor carries 15 mA and dissipates 135 mW. This is a significant amount of power and must therefore be included in the overall device power dissipation calculations. For ac signals, rms analysis is required.

DISABLE FEATURE

The ADA4922-1 includes a disable feature that can be asserted to minimize power consumption in a device that is not needed at a particular time. When asserted, the disable feature does not place the device output in a high impedance or three-state condition. The disable feature is asserted by applying a control voltage to the $\overline{DIS}$ pin and is active low. See the Specifications section for the high and low level voltage specifications.

DRIVING A DIFFERENTIAL INPUT ADC

The ADA4922-1 provides the single-ended-to-differential conversion that is required to drive most high resolution ADCs. Figure 50 shows how the ADA4922-1 simplifies ADC driving.

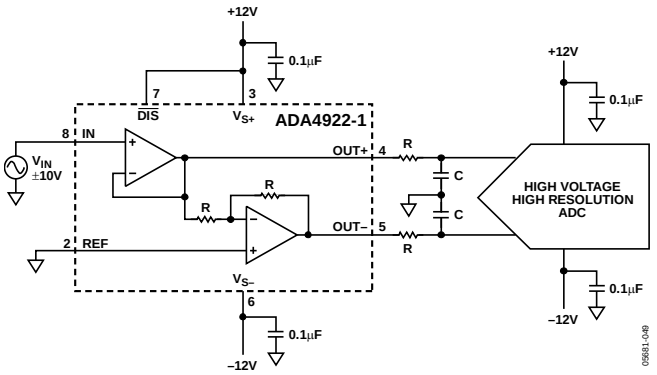


Figure 50. Driving a Differential Input ADC

For example, consider the case where the input signal bandwidth is 100 kHz and R = 41.2 Ω and C = 3.9 nF, as is shown in Figure 50, to form a single-pole filter with −3 dB bandwidth of approximately 1 MHz. The ADA4922-1 output noise (with zero source resistance) integrated over this bandwidth appears at the ADC input and is calculated as

$$V_{n,\,ADC,dm}(rms) = \left(12\,\text{nV}/\sqrt{\text{Hz}}\right)\sqrt{\left(\frac{\pi}{2}\right)\left(1\,\text{MHz}\right)} = 15\,\mu\text{V rms} \quad (14)$$

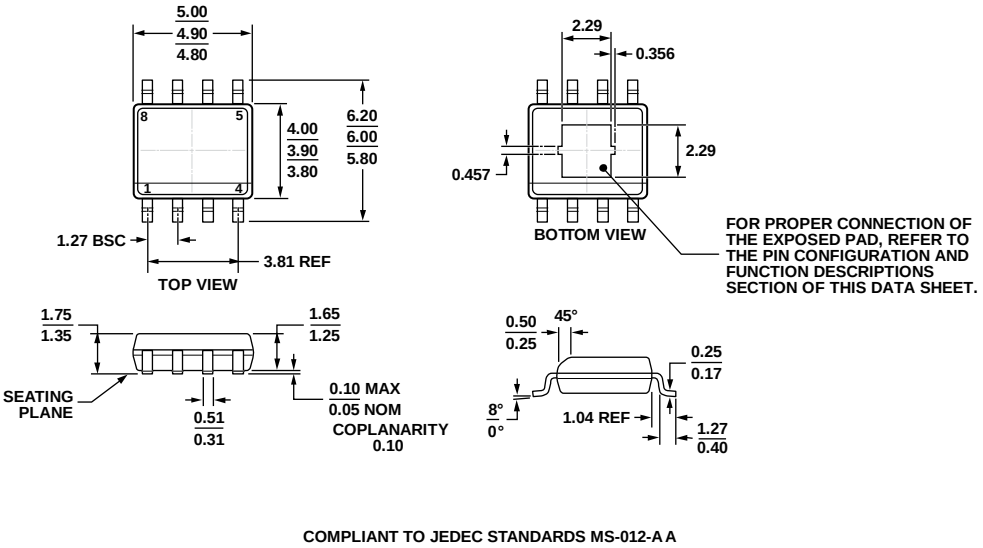
The rms value of a 20 V p-p signal at the ADC input is 7 V rms, yielding a SNR of 113 dB at the ADC input.

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

Although the ADA4922-1 is used in many applications involving frequencies that are well below 1 MHz, some general high speed layout practices must be adhered to because it is a high speed amplifier. Controlled impedance transmission lines are not required for low frequency signals, provided the signal rise times are longer than approximately 5 times the electrical delay of the interconnections. For reference, typical 50 Ω transmission lines on FR-4 material exhibit approximately 140 ps/in delay on outer layers and 180 ps/in for inner layers. Most connections between the ADA4922-1 and the ADC can be kept very short.

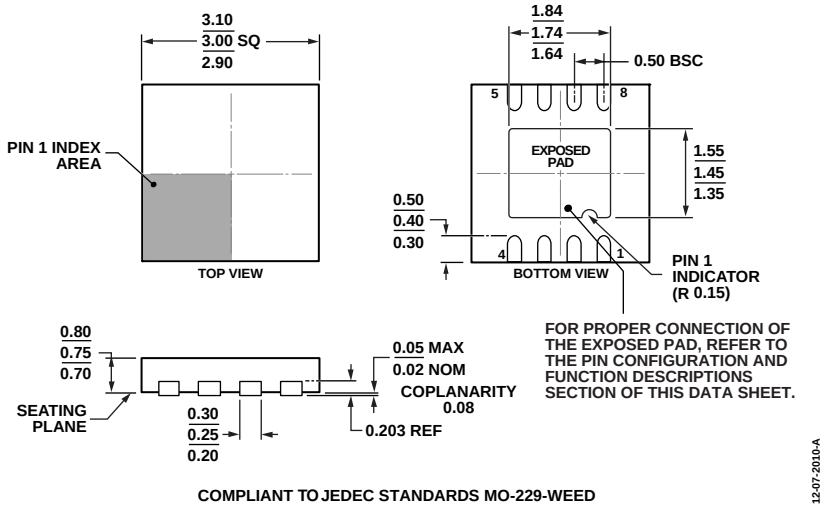
Place broadband power supply decoupling networks as close as possible to the supply pins. Small surface-mount ceramic capacitors are recommended for these networks, and tantalum capacitors are recommended for bulk supply decoupling.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-A A

Figure 51. 8-Lead Standard Small Outline Package with Exposed Pad [SOIC_N_EP]
Narrow Body
(RD-8-1)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-229-WEED

Figure 52. 8-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-8-13)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADA4922-1ARDZ	–40°C to +85°C	8-Lead Standard Small Outline Package with Exposed Pad [SOIC_N_EP]	RD-8-1	
ADA4922-1ARDZ-RL	–40°C to +85°C	8-Lead Standard Small Outline Package with Exposed Pad [SOIC_N_EP]	RD-8-1	
ADA4922-1ACPZ-R2	–40°C to +85°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-13	HUB
ADA4922-1ACPZ-RL7	–40°C to +85°C	8-Lead Lead Frame Chip Scale Package [LFCSP]	CP-8-13	HUB
ADA4922-1ACP-EBZ		Evaluation Board		

[1] Z = RoHS-Compliant Part.