

TABLE OF CONTENTS

Features	1
Applications	1
General Description	1
Pin Connection Diagrams	1
Revision History	2
Specifications	3
Electrical Characteristics, ± 5 V	3
Electrical Characteristics, ± 15 V	5
Absolute Maximum Ratings	7
Thermal Resistance	7
ESD Caution	7
Pin Configurations and Function Descriptions	8

REVISION HISTORY

5/2017—Rev. D to Rev. E

Changes to Features Section, Applications Section, and Figure 1 ...	1
Added Maximum Reflow Temperature (MSL1 Rating) Parameter and Note 2, Table 4; Renumbered Sequentially	7
Changes to Figure 5, Figure 6, and Table 6	8
Changes to Figure 24 and Figure 27	13
Changes to Figure 29, Figure 30, Figure 31, Figure 32, Figure 33, and Figure 34	14
Changes to Figure 66	20
Added Test Circuit Section and Figure 69; Renumbered Sequentially	22
Added Long-Term Drift Section, Temperature Hysteresis Section, Figure 72, Figure 73, and Figure 74	24
Changes to Ordering Guide	27

10/2016—Rev. C to Rev. D

Changes to Table 2	3
Changes to Table 3	5
Changes to Figure 19	12
Changes to Figure 23 and Figure 26	13
Changes to Figure 29, Figure 30, Figure 32, and Figure 33	14

6/2015—Rev. B to Rev. C

Change to Figure 63	18
---------------------------	----

Typical Performance Characteristics	11
Test Circuit	21
Theory of Operation	22
Applications Information	23
Output Phase Reversal	23
Low Power Linearized RTD	23
Proper Board Layout	23
Long-Term Drift	24
Temperature Hysteresis	24
Outline Dimensions	25
Ordering Guide	27

1/2014—Rev. A to Rev. B

Added ADA4077-1	Universal
Changes to Features Section	1
Added Figure 1; Renumbered Sequentially	1
Changes to Table 2	3
Changes to Table 3	4
Added Figure 5, Figure 6, and Table 6; Renumbered Sequentially	7
Changes to Figure 17, Figure 20, and Figure 21	11
Changes to Figure 65	19
Added Figure 67 and Figure 68	19
Changes to Output Phase Reversal Section and Figure 70	21
Changes to Ordering Guide	24

10/2013—Rev. 0 to Rev. A

Added ADA4077-4	Universal
Changes to Features, General Description, and Figure 1	1
Deleted Figure 2; Renumbered Sequentially	1
Added Figure 2	1
Changes to Table 2	3
Changes to Table 3	4
Changes to Table 4	6
Added Figure 6, Figure 7, and Table 7; Renumbered Sequentially	8
Changes to Typical Performance Characteristics Section	9
Changes to Figure 65	20
Updated Outline Dimensions	21
Changes to Ordering Guide	23

10/2012—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS, ± 5 V

$V_{SY} = \pm 5.0$ V, $V_{CM} = 0$ V, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V _{OS}					
ADA4077-1/ADA4077-2						
B Grade, SOIC		−40°C < T _A < +125°C	10	25	μV	
				65	μV	
A Grade, SOIC		−40°C < T _A < +125°C	15	50	μV	
				105	μV	
A Grade, MSOP		−40°C < T _A < +125°C	50	90	μV	
				220	μV	
ADA4077-4						
A Grade, SOIC		−40°C < T _A < +125°C	15	50	μV	
				105	μV	
A Grade, TSSOP	−40°C < T _A < +125°C	15	120	μV		
				220	μV	
Offset Voltage Drift	ΔV _{OS} /ΔT	−40°C < T _A < +125°C				
ADA4077-1/ADA4077-2						
B Grade, SOIC			0.1	0.25	μV/°C	
A Grade, SOIC			0.25	0.55	μV/°C	
A Grade, MSOP			0.5	1.2	μV/°C	
ADA4077-4						
A Grade, SOIC			0.4	0.75	μV/°C	
A Grade, TSSOP		0.5	1.2	μV/°C		
Input Bias Current	I _B	−40°C < T _A < +125°C	−1	−0.4	+1	nA
			−1.5		+1.5	nA
Input Offset Current	I _{OS}	−40°C < T _A < +125°C	−0.5	+0.1	+0.5	nA
			−1		+1	nA
Input Voltage Range			−3.8		+3	V
Common-Mode Rejection Ratio	CMRR	V _{CM} = −3.8 V to +3 V	122	140		dB
		V _{CM} = −3.8 V to +3 V, −40°C < T _A < +85°C	120			dB
		V _{CM} = −3.8 V to +2.8 V, 85°C < T _A < 125°C	120			dB
Large Signal Voltage Gain	A _v	R _L = 2 kΩ, V _O = −3.0 V to +3.0 V	121	130		dB
		−40°C < T _A < +125°C	120			dB
Input Capacitance	C _{INCM}	Common mode		5		pF
Input Resistance	R _{IN}	Common mode		70		GΩ
OUTPUT CHARACTERISTICS						
Output Voltage High	V _{OH}	I _L = 1 mA	3.8			V
		−40°C < T _A < +125°C	3.7			V
Output Voltage Low	V _{OL}	I _L = 1 mA			−3.8	V
		−40°C < T _A < +125°C			−3.7	V
Output Current	I _{OUT}	V _{DROPOUT} < 1.6 V		±10		mA
Short-Circuit Current	I _{SC}	T _A = 25°C		22		mA
Closed-Loop Output Impedance	Z _{OUT}	f = 1 kHz, A _v = +1		0.05		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V _S = ±2.5 V to ±18 V	123	128		dB
		−40°C < T _A < +125°C	120			dB
Supply Current per Amplifier	I _{SY}	V _O = 0 V		400	450	μA
		−40°C < T _A < +125°C			650	μA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		1.2		V/ μ s
Settling Time to 0.1%	t_s	$V_{IN} = 1\text{ V step}, R_L = 2\text{ k}\Omega, A_V = -1$		3		μ s
Gain Bandwidth Product	GBP	$V_{IN} = 10\text{ mV p-p}, R_L = 2\text{ k}\Omega, A_V = +100$		3.9		MHz
Unity-Gain Crossover	UGC	$V_{IN} = 10\text{ mV p-p}, R_L = 2\text{ k}\Omega, A_V = +1$		3.9		MHz
–3 dB Closed-Loop Bandwidth	–3 dB	$A_V = +1, V_{IN} = 10\text{ mV p-p}, R_L = 2\text{ k}\Omega$		5.9		MHz
Phase Margin	Φ_M	$V_{IN} = 10\text{ mV p-p}, R_L = 2\text{ k}\Omega, A_V = +1$		55		Degrees
Total Harmonic Distortion Plus Noise	THD + N	$V_{IN} = 1\text{ V rms}, A_V = +1, R_L = 2\text{ k}\Omega, f = 1\text{ kHz}$		0.004		%
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.25		μ V p-p
Voltage Noise Density	e_n	$f = 1\text{ Hz}$		13		nV/ $\sqrt{\text{Hz}}$
		$f = 100\text{ Hz}$		7		nV/ $\sqrt{\text{Hz}}$
		$f = 1000\text{ Hz}$		6.9		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		0.2		pA/ $\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f = 1\text{ kHz}$		0.2		pA/ $\sqrt{\text{Hz}}$
MULTIPLE AMPLIFIERS CHANNEL SEPARATION	C_s	$f = 1\text{ kHz}, R_L = 10\text{ k}\Omega$		–125		dB

ELECTRICAL CHARACTERISTICS, ± 15 V

$V_{SY} = \pm 15$ V, $V_{CM} = 0$ V, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}					
ADA4077-1/ADA4077-2						
B Grade, SOIC				10	35	μV
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			65	μV
A Grade, SOIC				15	50	μV
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			105	μV
A Grade, MSOP				50	90	μV
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			220	μV
ADA4077-4						
A Grade, SOIC				15	50	μV
	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			105	$\mu\text{V}/^\circ\text{C}$
A Grade, TSSOP				15	120	μV
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			220	$\mu\text{V}/^\circ\text{C}$
Offset Voltage Drift						
ADA4077-1/ADA4077-2						
B Grade, SOIC		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.1	0.25	$\mu\text{V}/^\circ\text{C}$
A Grade, SOIC		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.25	0.55	$\mu\text{V}/^\circ\text{C}$
A Grade, MSOP		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.5	1.2	$\mu\text{V}/^\circ\text{C}$
ADA4077-4						
A Grade, SOIC		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.4	0.75	$\mu\text{V}/^\circ\text{C}$
A Grade, TSSOP		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.5	1.2	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B		-1	-0.4	+1	nA
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-1.5		+1.5	nA
Input Offset Current	I_{OS}		-0.5	+0.1	+0.5	nA
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-1		+1	nA
Input Voltage Range			-13.8		+13	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -13.8$ V to +13 V	132	150		dB
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	130			dB
Large Signal Voltage Gain	A_v					
ADA4077-1/ADA4077-2 (SOIC, MSOP)		$R_L = 2$ k Ω , $V_O = -13.0$ V to +13.0 V	125	130		dB
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	120			dB
ADA4077-4 (SOIC, TSSOP)		$R_L = 2$ k Ω , $V_O = -13.0$ V to +13.0 V	122	130		dB
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	120			dB
Input Capacitance	C_{INDM}	Differential mode		3		pF
	C_{INCM}	Common mode		5		pF
Input Resistance	R_{IN}	Common mode		70		G Ω
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_L = 1$ mA	13.8			V
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	13.7			V
Output Voltage Low	V_{OL}	$I_L = 1$ mA			-13.8	V
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			-13.7	V
Output Current	I_{OUT}	$V_{DROPOUT} < 1.2$ V		± 10		mA
Short-Circuit Current	I_{SC}	$T_A = 25^\circ\text{C}$		22		mA
Closed-Loop Output Impedance	Z_{OUT}	$f = 1$ kHz, $A_v = +1$		0.05		Ω

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5 \text{ V to } \pm 18 \text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	123	128		dB
Supply Current per Amplifier	I_{SY}	$V_O = 0 \text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	120	400	500 650	dB μA μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2 \text{ k}\Omega$		1.2		$\text{V}/\mu\text{s}$
Settling Time to 0.01%	t_s	$V_{IN} = 10 \text{ V p-p}, R_L = 2 \text{ k}\Omega, A_V = -1$		16		μs
Settling Time to 0.1%	t_s	$V_{IN} = 10 \text{ V p-p}, R_L = 2 \text{ k}\Omega, A_V = -1$		10		μs
Gain Bandwidth Product	GBP	$V_{IN} = 10 \text{ mV p-p}, R_L = 2 \text{ k}\Omega, A_V = +100$		3.6		MHz
Unity-Gain Crossover	UGC	$V_{IN} = 10 \text{ mV p-p}, R_L = 2 \text{ k}\Omega, A_V = +1$		3.9		MHz
–3 dB Closed-Loop Bandwidth	–3 dB	$A_V = +1, V_{IN} = 10 \text{ mV p-p}, R_L = 2 \text{ k}\Omega$		5.5		MHz
Phase Margin	Φ_M	$V_{IN} = 10 \text{ mV p-p}, R_L = 2 \text{ k}\Omega, A_V = +1$		58		Degrees
Total Harmonic Distortion Plus Noise	THD + N	$V_{IN} = 1 \text{ V rms}, A_V = +1, R_L = 2 \text{ k}\Omega,$ $f = 1 \text{ kHz}$		0.004		%
NOISE PERFORMANCE						
Voltage Noise	$e_n \text{ p-p}$	0.1 Hz to 10 Hz		0.25		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1 \text{ Hz}$		13		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 100 \text{ Hz}$		7		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1000 \text{ Hz}$		6.9		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f = 1 \text{ kHz}$		0.2		$\text{pA}/\sqrt{\text{Hz}}$
MULTIPLE AMPLIFIERS CHANNEL SEPARATION	C_S	$f = 1 \text{ kHz}, R_L = 10 \text{ k}\Omega$		–125		dB

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	36 V
Input Voltage	$\pm V_{SY}$
Input Current ¹	± 10 mA
Differential Input Voltage	$\pm V_{SY}$
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	–40°C to +125°C
Junction Temperature Range	–65°C to +150°C
Maximum Reflow Temperature (MSL1 Rating) ²	260°C
Lead Temperature, Soldering (10 sec)	300°C
Electrostatic Discharge (ESD)	
Human Body Model (HBM) ³	6 kV
Field Induced Charge Device Model (FICDM) ⁴	1.25 kV

¹ The input pins have clamp diodes to the power supply pins and to each other. Limit the input current to 10 mA or less whenever input signals exceed the power supply rail by 0.3 V.

² IPC/JEDEC J-STD-020 applicable standard.

³ ESDA/JEDEC JS-001-2011 applicable standard.

⁴ JESD22-C101 (ESD FICDM standard of JEDEC) applicable standard.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP	190	44	°C/W
8-Lead SOIC	158	43	°C/W
14-Lead TSSOP	240	43	°C/W
14-Lead SOIC	115	36	°C/W

ESD CAUTION**ESD (electrostatic discharge) sensitive device.**

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

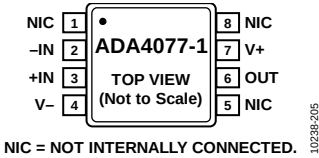


Figure 5. ADA4077-1 Pin Configuration, 8-Lead MSOP (RM-8)

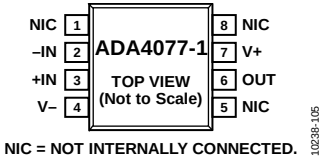


Figure 6. ADA4077-1 Pin Configuration, 8-Lead SOIC (R-8)

Table 6. ADA4077-1 Pin Function Descriptions, 8-Lead MSOP and 8-Lead SOIC

Pin No.	Mnemonic	Description
1, 5, 8	NIC	Not internally connected.
2	-IN	Inverting Input.
3	+IN	Noninverting Input.
4	V-	Negative Supply Voltage.
6	OUT	Output.
7	V+	Positive Supply Voltage.

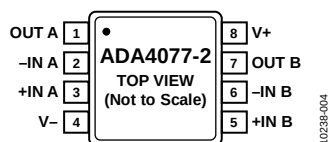


Figure 7. ADA4077-2 Pin Configuration, 8-Lead MSOP

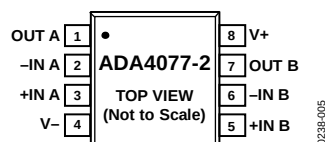


Figure 8. ADA4077-2 Pin Configuration, 8-Lead SOIC

Table 7. ADA4077-2 Pin Function Descriptions, 8-Lead MSOP and 8-Lead SOIC

Pin No.	Mnemonic	Description
1	OUT A	Output Channel A.
2	-IN A	Inverting Input Channel A.
3	+IN A	Noninverting Input Channel A.
4	V-	Negative Supply Voltage.
5	+IN B	Noninverting Input Channel B.
6	-IN B	Inverting Input Channel B.
7	OUT B	Output Channel B.
8	V+	Positive Supply Voltage.

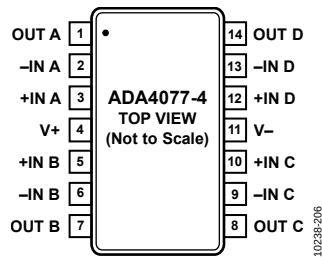


Figure 9. ADA4077-4 Pin Configuration, 14-Lead TSSOP

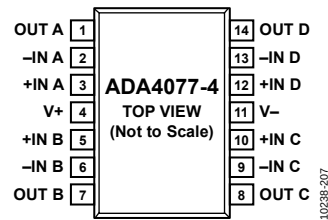
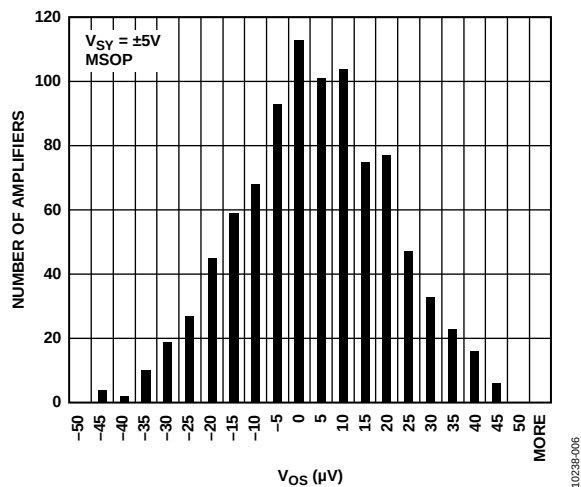
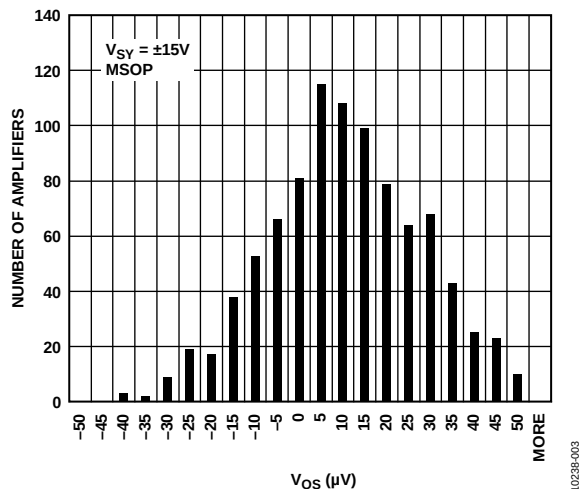
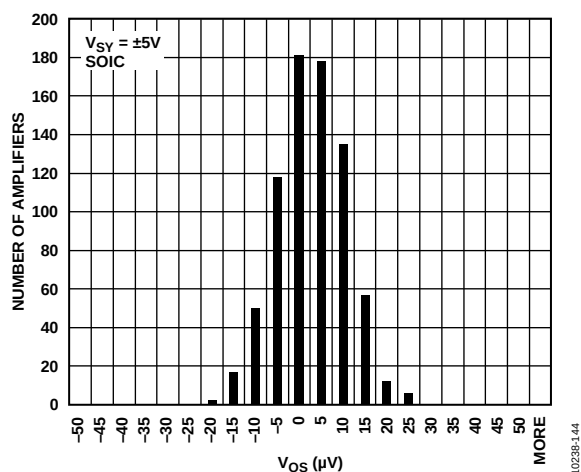
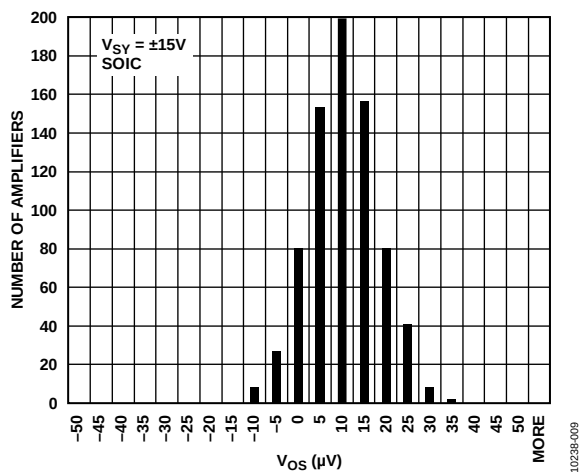
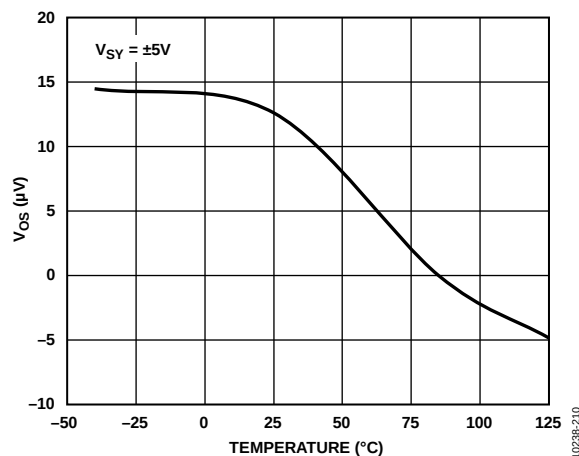
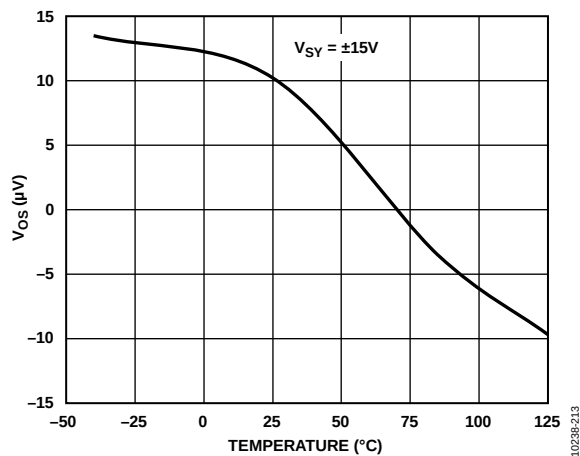


Figure 10. ADA4077-4 Pin Configuration, 14-Lead SOIC

Table 8. ADA4077-4 Pin Function Descriptions, 14-Lead TSSOP and 14-Lead SOIC

Pin No.	Mnemonic	Description
1	OUT A	Output Channel A.
2	-IN A	Negative Input Channel A.
3	+IN A	Positive Input Channel A.
4	V+	Positive Supply Voltage.
5	+IN B	Positive Input Channel B.
6	-IN B	Negative Input Channel B.
7	OUT B	Output Channel B.
8	OUT C	Output Channel C.
9	-IN C	Negative Input Channel C.
10	+IN C	Positive Input Channel C.
11	V-	Negative Supply Voltage.
12	+IN D	Positive Input Channel D.
13	-IN D	Negative Input Channel D.
14	OUT D	Output Channel D.

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 11. ADA4077-2 Offset Voltage (V_{OS}) Distribution, $V_{SY} = \pm 5V$ Figure 14. ADA4077-2 Offset Voltage (V_{OS}) Distribution, $V_{SY} = \pm 15V$ Figure 12. Offset Voltage (V_{OS}) Distribution, $V_{SY} = \pm 5V$ Figure 15. Offset Voltage (V_{OS}) Distribution, $V_{SY} = \pm 15V$ Figure 13. Offset Voltage (V_{OS}) vs. Temperature, $V_{SY} = \pm 5V$ Figure 16. Offset Voltage (V_{OS}) vs. Temperature, $V_{SY} = \pm 15V$

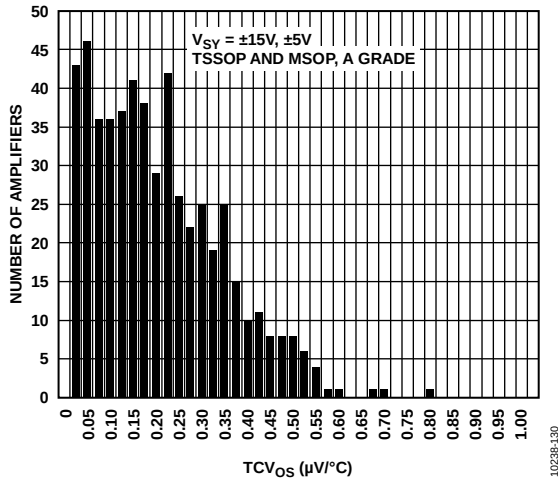


Figure 17. TCV_{OS} Distribution (TSSOP and MSOP, A Grade)

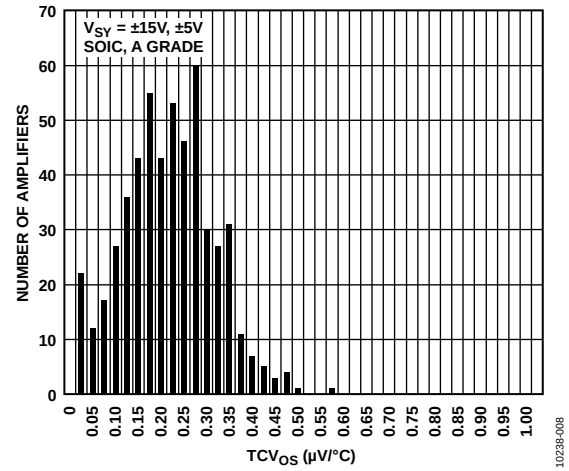


Figure 20. TCV_{OS} Distribution (SOIC, A Grade)

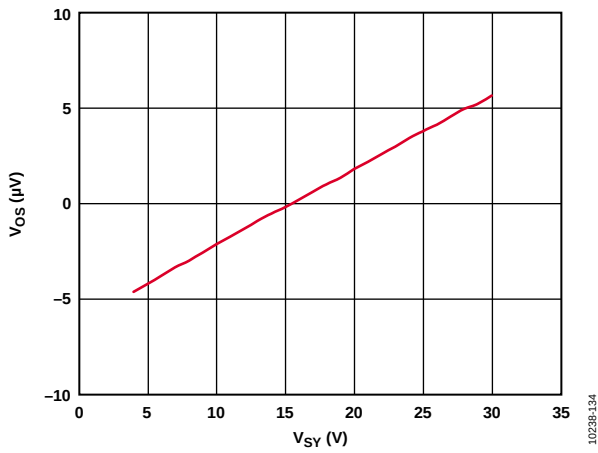


Figure 18. Offset Voltage (V_{OS}) vs. Power Supply Voltage (V_{SY})

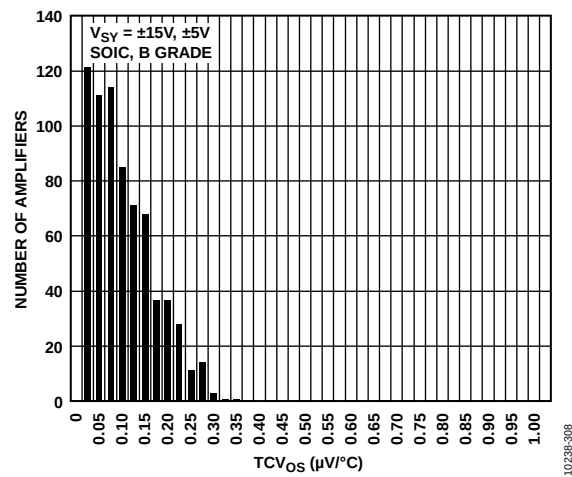


Figure 21. TCV_{OS} Distribution (SOIC, B Grade)

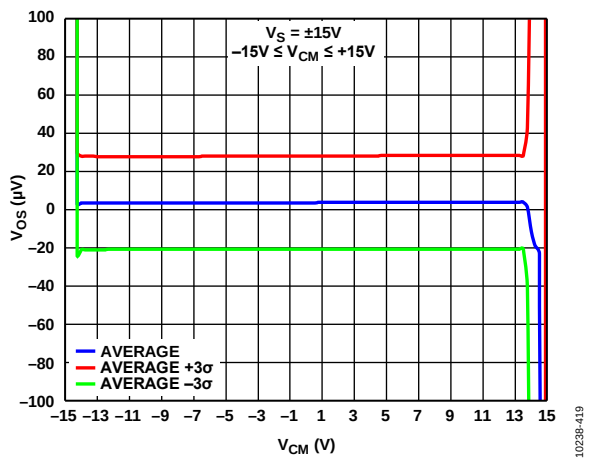


Figure 19. Offset Voltage (V_{OS}) vs. Common-Mode Voltage (V_{CM}), $V_{SY} = \pm 15 V$

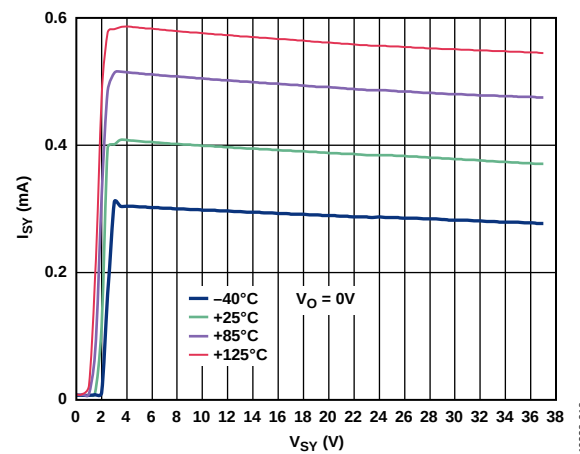
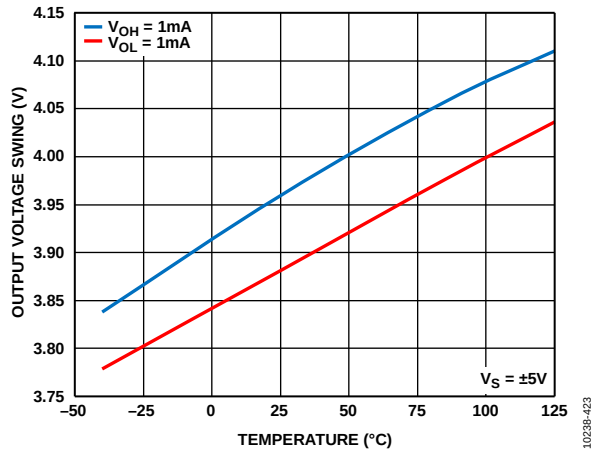
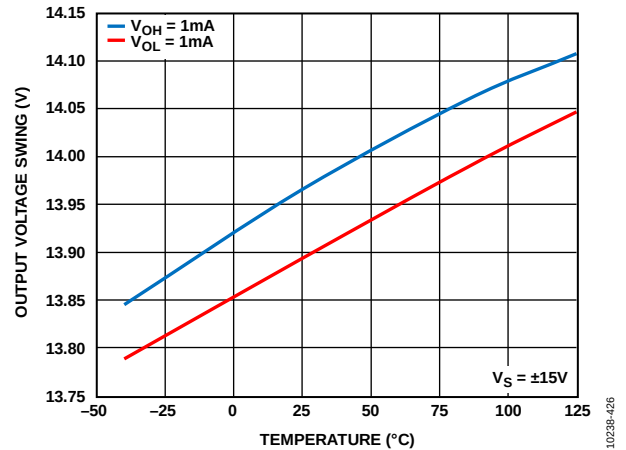
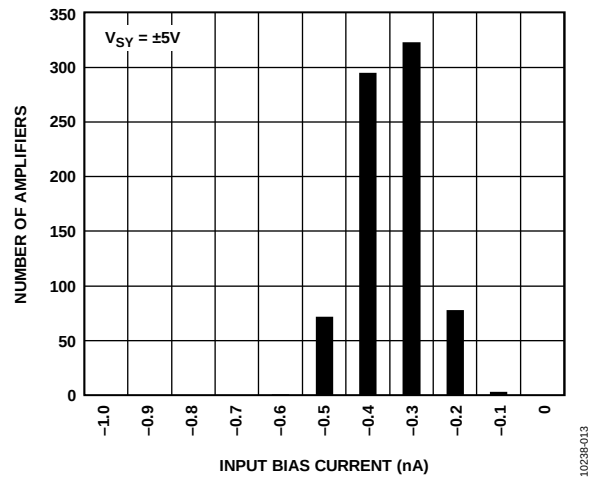
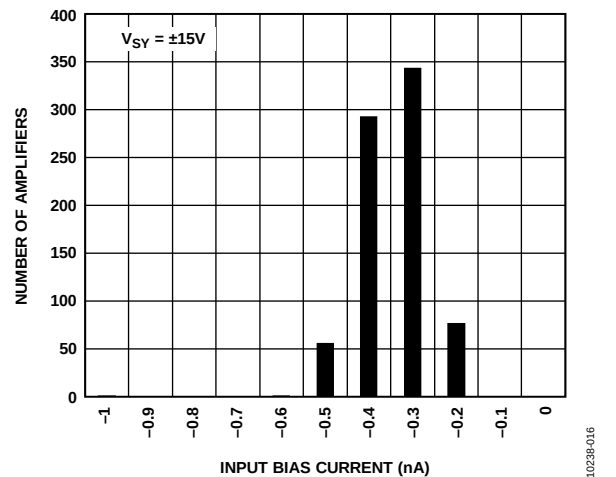
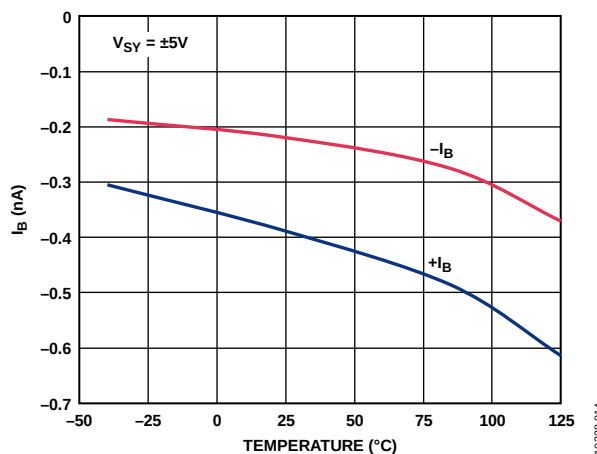
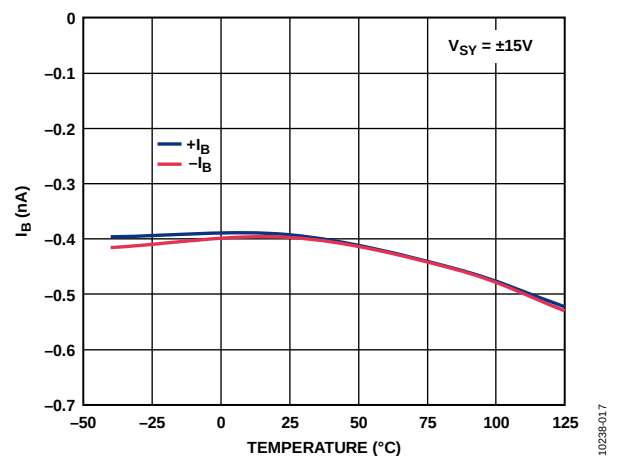


Figure 22. Supply Current per Amplifier (I_{SY}) vs. Power Supply Voltage (V_{SY})

Figure 23. Output Voltage Swing vs. Temperature, $V_{SY} = \pm 5V$ Figure 26. Output Voltage Swing vs. Temperature, $V_{SY} = \pm 15V$ Figure 24. Input Bias Current Distribution, $V_{SY} = \pm 5V$ Figure 27. Input Bias Current Distribution, $V_{SY} = \pm 15V$ Figure 25. Input Bias Current (I_B) vs. Temperature, $V_{SY} = \pm 5V$ Figure 28. Input Bias Current (I_B) vs. Temperature, $V_{SY} = \pm 15V$

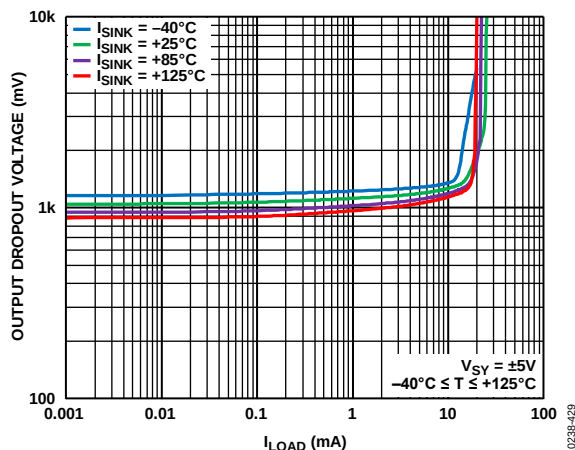


Figure 29. Output Dropout Voltage vs. I_{LOAD} , Sink Current, $V_{SY} = \pm 5V$

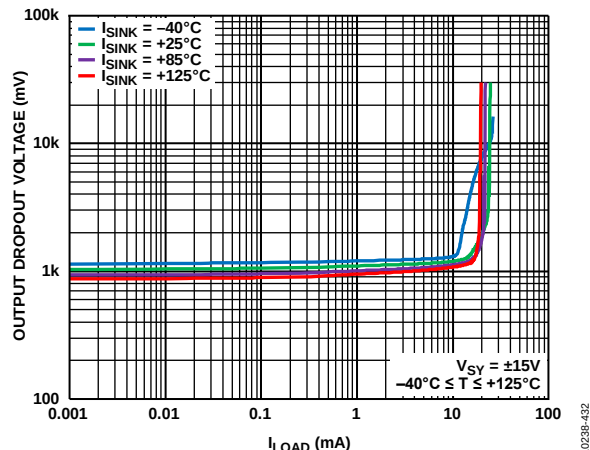


Figure 32. Output Dropout Voltage vs. I_{LOAD} , Sink Current, $V_{SY} = \pm 15V$

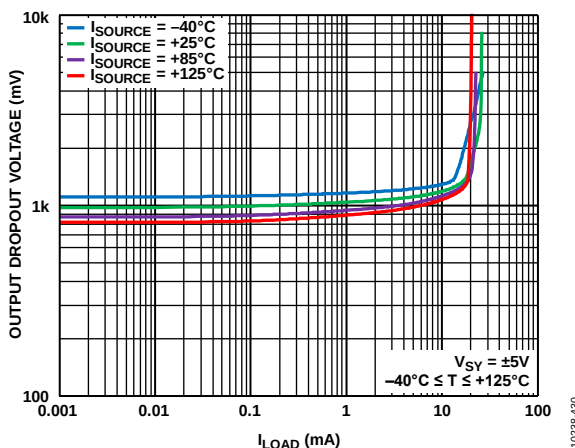


Figure 30. Output Dropout Voltage vs. I_{LOAD} , Source Current, $V_{SY} = \pm 5V$

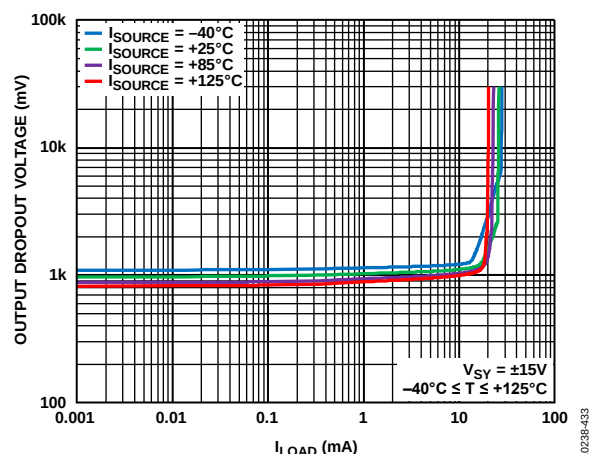


Figure 33. Output Dropout Voltage vs. I_{LOAD} , Source Current, $V_{SY} = \pm 15V$

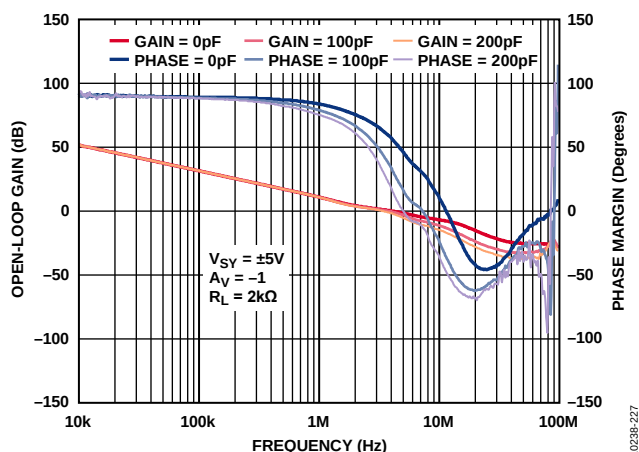


Figure 31. Open-Loop Gain and Phase Margin vs. Frequency, $V_{SY} = \pm 5V$

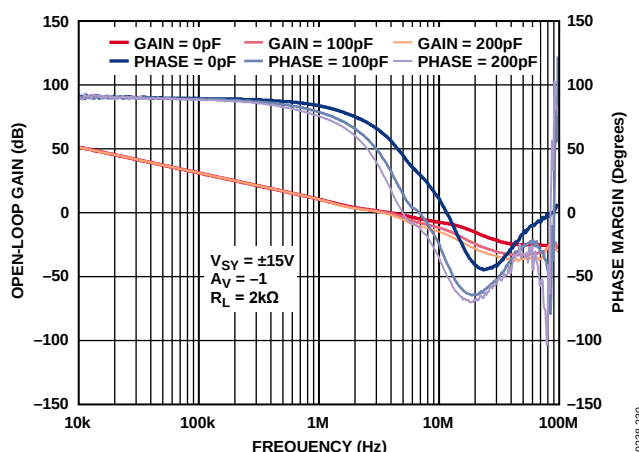
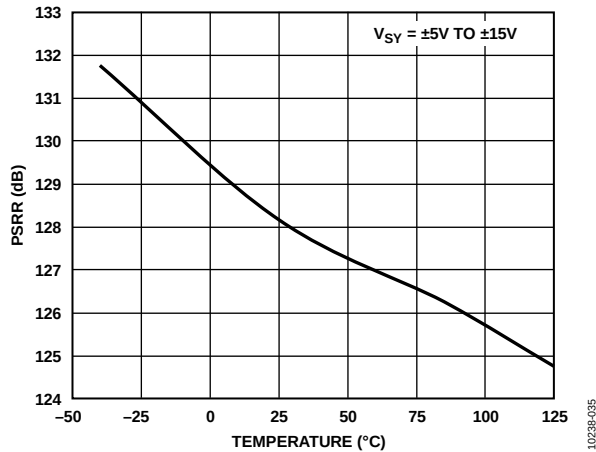
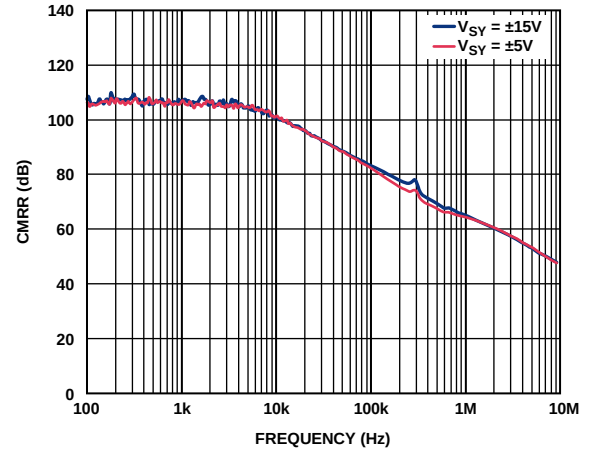


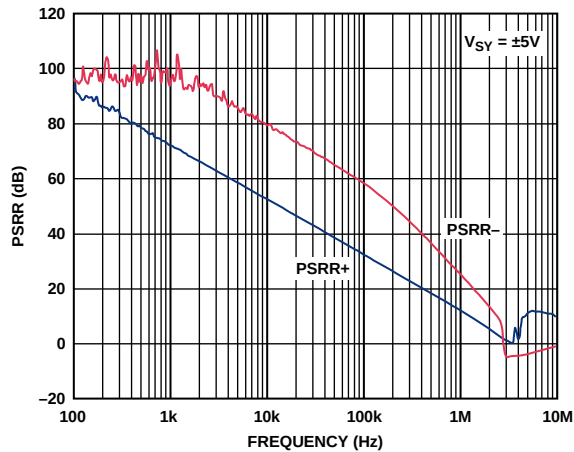
Figure 34. Open-Loop Gain and Phase Margin vs. Frequency, $V_{SY} = \pm 15V$

Figure 35. PSRR vs. Temperature, $V_{SY} = \pm 5 V$ to $\pm 15 V$

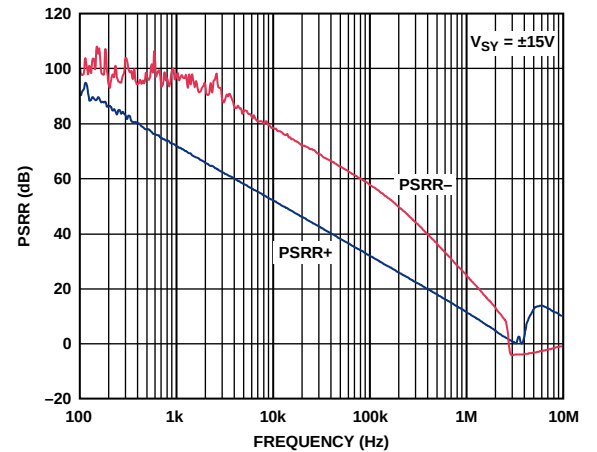
10238-035

Figure 38. CMRR vs. Frequency, $V_{SY} = \pm 5 V$ and $V_{SY} = \pm 15 V$

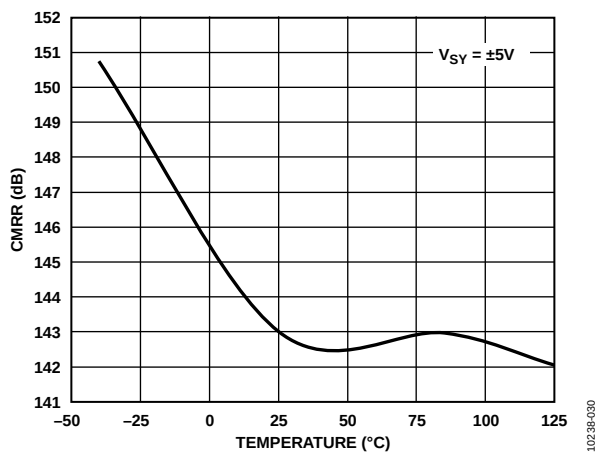
10238-029

Figure 36. PSRR vs. Frequency, $V_{SY} = \pm 5 V$

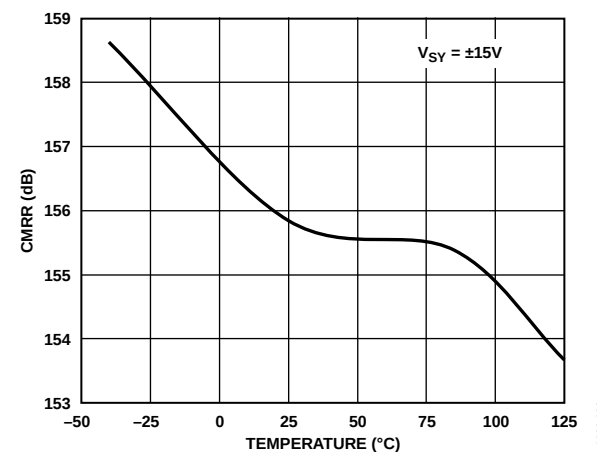
10238-034

Figure 39. PSRR vs. Frequency, $V_{SY} = \pm 15 V$

10238-037

Figure 37. CMRR vs. Temperature, $V_{SY} = \pm 5 V$

10238-030

Figure 40. CMRR vs. Temperature, $V_{SY} = \pm 15 V$

10238-033

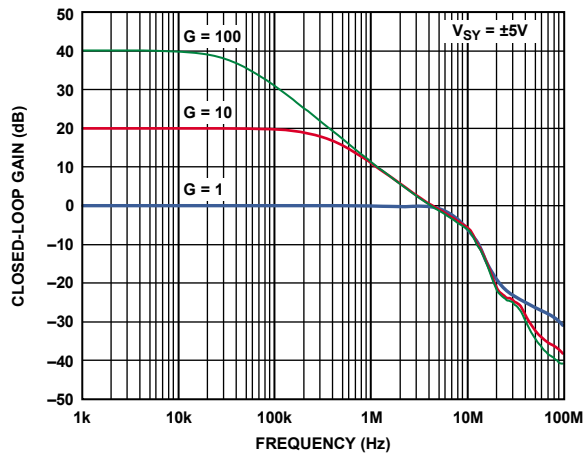


Figure 41. Closed-Loop Gain vs. Frequency, $V_{SY} = \pm 5V$

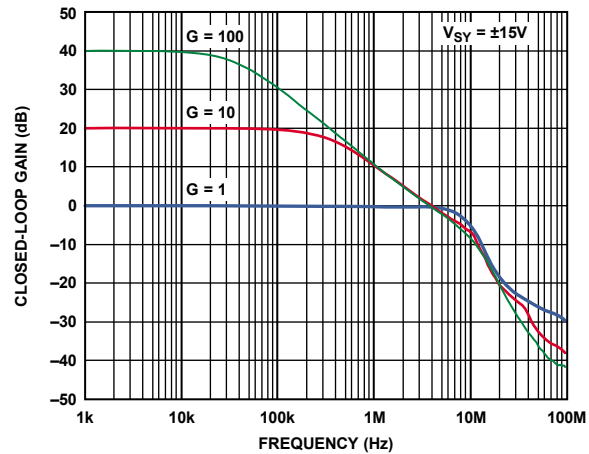


Figure 44. Closed-Loop Gain vs. Frequency, $V_{SY} = \pm 15V$

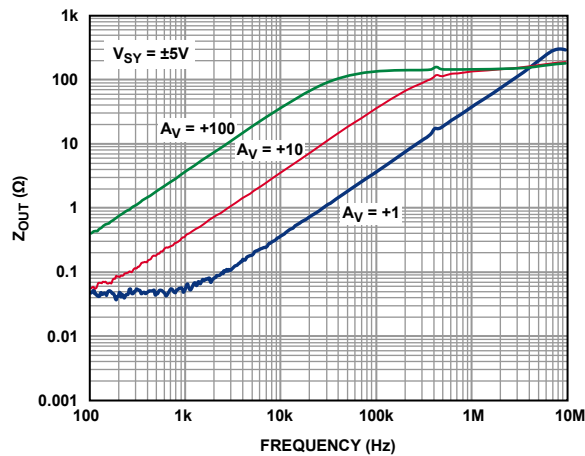


Figure 42. Output Impedance (Z_{OUT}) vs. Frequency, $V_{SY} = \pm 5V$

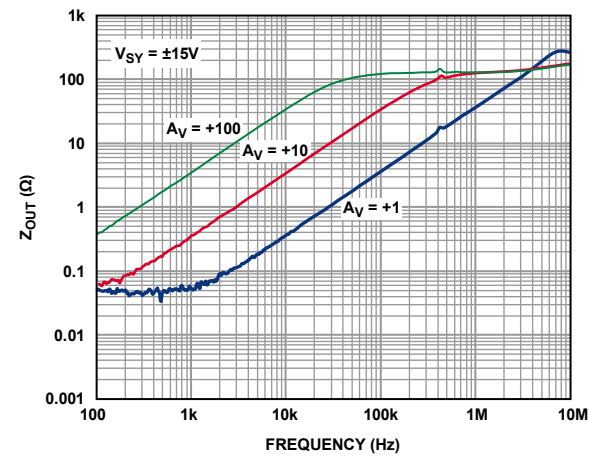


Figure 45. Output Impedance (Z_{OUT}) vs. Frequency, $V_{SY} = \pm 15V$

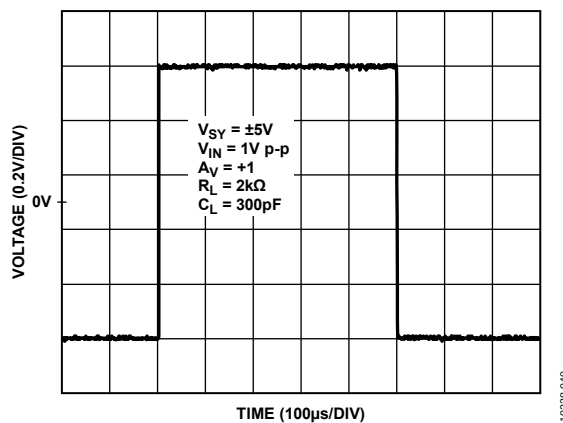


Figure 43. Large Signal Transient Response, $V_{SY} = \pm 5V$

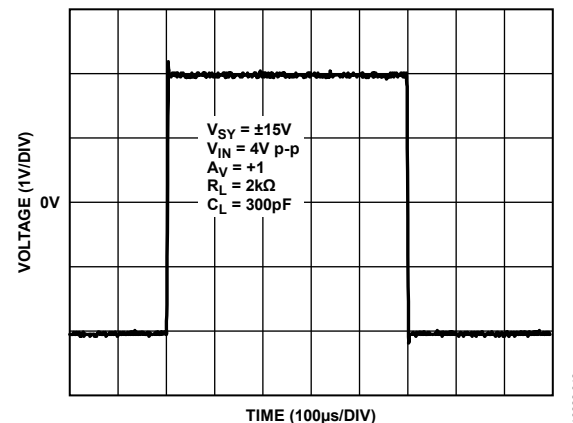
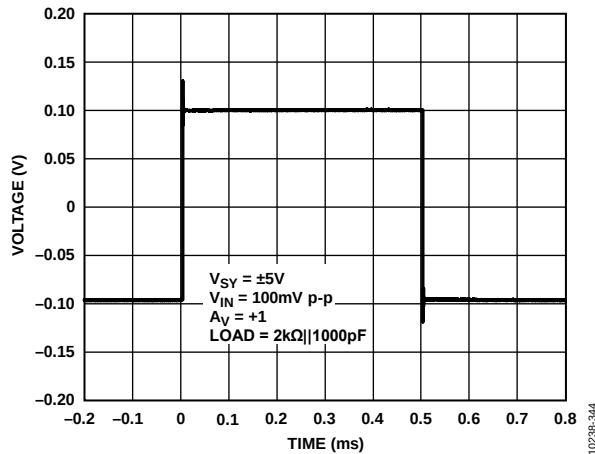
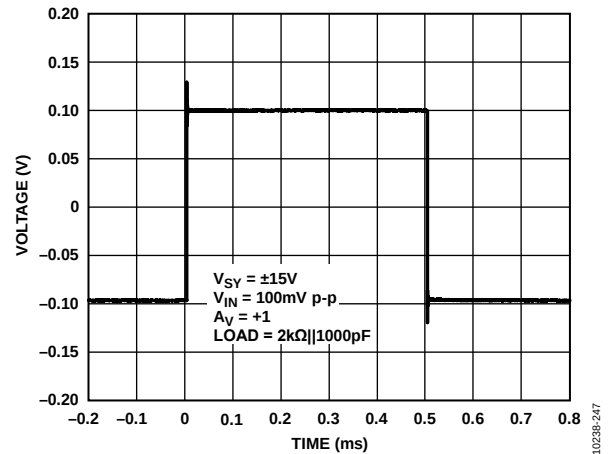
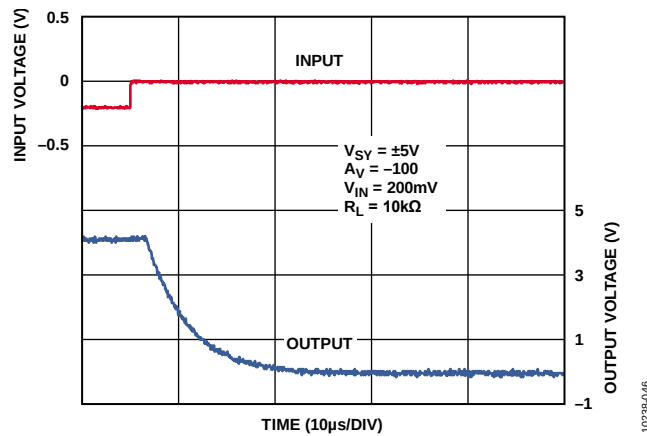
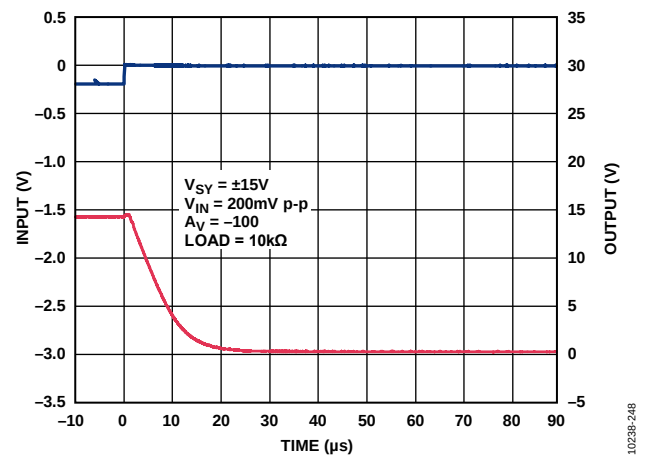
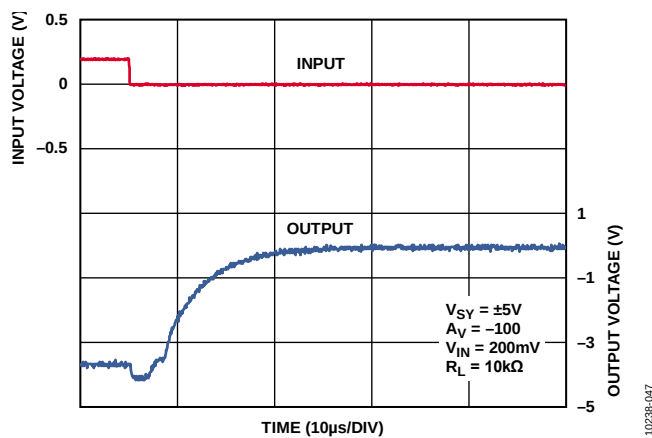
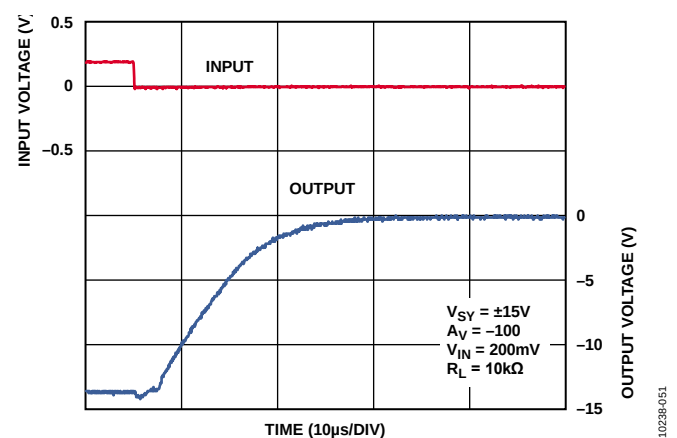


Figure 46. Large Signal Transient Response, $V_{SY} = \pm 15V$

Figure 47. Small Signal Transient Response, $V_{SY} = \pm 5\text{ V}$ Figure 50. Small Signal Transient Response, $V_{SY} = \pm 15\text{ V}$ Figure 48. Positive Overload Recovery, $V_{SY} = \pm 5\text{ V}$ Figure 51. Positive Overload Recovery, $V_{SY} = \pm 15\text{ V}$ Figure 49. Negative Overload Recovery, $V_{SY} = \pm 5\text{ V}$ Figure 52. Negative Overload Recovery, $V_{SY} = \pm 15\text{ V}$

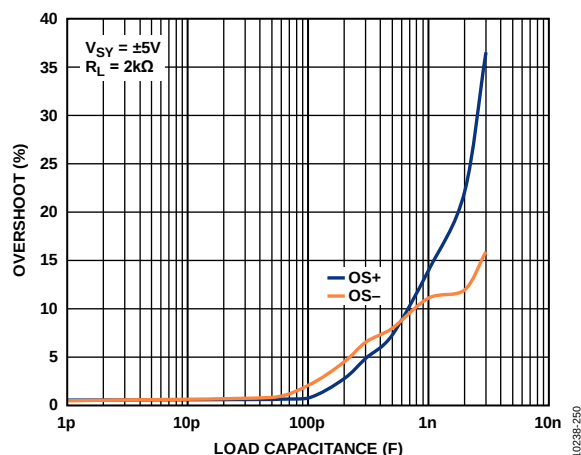


Figure 53. Small Signal Overshoot vs. Load Capacitance, $V_{SV} = \pm 5\text{ V}$

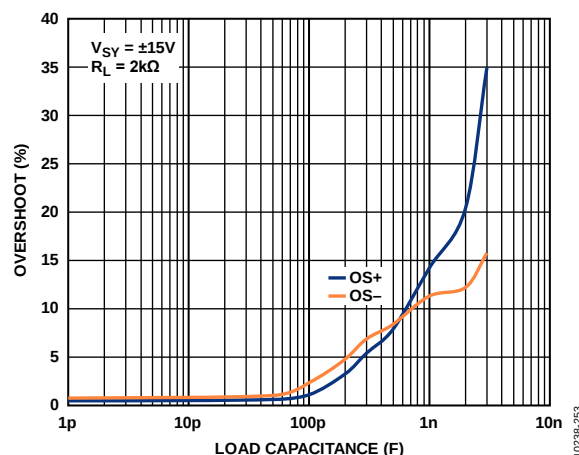


Figure 56. Small Signal Overshoot vs. Load Capacitance, $V_{SV} = \pm 15\text{ V}$

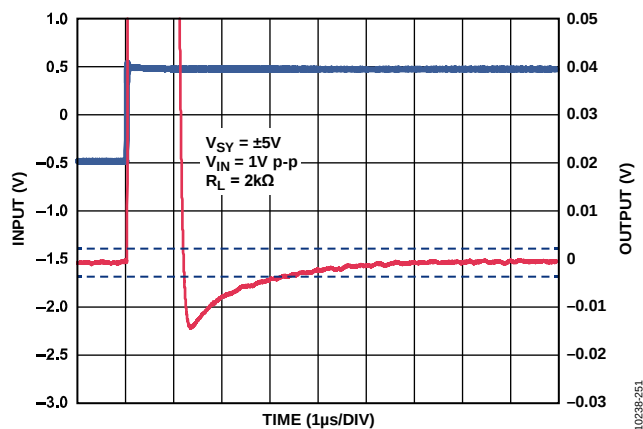


Figure 54. Positive 0.1% Settling Time, $V_{SV} = \pm 5\text{ V}$

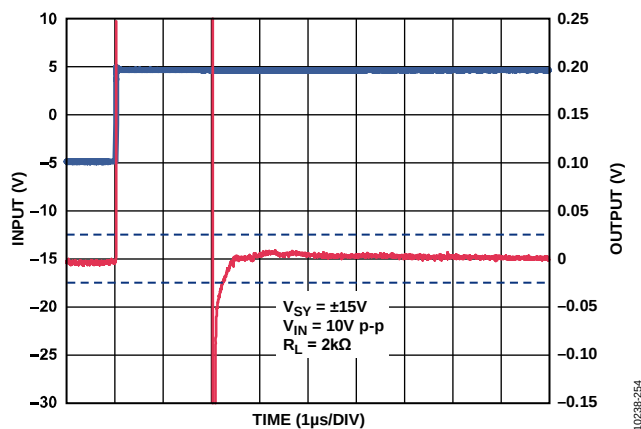


Figure 57. Positive 0.1% Settling Time, $V_{SV} = \pm 15\text{ V}$

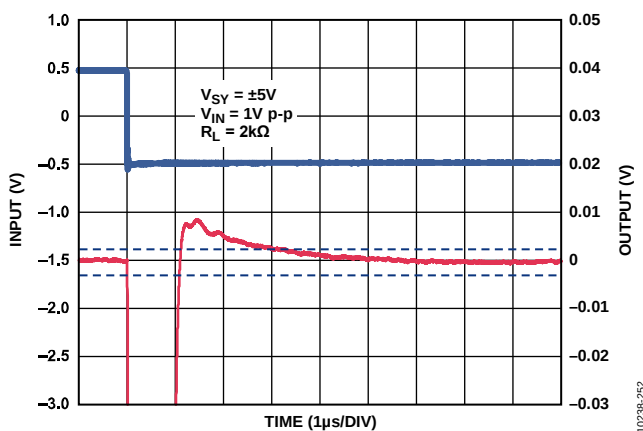


Figure 55. Negative 0.1% Settling Time, $V_{SV} = \pm 5\text{ V}$

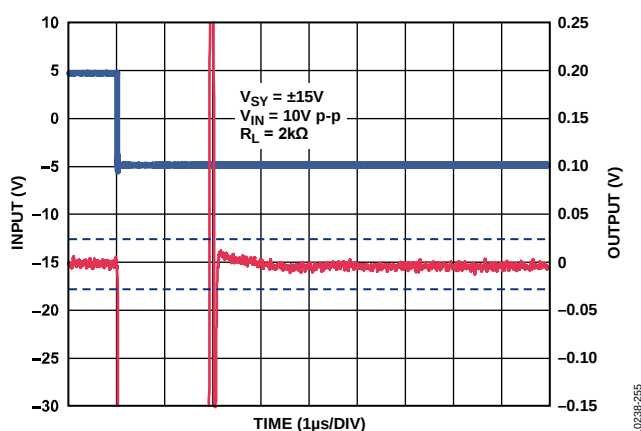
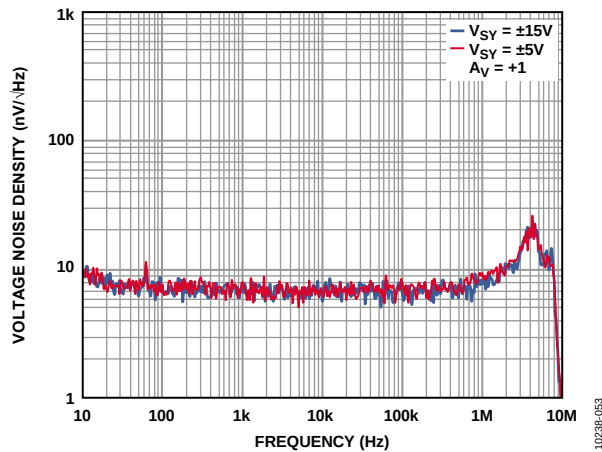
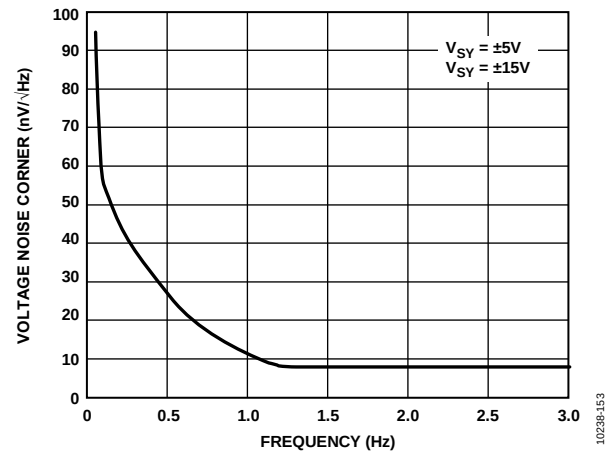
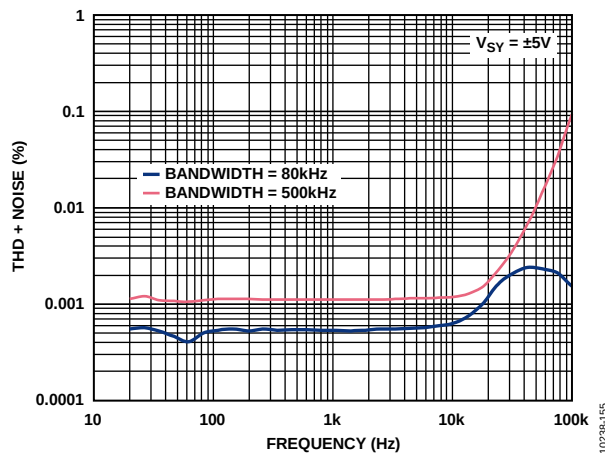
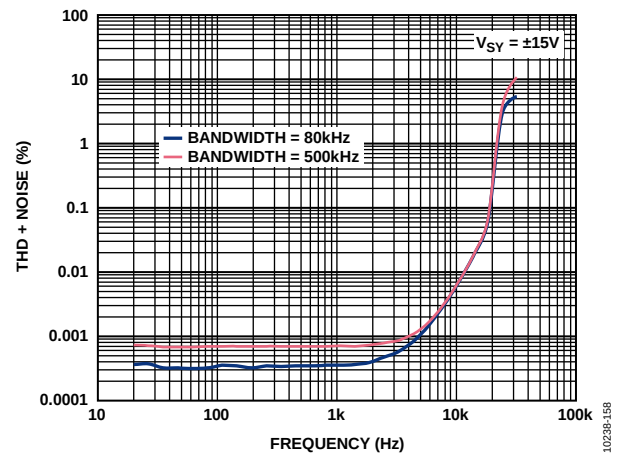
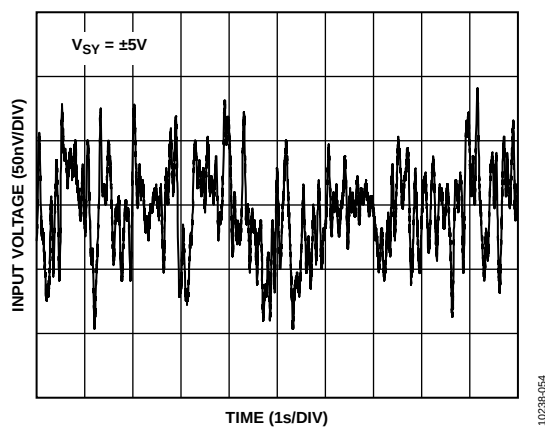
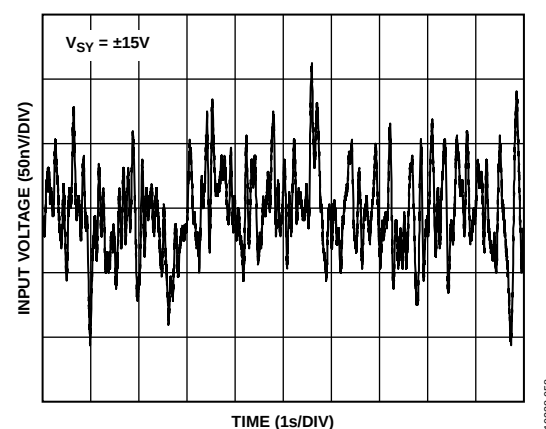


Figure 58. Negative 0.1% Settling Time, $V_{SV} = \pm 15\text{ V}$

Figure 59. Voltage Noise Density vs. Frequency, $V_{SY} = \pm 5\text{ V}$ and $V_{SY} = \pm 15\text{ V}$ Figure 62. Voltage Noise Corner vs. Frequency, $V_{SY} = \pm 15\text{ V}$ and $V_{SY} = \pm 5\text{ V}$ Figure 60. THD + Noise vs. Frequency, $V_{SY} = \pm 5\text{ V}$ Figure 63. THD + Noise vs. Frequency, $V_{SY} = \pm 15\text{ V}$ Figure 61. 0.1 Hz to 10 Hz Noise, $V_{SY} = \pm 5\text{ V}$ Figure 64. 0.1 Hz to 10 Hz Noise, $V_{SY} = \pm 15\text{ V}$

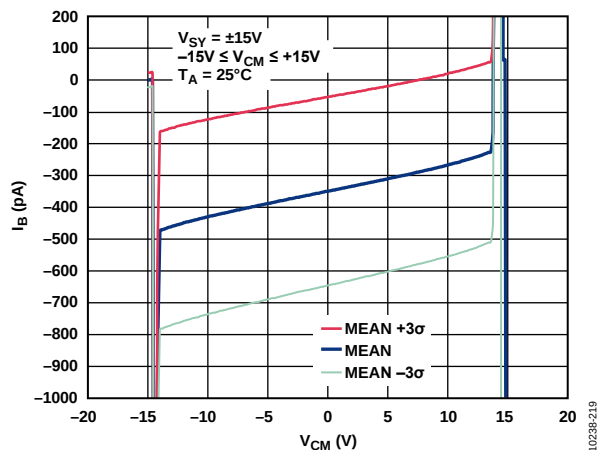


Figure 65. Input Bias Current (I_B) vs. Common-Mode Voltage (V_{CM})

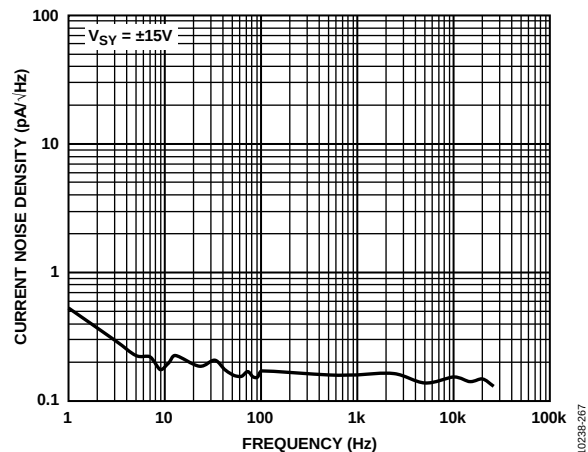


Figure 67. Current Noise Density, $V_{SY} = \pm 15 V$

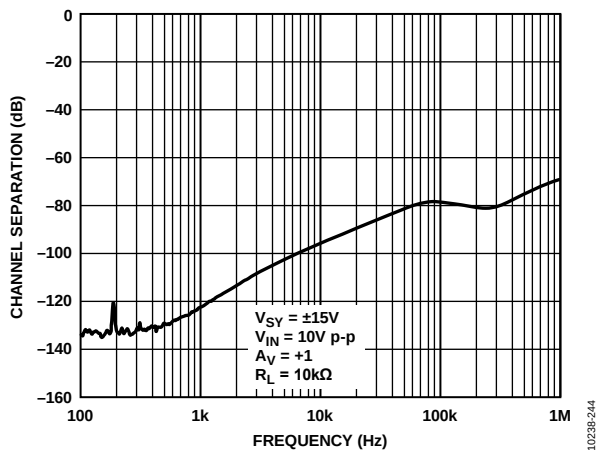


Figure 66. Channel Separation, $V_{SY} = \pm 15 V$ (See Figure 69)

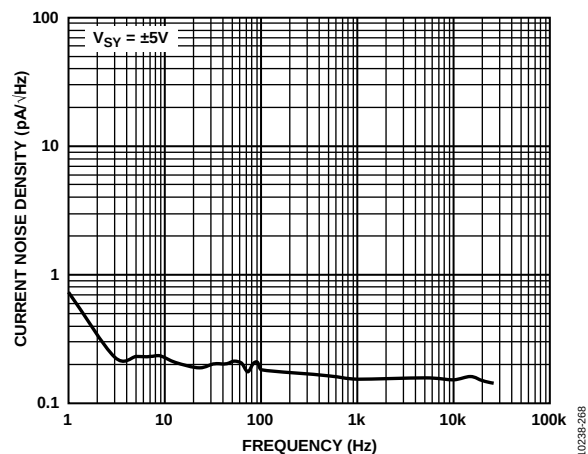
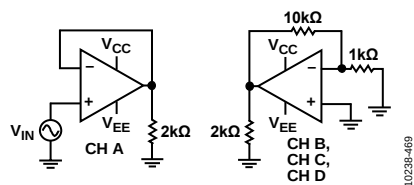


Figure 68. Current Noise Density, $V_{SY} = \pm 5 V$

TEST CIRCUIT



THEORY OF OPERATION

The [ADA4077-1/ADA4077-2/ADA4077-4](#) are the sixth generation of the Analog Devices, Inc., industry-standard [OP07](#) amplifier family. The [ADA4077-1/ADA4077-2/ADA4077-4](#) are high precision, low noise operational amplifiers with a combination of extremely low offset voltage and very low input bias currents. Unlike JFET amplifiers, the low bias and offset currents are relatively insensitive to ambient temperatures, even up to 125°C.

The Analog Devices proprietary process technology and linear design expertise have produced high voltage amplifiers with superior performance to the [OP07/OP77/OP177/OP1177](#) in tiny, 8-lead SOIC and 8-lead MSOP packages ([ADA4077-1](#) and [ADA4077-2](#)) and 14-lead TSSOP and 14-lead SOIC packages ([ADA4077-4](#)). Despite their small size, the [ADA4077-1/ADA4077-2/ADA4077-4](#) offer numerous improvements, including low wideband noise, wide bandwidth, lower offset and offset drift, lower input bias current, and complete freedom from phase inversion.

The [ADA4077-1/ADA4077-2/ADA4077-4](#) have an operating temperature range of -40°C to $+125^{\circ}\text{C}$ with an MSL1 rating, which is as wide as any similar device in a plastic surface-mount package. This MSL1 rating is increasingly important as printed circuit board (PCB) and overall system sizes continue to shrink, causing internal system temperatures to rise.

In the [ADA4077-1/ADA4077-2/ADA4077-4](#), the power consumption is reduced by a factor of four compared to the [OP177](#), and the bandwidth and slew rate are both increased by a factor of six. The low power dissipation and very stable performance vs. temperature also reduce warmup drift errors to insignificant levels.

Inputs are protected internally from overvoltage conditions referenced to either supply rail. Like any high performance amplifier, maximum performance is achieved by following appropriate circuit and PCB guidelines.

APPLICATIONS INFORMATION

OUTPUT PHASE REVERSAL

Phase reversal is defined as a change of polarity in the amplifier transfer function. Many operational amplifiers exhibit phase reversal when the voltage applied to the input is greater than the maximum common-mode voltage. In some instances, this phase reversal can cause permanent damage to the amplifier. In feedback loops, it can result in system lockups or equipment damage. The [ADA4077-1/ADA4077-2/ADA4077-4](#) are immune to phase reversal problems even at input voltages beyond the power supply settings.

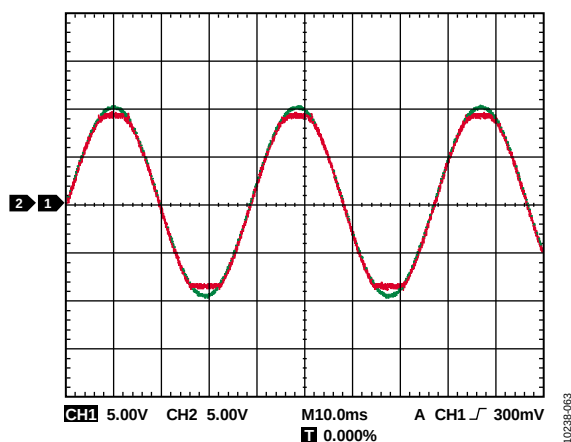


Figure 70. No Phase Reversal

LOW POWER LINEARIZED RTD

A common application for a single element varying bridge is an RTD thermometer amplifier, as shown in Figure 71. The excitation is delivered to the bridge by a 2.5 V reference applied at the top of the bridge.

RTDs can have a thermal resistance as high as 0.5°C/mW to 0.8°C/mW. To minimize errors due to resistor drift, keep the current low through each leg of the bridge. In this circuit, the amplifier supply current flows through the bridge. However, at a maximum supply current of 500 μ A for the [ADA4077-2](#), the RTD dissipates less than 0.1 mW of power, even at the highest resistance. Therefore, errors due to power dissipation in the bridge are kept under 0.1°C.

Calibration of the bridge is made at the minimum value of the temperature to be measured by adjusting R_P until the output is zero.

To calibrate the output span, set the full-scale and linearity potentiometers to midpoint, and apply a 500°C temperature to the sensor, or substitute the equivalent 500°C RTD resistance.

Adjust the full-scale potentiometer for a 5 V output. Finally, apply 250°C or the equivalent RTD resistance, and adjust the linearity potentiometer for a 2.5 V output. The circuit achieves higher than $\pm 0.5^\circ\text{C}$ accuracy after adjustment.

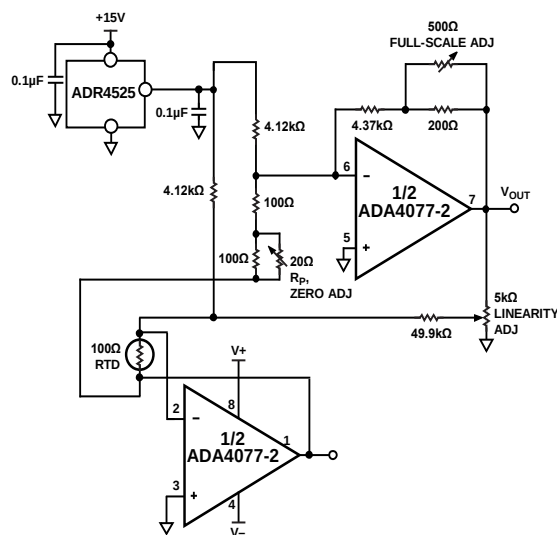


Figure 71. Low Power Linearized RTD Circuit

PROPER BOARD LAYOUT

The [ADA4077-1/ADA4077-2/ADA4077-4](#) are high precision devices. To ensure optimum performance at the PCB level, care must be taken in the design of the board layout.

To avoid leakage currents, maintain a clean and moisture free board surface. Coating the surface creates a barrier to moisture accumulation, and reduces parasitic resistance on the board.

Keeping supply traces short and properly bypassing the power supplies minimizes the power supply disturbances caused by the output current variation, such as when driving an ac signal into a heavy load. Connect bypass capacitors as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that the signal traces be kept at least 5 mm from supply lines to minimize coupling.

A variation in temperature across the PCB can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, orient resistors so that heat sources warm both ends equally. Ensure, where possible, that input signal paths contain matching numbers and types of components, to match the number and type of thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the opposite input path. Place matching components in close proximity to each other, and orient them in the same manner. Ensure that leads are of equal length so that thermal conduction is in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

The use of a ground plane is highly recommended. A ground plane reduces electromagnetic interference (EMI) noise and maintains a constant temperature across the circuit board.

LONG-TERM DRIFT

The stability of a precision signal path over its lifetime or between calibration procedures is dependent on the long-term stability of the analog components in the path, such as op amps, references, and data converters. To help system designers predict the long-term drift of circuits that use the [ADA4077-1/ADA4077-2/ADA4077-4](#), Analog Devices measured the offset voltage of multiple units for 10,000 hours (more than 13 months) using a high precision measurement system, including an ultrastable oil bath. To replicate real-world system performance, the devices under test (DUTs) were soldered onto an FR4 PCB using a standard reflow profile (as defined in the JEDEC J-STD-020D standard), as opposed to testing them in sockets. This manner of testing is important because expansion and contraction of the PCB can apply stress to the integrated circuit (IC) package and contribute to shifts in the offset voltage.

The [ADA4077-1/ADA4077-2/ADA4077-4](#) have extremely low long-term drift (LTD). Figure 72 shows the LTD of the [ADA4077-1](#) (SOIC package). The red, blue, and green traces show sample units. Note that the mean drift over 10,000 hours is less than 0.5 μV , or less than 2% of their maximum specified offset voltage of 25 μV at room temperature.

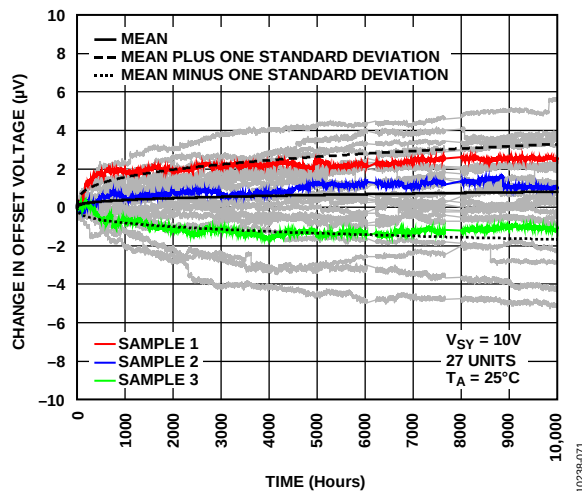


Figure 72. Measured Long-Term Drift of the [ADA4077-1/ADA4077-2/ADA4077-4](#) Offset Voltage over 10,000 Hours

TEMPERATURE HYSTERESIS

In addition to stability over time as described in the Long-Term Drift section, it is useful to know the temperature hysteresis, that is, the stability vs. cycling of temperature. Hysteresis is an important parameter because it tells the system designer how closely the signal returns to its starting amplitude after the ambient temperature changes and subsequent return to room temperature. Figure 73 shows the change in input offset voltage as the temperature cycles three times from room temperature to 125°C to -40°C and back to room temperature. The dotted line is an initial preconditioning cycle to eliminate the original temperature-induced offset shift from exposure to production solder reflow temperatures. In the three full cycles, the offset hysteresis is typically only 1 μV , or 1.5% of its 65 μV maximum offset voltage over the full operating temperature range. The histogram in Figure 74 shows that the hysteresis is larger when the device is cycled through only a half cycle, from room temperature to 125°C and back to room temperature.

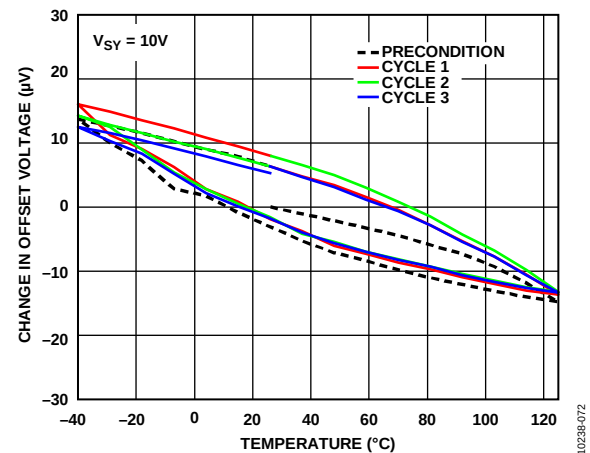


Figure 73. Change in Offset Voltage over Three Full Temperature Cycles

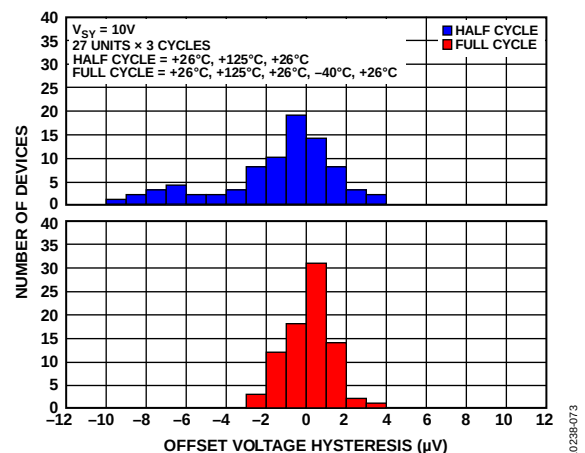
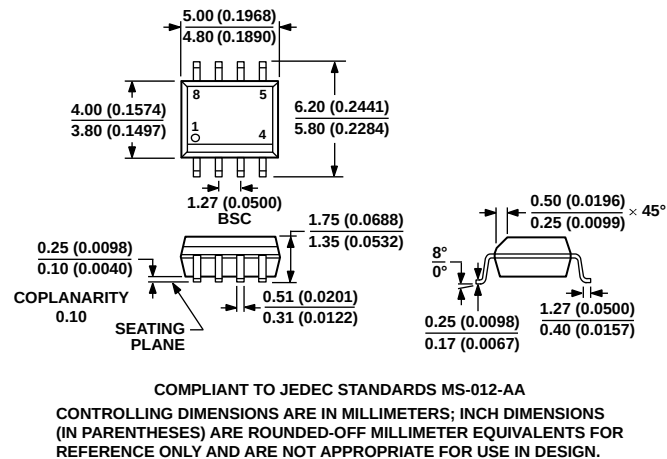
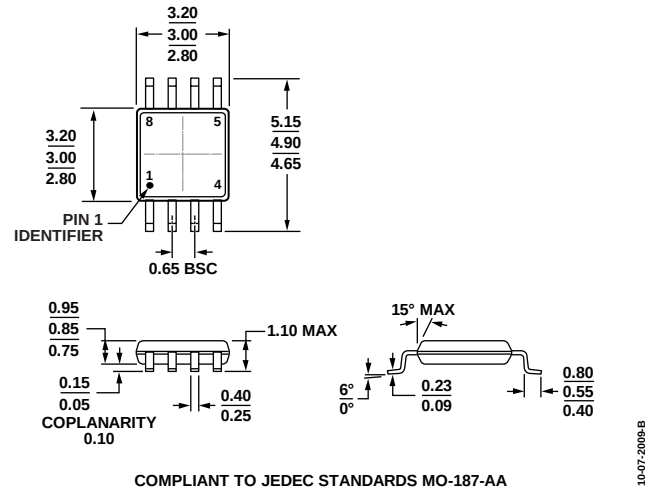
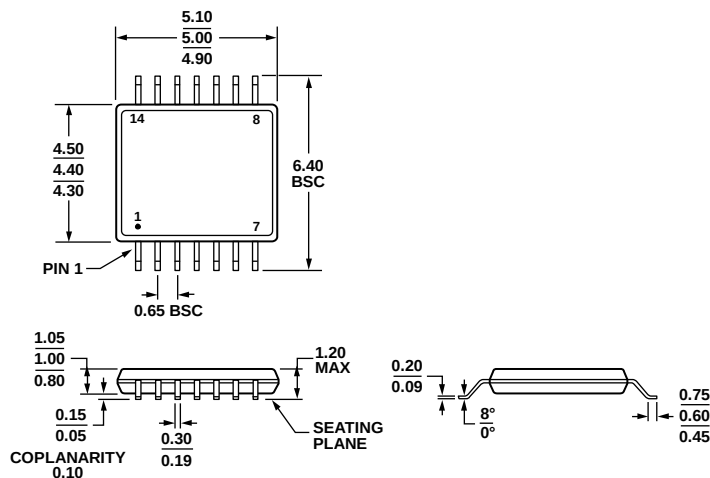


Figure 74. Histogram Showing the Temperature Hysteresis of the Offset Voltage over Three Full Cycles and over Three Half Cycles

OUTLINE DIMENSIONS

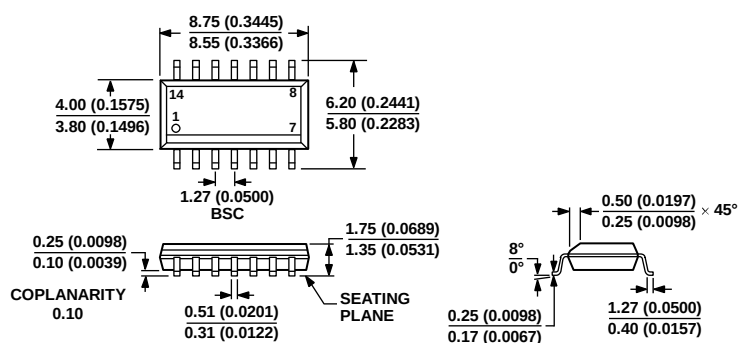




COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 77. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AB

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 78. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)

Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model ¹	Temperature Range	MSL Rating ²	Package Description	Package Option	Branding
ADA4077-1ARMZ	−40°C to +125°C	MSL1	8-Lead MSOP	RM-8	A35
ADA4077-1ARMZ-R7	−40°C to +125°C	MSL1	8-Lead MSOP	RM-8	A35
ADA4077-1ARMZ-RL	−40°C to +125°C	MSL1	8-Lead MSOP	RM-8	A35
ADA4077-1ARZ	−40°C to +125°C	MSL1	8-Lead SOIC_N	R-8	
ADA4077-1ARZ-R7	−40°C to +125°C	MSL1	8-Lead SOIC_N	R-8	
ADA4077-1ARZ-RL	−40°C to +125°C	MSL1	8-Lead SOIC_N	R-8	
ADA4077-1BRZ	−40°C to +125°C	MSL1	8-Lead SOIC_N	R-8	
ADA4077-1BRZ-R7	−40°C to +125°C	MSL1	8-Lead SOIC_N	R-8	
ADA4077-1BRZ-RL	−40°C to +125°C	MSL1	8-Lead SOIC_N	R-8	
ADA4077-2ARMZ	−40°C to +125°C	MSL1	8-Lead MSOP	RM-8	A2X
ADA4077-2ARMZ-R7	−40°C to +125°C	MSL1	8-Lead MSOP	RM-8	A2X
ADA4077-2ARMZ-RL	−40°C to +125°C	MSL1	8-Lead MSOP	RM-8	A2X
ADA4077-2ARZ	−40°C to +125°C	MSL1	8-Lead SOIC_N	R-8	
ADA4077-2ARZ-R7	−40°C to +125°C	MSL1	8-Lead SOIC_N	R-8	
ADA4077-2ARZ-RL	−40°C to +125°C	MSL1	8-Lead SOIC_N	R-8	
ADA4077-2BRZ	−40°C to +125°C	MSL1	8-Lead SOIC_N	R-8	
ADA4077-2BRZ-R7	−40°C to +125°C	MSL1	8-Lead SOIC_N	R-8	
ADA4077-2BRZ-RL	−40°C to +125°C	MSL1	8-Lead SOIC_N	R-8	
ADA4077-4ARUZ	−40°C to +125°C	MSL1	14-Lead TSSOP	RU-14	
ADA4077-4ARUZ-R7	−40°C to +125°C	MSL1	14-Lead TSSOP	RU-14	
ADA4077-4ARUZ-RL	−40°C to +125°C	MSL1	14-Lead TSSOP	RU-14	
ADA4077-4ARZ	−40°C to +125°C	MSL1	14-Lead SOIC_N	R-14	
ADA4077-4ARZ-R7	−40°C to +125°C	MSL1	14-Lead SOIC_N	R-14	
ADA4077-4ARZ-RL	−40°C to +125°C	MSL1	14-Lead SOIC_N	R-14	

¹ Z = RoHS Compliant Part.² See the Absolute Maximum Ratings section.