AD75019–SPECIFICATIONS[1] (T_A = +25°C, V_{DD} and V_{SS} = ±12 V, V_{CC} = +5 V unless otherwise noted)

AD75019	Symbol	Min	Typ	Max	Units
MULTIPLEXER					
Input Signal Range	V_{IN}	V_{SS} – 0.5		V_{DD} + 0.5	V
Switch ON Resistance, V_{DD} and V_{SS} = ±12 V, V_{SIGNAL} = ±12 V	R_{ON}		150	**300**	Ω
Switch ON Resistance, V_{DD} and V_{SS} = ±5 V, V_{SIGNAL} = ±5 V	R_{ON}		300	500	Ω
Switch ON Resistance Matching[2], V_{SIGNAL} = ±12 V	ΔR_{ON}		20	**30**	Ω
Leakage Current, V_{SIGNAL} = ±10 V			2	10	nA
Input/Output Capacitance	C_{IN}			25	pF
Isolation Between Any Two Channels					
R_S = 600 Ω, R_L = 10 kΩ, V_{SIGNAL} = 2 V p-p					
f_{SIGNAL} = 1 kHz		92			dB
f_{SIGNAL} = 20 kHz		69			dB
f_{SIGNAL} = 1 MHz		38			dB
Total Harmonic Distortion					
R_S = 600 Ω, R_L = 10 kΩ, V_{SIGNAL} = 2 V p-p				0.01	%
Switch Frequency Response, –3 dB					
R_S = 600 Ω, R_L = 10 kΩ, V_{SIGNAL} = 2 V p-p		20			MHz
Propagation Delay			4	8	ns
DIGITAL INPUTS (SIN, SCLK, PCLK)					
Logic Levels (TTL Compatible)					
Input Voltage, Logic "1"	V_{IH}	**2.4**		5.5	V
Input Voltage, Logic "0"	V_{IL}	0		**0.8**	V
Input Current, V_{IH} = 5.5 V	I_{IH}			±1	μA
Input Current, V_{IL} = 0.8 V	I_{IL}			±1	μA
Input Capacitance	C_{IN}			10	pF
DIGITAL OUTPUTS (SOUT)					
Logic Levels (TTL Compatible)					
Output Voltage, Logic "1"	V_{OH}	2.8			V
Output Voltage, Logic "0"	V_{OL}			0.4	V
Output Current, V_{OH} = 2.8 V	I_{OH}	3.2			mA
Output Current, V_{OL} = 0.4 V	I_{OL}	3.2			mA
POWER SUPPLY REQUIREMENTS					
Voltage Range, Total Analog	$V_{DD} - V_{SS}$	9.0		25.2	V
Voltage Range, Positive Analog	$V_{DD} - V_{DGND}$	(V_{CC} – 0.5)		25.2	V
Voltage Range, Negative Analog	$V_{SS} - V_{DGND}$	–20.7		0	V
Voltage Range, Digital	$V_{CC} - V_{DGND}$	4.5	5	5.5	V
Supply Current, SCLK = 5 MHz,	I_{DD}, I_{SS}			±70	mA
V_{IL} = 0.8 V, V_{IH} = 2.4 V	I_{CC}			800	μA
Supply Current, Quiescent,	I_{DD}, I_{SS}		_	**±400**	μA
V_{IL} = 0.8 V, V_{IH} = 2.4 V	I_{CC}		_	**100**	μA

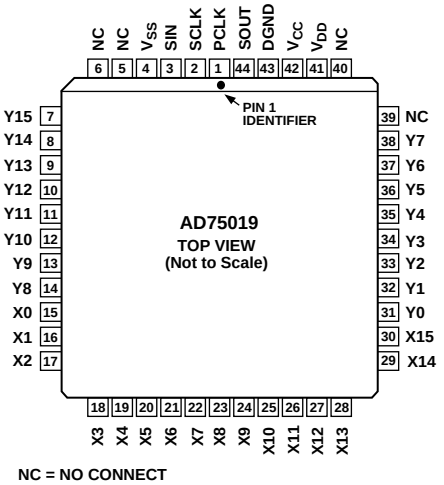
NOTES
[1]All minimum and maximum specifications are guaranteed, and specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.
[2]Switch resistance matching is measured with zero volts at each analog input and refers to the difference between the maximum and minimum values.
Specifications subject to change without notice.

PIN FUNCTION DESCRIPTIONS

Pin	Name	Description
1	PCLK	Parallel Clock Input
2	SCLK	Serial Clock Input
3	SIN	Serial Data Input
4	V_{SS}	Negative Analog Power Supply
5	NC	No Internal Connection
6	NC	No Internal Connection
7	Y15	Analog Output (or Input)
8	Y14	Analog Output (or Input)
9	Y13	Analog Output (or Input)
10	Y12	Analog Output (or Input)
11	Y11	Analog Output (or Input)
12	Y10	Analog Output (or Input)
13	Y9	Analog Output (or Input)
14	Y8	Analog Output (or Input)
15	X0	Analog Input (or Output)
16	X1	Analog Input (or Output)
17	X2	Analog Input (or Output)
18	X3	Analog Input (or Output)
19	X4	Analog Input (or Output)
20	X5	Analog Input (or Output)
21	X6	Analog Input (or Output)
22	X7	Analog Input (or Output)

Pin	Name	Description
23	X8	Analog Input (or Output)
24	X9	Analog Input (or Output)
25	X10	Analog Input (or Output)
26	X11	Analog Input (or Output)
27	X12	Analog Input (or Output)
28	X13	Analog Input (or Output)
29	X14	Analog Output (or Input)
30	X15	Analog Output (or Input)
31	Y0	Analog Output (or Input)
32	Y1	Analog Output (or Input)
33	Y2	Analog Output (or Input)
34	Y3	Analog Output (or Input)
35	Y4	Analog Output (or Input)
36	Y5	Analog Output (or Input)
37	Y6	Analog Output (or Input)
38	Y7	Analog Output (or Input)
39	NC	No Internal Connection
40	NC	No Internal Connection
41	V_{DD}	Positive Analog Power Supply
42	V_{CC}	Digital Power Supply
43	DGND	Digital Ground
44	SOUT	Serial Data Output: Positive True

PIN CONFIGURATION



NC = NO CONNECT

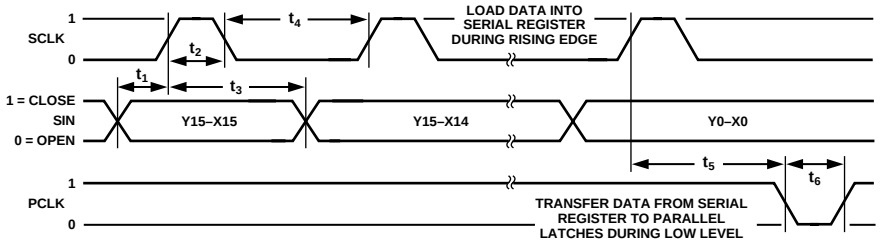
TIMING CHARACTERISTICS[1] ($T_A = T_{MIN}$ to T_{MAX}, rated power supplies unless otherwise noted)

Parameter	Symbol	Value	Units	Condition
Data Setup Time	t_1	20	ns	min
SCLK Pulsewidth	t_2	100	ns	min
Data Hold Time	t_3	40	ns	min
SCLK Pulse Separation	t_4	100	ns	min
SCLK to PCLK Delay	t_5	65	ns	min
SCLK to PCLK Delay and Release	$(t_5 + t_6)$	5	ms	max
PCLK Pulsewidth	t_6	65	ns	min
Propagation Delay, PCLK to Switches On or Off	–	70	ns	max
Data Load Time	–	52	µs	SCLK = 5 MHz
SCLK Frequency	–	20	kHz	min
SCLK, PCLK Rise and Fall Times	–	1	µs	max

NOTES
[1]Timing measurement reference level is 1.5 V.

Specifications subject to change without notice.

TIMING DIAGRAM



OPERATION TRUTH TABLE

Control Lines PCLK	SCLK	SIN	SOUT	Operation/Comment
1	0	X	X	No operation.
1	1	$Data_i$	$Data_{i-256}$	The data on the SIN line is loaded into the serial register; data clocked into the serial register 256 clocks ago appears at the SOUT output.
0	X	X	X	Data in the serial shift register transfers into the parallel latches which control the switch array.

APPLICATIONS INFORMATION

Loading Data

Data to control the switches is clocked serially into a 256-bit shift register and then transferred in parallel to 256 bits of memory. The rising edge of SCLK, the serial clock input, loads data into the shift register. The first bit loaded via SIN, the serial data input, controls the switch at the intersection of row Y15 and column X15. The next bits control the remaining columns (down to X0) of row Y15, and are followed by the bits for row Y14, and so on down to the data for the switch at the intersection of row Y0 and column X0. The shift register is dynamic, so there is a minimum clock rate, specified as 20 kHz.

After the shift register is filled with the new 256 bits of control data, PCLK is activated (pulsed low) to transfer the data to the parallel latches. Since the shift register is dynamic, there is a maximum time delay specified before the data is lost: PCLK must be activated and brought back high within 5 ms after filling the shift register. The switch control latches are static and will hold their data as long as power is applied.

To extend the number of switches in the array, you may cascade multiple AD75019s. The SOUT output is the end of the shift register, and may be directly connected to the SIN input of the next AD75019.

Power Supply Sequencing and Bypassing

All junction-isolated parts operating on multiple power supplies require proper attention to supply sequencing. Because BiMOS II is a junction-isolated process, parasitic diodes exist between V_{DD} and V_{CC}, and between V_{SS} and DGND. As a result, V_{DD} must always be greater than (V_{CC} – 0.5 V), and V_{SS} must always be less than (DGND + 0.5 V).

If you can't ensure that system power supplies will sequence to meet these conditions, external Schottky (e.g., 1N5818) or silicon (e.g., 1N4001) diodes may be used. To protect the positive side, the anode would connect to V_{CC} (Pin 42) and the cathode to V_{DD} (Pin 41). For the negative side, connect the anode to V_{SS} (Pin 4) and the cathode to DGND (Pin 43).

Each of the three power supply pins [V_{DD} (Pin 41), V_{CC} (Pin 42) and V_{SS} (Pin 4)] should be bypassed to DGND (Pin 43) through a 0.1 µF ceramic capacitor located close to the package pins.

Transistor Count

AD75019 contains 5,472 transistors. This number may be used for calculating projected reliability.

ABSOLUTE MAXIMUM RATINGS*

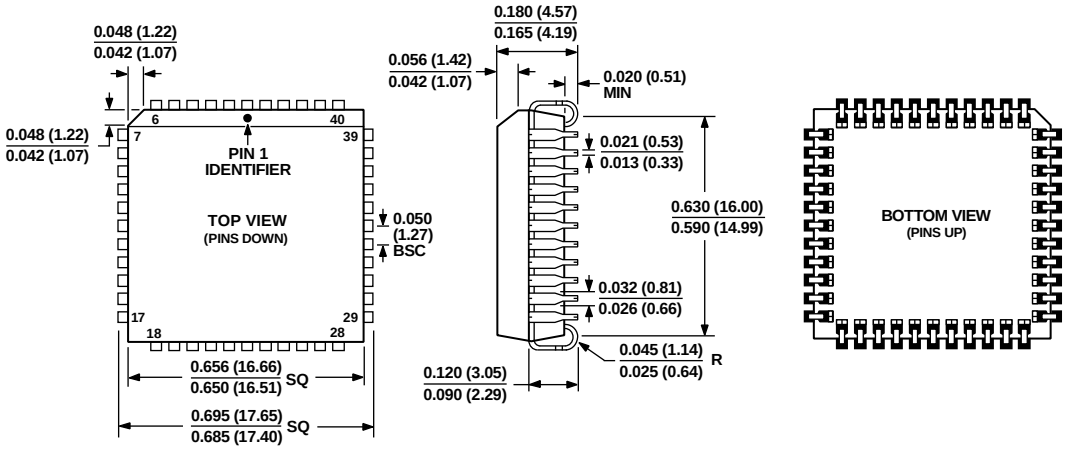
	Min	Max	Units	Conditions
V_{DD} to DGND	–0.5	+25.2	V	
V_{SS} to DGND	–25.2	+0.5	V	
V_{CC} to DGND	–0.5	+7.0	V	
V_{DD} to V_{SS}	–0.5	+25.2	V	
V_{CC} to V_{SS}	–0.5	+25.2	V	
Digital Inputs to DGND	–0.3	V_{CC} + 0.5	V	
Power Dissipation		1.0	W	$T_A \leq 75°C$
Operating Temperature Range	0	+70	°C	
Storage Temperature	–65	+150	°C	
Lead Temperature		+300	°C	Soldering, 10 sec

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are Zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-047-AC
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 1. 44-Lead Plastic Leaded Chip Carrier [PLCC]
(P-44)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD75019JPZ	0°C to 70°C	44-Lead Plastic Leaded Chip Carrier [PLCC]	P-44
AD75019JPZ-REEL	0°C to 70°C	44-Lead Plastic Leaded Chip Carrier [PLCC]	P-44

[1] Z = RoHS Compliant Part.

REVISION HISTORY

10/2018—Rev. C to Rev. D

Changes to Temperature Range Parameter,
AD75019—Specifications Table 2
Moved Outline Dimensions and Ordering Guide 5
Updated Outline Dimensions 5
Changes to Ordering Guide 5