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## REVISION HISTORY

### 5/09—Rev. 0 to Rev A

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### 5/09—Revision 0: Initial Version

## SPECIFICATIONS

$AV_{DD} = 3\text{ V}$  to  $5.25\text{ V}$ ;  $DV_{DD} = 2.7\text{ V}$  to  $5.25\text{ V}$ ;  $AGND = DGND = 0\text{ V}$ ;  $REFIN(+)$  =  $AV_{DD}$ ;  $REFIN(-)$  =  $AGND$ ;  $MCLK = 4.92\text{ MHz}$ ; all specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 1.

Parameter <sup>1</sup>	AD7191B	Unit	Test Conditions/Comments
Output Data Rate	10, 50, 60, 120	Hz nom	
No Missing Codes <sup>2</sup>	24	Bits min	
Resolution			See the RMS Noise and Resolution Specifications section
RMS Noise and Update Rates			See the RMS Noise and Resolution Specifications section
Integral Nonlinearity			
Gain = 1 <sup>2</sup>	±10	ppm of FSR max	±2 ppm typical, $AV_{DD} = 5\text{ V}$
	±15	ppm of FSR max	±2 ppm typical, $AV_{DD} = 3\text{ V}$
Gain > 1	±5	ppm of FSR typ	$AV_{DD} = 5\text{ V}$
	±12	ppm of FSR typ	$AV_{DD} = 3\text{ V}$
Offset Error	±150/gain	μV typ	
Offset Error Drift vs. Temperature	±150/gain	nV/°C typ	Gain = 1 or 8
	±5	nV/°C typ	Gain = 64 or 128
Offset Error Drift vs. Time	25	nV/1000 hours typ	Gain = 64 or 128
Gain Error	±0.4	% typ	
Gain Drift vs. Temperature	±1	ppm/°C typ	
Gain Drift vs. Time	10	ppm/1000 hours typ	Gain = 1
Power Supply Rejection	90	dB typ	Gain = 1, $A_{IN} = 1\text{ V}$
	95	dB min	110 dB typical, gain > 1, $A_{IN} = 1\text{ V/gain}$
Normal Mode Rejection <sup>2</sup>			
Internal Clock			
@ 50 Hz, 60 Hz	100	dB min	10 Hz output data rate, $50 \pm 1\text{ Hz}$ , $60 \pm 1\text{ Hz}$
	74	dB min	50 Hz output data rate, $50 \pm 1\text{ Hz}$ , $60 \pm 1\text{ Hz}$
@ 60 Hz	97	dB min	60 Hz output data rate, $60 \pm 1\text{ Hz}$ .
External Clock			
@ 50 Hz, 60 Hz	120	dB min	10 Hz output data rate, $50 \pm 1\text{ Hz}$ , $60 \pm 1\text{ Hz}$ .
	82	dB min	50 Hz output data rate, $50 \pm 1\text{ Hz}$ , $60 \pm 1\text{ Hz}$ .
@ 60 Hz	120	dB min	60 Hz output data rate, $60 \pm 1\text{ Hz}$
Common-Mode Rejection			
@ DC <sup>2</sup>	100	dB min	Gain = 1, $A_{IN} = 1\text{ V}$
@ DC	110	dB min	Gain > 1, $A_{IN} = 1\text{ V/gain}$
@ 50 Hz, 60 Hz <sup>2</sup>	120	dB min	10 Hz output data rate, $50 \pm 1\text{ Hz}$ , $60 \pm 1\text{ Hz}$
@ 50 Hz, 60 Hz <sup>2</sup>	120	dB min	$50 \pm 1\text{ Hz}$ (50 Hz output data rate), $60 \pm 1\text{ Hz}$ (60 Hz output data rate)
ANALOG INPUTS			
Differential Input Voltage Ranges	± $V_{REF}$ /gain	V nom	$V_{REF} = REFIN(+)$ – $REFIN(-)$ , gain = 1, 8, 64, or 128
	±( $AV_{DD} - 1.25\text{ V}$ )/gain	V min/V max	Gain > 1
Absolute $A_{IN}$ Voltage Limits <sup>2</sup>			
	$AGND + 250\text{ mV}$	V min	
	$AV_{DD} - 250\text{ mV}$	V max	

# AD7191

Parameter <sup>1</sup>	AD7191B	Unit	Test Conditions/Comments
Analog Input Current	±2	nA max	Gain = 1
Input Current <sup>2</sup>	±3	nA max	Gain > 1
Input Current Drift	±5	pA/°C typ	
REFERENCE INPUT			
REFIN Voltage	AV <sub>DD</sub>	V nom	REFIN = REFIN(+) – REFIN(–).
Reference Voltage Range <sup>2</sup>	1 AV <sub>DD</sub>	V min V max	The differential input must be limited to ±(AV <sub>DD</sub> – 1.25 V)/gain when gain > 1.
Absolute REFIN Voltage Limits <sup>2</sup>	AGND – 50 mV AV <sub>DD</sub> + 50 mV	V min V max	
Average Reference Input Current	4.5	µA/V typ	
Average Reference Input Current Drift	±0.03	nA/V/°C typ	External clock.
	±1.3	nA/V/°C typ	Internal clock.
Normal-Mode Rejection <sup>2</sup>	Same as for analog inputs		
Common-Mode Rejection	100	dB typ	
TEMPERATURE SENSOR			
Accuracy	±2	°C typ	Applies after user calibration at one temperature.
Sensitivity	2815	Codes/°C typ	
BRIDGE POWER-DOWN SWITCH			
R <sub>ON</sub>	10	Ω max	
Allowable Current <sup>2</sup>	30	mA max	Continuous current.
INTERNAL/EXTERNAL CLOCK			
Internal Clock			
Frequency	4.92 ± 4%	MHz min/MHz max	
Duty Cycle	50:50	% typ	
External Clock/Crystal			
Frequency	4.9152 2.4576/5.12	MHz nom MHz min/MHz max	
Input Low Voltage, V <sub>INL</sub>	0.8	V max	DV <sub>DD</sub> = 5 V.
	0.4	V max	DV <sub>DD</sub> = 3 V.
Input High Voltage, V <sub>INH</sub>	2.5	V min	DV <sub>DD</sub> = 3 V.
	3.5	V min	DV <sub>DD</sub> = 5 V.
Input Current	±10	µA max	MCLKIN = DV <sub>DD</sub> or DGND.
LOGIC INPUTS			
Input High Voltage, V <sub>INH</sub> <sup>2</sup>	2	V min	
Input Low Voltage, V <sub>INL</sub> <sup>2</sup>	0.8	V max	
Hysteresis <sup>2</sup>	0.1/0.25	V min/V max	
Input Currents	±10	µA max	V <sub>IN</sub> = DV <sub>DD</sub> or DGND.
LOGIC OUTPUT (DOUT/RDY)			
Output High Voltage, V <sub>OH</sub> <sup>2</sup>	DV <sub>DD</sub> – 0.6	V min	DV <sub>DD</sub> = 3 V, I <sub>SOURCE</sub> = 100 µA.
Output Low Voltage, V <sub>OL</sub> <sup>2</sup>	0.4	V max	DV <sub>DD</sub> = 3 V, I <sub>SINK</sub> = 100 µA.
Output High Voltage, V <sub>OH</sub> <sup>2</sup>	4	V min	DV <sub>DD</sub> = 5 V, I <sub>SOURCE</sub> = 200 µA.
Output Low Voltage, V <sub>OL</sub> <sup>2</sup>	0.4	V max	DV <sub>DD</sub> = 5 V, I <sub>SINK</sub> = 1.6 mA.

Parameter <sup>1</sup>	AD7191B	Unit	Test Conditions/Comments
Floating-State Leakage Current	±10	μA max	
Floating-State Output Capacitance	10	pF typ	
Data Output Coding	Offset binary		
POWER REQUIREMENTS <sup>3</sup>			
Power Supply Voltage			
AV <sub>DD</sub> – AGND	3/5.25	V min/V max	
DV <sub>DD</sub> – DGND	2.7/5.25	V min/V max	
Power Supply Currents			
AI <sub>DD</sub> Current	0.85	mA max	0.75 mA typical, gain = 1.
	3.6	mA max	3 mA typical, gain = 8.
	5	mA max	4 mA typical, gain = 64 or 128.
DI <sub>DD</sub> Current	0.4	mA max	0.35 mA typical, DV <sub>DD</sub> = 3 V.
	0.6	mA max	0.5 mA typical, DV <sub>DD</sub> = 5 V.
	1.5	mA typ	External crystal used.
I <sub>DD</sub> (Power-Down Mode)	3	μA max	

<sup>1</sup> Temperature range: –40°C to +105°C.

<sup>2</sup> Specification is not production tested but is supported by characterization data at initial product release.

<sup>3</sup> Digital inputs equal to DV<sub>DD</sub> or DGND.

## TIMING CHARACTERISTICS

$AV_{DD} = 3\text{ V}$  to  $5.25\text{ V}$ ;  $DV_{DD} = 2.7\text{ V}$  to  $5.25\text{ V}$ ;  $AGND = DGND = 0\text{ V}$ , Input Logic 0 =  $0\text{ V}$ , Input Logic 1 =  $DV_{DD}$ , unless otherwise noted.

Table 2.

Parameter <sup>1, 2</sup>	Limit at $T_{MIN}$ , $T_{MAX}$ (B Version)	Unit	Conditions/Comments
$t_3$	100	ns min	SCLK high pulse width
$t_4$	100	ns min	SCLK low pulse width
Read Operation			
$t_1$	0	ns min	PDOWN falling edge to $\overline{DOUT/RDY}$ active time
	60	ns max	$DV_{DD} = 4.75\text{ V}$ to $5.25\text{ V}$
	80	ns max	$DV_{DD} = 2.7\text{ V}$ to $3.6\text{ V}$
$t_2^3$	0	ns min	SCLK active edge to data valid delay <sup>4</sup>
	60	ns max	$DV_{DD} = 4.75\text{ V}$ to $5.25\text{ V}$
	80	ns max	$DV_{DD} = 2.7\text{ V}$ to $3.6\text{ V}$
$t_5^{5, 6}$	10	ns min	Bus relinquish time after PDOWN inactive edge
	80	ns max	
$t_6$	0	ns min	SCLK inactive edge to PDOWN inactive edge
$t_7$	10	ns min	SCLK inactive edge to $\overline{DOUT/RDY}$ high

<sup>1</sup> Sample tested during initial release to ensure compliance. All input signals are specified with  $t_R = t_F = 5\text{ ns}$  (10% to 90% of  $DV_{DD}$ ) and timed from a voltage level of  $1.6\text{ V}$ .

<sup>2</sup> See Figure 3.

<sup>3</sup> These numbers are measured with the load circuit shown in Figure 2 and defined as the time required for the output to cross the  $V_{OL}$  or  $V_{OH}$  limits.

<sup>4</sup> The SCLK active edge is the falling edge of SCLK.

<sup>5</sup> These numbers are derived from the measured time taken by the data output to change  $0.5\text{ V}$  when loaded with the circuit shown in Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the  $50\text{ pF}$  capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and, as such, are independent of external bus loading capacitances.

<sup>6</sup>  $\overline{RDY}$  returns high after a read of the ADC. The digital word can be read only once.

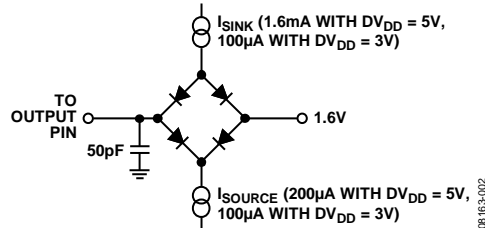


Figure 2. Load Circuit for Timing Characterization

## TIMING DIAGRAM

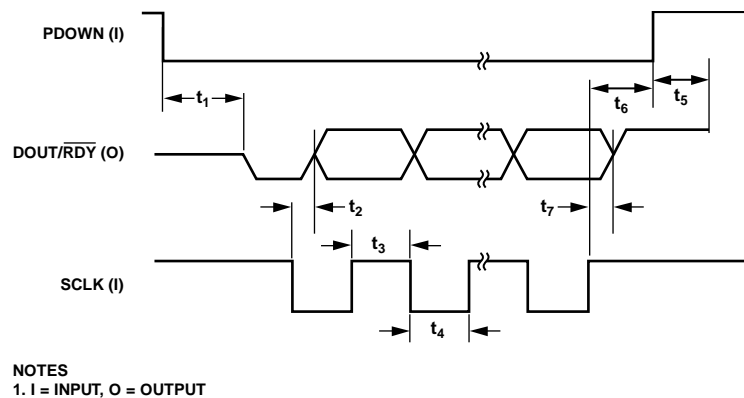


Figure 3. Read Cycle Timing Diagram

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 3.

Parameter	Rating
$AV_{DD}$ to AGND	$-0.3\text{ V to }+6.5\text{ V}$
$DV_{DD}$ to DGND	$-0.3\text{ V to }+6.5\text{ V}$
AGND to DGND	$-0.3\text{ V to }+0.3\text{ V}$
Analog Input Voltage to AGND	$-0.3\text{ V to }AV_{DD} + 0.3\text{ V}$
Reference Input Voltage to AGND	$-0.3\text{ V to }AV_{DD} + 0.3\text{ V}$
Digital Input Voltage to DGND	$-0.3\text{ V to }DV_{DD} + 0.3\text{ V}$
Digital Output Voltage to DGND	$-0.3\text{ V to }DV_{DD} + 0.3\text{ V}$
AIN/Digital Input Current	10 mA
Operating Temperature Range	$-40^\circ\text{C to }+105^\circ\text{C}$
Storage Temperature Range	$-65^\circ\text{C to }+150^\circ\text{C}$
Maximum Junction Temperature TSSOP	$150^\circ\text{C}$
$\theta_{JA}$ Thermal Impedance	$128^\circ\text{C/W}$
$\theta_{JC}$ Thermal Impedance	$42^\circ\text{C/W}$
Lead Temperature, Soldering Reflow	$260^\circ\text{C}$

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

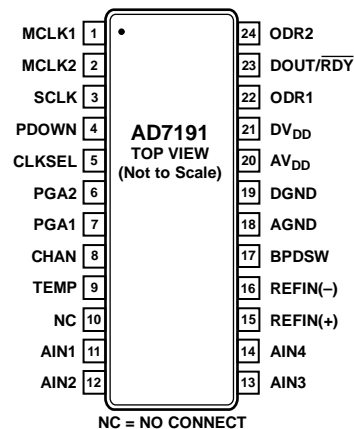


Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	MCLK1	When the master clock for the device is provided externally by a crystal, the crystal is connected between MCLK1 and MCLK2. Alternatively, the MCLK1 pin can be driven with a CMOS-compatible clock and MCLK2 left unconnected.
2	MCLK2	When the master clock for the device is provided externally by a crystal, the crystal is connected between MCLK1 and MCLK2.
3	SCLK	Serial Clock Input. This serial clock input is for controlling data transfers from the ADC. The SCLK has a Schmitt-triggered input, making the interface suitable for opto-isolated applications. The serial clock can be continuous with all data transmitted in a continuous train of pulses. Alternatively, it can be a non-continuous clock with the information transmitted to or from the ADC in smaller batches of data.
4	PDOWN	Power-Down Pin, Digital Input. The PDOWN pin functions as a power-down pin and a reset pin. When PDOWN is taken high, the AD7191 is powered down and the DOUT/RDY pin is tristated. The circuitry and serial interface are also reset. This resets the logic, the digital filter, and the analog modulator. PDOWN must be held high for 100 ns minimum to initiate the reset function.
5	CLKSEL	Clock Select, Digital Input Pin. This pin selects the clock source to be used by the AD7191. When CLKSEL is tied low, the external clock/crystal is used as the clock source. When CLKSEL is tied high, the internal 4.92 MHz clock is used as the clock source to the AD7191.
6	PGA2	Gain Select, Digital Input Pin. This pin is used in conjunction with PGA1 to set the gain. See Table 7.
7	PGA1	Gain Select, Digital Input Pin. This pin is used in conjunction with PGA2 to set the gain. See Table 7.
8	CHAN	Channel Select, Digital Input Pin. This pin is used to select the channel. When CHAN is tied low, channel AIN1/AIN2 is selected. When CHAN is tied high, channel AIN3/AIN4 is selected.
9	TEMP	Temperature Sensor Select, Digital Input Pin. The internal temperature sensor is selected when TEMP is tied high. When TEMP is tied low, the analog input channel AIN1/AIN2 or AIN3/AIN4 is the selected channel (as determined by the CHAN pin).
10	NC	No Connect. This pin should be tied to AGND.
11	AIN1	Analog Input. AIN1 is the positive input of the fully differential input pair AIN1/AIN2.
12	AIN2	Analog Input. AIN2 is the negative input of the fully differential input pair AIN1/AIN2.
13	AIN3	Analog Input. AIN3 is the positive input of the fully differential input pair AIN3/AIN4.
14	AIN4	Analog Input. AIN4 is the negative input of the fully differential input pair AIN3/AIN4.
15	REFIN(+)	Positive Reference Input. An external reference can be applied between REFIN(+) and REFIN(-). REFIN(+) can lie anywhere between AV <sub>DD</sub> and AGND + 1 V. The nominal reference voltage, (REFIN(+) – REFIN(-)), is AV <sub>DD</sub> , but the part functions with a reference from 1 V to AV <sub>DD</sub> .
16	REFIN(-)	Negative Reference Input. This reference input can lie anywhere between AGND and AV <sub>DD</sub> – 1 V.
17	BPDSW	Bridge Power-Down Switch to AGND. When PDOWN is low, the bridge power-down switch is closed. When PDOWN is high, the bridge power-down switch is opened.
18	AGND	Analog Ground Reference Point.
19	DGND	Digital Ground Reference Point.

Pin No.	Mnemonic	Description
20	AV <sub>DD</sub>	Analog Supply Voltage, 3 V to 5.25 V. AV <sub>DD</sub> is independent of DV <sub>DD</sub> . Therefore, DV <sub>DD</sub> can be operated at 3 V with AV <sub>DD</sub> at 5 V or vice versa.
21	DV <sub>DD</sub>	Digital Supply Voltage, 2.7 V to 5.25 V. DV <sub>DD</sub> is independent of AV <sub>DD</sub> . Therefore, AV <sub>DD</sub> can be operated at 3 V with DV <sub>DD</sub> at 5 V or vice versa.
22	ODR1	Output Data Rate, Digital Input Pin. This pin is used with ODR2 to select the output data rate. See Table 5.
23	DOUT/RDY	Serial Data Output/Data Ready Output. DOUT/RDY serves a dual purpose. It functions as a serial data output pin to access the data conversions from the ADC. In addition, DOUT/RDY operates as a data ready pin, going low to indicate the completion of a conversion. If the data is not read after the conversion, the pin goes high before the next update occurs. The serial interface is reset each time that a conversion is available. The DOUT/RDY falling edge can be used as an interrupt to a processor, indicating that valid data is available. With an external serial clock, the data can be read using the DOUT/RDY pin. Data is placed on the DOUT/RDY pin on the SCLK falling edge and is valid on the SCLK rising edge.
24	ODR2	Output Data Rate, Digital Input Pin. This pin is used with ODR1 to select the output data rate. See Table 5.



## TYPICAL PERFORMANCE CHARACTERISTICS

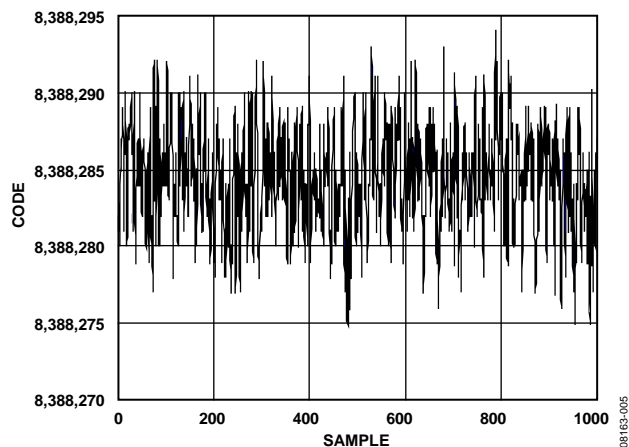


Figure 5. Noise ( $V_{REF} = AV_{DD}$ , Output Data Rate = 10 Hz, Gain = 128)

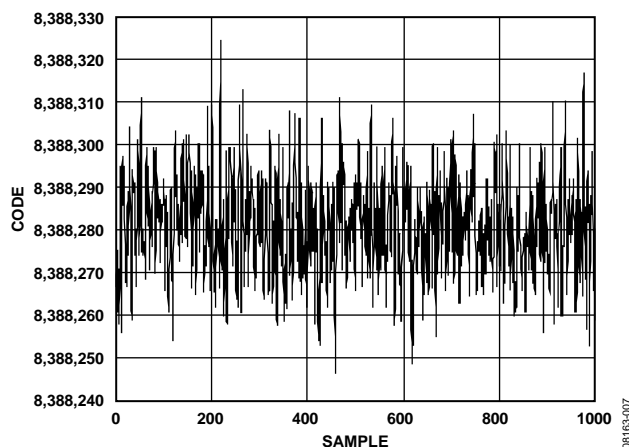


Figure 7. Noise ( $V_{REF} = AV_{DD}$ , Output Data Rate = 120 Hz, Gain = 128)

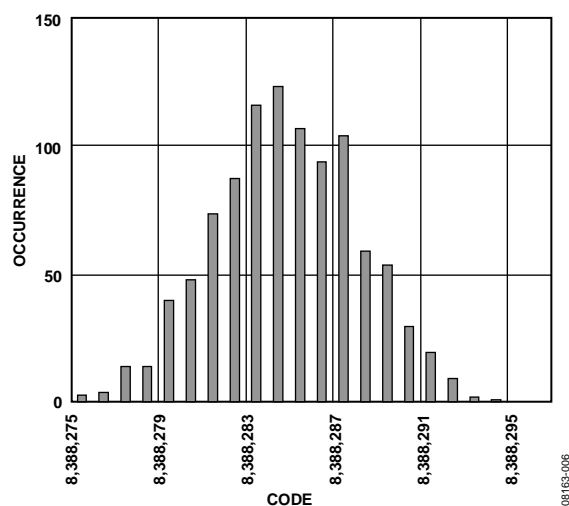


Figure 6. Noise Distribution Histogram ( $V_{REF} = AV_{DD}$ , Output Data Rate = 10 Hz, Gain = 128)

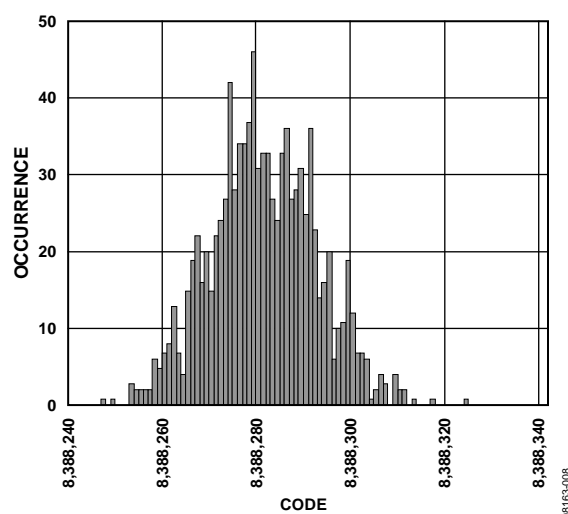


Figure 8. Noise Distribution Histogram ( $V_{REF} = AV_{DD}$ , Output Data Rate = 120 Hz, Gain = 128)

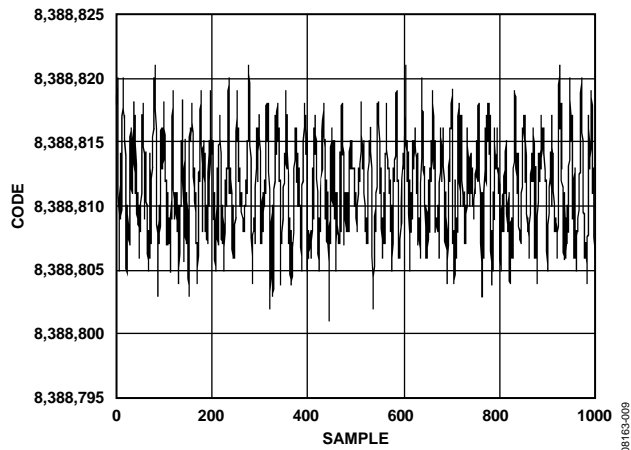


Figure 9. Noise ( $V_{REF} = AV_{DD}$ , Output Data Rate = 120 Hz, Gain = 1)

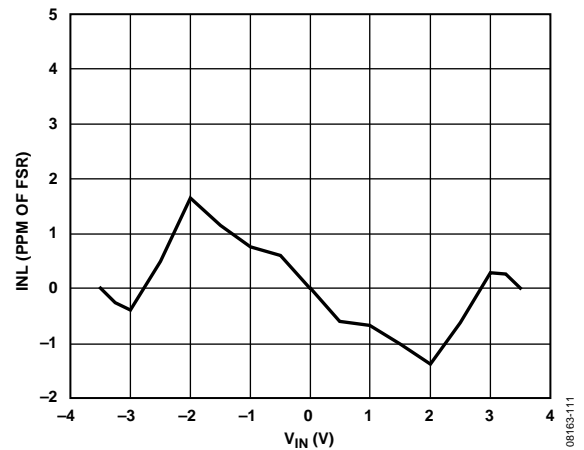


Figure 11. INL (Gain = 1)

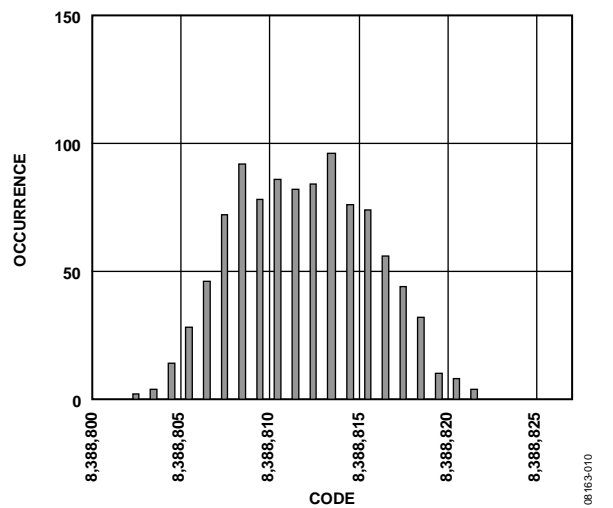


Figure 10. Noise Distribution Histogram ( $V_{REF} = AV_{DD}$ , Output Data Rate = 120 Hz, Gain = 1)

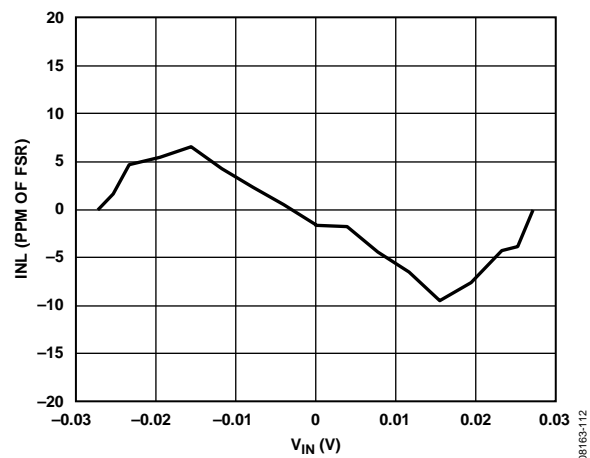


Figure 12. INL (Gain = 128)

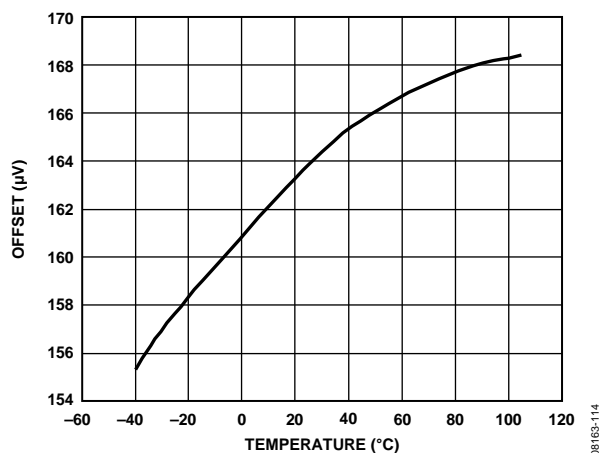


Figure 13. Offset Error (Gain = 1)

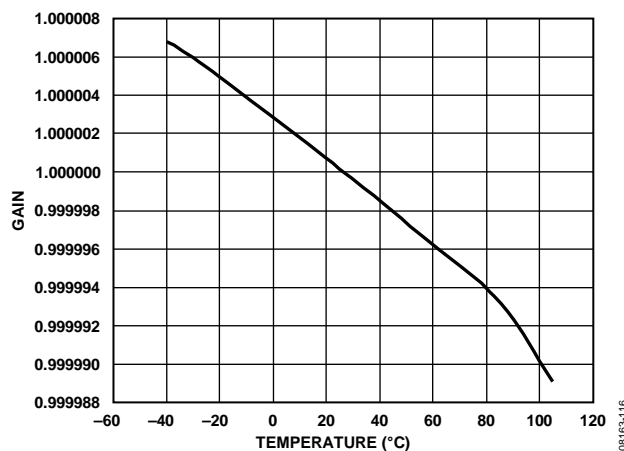


Figure 15. Gain Error (Gain = 1)

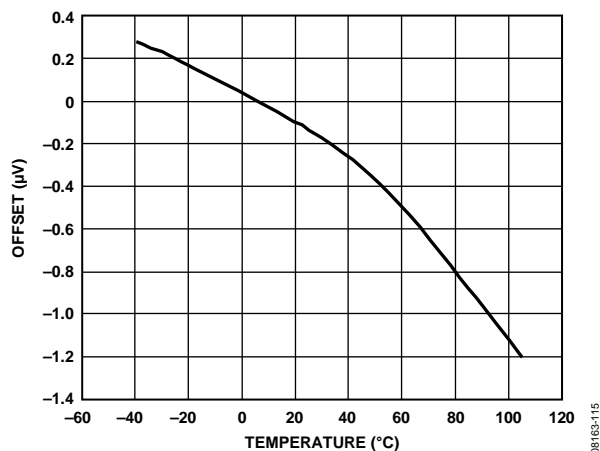


Figure 14. Offset Error (Gain = 128)

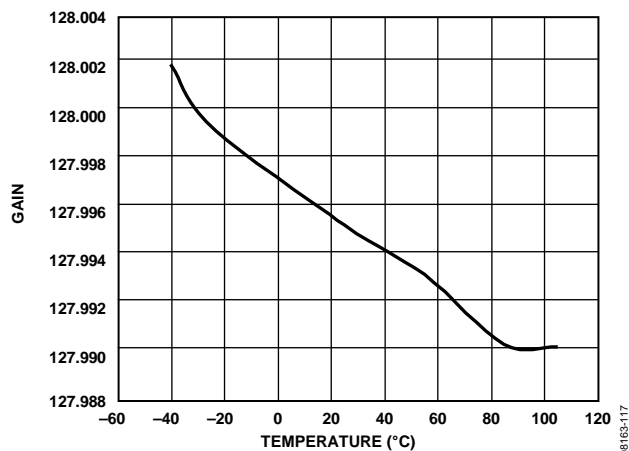


Figure 16. Gain Error (Gain = 128)

## RMS NOISE AND RESOLUTION SPECIFICATIONS

Table 5 shows the rms noise of the AD7191 for the four output data rates and four gains. The numbers given are for an external 5 V reference. These numbers are typical and are generated with a differential input voltage of 0 V. Table 6 shows the effective resolution; the output peak-to-peak (p-p) resolution is listed in brackets. It is important to note that the effective resolution is calculated using the rms noise, whereas the p-p resolution is calculated based on peak-to-peak noise. The p-p resolution represents the resolution for which there is

no code flicker. These numbers are typical and are rounded to the nearest half-LSB.

The effective resolution (ENOB) is defined as

$$ENOB = \log_2 (Full\text{-}Scale\ Range / rms\ Noise)$$

The noise-free bits or p-p resolution is defined as

$$p\text{-}p\ Resolution = \log_2 (Full\text{-}Scale\ Range / p\text{-}p\ Noise)$$

where  $Full\text{-}Scale\ Range = 2 \times V_{REF} / Gain$ .

**Table 5. RMS Noise (nV) vs. Gain and Output Data Rate Using a 5 V Reference**

ODR2, ODR1	Output Data Rate (Hz)	Settling Time (ms)	Gain of 1	Gain of 8	Gain of 64	Gain of 128
11	10	400	490	85	17	15
10	50	80	2000	260	46	34
01	60	66.7	2100	273	48	38
00	120	33.3	2400	315	64	51

**Table 6. Typical Resolution (Bits) vs. Gain and Output Update Rate Using a 5 V Reference**

ODR2, ODR1	Output Data Rate (Hz)	Settling Time (ms)	Gain of 1	Gain of 8	Gain of 64	Gain of 128
11	10	400	24 (21.5)	23.5 (21)	23 (20.5)	22 (19.5)
10	50	80	22 (19.5)	22 (19.5)	21.5 (19)	20.5 (18)
01	60	66.7	22 (19.5)	22 (19.5)	21.5 (19)	20.5 (18)
00	120	33.3	22 (19.5)	21.5 (19)	21 (18.5)	20 (17.5)

## ADC CIRCUIT INFORMATION

### OVERVIEW

The AD7191 is a low noise, complete analog front end for high precision measurement applications. It contains a low noise, 24-bit,  $\Sigma$ - $\Delta$  ADC, a PGA, and an on-chip digital filter intended for measuring wide dynamic range signals.

The device has an internal clock and two differential analog inputs. It offers a choice of four output data rates (10 Hz, 50 Hz, 60 Hz, and 120 Hz) and four gain settings (1, 8, 64, and 128). The device also has an internal temperature sensor. These functions are controlled using dedicated pins, which make the interface easy to configure. A 2-wire interface simplifies data retrieval from the AD7191.

### FILTER, DATA RATE, AND SETTLING TIME

The AD7191 has four output data rates, which are selected using the ODR2 and ODR1 pins (see Table 5). When the polarity of ODR2 or ODR1 is changed, the AD7191 modulator and filter are reset immediately.  $\overline{\text{DOUT/RDY}}$  is set high, and the ADC then begins conversions using the selected output data rate. The first conversion requires the complete settling time of the filter. Subsequent conversions occur at the selected output data rate. The settling time of the digital filter,  $t_{\text{SETTLE}}$ , is

$$t_{\text{SETTLE}} = 4/\text{Output Data Rate}$$

That is, the settling time is equal to four conversion cycles.

When a step change occurs on the analog input, the AD7191 requires several conversion cycles to generate a valid conversion. If the step change occurs synchronous to the conversion period (see Figure 17), then to generate a valid conversion, the settling time of the AD7191 must be allowed. If the step change occurs asynchronous to the end of a conversion (see Figure 18), then to generate a valid conversion, an extra conversion period must be allowed. The diagrams show the case for an output data rate of 50 Hz; therefore, an asynchronous step change can increase the time to generate a valid conversion by 20 ms. The data register is updated with all the conversions but, for an accurate result, the user must allow the required time.

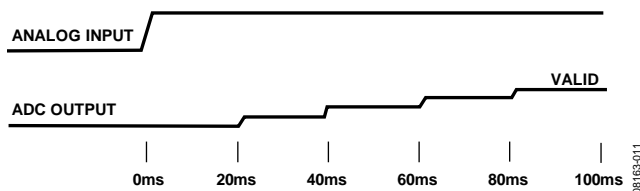


Figure 17. Synchronous Analog Input Step Change

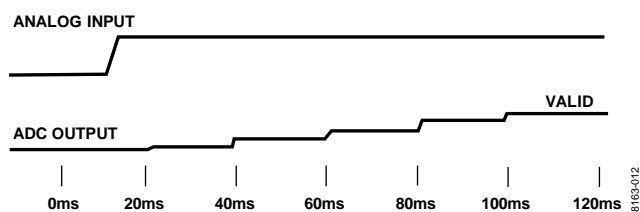


Figure 18. Asynchronous Analog Input Step Change

Figure 19 to Figure 22 show the filter response for each of the allowed output data rates. The filter provides more than  $-53$  dB of rejection in the stop band. When the output data rate is equal to 10 Hz, 60 Hz, or 120 Hz, the first notch occurs at a frequency equal to the output data rate. The other notches occur at multiples of the output data rate. Therefore, when the output data rate is equal to 10 Hz, notches are placed at 50 Hz and 60 Hz, giving simultaneous 50 Hz/60 Hz rejection. When the 60 Hz output data rate is selected, 60 Hz rejection is achieved. When the 50 Hz output data rate is selected, notches are placed at 50 Hz and multiples of 50 Hz. A notch is also placed at 60 Hz. This gives simultaneous 50 Hz/60 Hz rejection for an output data rate of 50 Hz.

When the output data rate is changed,  $\overline{\text{DOUT/RDY}}$  goes high and remains high until the appropriate settling time has elapsed. Therefore, the user should complete any read operations before changing the output data rate. Otherwise, 1s are read back from the AD7191 as the  $\overline{\text{DOUT/RDY}}$  pin is set high following the change in output data rate.

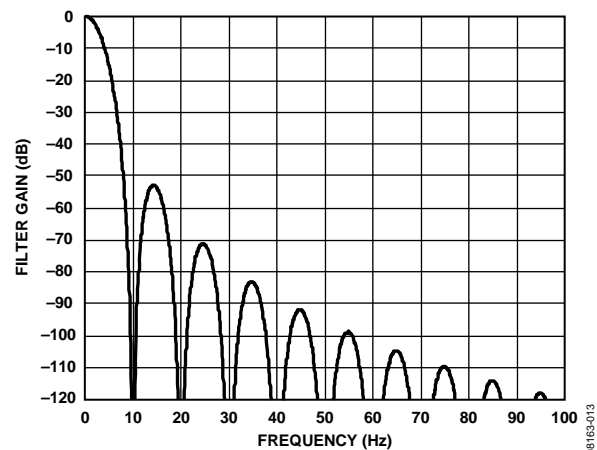


Figure 19. Filter Profile for the 10 Hz Output Data Rate

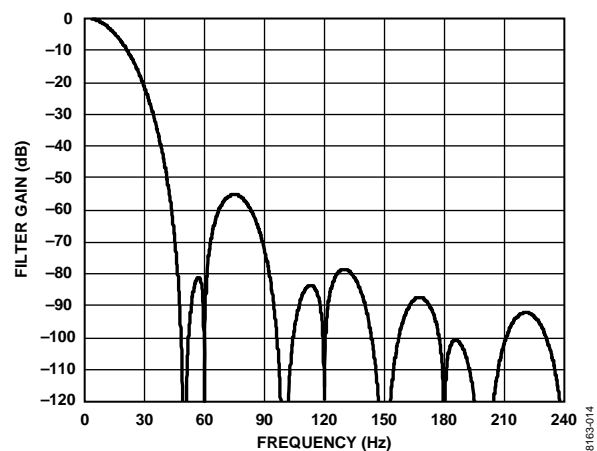


Figure 20. Filter Profile for the 50 Hz Output Data Rate

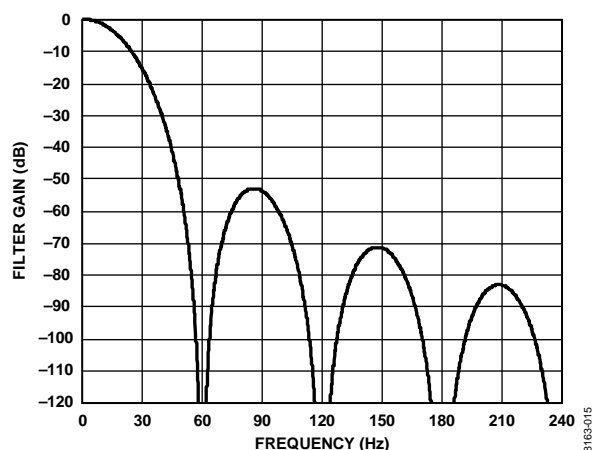


Figure 21. Filter Profile for the 60 Hz Output Data Rate

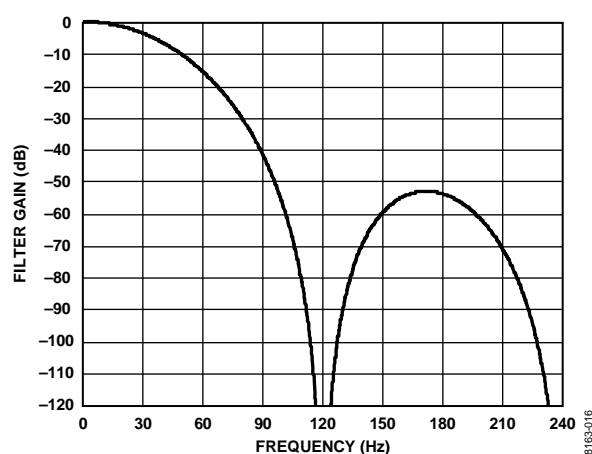


Figure 22. Filter Profile for the 120 Hz Output Data Rate

## GAIN

The AD7191 has four gain options: gain = 1, gain = 8, gain = 64, and gain = 128. The PGA2 and PGA1 pins are used to set the gain. The analog input range is  $\pm V_{REF}/\text{gain}$ . Table 7 shows the gains and the corresponding analog input ranges.

Table 7. Gain Settings

PGA2	PGA1	GAIN	Input Range
0	0	1	$\pm V_{REF}$
0	1	8	$\pm V_{REF}/8$
1	0	64	$\pm V_{REF}/64$
1	1	128	$\pm V_{REF}/128$

When the polarity of the PGA2 pin or PGA1 pin is changed, the AD7191 modulator and filter are reset immediately. DOUT/RDY is set high. The ADC then begins conversions. DOUT/RDY remains high until the appropriate settling time for the filter has elapsed. Therefore, any read operations should be completed before changing the gain. Otherwise, all 1s are read back from the AD7191 as the DOUT/RDY pin is set high following the gain change. The complete settling time of the filter is required to generate the first conversion after the gain change, whereas subsequent conversions occur at the selected output data rate.

## ANALOG INPUT CHANNELS

The AD7191 has two differential analog input channels, AIN1/AIN2 and AIN3/AIN4. Each input channel feeds into a high impedance input stage of the amplifier. Therefore, the input can tolerate high source impedances and is tailored for direct connection to external resistive-type sensors such as strain gauges or loadcells. The channel is selected using the CHAN pin. When CHAN is tied low, channel AIN1/AIN2 is selected, whereas channel AIN3/AIN4 is selected when the CHAN pin is tied high.

The absolute input voltage range is restricted to a range between AGND + 250 mV and  $AV_{DD} - 250$  mV. Care must be taken in setting up the common-mode voltage to avoid exceeding these limits. Otherwise, there is degradation in linearity and noise performance.

The low noise PGA means that signals of small amplitude can be amplified within the AD7191 while still maintaining excellent noise performance. The amplifier can be configured to have a gain of 1, 8, 64, or 128 using the PGA2 and PGA1 pins. The analog input range is equal to  $\pm V_{REF}/\text{gain}$ .

The analog input range must be limited to  $(AV_{DD} - 1.25 \text{ V})/\text{gain}$  because the PGA requires some headroom. Therefore, if  $AV_{DD} = 5 \text{ V}$ , the maximum analog input that can be applied to the AD7191 is  $\pm 3.75 \text{ V}/\text{gain}$ .

When the channel is changed, DOUT/RDY goes high and remains high until the appropriate settling time has elapsed. Therefore, any read operations should be completed before changing the channel. Otherwise, all 1s are read back from the AD7191 as the DOUT/RDY pin is set high following the channel change.

## TEMPERATURE SENSOR

Embedded in the AD7191 is a temperature sensor. The temperature sensor is selected when the TEMP pin is tied high. The TEMP pin has higher priority than the CHAN pin; therefore, when TEMP is high, the temperature sensor is selected irrespective of the polarity on the CHAN pin.

When the temperature sensor is selected, the device should return a code of 0x800000 when the temperature is 0 K. A one-point calibration is needed to get the optimum performance from the sensor. Therefore, a conversion at 25°C should be recorded and the sensitivity calculated. The sensitivity is 2815 codes/°C, approximately. The equation for the temperature sensor is

$$Temp (K) = (Conversion - 0x800000) / 2815 K$$

$$Temp (°C) = Temp (K) - 273$$

Following the one point calibration, the internal temperature sensor has an accuracy of ±2°C, typically.

Each time the temperature sensor is selected, DOUT/RDY goes high and remains high until the appropriate settling time elapses. Therefore, any read operations should be completed before selecting the temperature sensor. Otherwise, all 1s are read back from the AD7191 as the DOUT/RDY pin is set high following the channel change.

## POWER-DOWN (PDOWN)

The PDOWN pin functions as a power-down pin and a reset pin. When PDOWN is taken high, the AD7191 is powered down and the DOUT/RDY pin is tristated. If the on-chip clock is selected, it will be powered down also. If an external crystal is being used, the on-chip oscillator circuitry remains active.

With PDOWN high, the circuitry and serial interface are also reset. This resets the logic, the digital filter, and the analog modulator. PDOWN must be held high for 100 ns minimum to initiate the reset function.

When PDOWN is taken low, the AD7191 is taken out of power-down mode. When the on-chip clock has powered up (1 ms, typically), the modulator begins sampling the analog input, and the DOUT/RDY pin becomes active. When an external crystal or clock is used as the master clock source to the AD7191, the 1 ms power-up time is not required. A reset is automatically performed on power-up.

## CLOCK

The AD7191 has an internal 4.92 MHz clock that has a 4% tolerance. The AD7191 can use the internal clock or, alternatively, an external clock or crystal can be used. The CLKSEL pin is used to select the clock source. When CLKSEL is low, an external clock/crystal is selected. When CLKSEL is high, the internal clock is selected. If a crystal is used, the crystal should be connected between MCLK1 and MCLK2. The user should refer to the crystal data sheet for details on the capacitor values. If an external clock source is used, it should be applied to MCLK1. MCLK2 should be left unconnected.

When the polarity of CLKSEL is changed, DOUT/RDY goes high and remains high until the appropriate settling time elapses.

## BIPOLAR CONFIGURATION

The AD7191 accepts a bipolar input range. A bipolar input range does not imply that the part can tolerate negative voltages with respect to system AGND. Signals on the positive analog input pin are referenced to the voltage on the negative analog input pin. For example, if AIN2 is 2.5 V, the analog input range on the AIN1 input is 2.461 V to 2.539 V for a gain of 128 when a 5 V reference is used.

## DATA OUTPUT CODING

The AD7191 uses offset binary coding. Therefore, a negative full-scale voltage results in a code of 000...000, a zero differential input voltage results in a code of 100...000, and a positive full-scale input voltage results in a code of 111...111. The output code for any analog input voltage can be represented as

$$Code = 2^{N-1} \times [(AIN \times Gain / V_{REF}) + 1]$$

where AIN is the analog input voltage (AIN1 – AIN2 or AIN3 – AIN4), Gain is 1, 8, 64, or 128, and N = 24 for the AD7191.

## BRIDGE POWER-DOWN SWITCH

The bridge power-down switch (BPDSW) is useful in battery-powered applications where it is essential that the power consumption of the system be optimized. A 350 Ω load cell consumes 15 mA typically when excited with a 5 V power supply. To minimize the current consumption, the load cell is disconnected when it is not being used. The bridge power-down switch can be included in series with the load cell. When PDOWN is low, the bridge power-down switch is closed, and the load cell measures the strain. When PDOWN is high, the bridge power-down switch is opened so that no current flows through the load cell. Therefore, the current consumption of the system is minimized. The bridge power-down switch has an on-resistance of 10 Ω maximum, and it is capable of withstanding 30 mA of continuous current.

## REFERENCE

The AD7191 has a fully differential input capability. The common-mode range for these differential inputs is AGND to AV<sub>DD</sub>. The reference input is unbuffered; therefore, excessive R-C source impedances introduce gain errors. The reference voltage REFIN (REFIN(+) – REFIN(–)) is AV<sub>DD</sub> nominal, but the AD7191 is functional with reference voltages of 1 V to AV<sub>DD</sub>. In applications where the excitation (voltage or current) of the transducer connected to the analog input also drives the reference voltage for the part, the effect of the low frequency noise in the excitation source is removed because the application is ratio-metric. If the AD7191 is used in a nonratiometric application, a low noise reference should be used.

Recommended 2.5 V reference voltage sources for the AD7191 include the [ADR421](#), which is a low noise reference. These references have low output impedances and are, therefore,

tolerant to decoupling capacitors on REFIN(+) without introducing gain errors in the system. Deriving the reference input voltage across an external resistor means that the reference input sees a significant external source impedance. External decoupling on the REFIN pins is not recommended in this type of circuit configuration.

## DIGITAL INTERFACE

The serial interface of the AD7191 consists of two signals: SCLK and DOUT/RDY. SCLK is the serial clock input for the device, and data transfers occur with respect to the SCLK signal. The DOUT/RDY pin is dual purpose: it functions as a data ready pin and as a data output pin. DOUT/RDY goes low when a new data-word is available in the output register. A 24-bit word is placed on the DOUT/RDY pin when sufficient SCLK pulses are applied.

DOUT/RDY is reset high when the conversion has been read. If the conversion is not read, DOUT/RDY goes high prior to the next data register update to indicate when not to read from the device. This ensures that a read operation is not attempted while the register is being updated. Each conversion can be read only once. The data register is updated for every conversion. Thus, when a conversion is complete, the serial interface is reset, and the new conversion is placed in the data register. Therefore, the user must ensure that the complete word is read before the next conversion is complete.

When PDOWN is high, the DOUT/RDY pin is tristated. When PDOWN is taken low, the internal clock requires 1 ms approximately to power up. Following this, the ADC continuously converts. The first conversion requires the complete settling time. DOUT/RDY goes high when PDOWN is taken low and returns low only when a conversion is available. The ADC then converts continuously, and subsequent conversions are available at the selected output data rate. Figure 3 shows the timing for a read operation from the AD7191.

When the output data rate, gain, channel, or clock source is changed, the modulator and filter are reset immediately. DOUT/RDY is set high.

The ADC then begins conversions using the new configuration. DOUT/RDY remains high until the appropriate settling time for the filter elapses. Therefore, any read operations should be completed before changing the operating conditions or channel. Otherwise, all 1s are read back from the AD7191 as the DOUT/RDY pin is set high following the channel change or configuration change.

## GROUNDING AND LAYOUT

Because the analog inputs and reference input on the AD7191 are differential, most of the voltages in the analog modulator are common-mode voltages. The excellent common-mode rejection of the part removes common-mode noise on these inputs.

The analog and digital supplies to the AD7191 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The AD7191 can be operated with 5 V analog and 3 V digital supplies or vice versa. The digital filter provides rejection of broadband noise on the power supplies, except at integer multiples of the modulator sampling frequency. A simple R-C low-pass filter on the analog inputs rejects any interference at the clock frequency. The digital filter also removes noise from the analog and reference inputs, provided that these noise sources do not saturate the analog modulator. As a result, the AD7191 is more immune to noise interference than a conventional high resolution converter. However, because the resolution of the AD7191 is so high, and the noise levels from the AD7191 are so low, care must be taken with regard to grounding and layout.

The printed circuit board should be designed such that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. A minimum etch technique is generally best for ground planes because it gives the best shielding.

Although the AD7191 has separate pins for analog and digital ground, the AGND and DGND pins are tied together within the device via the substrate. The user must not tie these pins externally to separate ground planes unless the ground planes are connected together near the AD7191.



## AD7191

In systems where the AGND and DGND pins are connected somewhere else in the system (that is, at the system power supply), they should not be connected again at the AD7191 because a ground loop results. In these situations, it is recommended that the AD7191 AGND and DGND pins be tied to the AGND plane. In any layout, it is important that the user keep in mind the flow of currents in the system, ensuring that the return paths for all currents are as close as possible to the paths the currents took to reach their destinations. Avoid forcing digital currents to flow through the AGND sections of the layout.

Avoid running digital lines under the device because these couple noise onto the die. The analog ground plane should be allowed to run under the AD7191 to prevent noise coupling. The power supply lines to the AD7191 should use as wide a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite

sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, and signals are placed on the solder side.

Good decoupling is important when using high resolution ADCs. All analog supplies should be decoupled with 10  $\mu\text{F}$  tantalum capacitors in parallel with 0.1  $\mu\text{F}$  capacitors to AGND. To achieve the best from these decoupling components, they have to be placed as close as possible to the device, ideally right up against the device. All logic chips should be decoupled with 0.1  $\mu\text{F}$  ceramic capacitors to DGND. In systems where a common supply voltage is used to drive both the  $\text{AV}_{\text{DD}}$  and  $\text{DV}_{\text{DD}}$  of the AD7191, it is recommended that the system  $\text{AV}_{\text{DD}}$  supply be used. This supply should have the recommended analog supply decoupling capacitors between the  $\text{AV}_{\text{DD}}$  pin of the AD7191 and AGND, and the recommended digital supply decoupling capacitor between the  $\text{DV}_{\text{DD}}$  pin of the AD7191 and DGND.

## APPLICATIONS INFORMATION

The AD7191 provides a low-cost, high resolution analog-to-digital function. Because the analog-to-digital function is provided by a  $\Sigma$ - $\Delta$  architecture, the part is more immune to noisy environments, making it ideal for use in sensor measurement and industrial and process control applications.

### WEIGH SCALES

Figure 24 shows the AD7191 being used in a weigh scale application. The load cell is arranged in a bridge network and gives a differential output voltage between its OUT+ and OUT- terminals. Assuming a 5 V excitation voltage, the full-scale output range from the transducer is 10 mV when the sensitivity is 2 mV/V. The excitation voltage for the bridge can be used to directly provide the reference for the ADC because the reference input range includes the supply voltage.

A second advantage of using the AD7191 in transducer-based applications is that the bridge power-down switch can be fully utilized in low power applications. The bridge power-down switch is connected in series with the low side of the bridge. In normal operation, the switch is closed and measurements can be taken. In applications where power is of concern, the AD7191 can be placed in power-down mode, thus significantly reducing the power consumed in the application. In addition, the bridge power-down switch is opened while in power-down mode, thus avoiding unnecessary power consumption by the front-end transducer. When the part is taken out of power-down mode and the bridge power-down switch is closed, the user should ensure that the front-end circuitry is fully settled before attempting a read from the AD7191.

The load cell has an offset or TARE associated with it. This TARE is the main component of the system offset (load cell plus ADC) and is of a magnitude similar to the full-scale signal from

the load cell. For this reason, a system calibration that calibrates the offset and full-scale error of the ADC plus the load cell is required. A microprocessor can be used to perform the calibrations. The offset (the conversion result from the AD7191 when no load is applied to the load cell) and the full-scale error (the conversion result from the ADC when the maximum load is applied to the load cell) must be determined. Subsequent conversions from the AD7191 are then corrected using the offset and full-scale coefficients calculated from the above calibrations.

### EMI RECOMMENDATIONS

For simplicity, the EMI filters are not included in Figure 24. However, an R-C antialias filter should be included on each analog input. This filter is needed because the on-chip digital filter does not provide any rejection around MCLK/8 or multiples of this frequency. Suitable values are a 100  $\Omega$  resistor in series with each analog input, a 0.1  $\mu$ F capacitor from AIN(+) to AIN(-), and 0.01  $\mu$ F capacitors from AIN(+)/AIN(-) to AGND (see Figure 23).

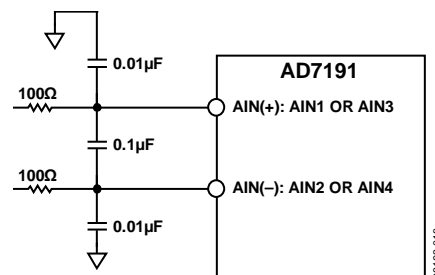


Figure 23. External Filtering Connections

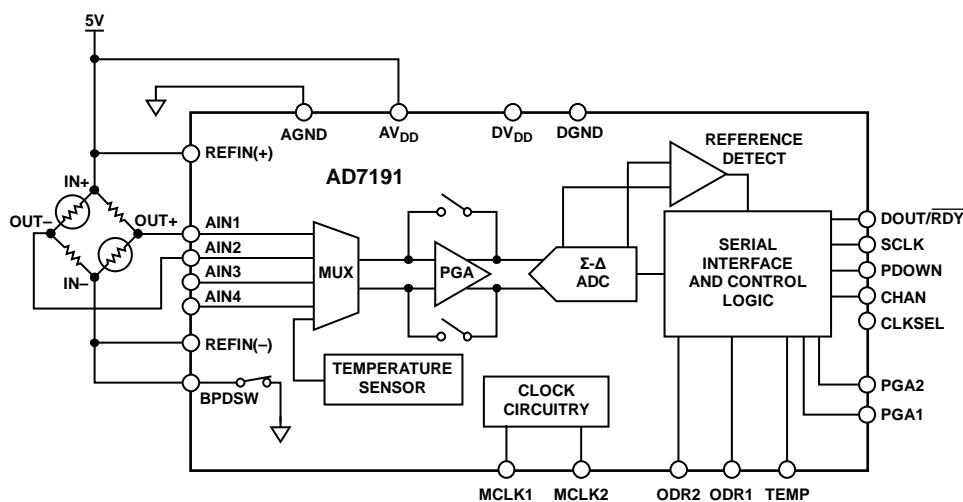
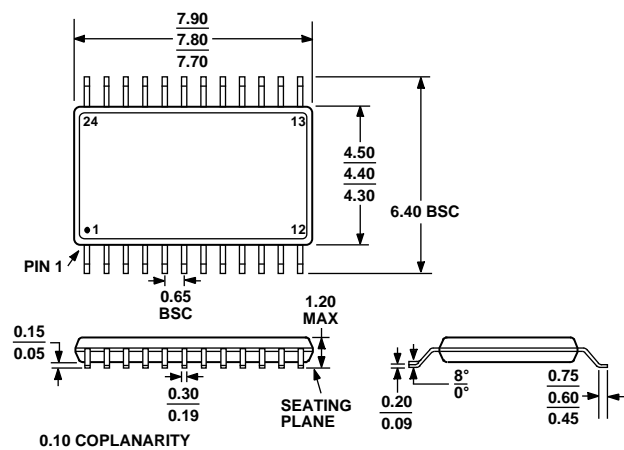


Figure 24. Typical Application (Weigh Scale)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AD

Figure 25. 24-Lead Thin Shrink Small Outline Package [TSSOP]  
(RU-24)  
Dimensions shown in millimeters

ORDERING GUIDE

Models	Temperature Range	Package Description	Package Option
AD7191BRUZ <sup>1</sup>	−40°C to +105°C	24-Lead TSSOP	RU-24
AD7191BRUZ-REEL <sup>1</sup>	−40°C to +105°C	24-Lead TSSOP	RU-24

<sup>1</sup> Z = RoHS Compliant Part.