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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—AD5272

V_{DD} = 2.7 V to 5.5 V, V_{SS} = 0 V; V_{DD} = 2.5 V to 2.75 V, V_{SS} = −2.5 V to −2.75 V; −40°C < T_A < +125°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resolution			10			Bits
Resistor Integral Nonlinearity[2, 3]	R-INL	R_{AW}= 20 kΩ, $\|V_{DD} - V_{SS}\|$ = 3.0 V to 5.5 V	−1		+1	LSB
		R_{AW}= 20 kΩ, $\|V_{DD} - V_{SS}\|$ = 2.7 V to 3.0 V	−1		+1.5	LSB
		R_{AW}= 50 kΩ, 100 kΩ	−1		+1	LSB
Resistor Differential Nonlinearity[2]	R-DNL		−1		+1	LSB
Nominal Resistor Tolerance						
R-Perf Mode[4]		See Table 2 and Table 3	−1	±0.5	+1	%
Normal Mode				±15		%
Resistance Temperature Coefficient[5, 6]		Code = full scale		5		ppm/°C
Wiper Resistance		Code = zero scale		35	70	Ω
RESISTOR TERMINALS						
Terminal Voltage Range[5, 7]			V_{SS}		V_{DD}	V
Capacitance[5] A		f = 1 MHz, measured to GND, code = half scale		90		pF
Capacitance[5] W		f = 1 MHz, measured to GND, code = half scale		40		pF
Common-Mode Leakage Current[5]		$V_A = V_W$			50	nA
DIGITAL INPUTS						
Input Logic[5]						
High	V_{INH}		2.0			V
Low	V_{INL}				0.8	V
Input Current	I_{IN}			±1		µA
Input Capacitance[5]	C_{IN}			5		pF
DIGITAL OUTPUT						
Output Voltage[5]						
High	V_{OH}	R_{PULL_UP} = 2.2 kΩ to V_{DD}	V_{DD} − 0.1			V
Low	V_{OL}	R_{PULL_UP} = 2.2 kΩ to V_{DD}				
		V_{DD} = 2.7 V to 5.5 V, V_{SS} = 0 V			0.4	V
		V_{DD} = 2.5 V to 2.75 V, V_{SS} = −2.5 V to −2.75 V			0.6	V
Tristate Leakage Current			−1		+1	µA
Output Capacitance[5]				5		pF
POWER SUPPLIES						
Single-Supply Power Range		V_{SS} = 0 V	2.7		5.5	V
Dual-Supply Power Range			±2.5		±2.75	V
Supply Current						
Positive	I_{DD}				1	µA
Negative	I_{SS}		−1			µA
50-TP Store Current[5, 8]						
Positive	$I_{DD\_OTP\_STORE}$			4		mA
Negative	$I_{SS\_OTP\_STORE}$			−4		mA
50-TP Read Current[5, 9]						
Positive	$I_{DD\_OTP\_READ}$				500	µA
Negative	$I_{SS\_OTP\_READ}$		−500			µA
Power Dissipation[10]		$V_{IH} = V_{DD}$ or V_{IL} = GND			5.5	µW

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
Power Supply Rejection Ratio[5]	PSRR	$\Delta V_{DD}/\Delta V_{SS}$ = ±5 V ± 10%				dB
		R_{AW} = 20 kΩ		−66	−55	
		R_{AW} = 50 kΩ		−75	−67	
		R_{AW} = 100 kΩ		−78	−70	
DYNAMIC CHARACTERISTICS[5, 11]						
Bandwidth		−3 dB, R_{AW} = 10 kΩ, Terminal W, see Figure 41				kHz
		R_{AW} = 20 kΩ		300		
		R_{AW} = 50 kΩ		120		
		R_{AW} = 100 kΩ		60		
Total Harmonic Distortion		V_A = 1 V rms, f = 1 kHz, code = half scale				dB
		R_{AW} = 20 kΩ		−90		
		R_{AW} = 50 kΩ		−88		
		R_{AW} = 100 kΩ		−85		
Resistor Noise Density		Code = half scale, T_A = 25°C, f = 10 kHz				nV/√Hz
		R_{AW} = 20 kΩ		13		
		R_{AW} = 50 kΩ		25		
		R_{AW} = 100 kΩ		32		

[1] Typical specifications represent average readings at 25°C, V_{DD} = 5 V, and V_{SS} = 0 V.
[2] Resistor position nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions.
[3] The maximum current in each code is defined by $I_{AW} = (V_{DD} - 1)/R_{AW}$.
[4] The terms, resistor performance mode and R-Perf mode, are used interchangeably. See the Resistor Performance Mode section.
[5] Guaranteed by design and not subject to production test.
[6] See Figure 24 for more details.
[7] Resistor Terminal A and Resistor Terminal W have no limitations on polarity with respect to each other. Dual-supply operation enables ground referenced bipolar signal adjustment.
[8] Different from operating current, the supply current for the fuse program lasts approximately 55 ms.
[9] Different from operating current, the supply current for the fuse read lasts approximately 500 ns.
[10] P_{DISS} is calculated from $(I_{DD} \times V_{DD}) + (I_{SS} \times V_{SS})$.
[11] All dynamic characteristics use V_{DD} = +2.5 V, V_{SS} = −2.5 V.

Table 2. AD5272 Resistor Performance Mode Code Range

Resistor Tolerance Per Code	$\lvert V_{DD} - V_{SS} \rvert$ = 4.5 V to 5.5 V	$\lvert V_{DD} - V_{SS} \rvert$ = 2.7 V to 4.5 V
R-TOLERANCE		
1% R-Tolerance	From 0x078 to 0x3FF	From 0x0BE to 0x3FF
2% R-Tolerance	From 0x037 to 0x3FF	From 0x055 to 0x3FF
3% R-Tolerance	From 0x028 to 0x3FF	From 0x037 to 0x3FF

Table 3. AD5272 50 kΩ and 100 kΩ Resistor Performance Mode Code Range

Resistor Tolerance Per Code	R_{AW} = 50 kΩ	R_{AW} = 100 kΩ
R-TOLERANCE		
1% R-Tolerance	From 0x078 to 0x3FF	From 0x04B to 0x3FF
2% R-Tolerance	From 0x055 to 0x3FF	From 0x032 to 0x3FF
3% R-Tolerance	From 0x032 to 0x3FF	From 0x019 to 0x3FF

ELECTRICAL CHARACTERISTICS—AD5274

V_{DD} = 2.7 V to 5.5 V, V_{SS} = 0 V; V_{DD} = 2.5 V to 2.75 V, V_{SS} = −2.5 V to −2.75 V; −40°C < T_A < +125°C, unless otherwise noted.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS— RHEOSTAT MODE						
Resolution			8			Bits
Resistor Integral Nonlinearity[2, 3]	R-INL		−1		+1	LSB
Resistor Differential Nonlinearity[2]	R-DNL		−1		+1	LSB
Nominal Resistor Tolerance						
R-Perf Mode[4]		See Table 5 and Table 6	−1	±0.5	+1	%
Normal Mode				±15		%
Resistance Temperature Coefficient[5, 6]		Code = full scale		5		ppm/°C
Wiper Resistance		Code = zero scale		35	70	Ω
RESISTOR TERMINALS						
Terminal Voltage Range[5, 7]			V_{SS}		V_{DD}	V
Capacitance[5] A		f = 1 MHz, measured to GND, code = half scale		90		pF
Capacitance[5] W		f = 1 MHz, measured to GND, code = half scale		40		pF
Common-Mode Leakage Current[5]		$V_A = V_W$			50	nA
DIGITAL INPUTS						
Input Logic[5]						
High	V_{INH}		2.0			V
Low	V_{INL}				0.8	V
Input Current	I_{IN}			±1		µA
Input Capacitance[5]	C_{IN}			5		pF
DIGITAL OUTPUT						
Output Voltage[5]						
High	V_{OH}	R_{PULL_UP} = 2.2 kΩ to V_{DD}	V_{DD} − 0.1			V
Low	V_{OL}	R_{PULL_UP} = 2.2 kΩ to V_{DD}				
		V_{DD} = 2.7 V to 5.5 V, V_{SS} = 0 V			0.4	V
		V_{DD} = 2.5 V to 2.75 V, V_{SS} = −2.5 V to −2.75 V			0.6	V
Tristate Leakage Current			−1		+1	µA
Output Capacitance[5]				5		pF
POWER SUPPLIES						
Single-Supply Power Range		V_{SS} = 0 V	2.7		5.5	V
Dual-Supply Power Range			±2.5		±2.75	V
Supply Current						
Positive	I_{DD}				1	µA
Negative	I_{SS}		−1			µA
OTP Store Current[5, 8]						
Positive	$I_{DD\_OTP\_STORE}$			4		mA
Negative	$I_{SS\_OTP\_STORE}$			−4		mA
OTP Read Current[5, 9]						
Positive	$I_{DD\_OTP\_READ}$				500	µA
Negative	$I_{SS\_OTP\_READ}$		−500			µA
Power Dissipation[10]		$V_{IH} = V_{DD}$ or V_{IL} = GND			5.5	µW
Power Supply Rejection Ratio[5]	PSRR	$\Delta V_{DD}/\Delta V_{SS}$ = ±5 V ± 10%				dB
		R_{AW} = 20 kΩ		−66	−55	
		R_{AW} = 50 kΩ		−75	−67	
		R_{AW} = 100 kΩ		−78	−70	

Parameter	Symbol	Test Conditions/Comments	Min	Typ[1]	Max	Unit
DYNAMIC CHARACTERISTICS[5, 11]						
Bandwidth		−3 dB, R_{AW} = 10 kΩ, Terminal W, see Figure 41				kHz
		R_{AW} = 20 kΩ		300		
		R_{AW} = 50 kΩ		120		
		R_{AW} = 100 kΩ		60		
Total Harmonic Distortion		V_A = 1 V rms, f = 1 kHz, code = half scale				dB
		R_{AW} = 20 kΩ		−90		
		R_{AW} = 50 kΩ		−88		
		R_{AW} = 100 kΩ		−85		
Resistor Noise Density		Code = half scale, T_A = 25°C, f = 10 kHz				nV/√Hz
		R_{AW} = 20 kΩ		13		
		R_{AW} = 50 kΩ		25		
		R_{AW} = 100 kΩ		32		

[1] Typical specifications represent average readings at 25°C, V_{DD} = 5 V, and V_{SS} = 0 V.
[2] Resistor position nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions.
[3] The maximum current in each code is defined by IAW = (V_{DD} − 1)/R_{AW}.
[4] The terms, resistor performance mode and R-Perf mode, are used interchangeably. See the Resistor Performance Mode section.
[5] Guaranteed by design and not subject to production test.
[6] See Figure 24 for more details.
[7] Resistor Terminal A and Resistor Terminal W have no limitations on polarity with respect to each other. Dual-supply operation enables ground referenced bipolar signal adjustment.
[8] Different from operating current, the supply current for the fuse program lasts approximately 55 ms.
[9] Different from operating current, the supply current for the fuse read lasts approximately 500 ns.
[10] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$) + ($I_{SS} \times V_{SS}$).
[11] All dynamic characteristics use V_{DD} = +2.5 V, V_{SS} = −2.5 V.

Table 5. AD5274 Resistor Performance Mode Code Range

Resistor Tolerance per Code	$\lvert V_{DD} - V_{SS} \rvert$ = 4.5 V to 5.5 V	$\lvert V_{DD} - V_{SS} \rvert$ = 2.7 V to 4.5 V
R-TOLERANCE		
1% R-Tolerance	From 0x1E to 0xFF	From 0x32 to 0xFF
2% R-Tolerance	From 0x0F to 0xFF	From 0x19 to 0xFF
3% R-Tolerance	From 0x06 to 0xFF	From 0x0E to 0xFF

Table 6. AD5274 50 kΩ and 100 kΩ Resistor Performance Mode Code Range

Resistor Tolerance per Code	R_{AW} = 50 kΩ	R_{AW} = 100 kΩ
R-TOLERANCE		
1% R-Tolerance	From 0x1E to 0xFF	From 0x14 to 0xFF
2% R-Tolerance	From 0x14 to 0xFF	From 0x0F to 0xFF
3% R-Tolerance	From 0x0A to 0xFF	From 0x0A to 0xFF

INTERFACE TIMING SPECIFICATIONS

V_{DD} = 2.5 V to 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 7.

Parameter	Conditions[1]	Limit at T_{MIN}, T_{MAX} Min	Max	Unit	Description
f_{SCL}[2]	Standard mode		100	kHz	Serial clock frequency
	Fast mode		400	kHz	Serial clock frequency
t_1	Standard mode	4		µs	t_{HIGH}, SCL high time
	Fast mode	0.6		µs	t_{HIGH}, SCL high time
t_2	Standard mode	4.7		µs	t_{LOW}, SCL low time
	Fast mode	1.3		µs	t_{LOW}, SCL low time
t_3	Standard mode	250		ns	$t_{SU;DAT}$, data setup time
	Fast mode	100		ns	$t_{SU;DAT}$, data setup time
t_4	Standard mode	0	3.45	µs	$t_{HD;DAT}$, data hold time
	Fast mode	0	0.9	µs	$t_{HD;DAT}$, data hold time
t_5	Standard mode	4.7		µs	$t_{SU;STA}$, set-up time for a repeated start condition
	Fast mode	0.6		µs	$t_{SU;STA}$, set-up time for a repeated start condition
t_6	Standard mode	4		µs	$t_{HD;STA}$, hold time (repeated) start condition
	Fast mode	0.6		µs	$t_{HD;STA}$, hold time (repeated) start condition
	High speed mode	160		ns	$t_{HD;STA}$, hold time (repeated) start condition
t_7	Standard mode	4.7		µs	t_{BUF}, bus free time between a stop and a start condition
	Fast mode	1.3		µs	t_{BUF}, bus free time between a stop and a start condition
t_8	Standard mode	4		µs	$t_{SU;STO}$, setup time for a stop condition
	Fast mode	0.6		µs	$t_{SU;STO}$, setup time for a stop condition
t_9	Standard mode		1000	ns	t_{RDA}, rise time of SDA signal
	Fast mode		300	ns	t_{RDA}, rise time of SDA signal
t_{10}	Standard mode		300	ns	t_{FDA}, fall time of SDA signal
	Fast mode		300	ns	t_{FDA}, fall time of SDA signal
t_{11}	Standard mode		1000	ns	t_{RCL}, rise time of SCL signal
	Fast mode		300	ns	t_{RCL}, rise time of SCL signal
t_{11A}	Standard mode		1000	ns	t_{RCL1}, rise time of SCL signal after a repeated start condition and after an acknowledge bit
	Fast mode		300	ns	t_{RCL1}, rise time of SCL signal after a repeated start condition and after an acknowledge bit
t_{12}	Standard mode		300	ns	t_{FCL}, fall time of SCL signal
	Fast mode		300	ns	t_{FCL}, fall time of SCL signal
t_{13}	$\overline{\text{RESET}}$ pulse time	20		ns	Minimum $\overline{\text{RESET}}$ low time
t_{SP}[3]	Fast mode	0	50	ns	Pulse width of spike suppressed
t_{EXEC}[4, 5]		500		ns	Command execute time
$t_{RDAC\_R\text{-}PERF}$			2	µs	RDAC register write command execute time (R-Perf mode)
t_{RDAC_NORMAL}			600	ns	RDAC register write command execute time (normal mode)
t_{MEMORY_READ}			6	µs	Memory readback execute time
$t_{MEMORY\_PROGRAM}$			350	ms	Memory program time
t_{RESET}			600	µs	Reset 50-TP restore time
$t_{POWER\text{-}UP}$[6]			2	ms	Power-on 50-TP restore time

[1] Maximum bus capacitance is limited to 400 pF.
[2] The SDA and SCL timing is measured with the input filters enabled. Switching off the input filters improves the transfer rate but has a negative effect on EMC behavior of the part.
[3] Input filtering on the SCL and SDA inputs suppress noise spikes that are less than 50 ns for fast mode.
[4] Refer to $t_{RDAC\_R\text{-}PERF}$ and t_{RDAC_NORMAL} for RDAC register write operations.
[5] Refer to t_{MEMORY_READ} and $t_{MEMORY\_PROGRAM}$ for memory commands operations.
[6] Maximum time after $V_{DD} - V_{SS}$ is equal to 2.5 V.

Shift Register and Timing Diagrams

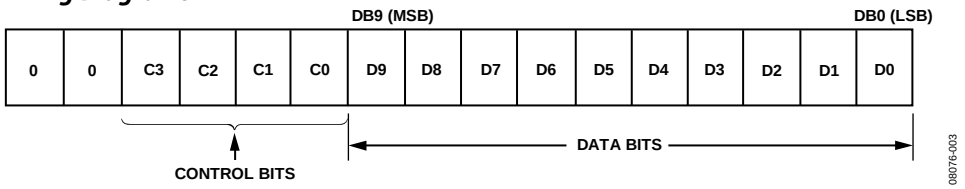

Figure 2. Shift Register Content

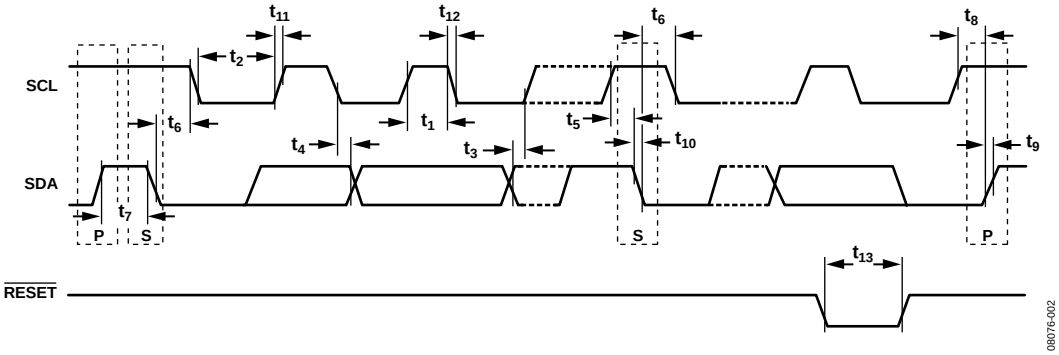

Figure 3. 2-Wire Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 8.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7.0 V
V_{SS} to GND	+0.3 V to −7.0 V
V_{DD} to V_{SS}	7 V
V_A, V_W to GND	V_{SS} − 0.3 V, V_{DD} + 0.3 V
Digital Input and Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
EXT_CAP to V_{SS}	7 V
I_A, I_W	
Continuous	
R_{AW} = 20 kΩ	±3 mA
R_{AW} = 50 kΩ, 100 kΩ	±2 mA
Pulsed[1]	
Frequency > 10 kHz	$\pm MCC^2/d^3$
Frequency ≤ 10 kHz	$\pm MCC^2/\sqrt{d^3}$
Operating Temperature Range[4]	−40°C to +125°C
Maximum Junction Temperature (T_J Maximum)	150°C
Storage Temperature Range	−65°C to +150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	20 sec to 40 sec
Package Power Dissipation	$(T_J \text{ max} - T_A)/\theta_{JA}$

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A and W terminals at a given resistance.
[2] Maximum continuous current
[3] Pulse duty factor.
[4] Includes programming of 50-TP memory.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is defined by JEDEC specification JESD-51 and the value is dependent on the test board and test environment.

Table 9. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}	Unit
10-Lead LFCSP	50	3	°C/W
10-Lead MSOP	135	N/A	°C/W

[1] JEDEC 2S2P test board, still air (0 m/s air flow).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

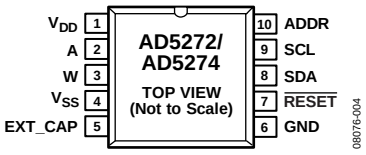

Figure 4. MSOP Pin Configuration

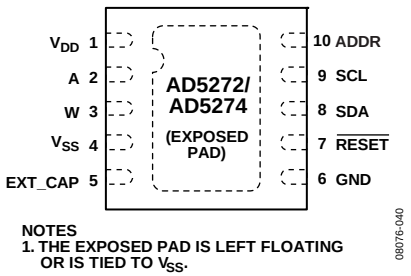

Figure 5. LFCSP Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Positive Power Supply. Decouple this pin with 0.1 µF ceramic capacitors and 10 µF capacitors.
2	A	Terminal A of RDAC. $V_{SS} \le V_A \le V_{DD}$.
3	W	Wiper terminal of RDAC. $V_{SS} \le V_W \le V_{DD}$.
4	V_{SS}	Negative Supply. Connect to 0 V for single-supply applications. Decouple this pin with 0.1 µF ceramic capacitors and 10 µF capacitors.
5	EXT_CAP	External Capacitor. Connect a 1 µF capacitor between EXT_CAP and V_{SS}. This capacitor must have a voltage rating of ≥7 V.
6	GND	Ground Pin, Logic Ground Reference.
7	$\overline{\text{RESET}}$	Hardware Reset Pin. Refreshes the RDAC register with the contents of the 50-TP memory register. Factory default loads midscale until the first 50-TP wiper memory location is programmed. $\overline{\text{RESET}}$ is active low. Tie $\overline{\text{RESET}}$ to V_{DD} if not used.
8	SDA	Serial Data Line. This is used in conjunction with the SCL line to clock data into or out of the 16-bit input registers. It is a bidirectional, open-drain data line that should be pulled to the supply with an external pull-up resistor.
9	SCL	Serial Clock Line. This is used in conjunction with the SDA line to clock data into or out of the 16-bit input registers.
10	ADDR	Tristate Address Input. Sets the two least significant bits (Bit A1, Bit A0) of the 7-bit slave address (see Table 11).
EPAD	Exposed Pad (LFCSP Only)	Leave floating or tie to V_{SS}.

TYPICAL PERFORMANCE CHARACTERISTICS

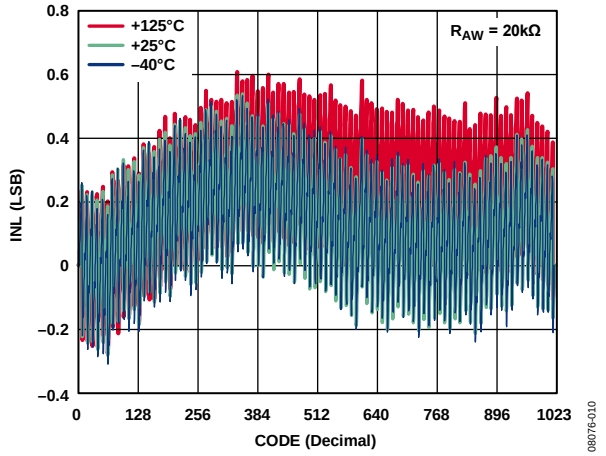

Figure 6. R-INL in R-Perf Mode vs. Code vs. Temperature (AD5272)

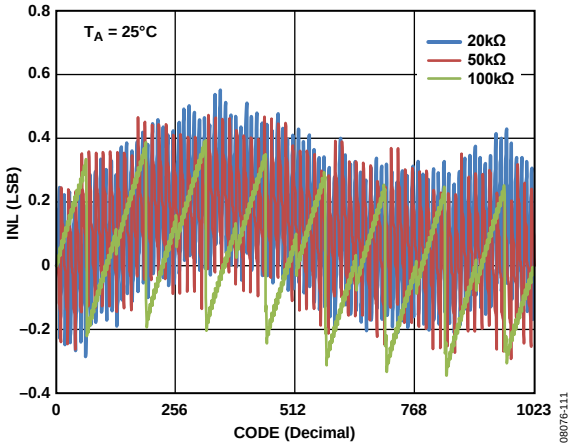

Figure 9. R-INL in R-Perf Mode vs. Code vs. Nominal Resistance (AD5272)

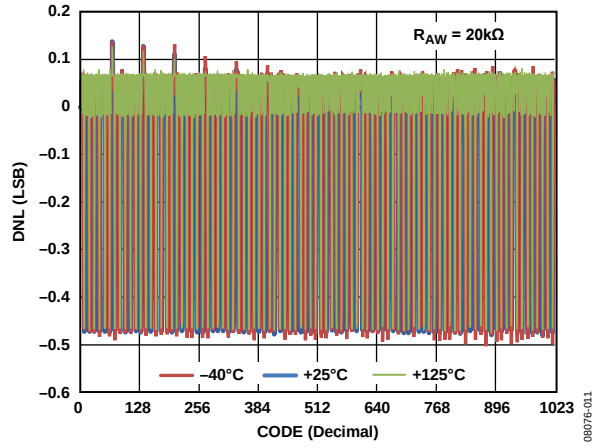

Figure 7. R-DNL in R-Perf Mode vs. Code vs. Temperature (AD5272)

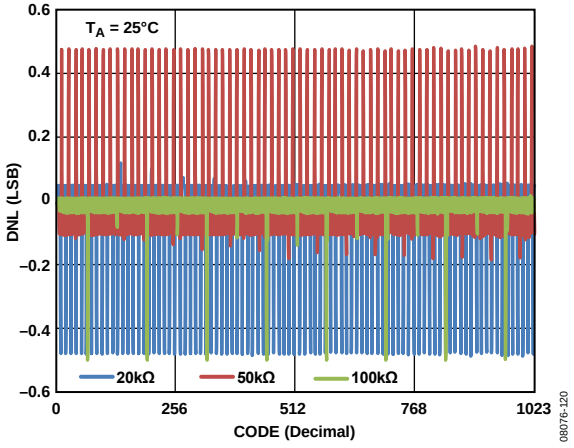

Figure 10. R-DNL in R-Perf Mode vs. Code vs. Nominal Resistance (AD5272)

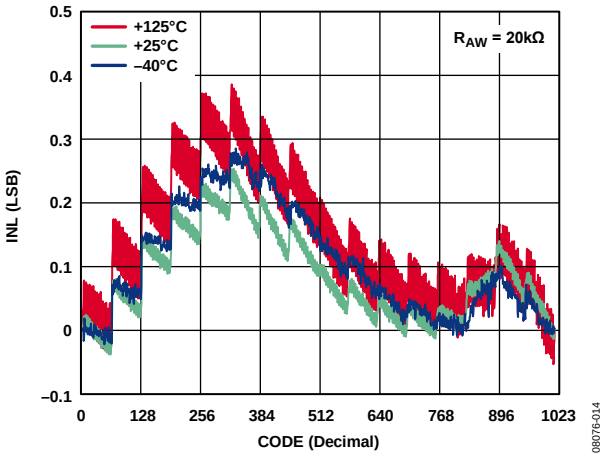

Figure 8. R-INL in Normal Mode vs. Code vs. Temperature (AD5272)

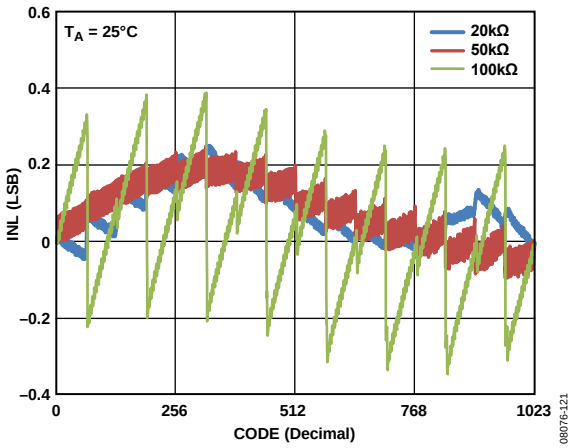

Figure 11. R-INL in Normal Mode vs. Code vs. Nominal Resistance (AD5272)

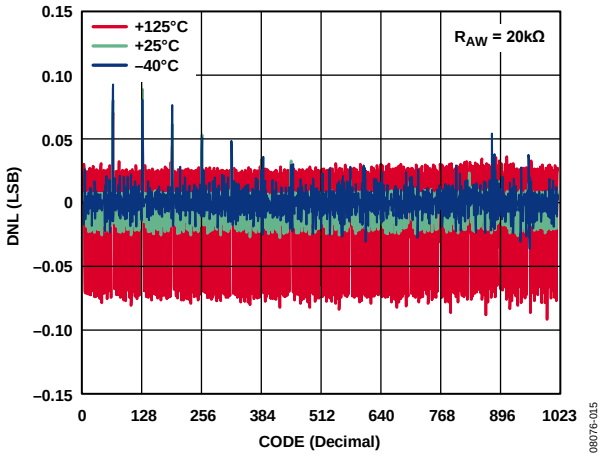

Figure 12. R-DNL in Normal Mode vs. Code vs. Temperature (AD5272)

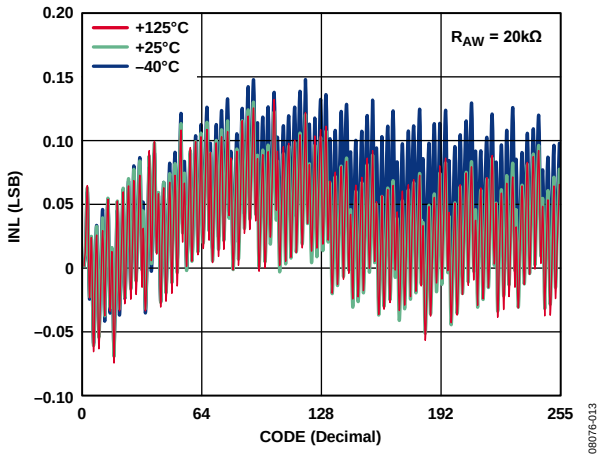

Figure 13. R-INL in R-Perf Mode vs. Code vs. Temperature (AD5274)

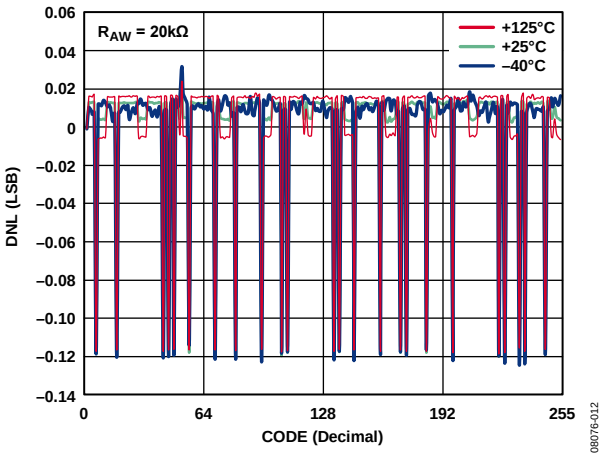

Figure 14. R-DNL in R-Perf Mode vs. Code vs. Temperature (AD5274)

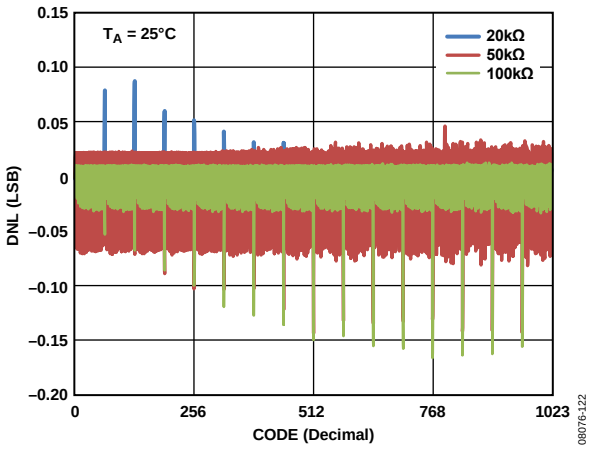

Figure 15. R-DNL in Normal Mode vs. Code vs. Nominal Resistance (AD5272)

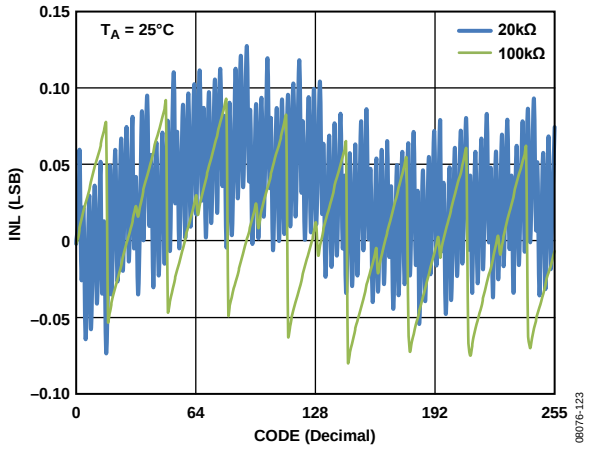

Figure 16. R-INL in R-Perf Mode vs. Code vs. Nominal Resistance (AD5274)

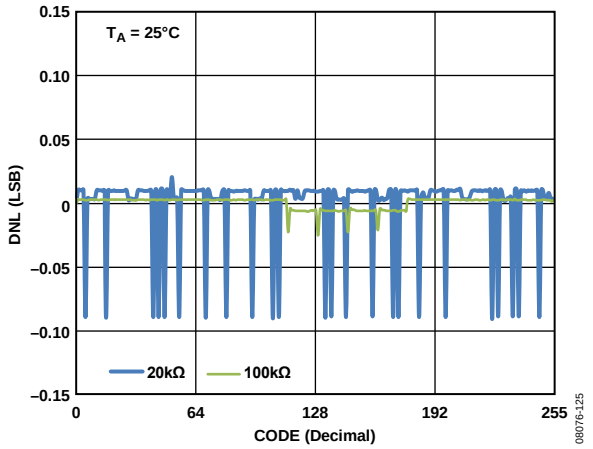

Figure 17. R-DNL in R-Perf Mode vs. Code vs. Nominal Resistance (AD5274)

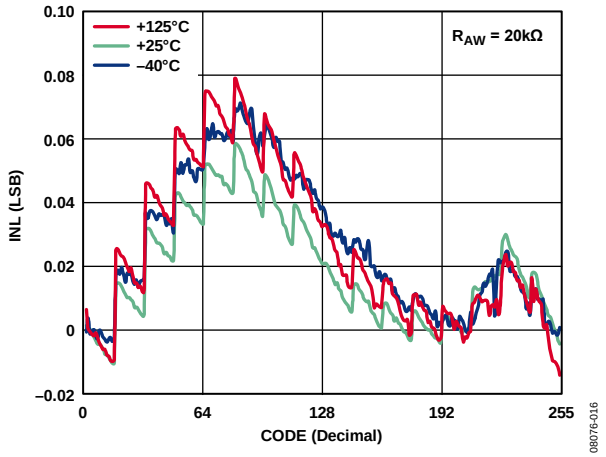

Figure 18. R-INL in Normal Mode vs. Code vs. Temperature (AD5274)

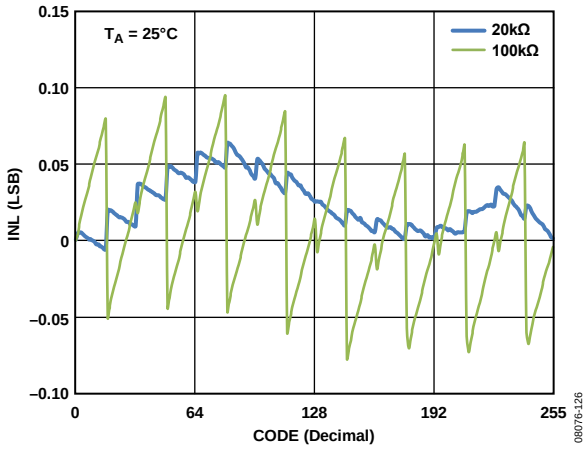

Figure 21. R-INL in Normal Mode vs. Code vs. Nominal Resistance (AD5274)

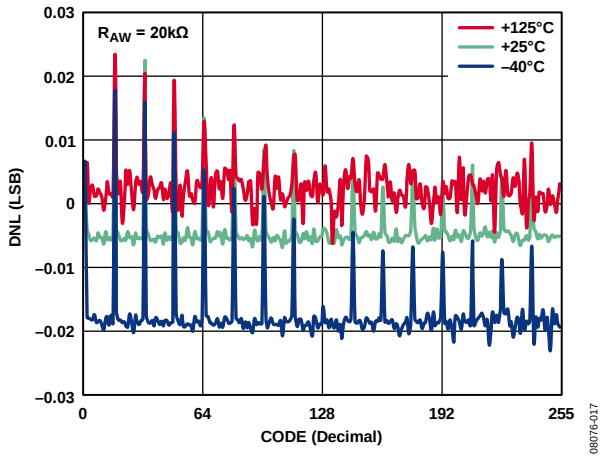

Figure 19. R-DNL in Normal Mode vs. Code vs. Temperature (AD5274)

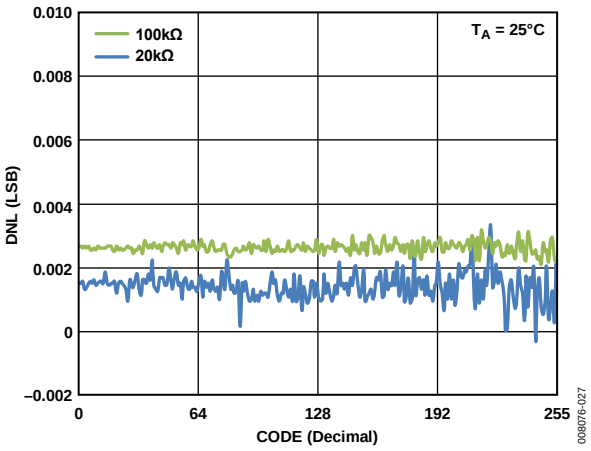

Figure 22. R-DNL in Normal Mode vs. Code vs. Nominal Resistance (AD5274)

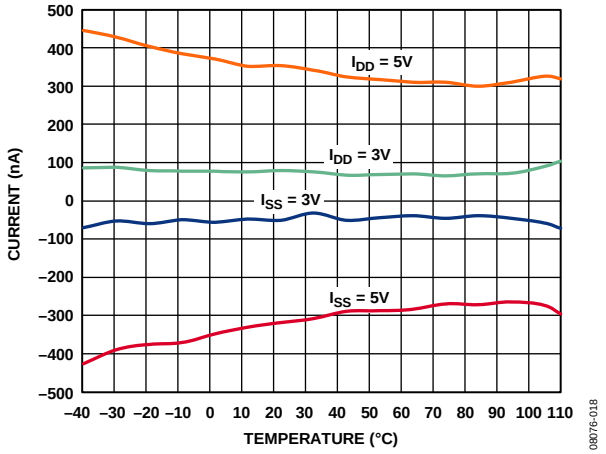

Figure 20. Supply Current (I_{DD}, I_{SS}) vs. Temperature

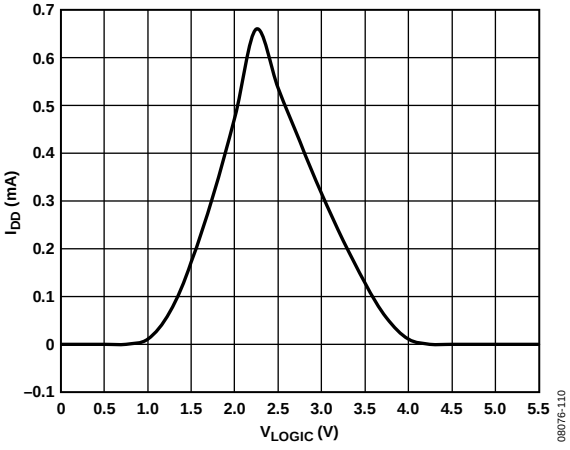

Figure 23. Supply Current (I_{DD}) vs. Digital Input Voltage

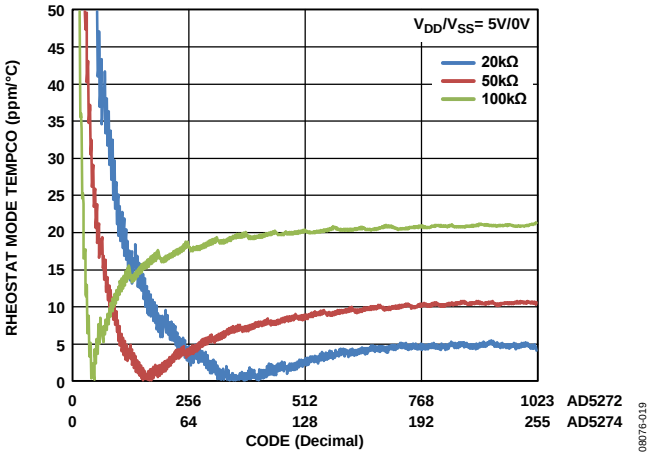

Figure 24. Tempco $\Delta R_{WA}/\Delta T$ vs. Code

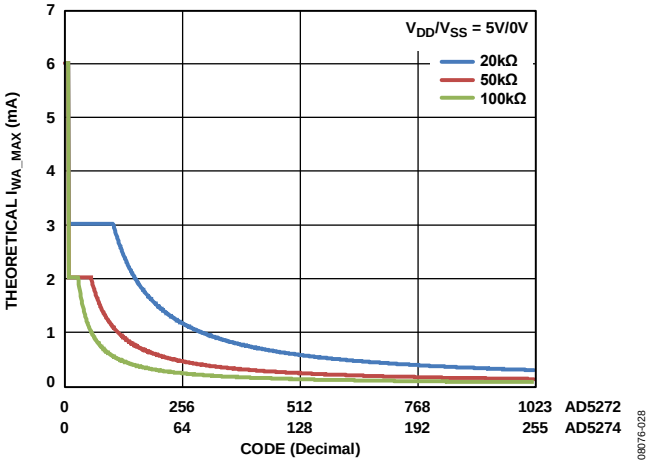

Figure 27. Theoretical Maximum Current vs. Code

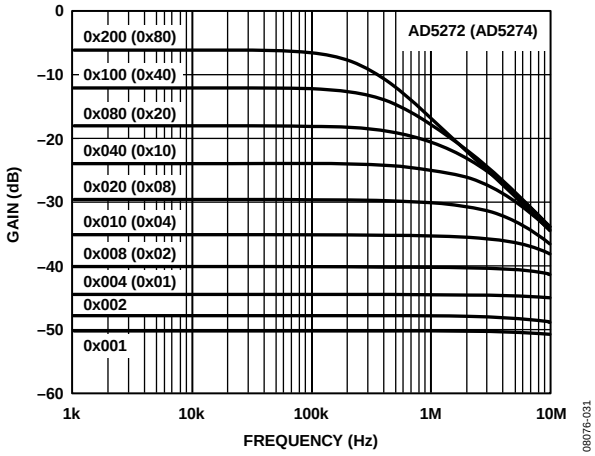

Figure 25. 20 kΩ Gain vs. Code vs. Frequency

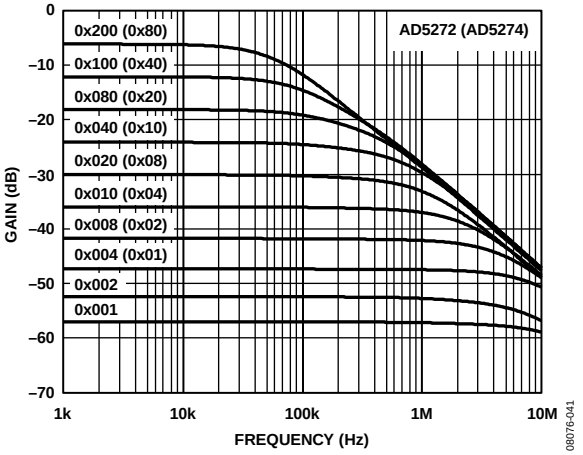

Figure 28. 100 kΩ Gain vs. Code vs. Frequency

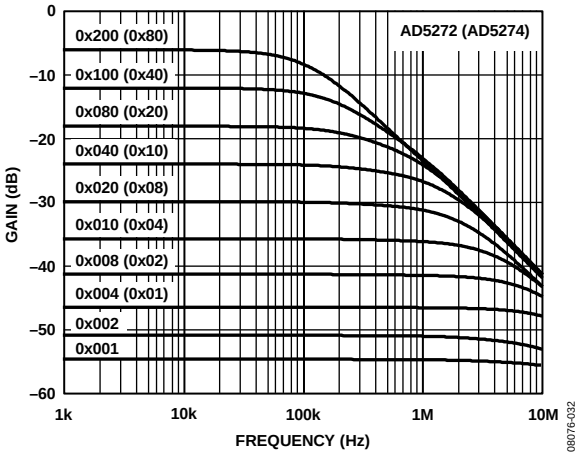

Figure 26. 50 kΩ Gain vs. Code vs. Frequency

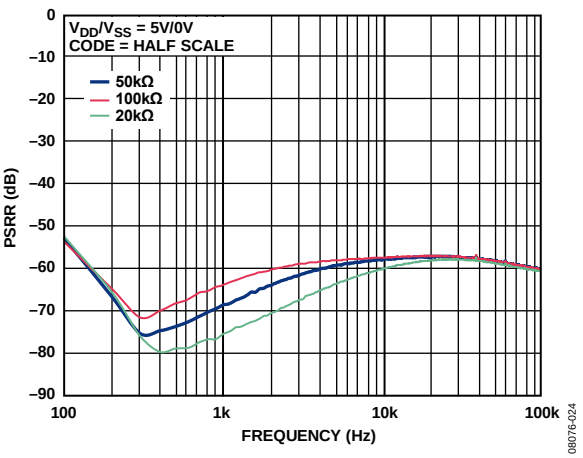

Figure 29. PSRR vs. Frequency

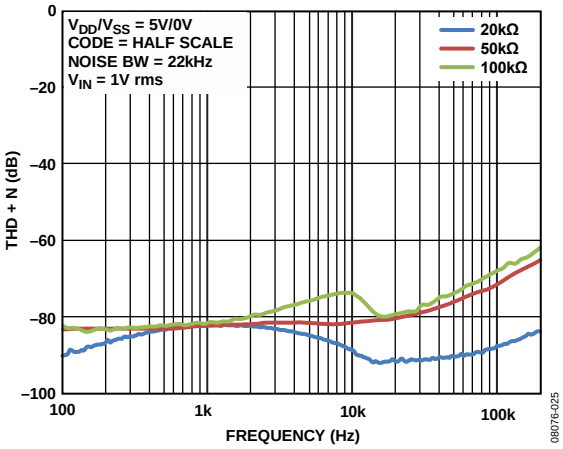

Figure 30. THD + N vs. Frequency

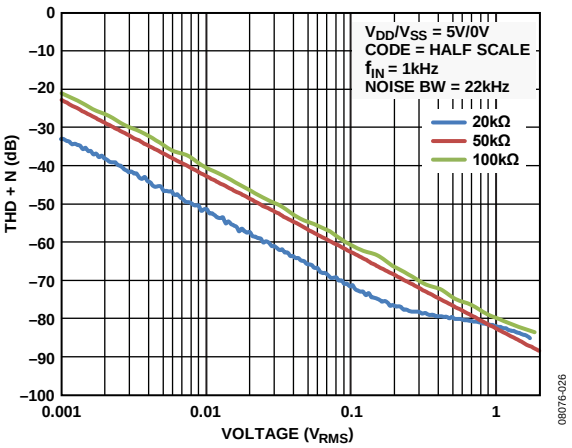

Figure 33. THD + N vs. Amplitude

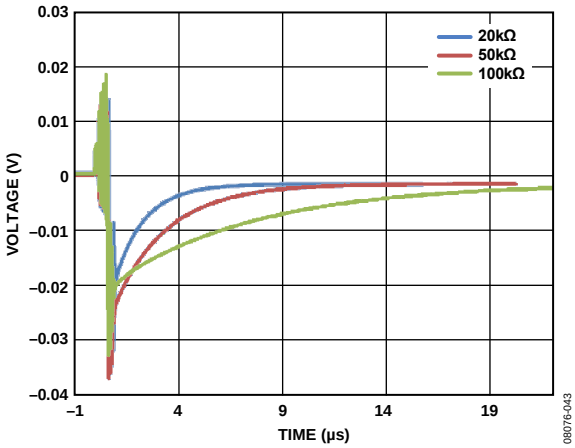

Figure 31. Maximum Glitch Energy

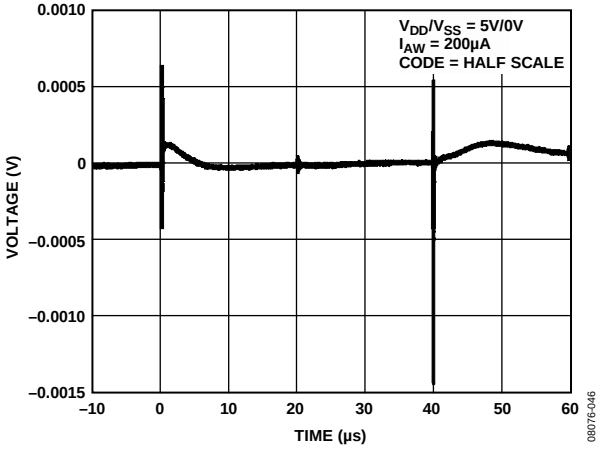

Figure 34. Digital Feedthrough

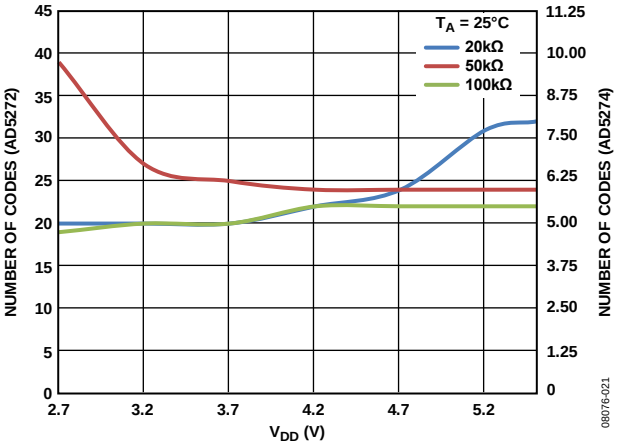

Figure 32. Maximum Code Loss vs. Temperature

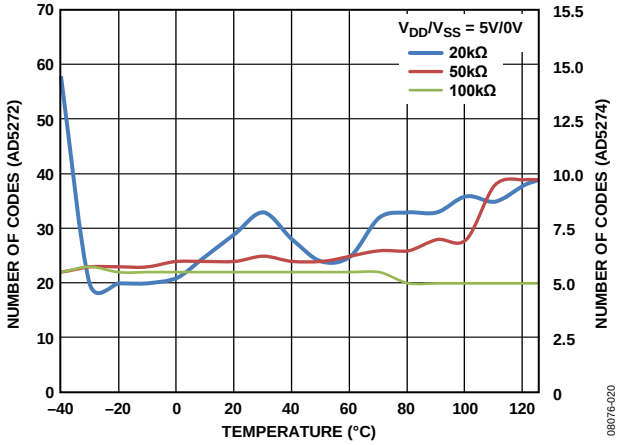

Figure 35. Maximum Code Loss vs. Power Supply Range

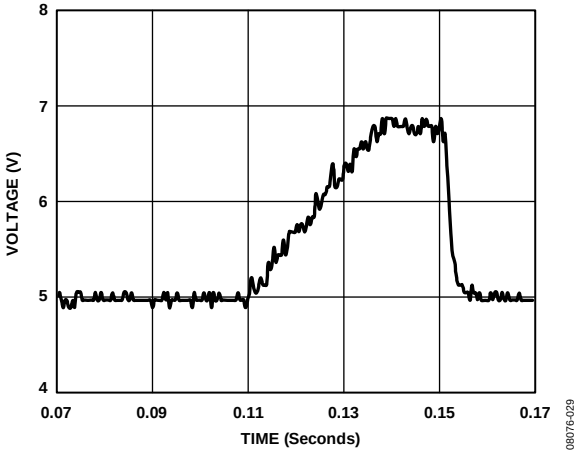

Figure 36. V_{EXT_CAP} Waveform While Writing Fuse

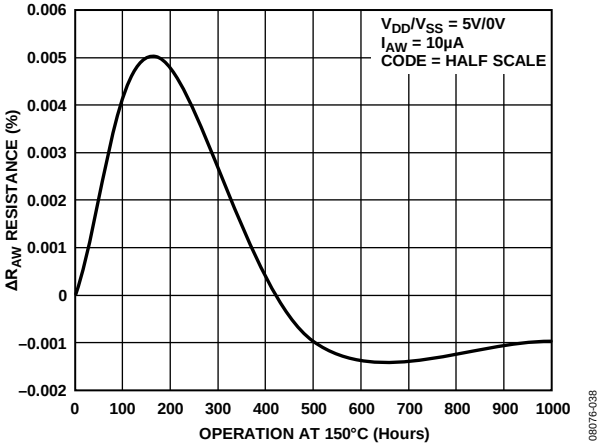

Figure 37. Long-Term Drift Accelerated Average by Burn-In

TEST CIRCUITS

Figure 38 to Figure 42 define the test conditions used in the Specifications section.

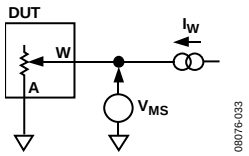

Figure 38. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

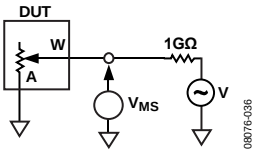

Figure 41. Gain vs. Frequency

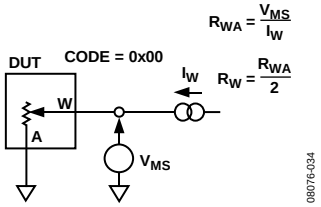

Figure 39. Wiper Resistance

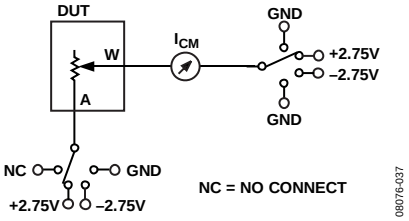

Figure 42. Common Leakage Current

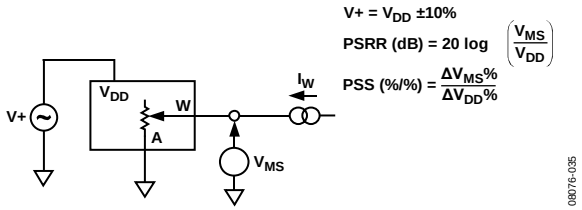

Figure 40. Power Supply Sensitivity (PSS, PSRR)

THEORY OF OPERATION

The AD5272 and AD5274 digital rheostats are designed to operate as true variable resistors for analog signals within the terminal voltage range of $V_{SS} < V_{TERM} < V_{DD}$. The RDAC register contents determine the resistor wiper position. The RDAC register acts as a scratchpad register, which allows unlimited changes of resistance settings. The RDAC register can be programmed with any position setting using the I²C interface. When a desirable wiper position is found, this value can be stored in a 50-TP memory register. Thereafter, the wiper position is always restored to that position for subsequent power-up. The storing of 50-TP data takes approximately 350 ms; during this time, the AD5272/AD5274 is locked and does not acknowledge any new command thereby preventing any changes from taking place. The acknowledge bit can be polled to verify that the fuse program command is complete.

The AD5272/AD5274 also feature a patented 1% end-to-end resistor tolerance. This simplifies precision, rheostat mode, and open-loop applications where knowledge of absolute resistance is critical.

SERIAL DATA INTERFACE

The AD5272/AD5274 have 2-wire I²C-compatible serial interfaces. Each of these devices can be connected to an I²C bus as a slave device under the control of a master device; see Figure 3 for a timing diagram of a typical write sequence.

The AD5272/AD5274 support standard (100 kHz) and fast (400 kHz) data transfer modes. Support is not provided for 10-bit addressing and general call addressing.

The AD5272/AD5274 each has a 7-bit slave address. The five MSBs are 01011 and the two LSBs are determined by the state of the ADDR pin. The facility to make hardwired changes to ADDR allows the user to incorporate up to three of these devices on one bus as outlined in Table 11.

The 2-wire serial bus protocol operates as follows: The master initiates a data transfer by establishing a start condition, which is when a high-to-low transition on the SDA line occurs while SCL is high. The next byte is the address byte, which consists of the 7-bit slave address and a R/$\overline{W}$ bit. The slave device corresponding to the transmitted address responds by pulling SDA low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to, or read from, its shift register.

Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.

When all data bits have been read or written, a stop condition is established. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition. In read mode, the master issues a no acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the 10th clock pulse, and then high during the 10th clock pulse to establish a stop condition.

SHIFT REGISTER

For the AD5272/AD5274, the shift register is 16 bits wide, as shown in Figure 2. The 16-bit word consists of two unused bits, which should be set to zero, followed by four control bits and 10 RDAC data bits (note that for the AD5274 only, the lower two RDAC data bits are don't care if the RDAC register is read from or written to), and data is loaded MSB first (Bit 15). The four control bits determine the function of the software command (Table 12). Figure 43 shows a timing diagram of a typical AD5272/AD5274 write sequence.

The command bits (Cx) control the operation of the digital potentiometer and the internal 50-TP memory. The data bits (Dx) are the values that are loaded into the decoded register.

Table 11. Device Address Selection

ADDR	A1	A0	7-Bit I²C Device Address
GND	1	1	0101111
V_{DD}	0	0	0101100
NC (No Connection)[1]	1	0	0101110

[1] Not available in bipolar mode. $V_{SS} < 0$ V.

WRITE OPERATION

It is possible to write data for the RDAC register or the control register. When writing to the AD5272/AD5274, the user must begin with a start command followed by an address byte (R/$\overline{W}$ = 0), after which the AD5272/AD5274 acknowledges that it is prepared to receive data by pulling SDA low.

Two bytes of data are then written to the RDAC, the most significant byte followed by the least significant byte; both of these data bytes are acknowledged by the AD5272/AD5274. A stop condition follows. The write operations for the AD5272/AD5274 are shown in Figure 43.

A repeated write function gives the user flexibility to update the device a number of times after addressing the part only once, as shown in Figure 44.

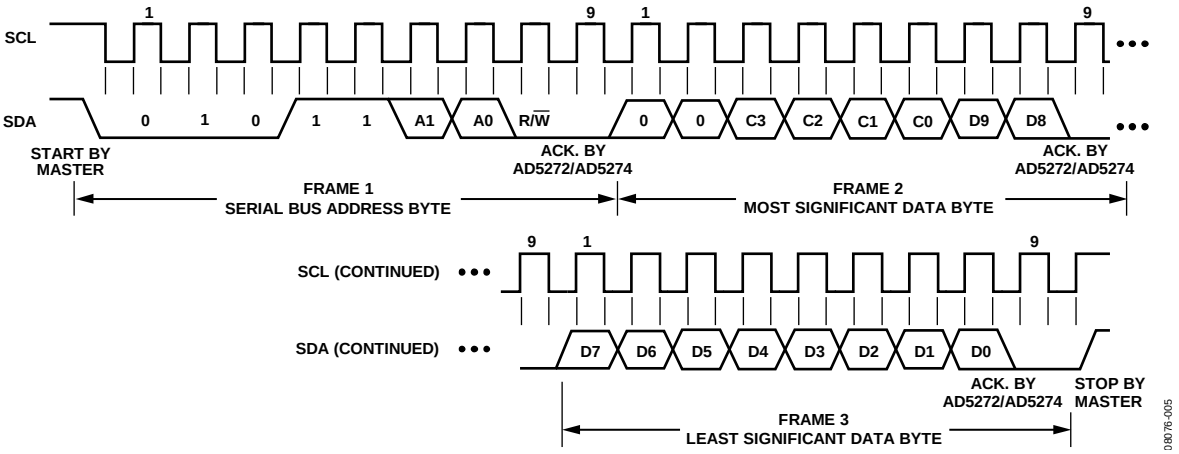

Figure 43. Write Command

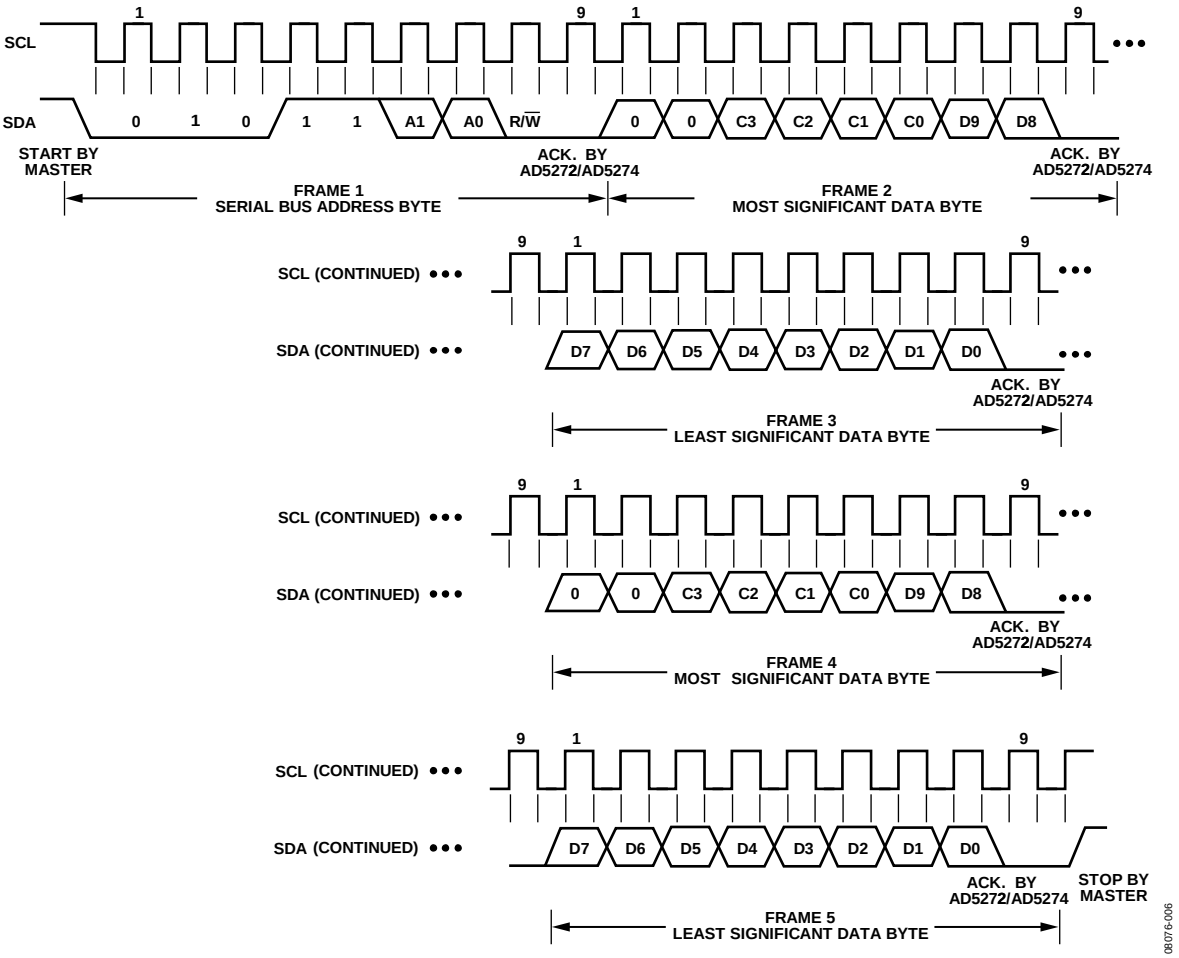

Figure 44. Multiple Write

READ OPERATION

When reading data back from the AD5272/AD5274, the user must first issue a readback command to the device, this begins with a start command followed by an address byte (R/$\overline{W}$ = 0), after which the AD5272/AD5274 acknowledges that it is prepared to receive data by pulling SDA low.

Two bytes of data are then written to the AD5272/AD5274, the most significant byte followed by the least significant byte; both of these data bytes are acknowledged by the AD5272/AD5274.

A stop condition follows. These bytes contain the read instruction, which enables readback of the RDAC register, 50-TP memory, or the control register. The user can then read back the data beginning with a start command followed by an address byte (R/$\overline{W}$ = 1), after which the device acknowledges that it is prepared to transmit data by pulling SDA low. Two bytes of data are then read from the device, as shown in Figure 45. A stop condition follows. If the master does not acknowledge the first byte, the second byte is not transmitted by the AD5272/AD5274.

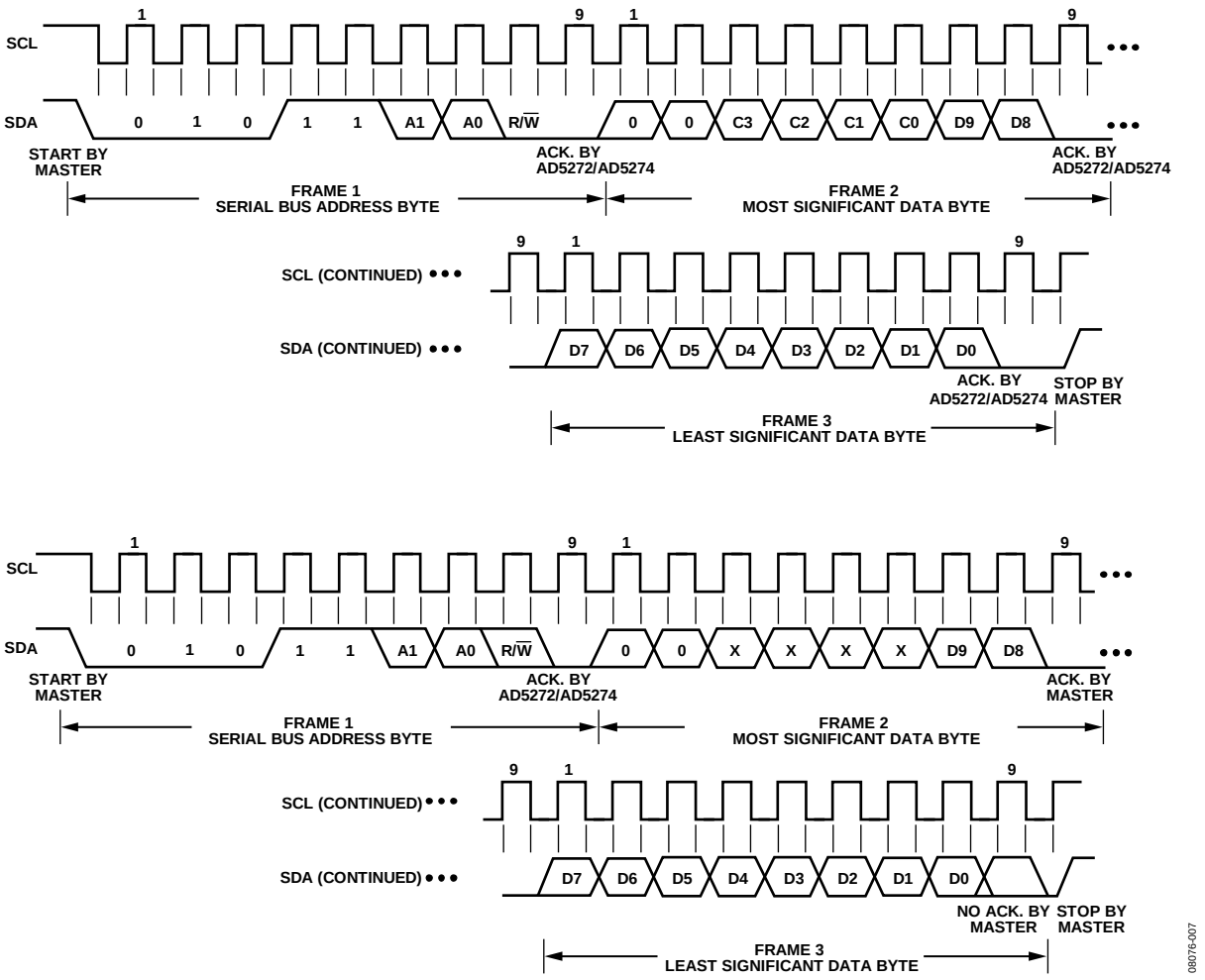

Figure 45. Read Command

RDAC REGISTER

The RDAC register directly controls the position of the digital rheostat wiper. For example, when the RDAC register is loaded with all zeros, the wiper is connected to Terminal A of the variable resistor. It is possible to both write to and read from the RDAC register using the I²C interface. The RDAC register is a standard logic register; there is no restriction on the number of changes allowed.

50-TP MEMORY BLOCK

The AD5272/AD5274 contain an array of 50-TP programmable memory registers, which allow the wiper position to be programmed up to 50 times. Table 16 shows the memory map. Command 3 in Table 12 programs the contents of the RDAC register to memory. The first address to be programmed is Location 0x01, see Table 16, and the AD5272/AD5274 increments the 50-TP memory address for each subsequent program until the memory is full. Programming data to 50-TP consumes approximately 4 mA for 55 ms, and takes approximately 350 ms to complete, during which time the shift register is locked preventing any changes from taking place. Bit C3 of the control register in Table 15 can be polled to verify that the fuse program command was successful. No change in supply voltage is required to program the 50-TP memory; however, a 1 µF capacitor on the EXT_CAP pin is required as shown in Figure 47.

Prior to 50-TP activation, the AD5272/AD5274 is preset to midscale on power-up. It is possible to read back the contents of any of the 50-TP memory registers through the I²C interface by using Command 5 in Table 12. The lower six LSB bits, D0 to D5 of the data byte, select which memory location is to be read back. A binary encoded version address of the most recently programmed wiper memory location can be read back using Command 6 in Table 12. This can be used to monitor the spare memory status of the 50-TP memory block.

WRITE PROTECTION

On power-up, serial data input register write commands for both the RDAC register and the 50-TP memory registers are disabled. The RDAC write protect bit (Bit C1) of the control register (see Table 14 and Table 15) is set to 0 by default. This disables any change of the RDAC register content regardless of the software commands, except that the RDAC register can be refreshed from the 50-TP memory using the software reset, Command 4, or through hardware by the $\overline{\text{RESET}}$ pin. To enable programming of the variable resistor wiper position (programming the RDAC register), the write protect bit (Bit C1) of the control register must first be programmed. This is accomplished by loading the serial data input register with Command 7 (see Table 12). To enable programming of the 50-TP memory block, Bit C0 of the control register, which is set to 0 by default, must first be set to 1.

Table 12. Command Operation Truth Table

Command Number	Command[DB13:DB10]				Data[DB9:B0][1]										
	C3	C2	C1	C0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Operation
0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	NOP: do nothing.
1	0	0	0	1	D9	D8	D7	D6	D5	D4	D3	D2	D1[2]	D0[2]	Write contents of serial register data to RDAC.
2	0	0	1	0	X	X	X	X	X	X	X	X	X	X	Read contents of RDAC wiper register.
3	0	0	1	1	X	X	X	X	X	X	X	X	X	X	Store wiper setting: store RDAC setting to 50-TP.
4	0	1	0	0	X	X	X	X	X	X	X	X	X	X	Software reset: refresh RDAC with the last 50-TP memory stored value.
5[3]	0	1	0	1	X	X	X	X	D5	D4	D3	D2	D1	D0	Read contents of 50-TP from the SDO output in the next frame.
6	0	1	1	0	X	X	X	X	X	X	X	X	X	X	Read address of the last 50-TP programmed memory location.
7[4]	0	1	1	1	X	X	X	X	X	X	X	D2	D1	D0	Write contents of the serial register data to the control register.
8	1	0	0	0	X	X	X	X	X	X	X	X	X	X	Read contents of the control register.
9	1	0	0	1	X	X	X	X	X	X	X	X	X	D0	Software shutdown. D0 = 0; normal mode. D0 = 1; shutdown mode.

[1] X = don't care.
[2] AD5274 = don't care.
[3] See Table 16 for the 50-TP memory map.
[4] See Table 15 for bit details.

Table 13. Write and Read to RDAC and 50-TP memory

DIN	SDO[1]	Action
0x1C03	0xXXXX	Enable update of wiper position and 50-TP memory contents through digital interface.
0x0500	0x1C03	Write 0x100 to the RDAC register, wiper moves to ¼ full-scale position.
0x0800	0x0500	Prepare data read from RDAC register.
0x0C00	0x100	Stores RDAC register content into 50-TP memory. 16-bit word appears out of SDO, where last 10-bits contain the contents of the RDAC Register 0x100.
0x1800	0x0C00	Prepare data read of last programmed 50-TP memory monitor location.
0x0000	0xXX19	NOP Instruction 0 sends a 16-bit word out of SDO, where the six LSBs last 6-bits contain the binary address of the last programmed 50-TP memory location, for example, 0x19 (see Table 16).
0x1419	0x0000	Prepares data read from Memory Location 0x19.
0x2000	0x0100	Prepare data read from the control register. Sends a 16-bit word out of SDO, where the last 10-bits contain the contents of Memory Location 0x19.
0x0000	0xXXXX	NOP Instruction 0 sends a 16-bit word out of SDO, where the last four bits contain the contents of the control register. If Bit C3 = 1, fuse program command successful.

[1] X is don't care.

Table 14. Control Register Bit Map

DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	C3	C2	C1	C0

Table 15. Control Register Description

Bit Name	Description
C0	50-TP program enable 0 = 50-TP program disabled (default) 1 = enable device for 50-TP program
C1	RDAC register write protect 0 = wiper position frozen to value in 50-TP memory (default)[1] 1 = allow update of wiper position through a digital interface
C2	Resistor performance enable 0 = RDAC resistor tolerance calibration enabled (default) 1 = RDAC resistor tolerance calibration disabled
C3	50-TP memory program success bit 0 = fuse program command unsuccessful (default) 1 = fuse program command successful

[1] Wiper position is frozen to the last value programmed in the 50-TP memory. Wiper freezes to midscale if 50-TP memory has not been previously programmed.

Table 16. Memory Map

	Data Byte [DB9:DB8][1]										
Command Number	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Register Contents
5	X	X	X	0	0	0	0	0	0	0	Reserved
	X	X	X	0	0	0	0	0	0	1	1st programmed wiper location (0x01)
	X	X	X	0	0	0	0	0	1	0	2nd programmed wiper location (0x02)
	X	X	X	0	0	0	0	0	1	1	3rd programmed wiper location (0x03)
	X	X	X	0	0	0	0	1	0	0	4th programmed wiper location (0x04)
	…	…	…	…	…	…	…	…	…	…	…
	X	X	X	0	0	0	1	0	1	0	10th programmed wiper location (0xA)
	X	X	X	0	0	1	0	1	0	0	20th programmed wiper location (0x14)
	X	X	X	0	0	1	1	1	1	0	30th programmed wiper location (0x1E)
	X	X	X	0	1	0	1	0	0	0	40th programmed wiper location (0x28)
	X	X	X	0	1	1	0	0	1	0	50th programmed wiper location (0x32)

[1] X is don't care.

50-TP MEMORY WRITE-ACKNOWLEDGE POLLING

After each write operation to the 50-TP registers, an internal write cycle begins. The I²C interface of the device is disabled. To determine if the internal write cycle is complete and the I²C interface is enabled, interface polling can be executed. I²C interface polling can be conducted by sending a start condition, followed by the slave address and the write bit. If the I²C interface responds with an acknowledge (ACK), the write cycle is complete and the interface is ready to proceed with further operations. Otherwise, I²C interface polling can be repeated until it completes.

RESET

The AD5272/AD5274 can be reset through software by executing Command 4 (see Table 12) or through hardware on the low pulse of the $\overline{\text{RESET}}$ pin. The reset command loads the RDAC register with the contents of the most recently programmed 50-TP memory location. The RDAC register loads with midscale if no 50-TP memory location has been previously programmed. Tie $\overline{\text{RESET}}$ to V_{DD} if the $\overline{\text{RESET}}$ pin is not used.

RESISTOR PERFORMANCE MODE

This mode activates a new, patented 1% end-to-end resistor tolerance that ensures a ±1% resistor tolerance on each code, that is, code = half scale and R_{WA} = 10 kΩ ± 100 Ω. See Table 2, Table 3, Table 5, and Table 6 to check which codes achieve ±1% resistor tolerance. The resistor performance mode is activated by programming Bit C2 of the control register (see Table 14 and Table 15).

SHUTDOWN MODE

The AD5272/AD5274 can be shut down by executing the software shutdown command, Command 9 (see Table 12), and setting the LSB to 1. This feature places the RDAC in a zero-power-consumption state where Terminal Ax is disconnected from the wiper terminal. It is possible to execute any command from Table 12 while the AD5272 or AD5274 is in shutdown mode. The part can be taken out of shutdown mode by executing Command 9 and setting the LSB to 0, or by issuing a software or hardware reset.

RDAC ARCHITECTURE

To achieve optimum performance, Analog Devices has patented the RDAC segmentation architecture for all the digital potentiometers. In particular, the AD5272/AD5274 employ a three-stage segmentation approach, as shown in Figure 46. The AD5272/AD5274 wiper switch is designed with the transmission gate CMOS topology.

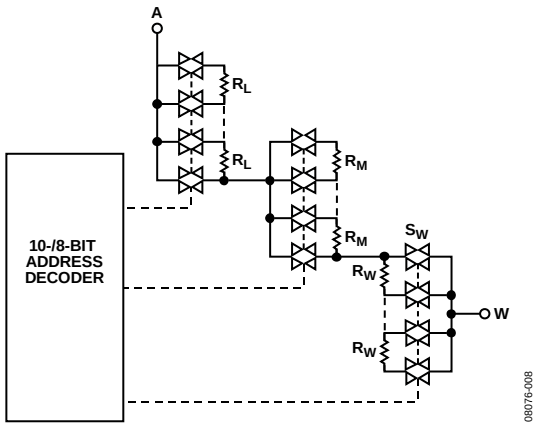

Figure 46. Simplified RDAC Circuit

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation—1% Resistor Tolerance

The nominal resistance between Terminal W and Terminal A, R_{WA}, is available in 20 kΩ, 50 kΩ, and 100 kΩ, and 1024-/256-tap points accessed by the wiper terminal. The 10-/8-bit data in the RDAC latch is decoded to select one of the 1024 or 256 possible wiper settings. The AD5272/ AD5274 contain an internal ±1% resistor tolerance calibration feature which can be disabled or enabled, enabled by default, or by programming Bit C2 of the control register (see Table 15). The digitally programmed output resistance between the W terminal and the A terminal, R_{WA}, is calibrated to give a maximum of ±1% absolute resistance error over both the full supply and temperature ranges. As a result, the general equations for determining the digitally programmed output resistance between the W terminal and A terminal are as follows:

For the AD5272

$$R_{WA}(D) = \frac{D}{1024} \times R_{WA} \quad (1)$$

For the AD5274

$$R_{WA}(D) = \frac{D}{256} \times R_{WA} \quad (2)$$

where:

D is the decimal equivalent of the binary code loaded in the 10-/8-bit RDAC register.

R_{WA} is the end-to-end resistance.

In the zero-scale condition, a finite total wiper resistance of 120 Ω is present. Regardless of which setting the part is operating in, take care to limit the current between the A terminal to B terminal, W terminal to A terminal, and W terminal to B terminal, to the maximum continuous current of ±3 mA, or the pulse current specified in Table 8. Otherwise, degradation or possible destruction of the internal switch contact can occur.

EXT_CAP CAPACITOR

A 1 µF capacitor to V_{SS} must be connected to the EXT_CAP pin (see Figure 47) on power-up and throughout the operation of the AD5272/AD5274.

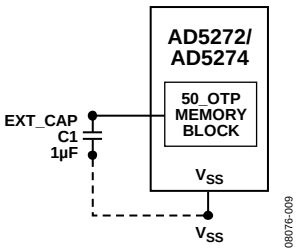

Figure 47. EXT_CAP Hardware Setup

TERMINAL VOLTAGE OPERATING RANGE

The positive V_{DD} and negative V_{SS} power supplies of the AD5272/AD5274 define the boundary conditions for proper 2-terminal digital resistor operation. Supply signals present on Terminal A and Terminal W that exceed V_{DD} or V_{SS} are clamped by the internal forward-biased diodes (see Figure 48).

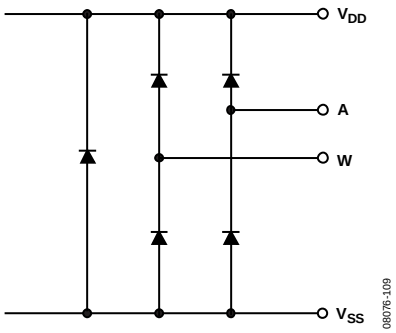

Figure 48. Maximum Terminal Voltages Set by V_{DD} and V_{SS}

The ground pins of the AD5272/AD5274 devices are primarily used as digital ground references. To minimize the digital ground bounce, join the AD5272/AD5274 ground terminal remotely to the common ground. The digital input control signals to the AD5272/AD5274 must be referenced to the device ground pin (GND) and satisfy the logic level defined in the Specifications section. An internal level shift circuit ensures that the common-mode voltage range of the three terminals extends from V_{SS} to V_{DD}, regardless of the digital input level.

POWER-UP SEQUENCE

Because there are diodes to limit the voltage compliance at Terminal A and Terminal W (see Figure 48), it is important to power V_{DD}/V_{SS} first before applying any voltage to Terminal A and Terminal W; otherwise, the diode is forward-biased such that V_{DD}/V_{SS} are powered unintentionally. The ideal power-up sequence is V_{SS}, GND, V_{DD}, digital inputs, V_A, and V_W. The order of powering V_A, V_W, and digital inputs is not important as long as they are powered after V_{DD}/V_{SS}.

As soon as V_{DD} is powered, the power-on preset activates, which first sets the RDAC to midscale and then restores the last programmed 50-TP value to the RDAC register.

OUTLINE DIMENSIONS

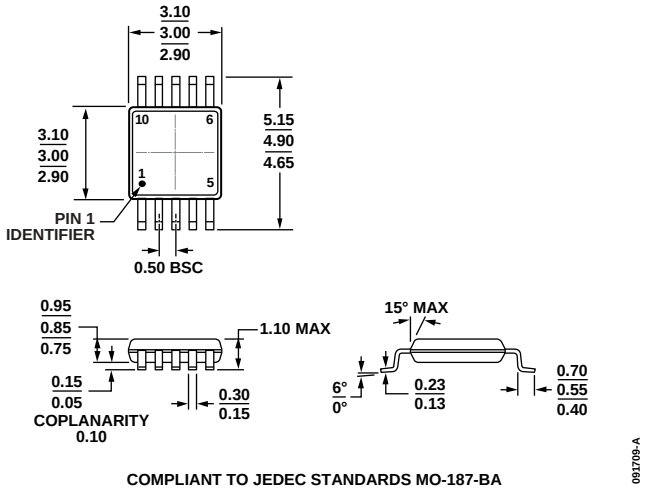

Figure 49. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

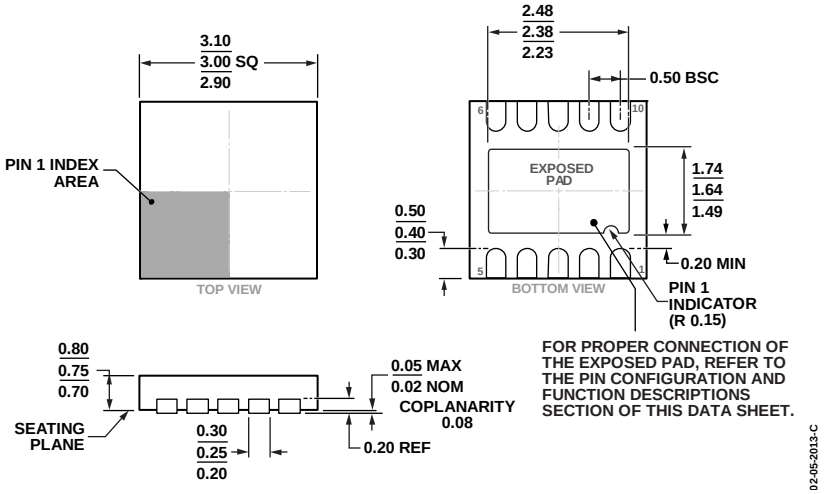

Figure 50. 10-Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3mm Body, Very Thin, Dual Lead
(CP-10-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	R_{AW} (kΩ)	Resolution	Temperature Range	Package Description	Package Option	Branding
AD5272BRMZ-20	20	1,024	−40°C to +125°C	10-Lead MSOP	RM-10	DE6
AD5272BRMZ-20-RL7	20	1,024	−40°C to +125°C	10-Lead MSOP	RM-10	DE6
AD5272BRMZ-50	50	1,024	−40°C to +125°C	10-Lead MSOP	RM-10	DE7
AD5272BRMZ-50-RL7	50	1,024	−40°C to +125°C	10-Lead MSOP	RM-10	DE7
AD5272BRMZ-100	100	1,024	−40°C to +125°C	10-Lead MSOP	RM-10	DE5
AD5272BRMZ-100-RL7	100	1,024	−40°C to +125°C	10-Lead MSOP	RM-10	DE5
AD5272BCPZ-20-RL7	20	1,024	−40°C to +125°C	10-Lead LFCSP_WD	CP-10-9	DE4
AD5272BCPZ-100-RL7	100	1,024	−40°C to +125°C	10-Lead LFCSP_WD	CP-10-9	DE3
AD5274BRMZ-20	20	256	−40°C to +125°C	10-Lead MSOP	RM-10	DEE
AD5274BRMZ-20-RL7	20	256	−40°C to +125°C	10-Lead MSOP	RM-10	DEE
AD5274BRMZ-100	100	256	−40°C to +125°C	10-Lead MSOP	RM-10	DED
AD5274BRMZ-100-RL7	100	256	−40°C to +125°C	10-Lead MSOP	RM-10	DED
AD5274BCPZ-20-RL7	20	256	−40°C to +125°C	10-Lead LFCSP_WD	CP-10-9	DE9
AD5274BCPZ-100-RL7	100	256	−40°C to +125°C	10-Lead LFCSP_WD	CP-10-9	DE8
EVAL-AD5272SDZ			Evaluation Board			

[1] Z = RoHS Compliant Part.

NOTES

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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