DESCRIPTION (continued)

The output is turned on when a south pole of sufficient strength perpendicular to the vertical Hall element is present. A north pole is necessary to turn the output off. Package type LH is a modified SOT23W surface-mount package that switches with magnetic fields oriented perpendicularly to the non-leaded side of the package. The UA package is an ultra-mini SIP, equipped for through-hole mounting and lead forming, that switches when a magnetic field is presented to the top of the package, parallel with the branded face. Both packages are RoHS-compliant and lead (Pb) free (suffix, -T), with 100% matte-tin-plated leadframes.

SPECIFICATIONS

SELECTION GUIDE

Part Number	Packing	Package	Ambient, T_A (°C)
A1260ELHLT-T	7-in. reel, 3000 pieces/reel	3-pin surface mount SOT23W	–40 to 85
A1260ELHLX-T	13-in. reel, 10000 pieces/reel	3-pin surface mount SOT23W	–40 to 85
A1260LLHLT-T	7-in. reel, 3000 pieces/reel	3-pin surface mount SOT23W	–40 to 150
A1260LLHLX-T	13-in. reel, 10000 pieces/reel	3-pin surface mount SOT23W	–40 to 150
A1260EUA-T	500 pieces per bulk bag	SIP-3 through hole	–40 to 85
A1260LUA-T	500 pieces per bulk bag	SIP-3 through hole	–40 to 150

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage [1]	V_{CC}		26.5	V
Reverse Supply Voltage [1]	V_{RCC}		–18	V
Output Off Voltage [1]	V_{OUT}		26	V
Reverse Output Voltage	V_{OUTR}		–0.3	V
Continuous Output Current	I_{OUT}		25	mA
Reverse Output Current	I_{OUTR}		–50	mA
Operating Ambient Temperature	T_A	Range E	–40 to 85	°C
		Range L	–40 to 150	°C
Maximum Junction Temperature	$T_{J(MAX)}$		165	°C
		For 1000 hours	175	°C
Storage Temperature	T_{stg}		–65 to 170	°C

[1] This rating does not apply to extremely short voltage transients such as Load Dump and/or ESD. Those events have individual ratings, specific to the respective transient voltage event.

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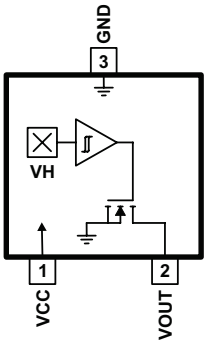
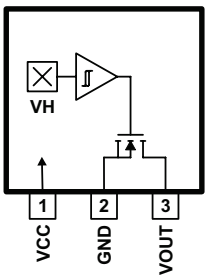
PINOUT DIAGRAMS AND TERMINAL LIST TABLE



Package LH Pinout



Package UA Pinout

Terminal List Table

Symbol	Pin Number		Description
	LH Package	UA Package	
VCC	1	1	Power supply to chip
VOUT	2	3	Output from circuit
GND	3	2	Ground

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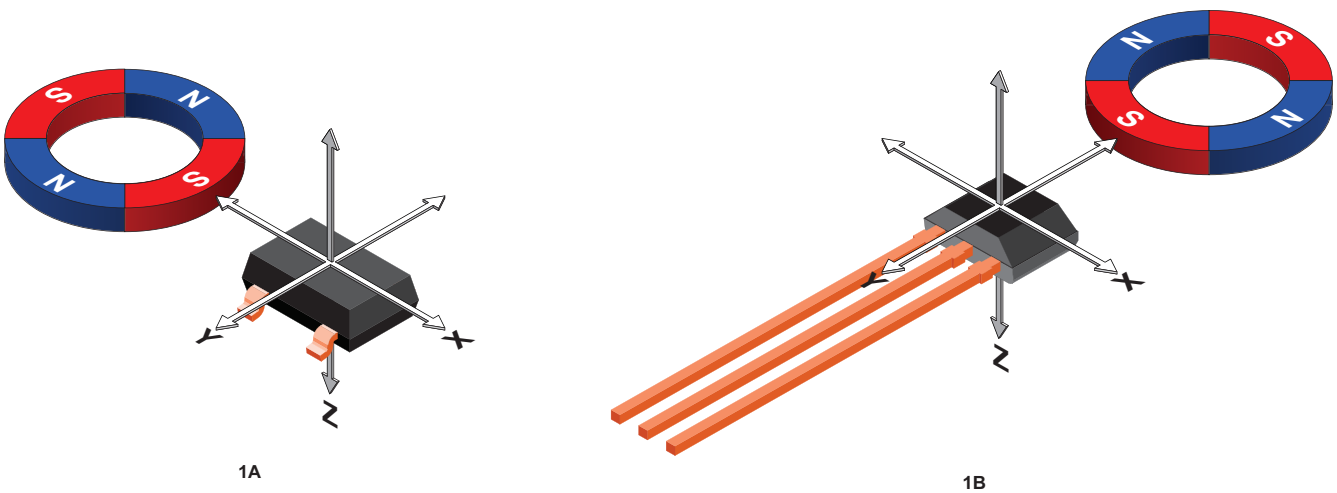
ELECTRICAL CHARACTERISTICS: Valid over full operating voltage and temperature ranges, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit [2]
Supply Voltage	V_{CC}	Operating, T_J < 165°C	3	–	24	V
Output Leakage Current	I_{OUTOFF}	V_{OUT} = 24 V, B < B_{RP}	–	–	10	μA
Output Saturation Voltage	$V_{OUT(SAT)}$	I_{OUT} = 20 mA, B > B_{OP}	–	230	500	mV
Output Current Limit	I_{OM}	B > B_{OP}	30	–	60	mA
Power-On Time [3]	t_{PO}	V_{CC} > 3.0 V, B < $B_{RP(MIN)}$ – 10 G, B > $B_{OP(MAX)}$ + 10 G	–	–	25	μs
Supply Voltage Rise Time	$t_{RISE(VCC)}$	Rise time defined as 10%-90% from 0 to V_{CC}	–	–	50	μs
Chopping Frequency	f_C		–	800	–	kHz
Output Rise Time [3][4]	t_r	$R_{PULL-UP}$ = 820 Ω, C_S = 20 pF	–	0.2	2	μs
Output Fall Time [3][4]	t_f	$R_{PULL-UP}$ = 820 Ω, C_S = 20 pF	–	0.1	2	μs
Supply Current	I_{CC}		–	2.5	4	mA
Reverse Battery Current	I_{RCC}	V_{RCC} = –18 V	–	–	–5	mA
Supply Zener Clamp Voltage	V_Z	I_{CC} = 5 mA, T_A = 25°C	28	34	–	V
Zener Impedance	I_Z	I_{CC} = 5 mA, T_A = 25°C	–	50	–	Ω

MAGNETIC CHARACTERISTICS: Valid over full operating voltage and temperature ranges, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [2]
Operate Point	B_{OP}		5	25	50	G
Release Point	B_{RP}		–50	–25	–5	G
Hysteresis	B_{HYS}	B_{OP} – B_{RP}	20	50	80	G



1A 1B

Figure 1: Magnet Orientation for Switching Output On for LH package (Panel 1A) and UA Package (Panel 1B)

[1] Typical data is at T_A = 25ºC and V_{CC} = 12 V and it is for design information only.
[2] 1 G (gauss) = 0.1 mT (millitesla).
[3] Power-On Time, Rise Time and Fall Time are guaranteed through device characterization.
[4] C_S = oscilloscope probe capacitance.

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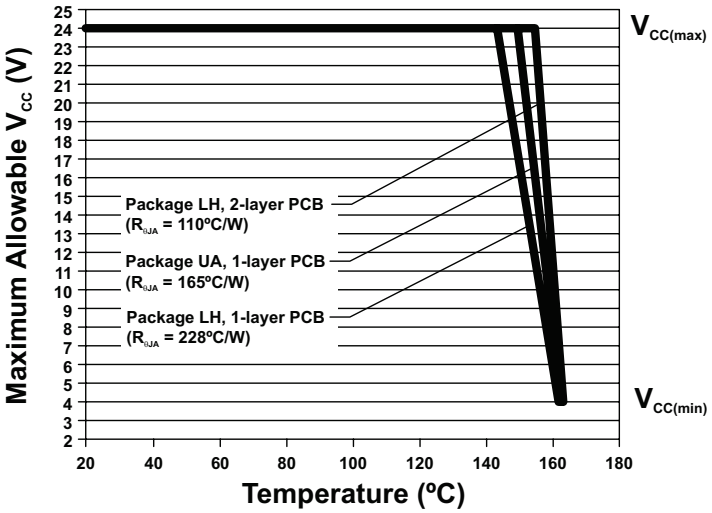
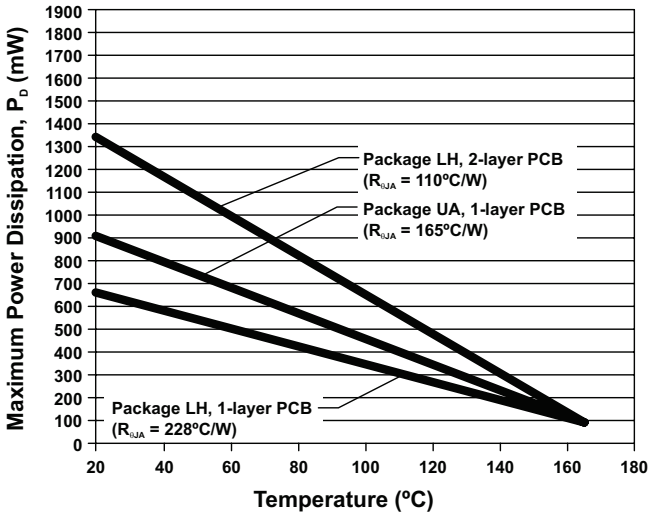
THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Notes	Rating	Unit
Package Thermal Resistance	$R_{\theta JA}$	Package LH, 2-layer PCB with 0.463 in.^{2} of copper area each side connected by thermal vias	110	°C/W
		Package LH, 1-layer PCB with copper limited to solder pads	228	°C/W
		Package UA, 1-layer PCB with copper limited to solder pads	165	°C/W



Power Derating Curve

$T_{J(max)}$ = 165ºC; $I_{CC} = I_{CC(max)}$



Power Dissipation versus Ambient Temperature

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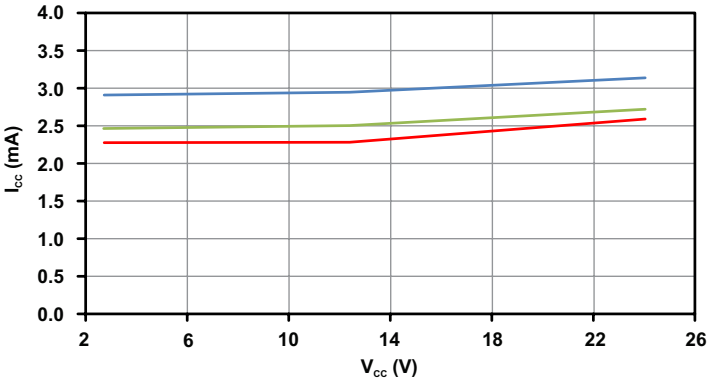
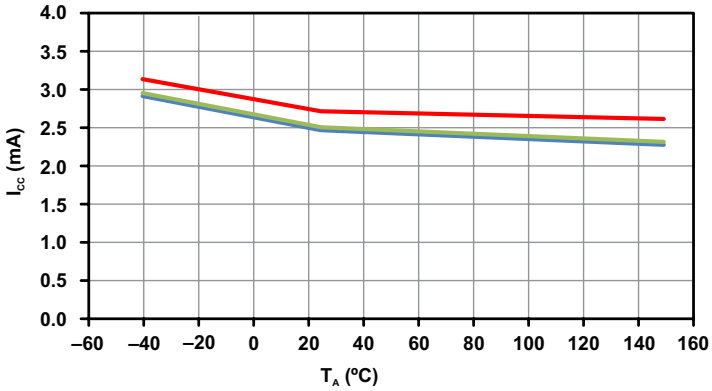
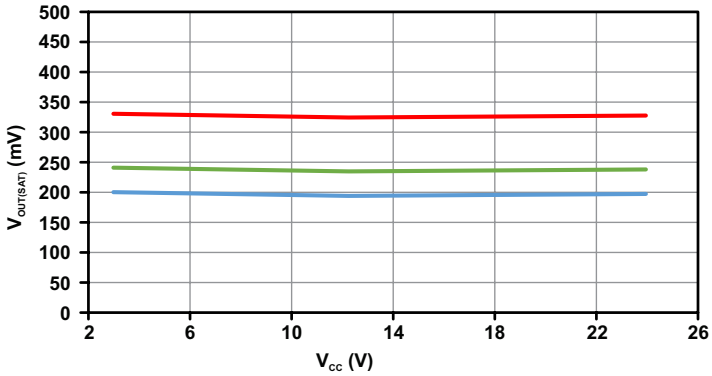
ELECTRICAL OPERATING CHARACTERISTICS



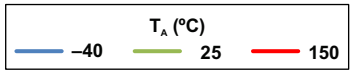
Average Supply Current versus Supply Voltage

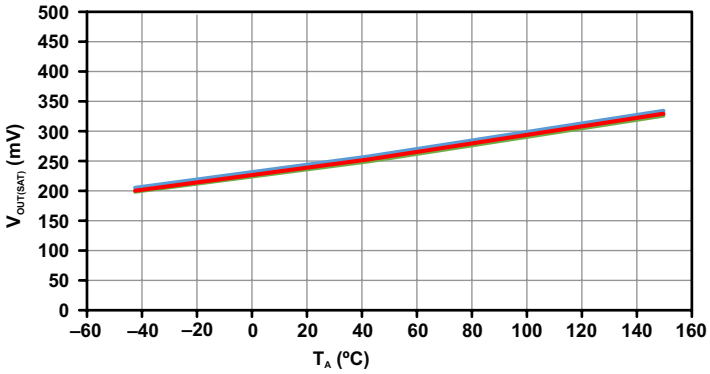


Average Supply Current versus Ambient Temperature

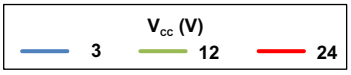


Average Low Output Voltage versus Supply Voltage





Average Low Output Voltage versus Ambient Temperature for I_{OUT} = 20 mA



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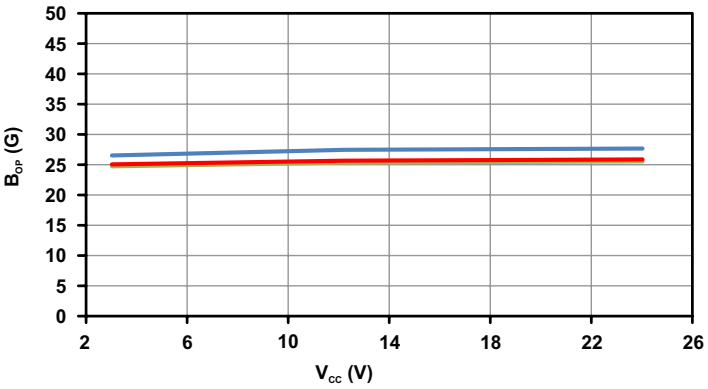
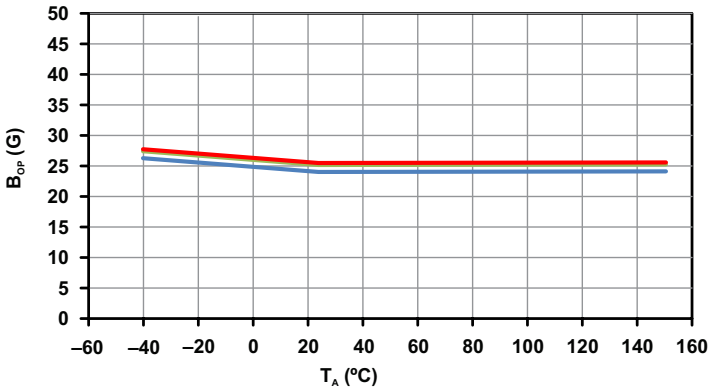
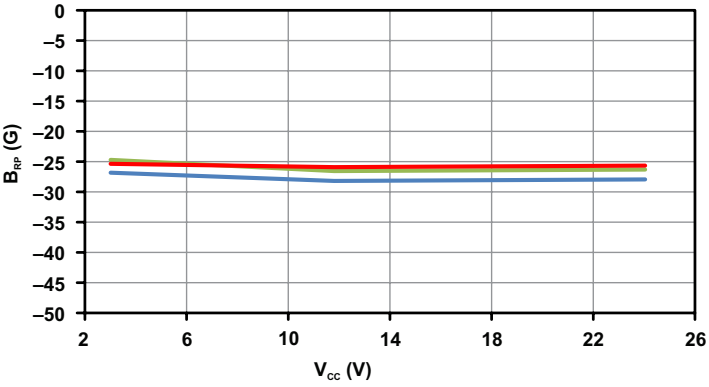
MAGNETIC OPERATING CHARACTERISTICS



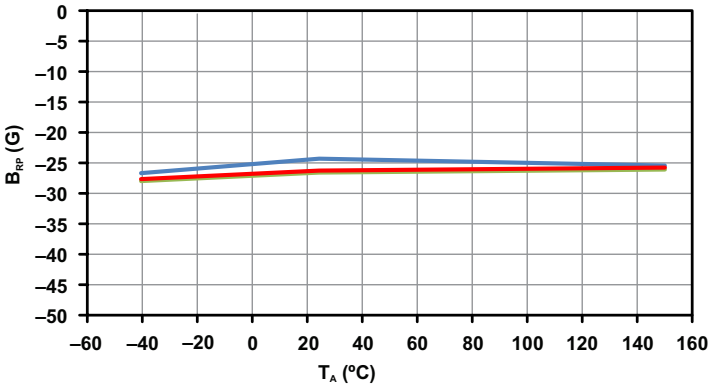
Average Operate Point versus Supply Voltage



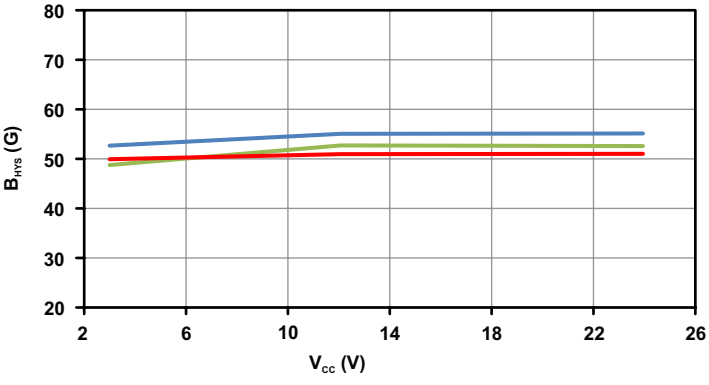
Average Operate Point versus Ambient Temperature



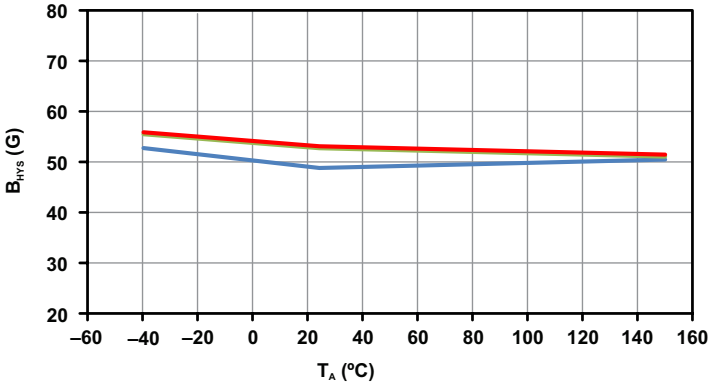
Average Release Point versus Supply Voltage



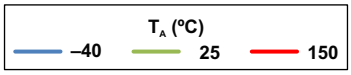
Average Release Point versus Ambient Temperature

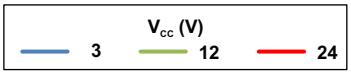


Average Switchpoint Hysteresis versus Supply Voltage



Average Switchpoint Hysteresis versus Ambient Temperature





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FUNCTIONAL DESCRIPTION

Operation

The output of these devices switches low (turns on) when a south polarity magnetic field perpendicular to the Hall-effect sensor exceeds the operate point threshold (B_{OP}). The LH package is offered with a vertical Hall element capable of sensing magnetic fields perpendicular to the non-leaded side of the package closest to pin 1. The UA package vertical Hall element senses fields perpendicular to the top of the package opposite of the device leads.

The magnetic field is perpendicular to the Hall-effect sensor when the direction of the field is parallel to the X-axis for the LH package (see panel 2A in Figure 2) and Y-axis for the UA package (see panel 2B in Figure 2). After turn-on, the output voltage is $V_{OUT(SAT)}$. The output transistor is capable of sinking current up to the short-circuit current limit I_{OM}, which is a minimum of 30 mA. The device output goes high (turns off) when the magnetic field is reduced below the release point (B_{RP}), which requires a north pole of sufficient strength.

Removal of the magnetic field will leave the device output latched on if the last crossed switch point is B_{OP}, or latched off if the last crossed switch point is B_{RP}.

The difference in the magnetic operate and release points is the hysteresis (B_{HYS}) of the device. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

Powering-on the device in the hysteresis range (less than B_{OP} and higher than B_{RP}) will give an indeterminate output state. A valid state is attained after the first excursion beyond B_{OP} or B_{RP}.

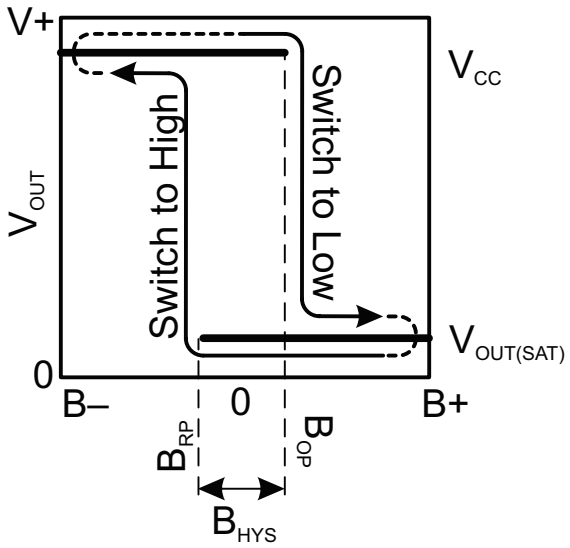

Figure 3: Switching Behavior of Latches

On the horizontal axis, the B+ direction indicates increasing south polarity magnetic field strength, and the B– direction indicates increasing north polarity magnetic field strength. Removal of the magnetic field will leave the device latched in its current state.

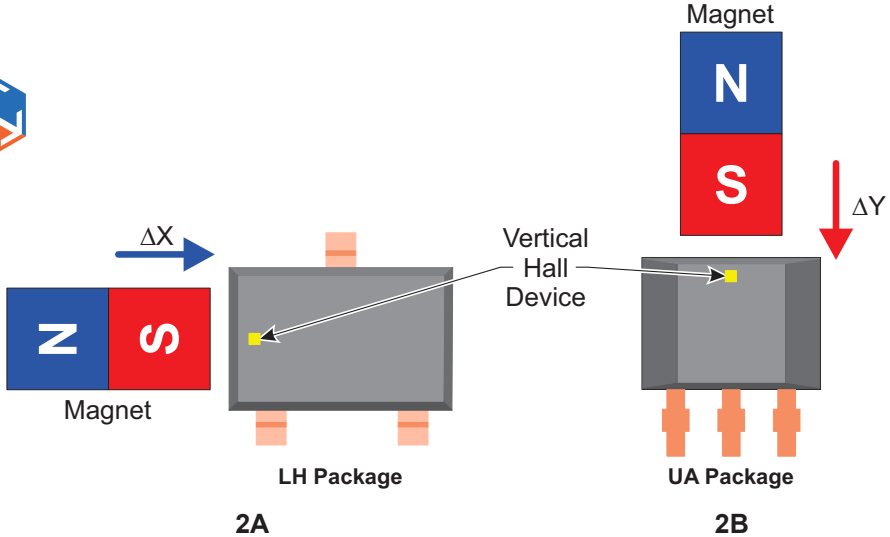

Figure 2: Vertical Hall Sensing

(Left) LH package orientation and (Right) UA package orientation (Not to scale)

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APPLICATIONS

It is strongly recommended that an external capacitor be connected (in close proximity to the Hall-effect sensor IC) between the supply and ground of the device to reduce both external noise and noise generated by the chopper stabilization technique. As shown in Figure 4, a 0.1 µF capacitor is typical.

In applications where the A1260 receives its power from an unregulated source such as a car battery, or where greater immunity is required, additional measures may be employed. Specifications for such transients will vary, so protection circuit design should be optimized for each application. For example, the Enhanced Protection Circuit shown in Figure 4 includes an optional series resistor and output capacitor which improves performance during Powered ESD testing (ISO 10605), Conducted Immunity testing (ISO 7637-2 and ISO 16750-2), and Bulk Current Injection testing (ISO 11452-4).

Extensive applications information on magnets and Hall-effect sensors is available in:

- *Hall-Effect IC Applications Guide, AN27701,*
- *Hall-Effect Devices: Guidelines For Designing Subassemblies Using Hall-Effect Devices AN27703.1*
- *Soldering Methods for Allegro's Products – SMT and Through-Hole, AN26009*

All are provided on the Allegro website:

www.allegromicro.com

Vertical Hall-Effect Sensor Linear Tools

System design and magnetic sensor evaluation often require an in-depth look at the overall strength and profile generated by a magnetic field input. To aid in this evaluation, Allegro MicroSystems provides a high-accuracy linear output tool capable of reporting the non-perpendicular magnetic field by means of a vertical Hall-effect sensor IC equipped with a calibrated analog output. For further information, contact your local Allegro field applications engineer or sales representative.

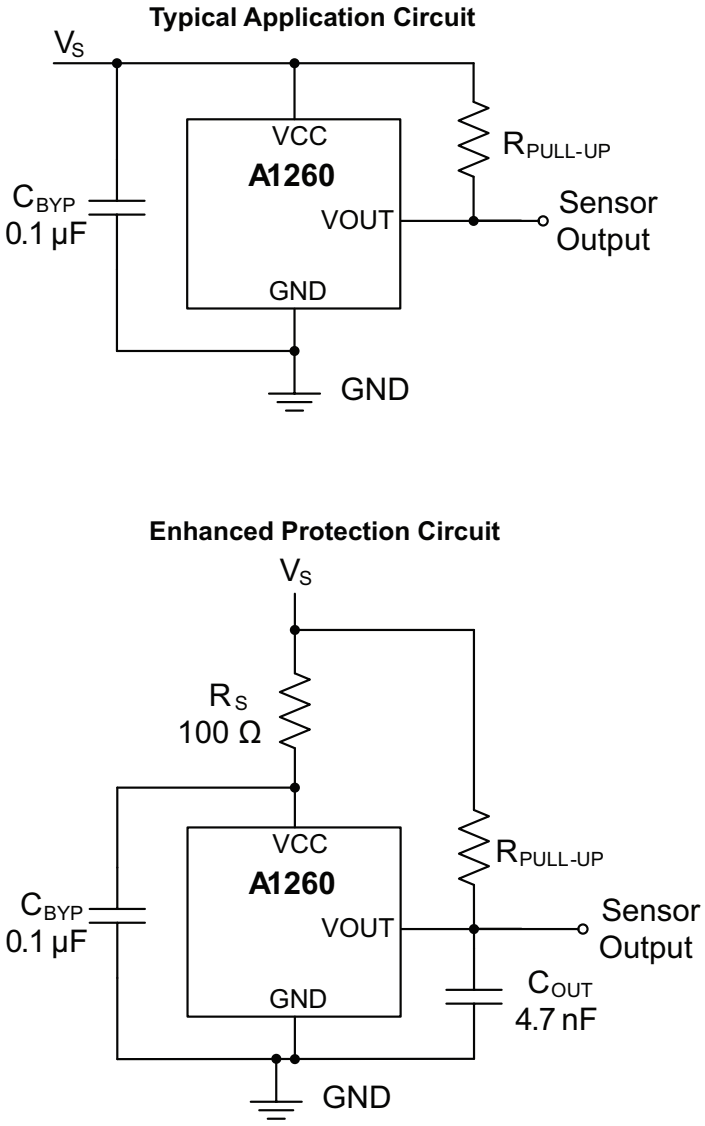

Figure 4: Typical and Enhanced Protection Application Circuits

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CHOPPER STABILIZATION

A limiting factor for switch point accuracy when using Hall-effect technology is the small-signal voltage developed across the Hall plate. This voltage is proportionally small relative to the offset that can be produced at the output of the Hall sensor. This makes it difficult to process the signal and maintain an accurate, reliable output over the specified temperature and voltage range. Chopper stabilization is a proven approach used to minimize Hall offset.

The Allegro technique, dynamic quadrature offset cancellation, removes key sources of the output drift induced by temperature and package stress. This offset reduction technique is based on a signal modulation-demodulation process. Figure 5: Model of Chopper Stabilization Circuit (Dynamic Offset Cancellation) illustrates how it is implemented.

The undesired offset signal is separated from the magnetically induced signal in the frequency domain through modulation. The subsequent demodulation acts as a modulation process for the offset causing the magnetically induced signal to recover its original spectrum at baseband while the DC offset becomes a high-frequency signal. Then, using a low-pass filter, the signal passes while the modulated DC offset is suppressed. Allegro's innovative chopper stabilization technique uses a high-frequency clock. The high-frequency operation allows a greater sampling rate that produces higher accuracy, reduced jitter, and faster signal processing. Additionally, filtering is more effective and results in a lower noise analog signal at the sensor output. Devices such as the A1260 that use this approach have an extremely stable quiescent Hall output voltage, are immune to thermal stress, and have precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process which allows the use of low offset and low noise amplifiers in combination with high-density logic and sample-and-hold circuits.

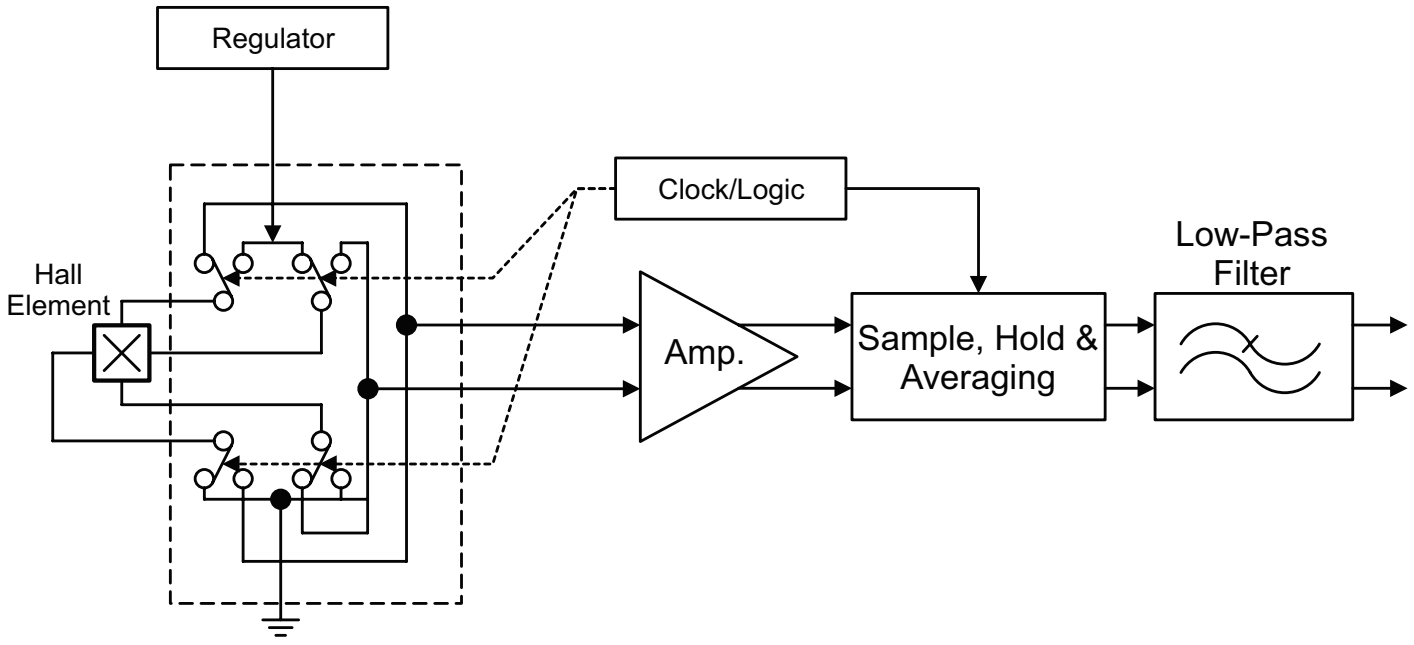

Figure 5: Model of Chopper Stabilization Circuit (Dynamic Offset Cancellation)

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POWER DERATING

The device must be operated below the maximum junction temperature of the device ($T_{J(max)}$). Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems website.)

The Package Thermal Resistance ($R_{\theta JA}$) is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity (K) of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case ($R_{\theta JC}$) is relatively small component of $R_{\theta JA}$. Ambient air temperature (T_A) and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta_T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta_T \quad (3)$$

For example, given common conditions such as:
T_A = 25°C, V_{CC} = 12 V, I_{CC} = 2.5 mA, and $R_{\theta JA}$ = 110°C/W for the LH package, then:

$$P_D = V_{CC} \times I_{CC} = 12\ V \times 2.5\ mA = 30\ mW$$

$$\Delta_T = P_D \times R_{\theta JA} = 30\ mW \times 110°C/W = 3.3°C$$

$$T_J = T_A + \Delta_T = 25°C + 3.3°C = 28.3°C$$

A worst-case estimate ($P_{D(max)}$) represents the maximum allowable power level ($V_{CC(max)}$, $I_{CC(max)}$), without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at T_A = 150°C, package LH, using low-K PCB.

Observe the worst-case ratings for the device, specifically:
$R_{\theta JA}$ = 228°C/W, $T_{J(max)}$ = 165°C, $V_{CC(max)}$ = 24 V, and $I_{CC(max)}$ = 4 mA.

Calculate the maximum allowable power level, $P_{D(max)}$. First, invert equation 3:

$$\Delta T_{max} = T_{J(max)} - T_A = 165°C - 150°C = 15°C$$

This provides the allowable increase to T_J resulting from internal power dissipation.

Then, invert equation 2:

$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15°C \div 228°C/W = 66\ mW$$

Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_{D(max)} \div I_{CC(max)} = 66\ mW \div 4\ mA = 16.4\ V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages ≤ $V_{CC(est)}$.

Compare $V_{CC(est)}$ to $V_{CC(max)}$. If $V_{CC(est)} \leq V_{CC(max)}$, then reliable operation between $V_{CC(est)}$ and $V_{CC(max)}$ requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \geq V_{CC(max)}$, then operation between $V_{CC(est)}$ and $V_{CC(max)}$ is reliable under these conditions.

In cases where the $V_{CC(max)}$ level is known, and the system designer would like to determine the maximum allowable ambient temperature ($T_{A(max)}$), the calculations can be reversed.

For example, in a worst case scenario with conditions $V_{CC(max)}$ = 24 V, $I_{CC(max)}$ = 4 mA, and $R_{\theta JA}$ = 228°C/W using equation 1 the largest possible amount of dissipated power is:

$$P_D = V_{IN} \times I_{IN}$$

$$P_D = 24\ V \times 4\ mA = 96\ mW$$

Then, by rearranging equations 3:

$$T_{A(max)} = T_{J(max)} - \Delta_T$$

$$T_{A\ (max)} = 165°C/W - (96\ mW \times 228°C/W)$$

$$T_{A\ (max)} = 165°C/W - 21.9°C = 143.1°C$$

In another example, the regulated supply voltage is equal to 3 V. Therefore, $V_{CC(max)}$ = 3 V and $I_{CC(max)}$ = 4 mA. By using equation 1 the largest possible amount of dissipated power is:

$$P_D = V_{IN} \times I_{IN}$$

$$P_D = 3\ V \times 4\ mA = 12\ mW$$

Then, by rearranging equation 3:

$$T_{A(max)} = T_{J(max)} - \Delta_T$$

$$T_{A(max)} = 165°C/W - (12\ mW \times 228°C/W)$$

$$T_{A(max)} = 165°C/W - 2.7°C = 162.3°C$$

The operating temperature range of the device (T_A) is limited to between -40°C and 150°C, and in the above case there is sufficient power dissipation head room to operate the device throughout this range.

In the above example, we are not exceeding the maximum junction temperature; however, performance beyond the maximum operating ambient temperature of 150ºC is not guaranteed.

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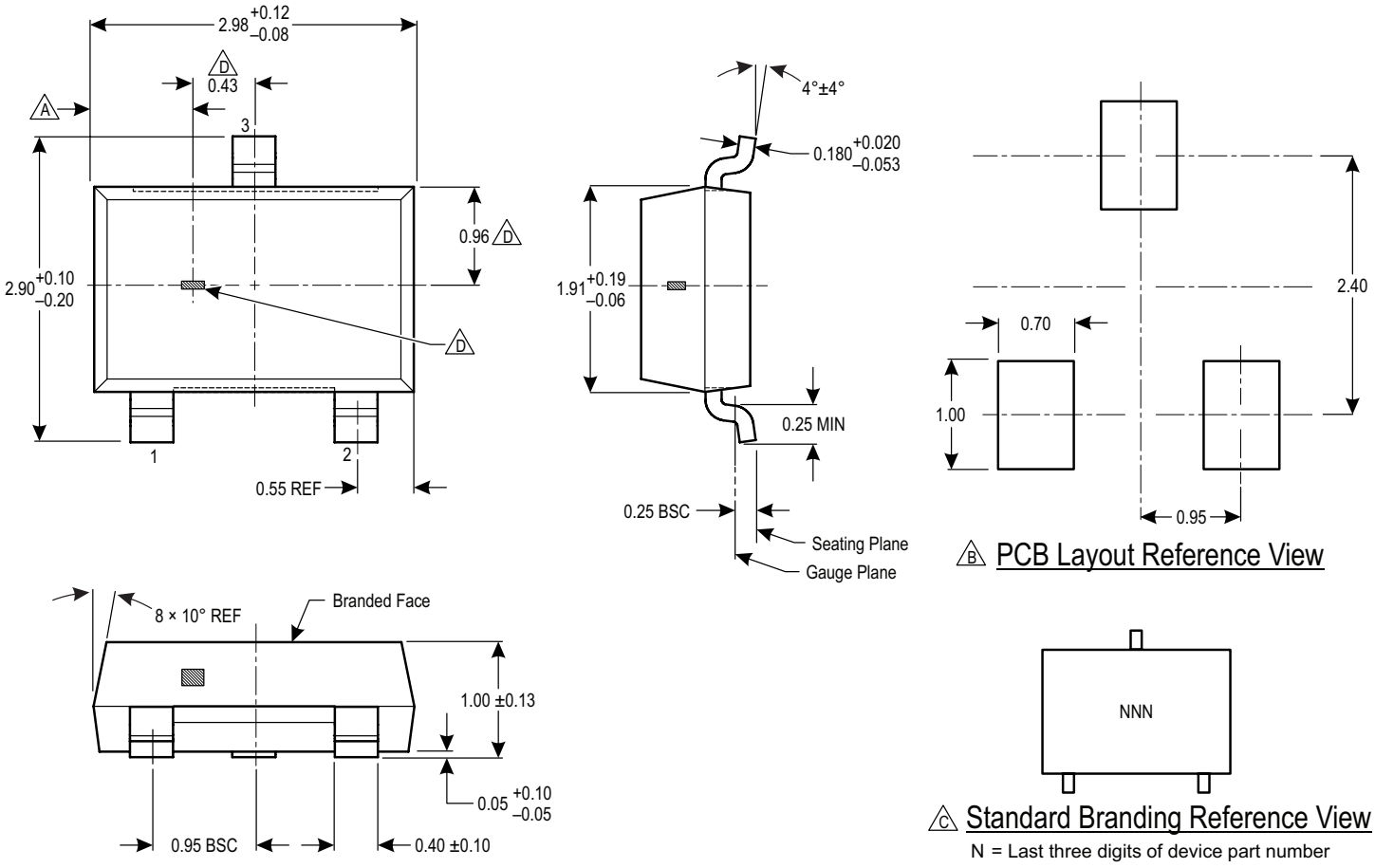
PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use

(Reference DWG-0000628)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Active Area Depth, 1.06 mm

B Reference land pattern layout
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

D Hall elements, not to scale

Figure 6: Package LH, 3-Pin SOT23-W

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(Reference DWG-0000404, Rev. 1)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

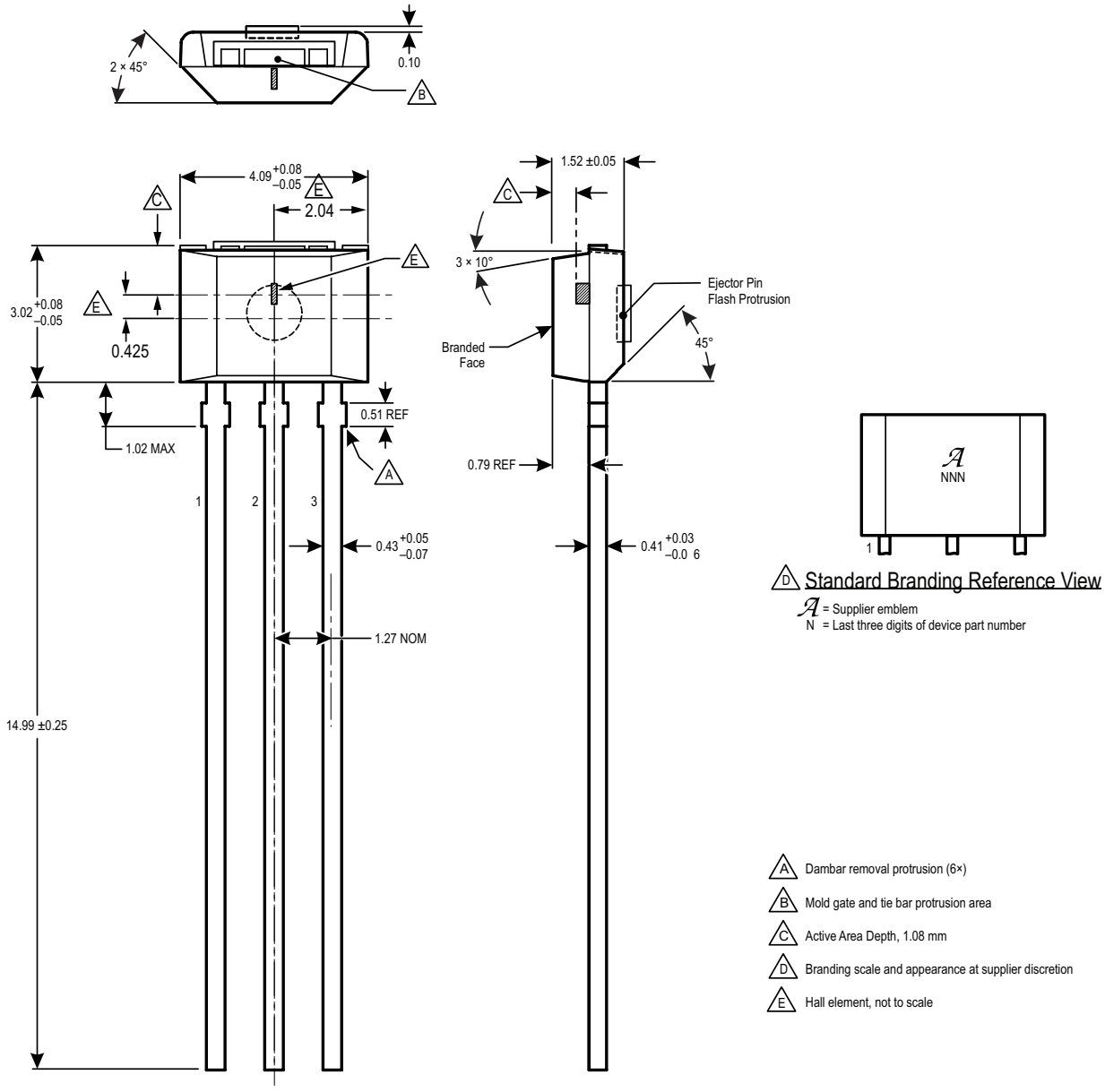

Figure 7: Package UA, 3-Pin SIP, Matrix Style

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Revision History

Number	Date	Description
–	March 10, 2015	Initial release
1	July 13, 2015	Corrected LH package Active Area Depth value
2	September 21, 2015	Added AEC-Q100 qualification under Features and Benefits
3	October 20, 2017	Added compliance for 175°C junction temperature operation; updated Absolute Maximums table, Figure 4, Package Outline Drawings, and minor editorial changes.
4	August 2, 2018	Updated availability of certain part options in Selection Guide (page 2), Maximum Junction Temperature notes (page 2), Output Rise and Fall Time resistor symbol (page 4), and Applications section (page 9).
5	December 3, 2018	Added Reverse Output Voltage to Absolute Maximum Ratings table (page 2)
6	December 12, 2019	Minor editorial updates
7	January 7, 2021	Updated Figure 1 (page 4), LH package outline drawing reference number (page 12); added Typical Applications (page 1).
8	March 25, 2021	Added Supply Voltage Rise Time characteristic (page 4); updated UA package outline drawing (page 13).

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