Change Summary

Changes from August 2011 issue to November 2012 issue. Page, section, figure and table numbers refer to this current issue.

Page	Item	Change
Multiple	Zarlink logo and name reference	Updated to Microsemi logo and name.

Changes from September 2007 issue to August 2011 issue. Page, section, figure and table numbers refer to this current issue.

Page	Item	Change
1	Ordering Information	Changed 96 Pin CABGA to 96 Pin VFBGA.
9	Package Drawing	Updated 96L VFBGA package drawing.

1.0 Functional Description

The ZL38005 is a hardware platform designed to support advanced acoustic echo canceller (with noise reduction) firmware applications available from Microsemi. These applications are resident in external memory and are down-loaded by the ZL38005 resident boot code during initialization.

The firmware product and manual available at the release of this data sheet is the ZLS38501: Acoustic Echo Canceller with Noise Reduction. If these applications do not meet your requirements, please contact your local Microsemi CMPG Sales Office for the latest firmware releases.

The ZL38005 Advanced Acoustic Echo Canceller with Noise Reduction platform integrates Microsemi's Voice Processor (ZVP) DSP Core with a number of internal peripherals. These peripherals include the following:

- Two independent ΔΣ CODECs
- Two PCM ports - ST BUS, GCI, McBSP or SSI operation
- An I^2S interface port
- A 2048 tap Filter Co-processor (LMS, FIR and FAP realizations)
- Two Auxiliary Timers and a Watchdog Timer
- 11 GPIO pins
- A UART interface
- A Slave SPI port and a Master SPI port
- A timing block that supports master and slave operation
- An IEEE - 1149.1 compatible JTAG port

The DSP Core can process up to four 8-bit audio channels, two 16-bit audio channels or two 8-bit and one 16-bit audio channel. These audio channels may originate and terminate with the ΣΔ CODECs, or be communicated to and from the DSP Core through the PCM ports or the I^2S port.

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2.0 Core DSP Functional Block

The ZL38005 DSP Core functional block, illustrated in Figure 1, is made up of a DSP Core, Interrupt Controller, Data RAM, Instruction RAM, BOOT ROM Hardware Accelerators. This block controls the timing (APLL and Timing Generator), peripheral interfaces through a peripheral address/data/control bus.

The ZL38005 implementation of DSP core and Filter Co-processor have been optimized to efficiently support voice processing applications. These applications are described in detail in the Firmware Manuals associated with this hardware platform.

2.1 DSP

The Core DSP is a 100 MIPS processor realized with two internal memory busses (Harvard architecture) to allow multiple accesses during the same instruction cycle. In addition the DSP uses hardware accelerators and a filter co processor that can be reused for different applications.

The Filter Co-Processor is used by the application firmware to realize the LMS filters up to a maximum of 2048 coefficients (taps).

3.0 Codec[1:0]

The ZL38005 has two 16-bit fully differential ΔΣ DACs (DAC 0/1) that meets G.712 requirements at 8 kHz sampling The ADC path consists of input signal pins C0/1_ADCi+ and C0/1_ADCi- (buffer output pins C0/1_BF0+ and C0/1_BFo-), which feed selectable Microphone Amplifier or Line Amplifier options. The ADC sampling is 8KHz.

4.0 PCM Port

4.1 PCM Port

The PCM port support data communication between an external peripheral device and the ZL38005 DSP Core using separate input (PCMi) and output (PCMo) serial streams with TDM (i.e., ST-BUS, GCI or McBSP) or SSI interface timing. Access to the control and status registers associated with these ports is through the Slave SPI port UART. These port signals are either in their input or high impedance states after a power-on reset and outputs signals PCMo may be put in a high impedance state at any time during normal operation. Refer to the associated Firmware Manual for PCM port control, status and mode selection.

Figure 2 illustrates the signals associated with the Master and Slave timing modes of operation for PCM Port. Insert A: PCM port Master TDM (Mode 0), shows data clock (PCM_CLKo) and frame pulse ($\overline{\text{PCMFP}}$) as outputs derived from the ZL38005 internal PLL. PCM_CLKo clocks data into the ZL38005 on PCMCMi and out of the ZL38005 on PCMo, and $\overline{\text{PCMFP}}$ delineates the 8 kHz frame boundaries for these signals. Insert B: PCM Master SSI (Mode3), functions the same way as the TDM Master except that selected channels are defined by enable outputs P0ENA1 and P0ENA2.

With slave operation the source of timing is not the ZL38005, so PCM_CLKi is the input clock and $\overline{\text{PCMFP}}$ is the 8 kHz input frame pulse. This is illustrated by Figure 2 C: PCM Port Slave TDM (Modes 1 & 2) and D: PCM Port Slave SSI (Modes 4, 5 & 6).

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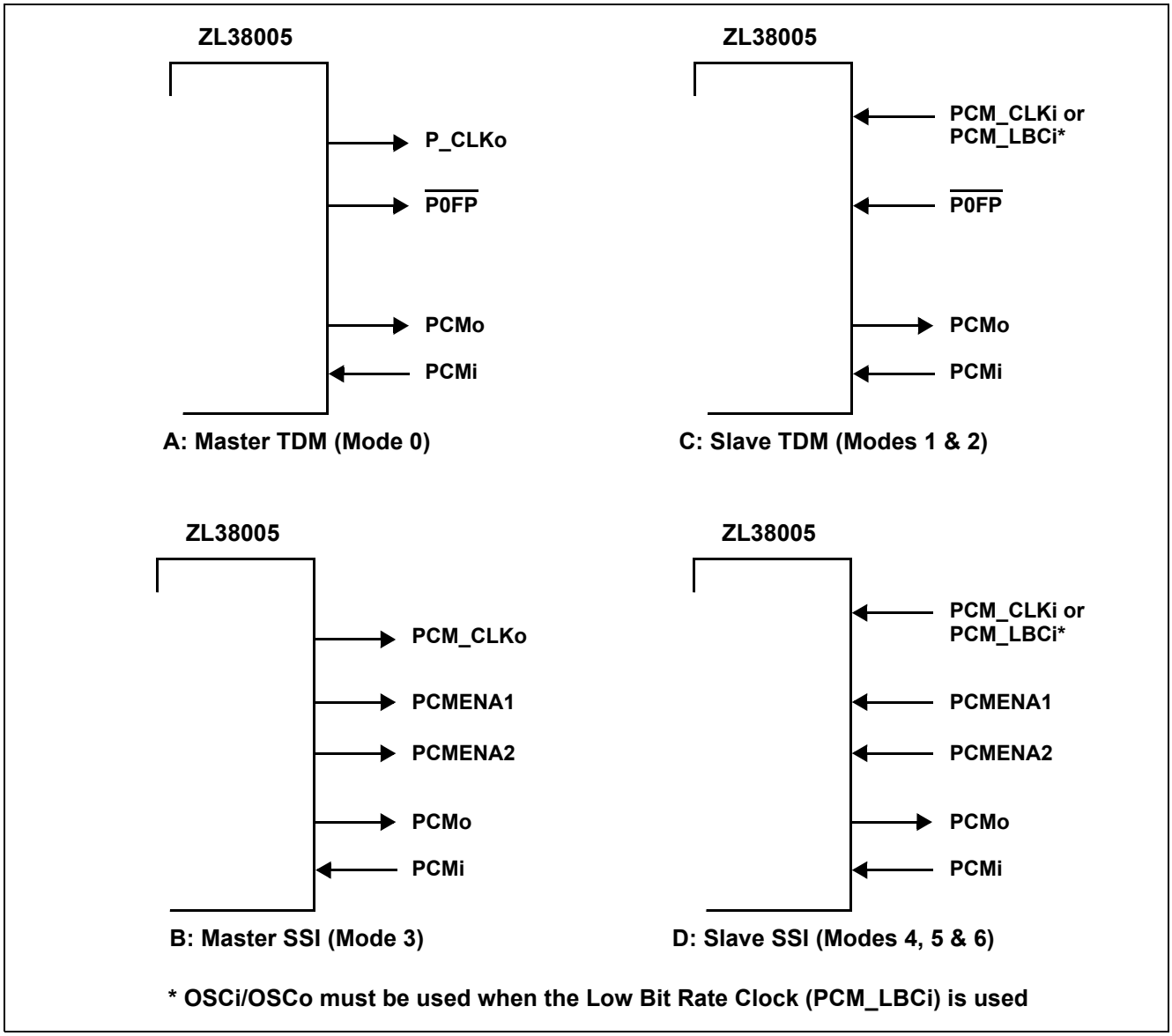

Figure 2 - PCM Port Signal Configurations for Master/Slave Operation

The ZL38005 will process audio channels of up to 16 bits in length. Audio channel sizes are designated as either 8-bit (Short) or 16-bit (Long) on the PCM interfaces. With TDM operation each audio channel is mapped on to one or more 8-bit time slots that are defined by the associated frame alignment signal. Each PCM port (0 & 1) supports from 1 to 4 Short Channels; 1 or 2 Short Channels and 1 Long (16-bit) Channel; or 2 Long Channels. Audio channels are defined as First and Second Long, and First, Second, Third and Fourth Short, see the Firmware Manual for assignment details. These channels may be assigned to different time slots on the input and output streams.

In SSI mode each PCM port supports 1 or 2 Short or Long channels, which are defined on PCMi0 by the position and length of enable signals P0ENA1 and P0ENA2. Audio channels are defined as First and Second Long, and First and Third Short, see the Firmware Manual for assignment details. Channel positions and length are common to input and output signals.

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4.2 SSI Operation

Figures 3 illustrates the SSI functional timing used when the two enable strobes (audio channels) are separated by a non-zero number of bit clock cycles. Here the enable signal polarities are active low, either bit clock polarity may be selected. In this format frames are delineated by the active edge of PCMENA1 minus 1/2 bit clock cycle. The frame repetition rate is 8 kHz. See Firmware Manual to program the positions of the Audio Channels within the 8 kHz frame.

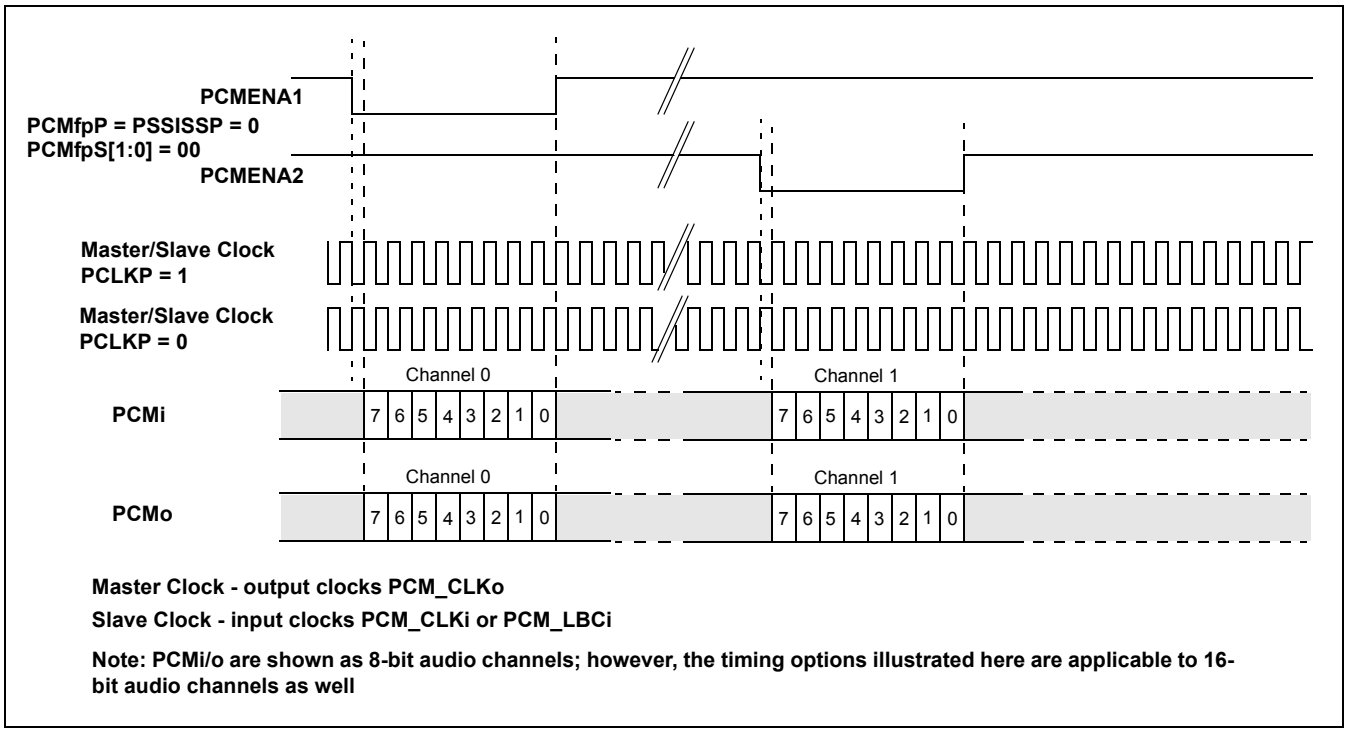

Figure 3 - SSI Mode: Separated Channels Functional Timing

4.3 I^2S Port Description

The I^2S (Inter-IC Sound) port and PCM Port One share the same physical pins of the ZL38005. Selection of either I^2S port operation or PCM Port One operation is done through the Port One PCM/I^2S Select Register. See Firmware Manual.

The I^2S port can be used to connect external Analog-to-Digital Converters or CODECs to the internal DSP. This port can operate in master mode, where the ZL38005 is the source of the port clocks, or slave mode, where the bit and sampling clocks (I^2S_SCK and I^2S_ LRCK) are inputs to the ZL38005. The master clock (I^2S_MCLK) is always an output. In I^2S port master mode the clock signal at output pin I^2S_LRCK is the sampling frequency (f_S), the clock signal at output I^2S_SCK is 32 x f_S, and the clock signal at output I^2S_MCLK is 256 x f_S. In I^2S port slave mode the relationship between the clock signal at input pin I^2S_LRCK and the clock signal at input I^2S_SCK must be 32 x f_S. In slave mode the 256 x f_S relationship between f_S and the I^2S_MCLK is not mandatory, and the I^2S_MCLK output pin will be in a high impedance state. See Firmware Manual for I^2S programming options.

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The I^2S interface can support two dual channel Analog-to-Digital Converters (Figure 4) or one dual channel CODEC (Figure 5). In Figure 4 pin I^2S_SDi/o is configured as an input (control bit I^2SSDi/oSel = 0) so that the four 16-bit channel processing capacity of the DSP is spread across the two input channels from Dual ADC (0) plus the two input channels from Dual ADC (1). See Firmware Manual for I^2S port setup.

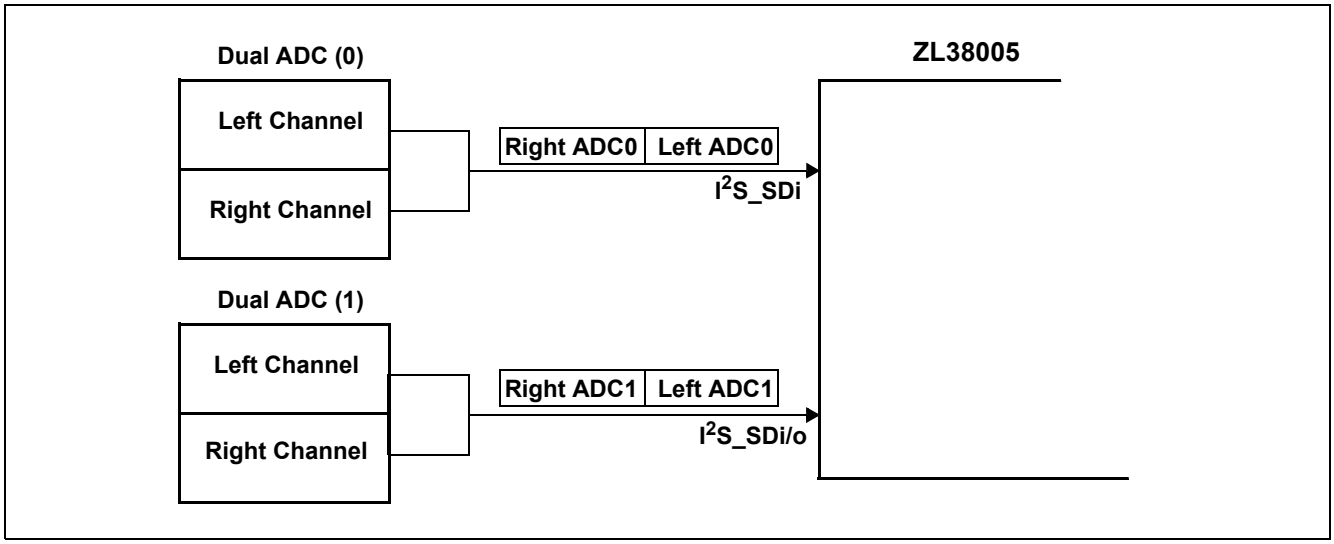

Figure 4 - Dual Analog-to-Digital Converter Configuration

In Figure 5 pin I^2S_SDi/o is configured as an output (control bit I^2SSDi/oSel = 1) so that the four 16-bit channel processing capacity of the DSP is spread across the two input channels from the ADCs of CODEC(0) and CODEC(1), as well as the two output channels from the ADCs of CODEC(0) and CODEC(1). See Firmware Manual for I^2S port setup.

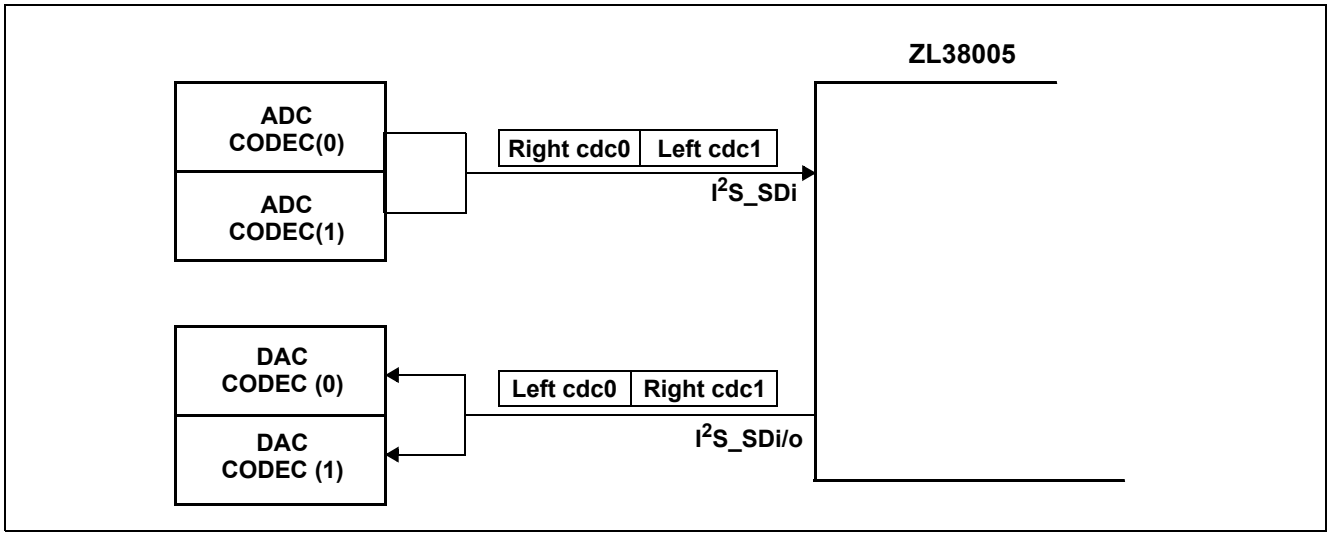

Figure 5 - Dual CODEC Configuration

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5.0 Host Microprocessor and Peripheral Interfaces

5.1 Master SPI (FLASH Port)

The Master SPI port is used by the ZL38005 to access one or two peripheral devices (chip select signals SPIM_CS[1:0]). It supports both SPI and MICROWIRE modes of operation and can write up to 40 bits or read up to 32 bits in a single access. The Chip Select output signals may be programmed for a single access or burst access. All communication is MSB first and all pins of the master SPI port are outputs controlled by the ZL38005, except SPIM_MISO, se

5.2 Host Interface Operation (Slave SPI and UART Ports)

The control/status registers and memory of the ZL38005 can be accessed (R/W) by an external host through the Slave SPI and the UART ports.

The slave SPI port may be used by an external host microprocessor to access (Read/Write) the ZL38005 internal control/status registers and memory. Access is initiated when the external host makes signal $\overline{\text{SPIS\_CS}}$ low and is ended when this signal goes high. The host will then apply a clock (maximum 25 MHz) to signal SPIS_CLK to clock data out of SPIS_MISO and in on SPIS_MOSI.

The UART (Universal Asynchronous Receiver Transmitter) port may be used by an external host microprocessor to access (Read/Write) the ZL38005 internal control/status registers and memory. The ZL38005 DSP will set up the initial parameters of this port (i.e., master/slave, baud rate, stop bits, parity bit...) during the Boot process. After the device has been booted these port options can be changed as per the Firmware Manual.

The UART port will support 8-bit data only with any combination of 1 start bit, 0 or 1 parity bit(s) and 1, 1.5 or 2 stop bit(s).

5.3 GPIO

The ZL38005 has 11 GPIO (General Purpose Input/Output) pins that can be individually configured as either input or output. These pins are intended for low frequency signalling.

When a GPIO pin is defined as an input the state of that input pin is sampled with the internal master clock (Mclk = 100 MHz) and latched into the GPIO Read Register.

Immediately after a power-on reset ($\overline{\text{RST}}$ pin) the GPIO pins are defined as inputs and their state is captured in the GPIO Start-Up Status Register. The state of this register is used by the Boot program to determine the base functionality and programming options of the device.

Individual GPIO pins may also be defined as outputs with associated enable/disable (active/high impedance) control. See the Firmware Manual for control and status programming.

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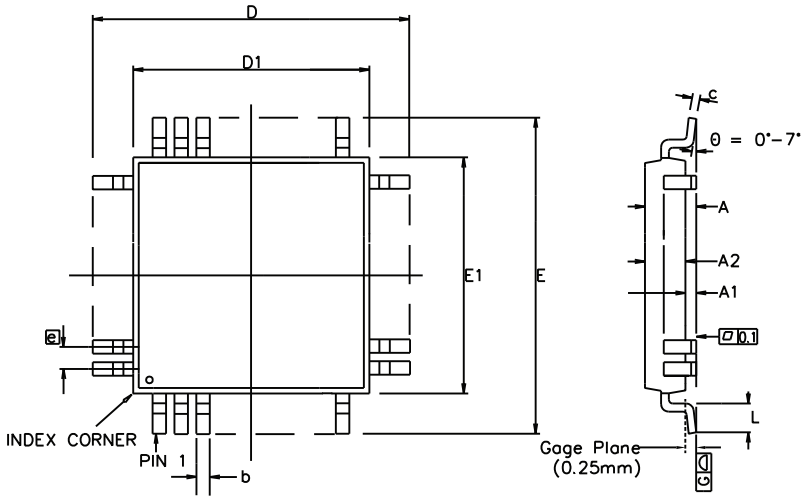

Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	---	1.60		---	0.063
A1	0.05	0.15		0.002	0.006
A2	1.35	1.45		0.053	0.057
D	16.00 BSC			0.630 BSC	
D1	14.00 BSC			0.551 BSC	
E	16.00 BSC			0.630 BSC	
E1	14.00 BSC			0.551 BSC	
L	0.45	0.75		0.018	0.030
e	0.50 BSC			0.020 BSC	
b	0.17	0.27		0.007	0.011
c	0.09	0.20		0.004	0.008
	Pin features				
N	100				
ND	25				
NE	25				
NOTE	SQUARE				

Conforms to JEDEC MS-026 BED Iss. C

Notes:
1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protusion.
5. Dimension b does not include dambar protusion.
6. Coplanarity, measured at seating plane G, to be 0.08 mm max.

This drawing supersedes 418/ED/51210/023 (Swindon)

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ACN	201373	207144	212447	
DATE	29Oct96	15Jul99	26Mar02	
APPRD.				

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Previous package codes: GP / B

Package Code: QC

Package Outline for 100 lead LQFP (14 x 14 x 1.4mm) 2.0mm Footprint

GPD00253

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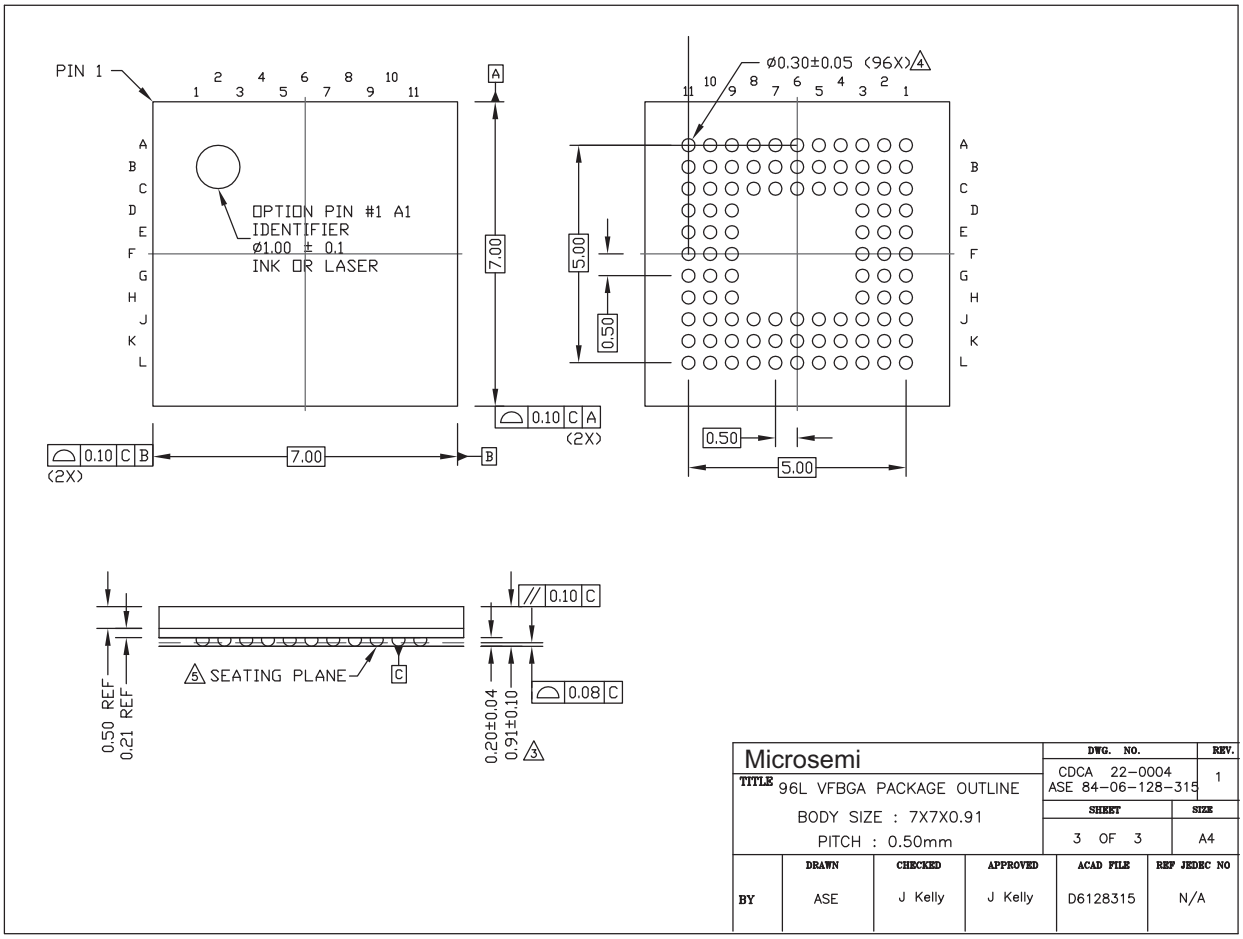

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Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

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