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1 GENERAL DESCRIPTION

The W71NW series is a Multi-Chip Package (MCP) memory product family that consists of a 1.8V NAND Flash Memory device and a 1.8V Low Power SDRAM device in one convenient VFBGA package.

W71NW11GC1DW consists of:

- W29N01GW - 1.8V 1G-Bit x16-BIT NAND Flash Memory
- W949D6KK - 1.8V 512M-Bit Low Power DDR SDRAM
- 130 Ball VFBGA - Dimension 8x9x1mm, ball pitch 0.65-mm, ball diameter 0.3-mm

2 FEATURES

W29N01GW NAND Flash Memory

- **Basic Features**
  - – Density : 1Gbit (Single chip solution)
  - – Vcc : 1.7V to 1.95V
  - – Bus width : x16
  - – Operating temperature
    - Industrial: - 40°C to 85°C
- **Single-Level Cell (SLC) technology.**
- **Organization**
  - – Density: 1G-bit/128M-byte
  - – Page size:1,056 words(1024 +32 words)
  - – Block size:64 pages(64K +2K words)
- **Highest Performance**
  - – Read performance (Max.)
    - Random read: 25us
    - Sequential read cycle: 35ns
  - – Write Erase performance
    - Page program time: 300us(typ.)
    - Block erase time: 2ms(typ.)
  - – Endurance 100K Erase/Program Cycles[1]
  - – 10-years data retention
- **Command set**
  - – Standard NAND command set
  - – Additional command support
    - Sequential Cache Read
    - Random Cache Read
    - Cache Program
    - Copy Back
    - OTP Data Program**,** Data Lock by Page **and** Data Read
  - – Contact Winbond for block Lock feature
- **Lowest power consumption**
  - – Read: 10mA(typ.)
  - – Program/Erase: 10mA(typ.)
  - – CMOS standby: 10uA(typ.)

W949D6KK Low Power DDR SDRAM

- Voltage Supply -
  - VDD = 1.7~1.95V
  - VDDQ = 1.7~1.95V;
- Data width: x16
- Clock rate: 200MHz (-5),166MHz (-6)
- Standard Self Refresh Mode
- Partial Array Self-Refresh(PASR)
- Auto Temperature Compensated Self-Refresh(ATCSR)
- Power Down Mode
- Deep Power Down Mode (DPD Mode)
- Programmable output buffer driver strength
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- Clock Stop capability during idle periods
- Auto Pre-charge option for each burst access
- Double data rate for data output
- Differential clock inputs (CK and #CK)
- Bidirectional, data strobe (DQS)
- #CAS Latency: 2 and 3
- Burst Length: 2, 4, 8 and 16
- Burst Type: Sequential or Interleave
- 64 ms Refresh period
- Interface: LVCMOS compatible
- Operating Temperature Range
  - Industrial (-40°C ~ 85°C)

Note:

1. **Endurance specification is based on 1bit/528 byte ECC (Error Correcting Code).**

3 BALL CONFIGURATION

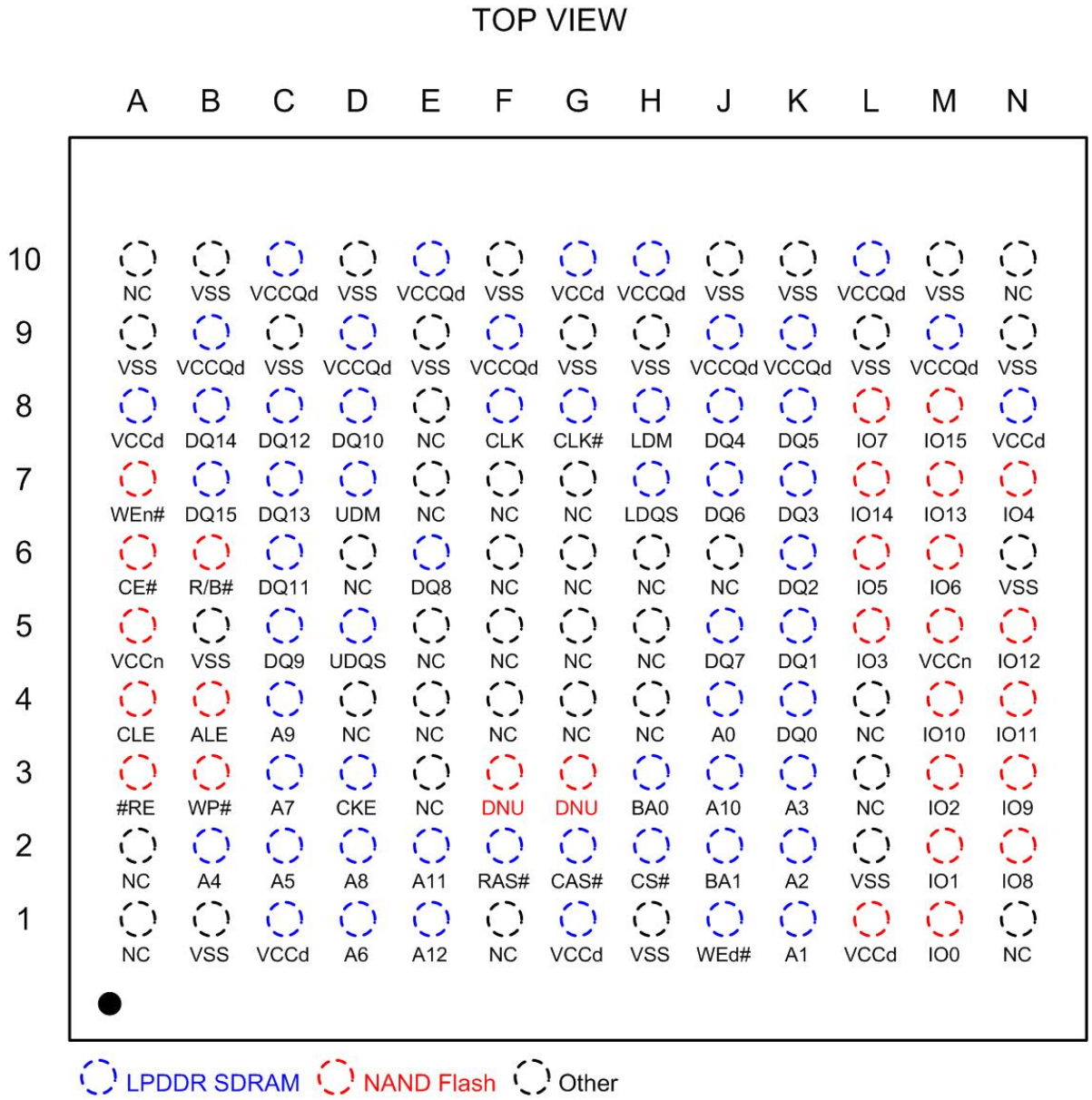


Figure 3-1 W71NW11GC1DW, 130 Ball VFBGA Package (Balls facing down)

3.1 130-Ball Description for W29N01GW NAND Flash Memory

Ball NO.	BALL NAME	I/O	FUNCTION
A7	WEn#	I	Write Enable
B3	WP#	I	Write Protect
B4	ALE	I	Address Latch Enable
A4	CLE	I	Command Latch Enable
A6	CE#	I	Chip Enable
A3	RE#	I	Read Enable
B6	R/B#	I	Ready/#Busy
M1	IO0	I/O	Data Input Output 0
M2	IO1	I/O	Data Input Output 1
M3	IO2	I/O	Data Input Output 2
L5	IO3	I/O	Data Input Output 3
N7	IO4	I/O	Data Input Output 4
L6	IO5	I/O	Data Input Output 5
M6	IO6	I/O	Data Input Output 6
L8	IO7	I/O	Data Input Output 7
N2	IO8	I/O	Data Input Output 8
N3	IO9	I/O	Data Input Output 9
M4	IO10	I/O	Data Input Output 10
N4	IO11	I/O	Data Input Output 11
N5	IO12	I/O	Data Input Output 12
M7	IO13	I/O	Data Input Output 13
L7	IO14	I/O	Data Input Output 14
M8	IO15	I/O	Data Input Output 15
A5, M5	VCCn		Power Supply NAND
A9, B1, B5, B10, C9, D10, E9, F10 G9, H1, H9, J10, K10, L2, L9, M10, N6, N9	VSS		Ground
F3, G3	DNU		Do Not Use
Multiple	NC		No Connection

Table 3-1 W29N01GW VFBGA-130 Ball Description

3.2 130-Ball Description for W949D6KK Low Power DDR SDRAM

BALL NO.	BALL NAME	I/O	FUNCTION
H2	CS#	I	Chip Select
D3	CKE	I	Clock Enable
F8	CLK	I	CK and CK# are differential clock inputs.
G8	CLK#	I	CK and CK# are differential clock inputs.
E1	A12	I	DDR Address Input
E2	A11	I	DDR Address Input
J3	A10	I	DDR Address Input
C4	A9	I	DDR Address Input
D2	A8	I	DDR Address Input
C3	A7	I	DDR Address Input
D1	A6	I	DDR Address Input
C2	A5	I	DDR Address Input
B2	A4	I	DDR Address Input
K3	A3	I	DDR Address Input
K2	A2	I	DDR Address Input
K1	A1	I	DDR Address Input
J4	A0	I	DDR Address Input
J2	BA1	I	Bank Select
H3	BA0	I	Bank Select
D7	UDM	I	Input Data Mask
H8	LDM	I	Input Data Mask
D5	UDQS	I/O	Data Strobe
H7	LDQS	I/O	Data Strobe
B7	DQ15	I/O	Data Inputs/Output
B8	DQ14	I/O	Data Inputs/Output
C7	DQ13	I/O	Data Inputs/Output
C8	DQ12	I/O	Data Inputs/Output
C6	DQ11	I/O	Data Inputs/Output
D8	DQ10	I/O	Data Inputs/Output
C5	DQ9	I/O	Data Inputs/Output
E6	DQ8	I/O	Data Inputs/Output
J5	DQ7	I/O	Data Inputs/Output
J7	DQ6	I/O	Data Inputs/Output

BALL NO.	BALL NAME	I/O	FUNCTION
K8	DQ5	I/O	Data Inputs/Output
J8	DQ4	I/O	Data Inputs/Output
K7	DQ3	I/O	Data Inputs/Output
K6	DQ2	I/O	Data Inputs/Output
K5	DQ1	I/O	Data Inputs/Output
K4	DQ0	I/O	Data Inputs/Output
F2	RAS#	I	Row Address Strobe
G2	CAS#	I	Column Address Strobe
J1	WEd#	I	Write Enable
A8, C1, G1, G10, L1, N8,	VCCd		Power Supply
B9, C10, D9, E10, F9, H10, J9, K9, L10, M9,	VCCQd		I/O Power Supply
A9, B1, B5, B10, C9, D10, E9, F10 G9, H1, H9, J10, K10, L2, L9, M10, N6, N9	VSS		Ground

Table 3-2 W949D6KK VFBGA-130 Ball Description

4 Block Diagram

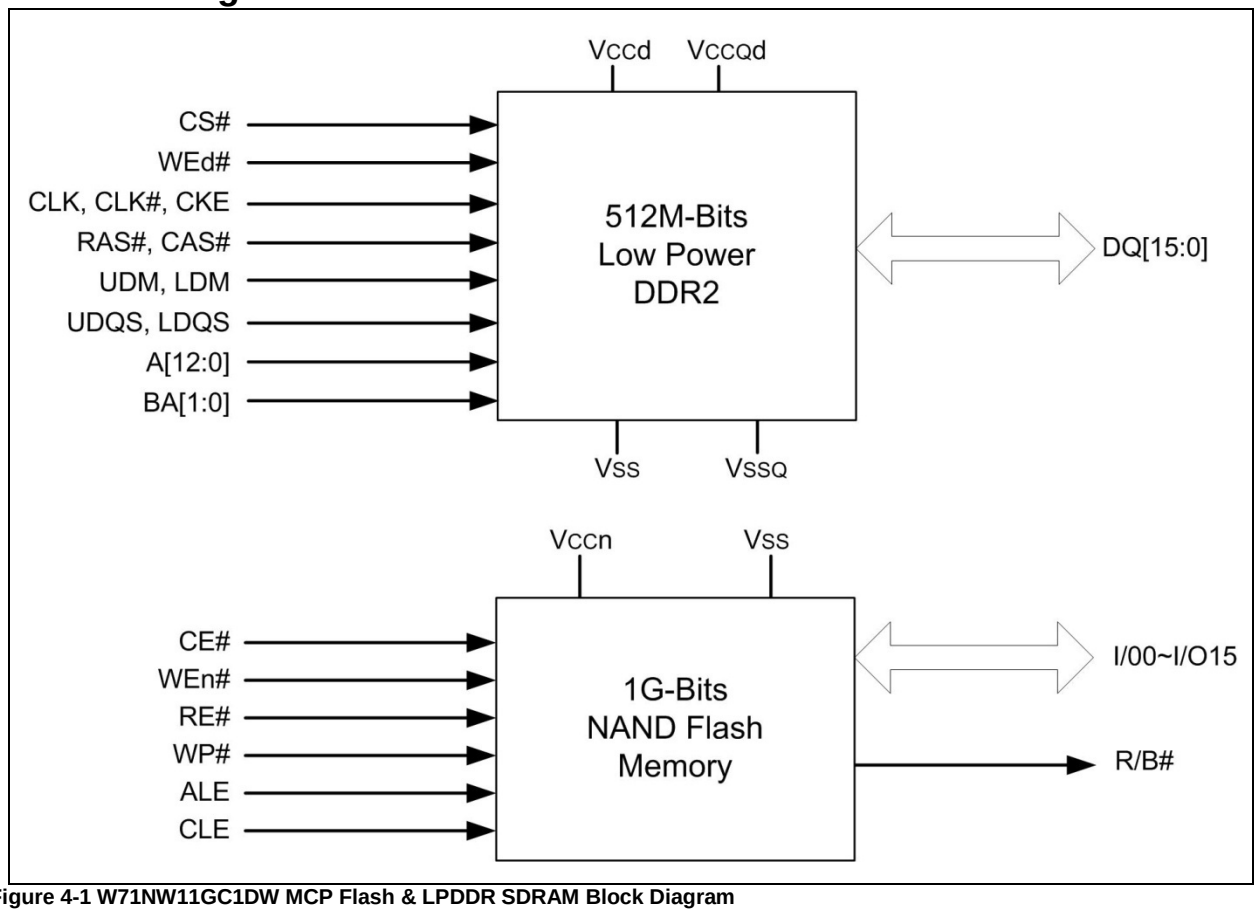
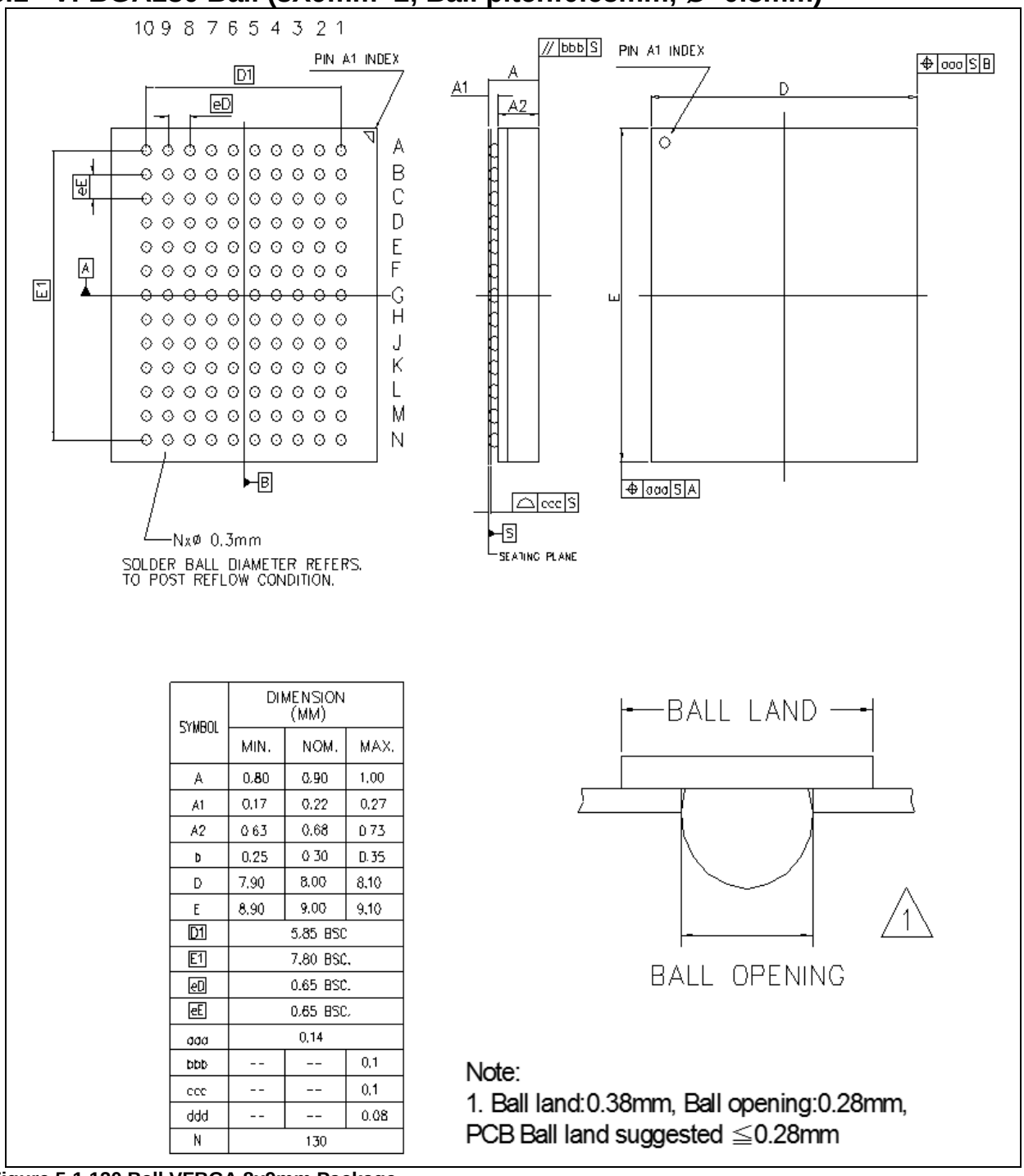


Figure 4-1 W71NW11GC1DW MCP Flash & LPDDR SDRAM Block Diagram

5 Package Specification

5.1 VFBGA130 Ball (8X9mm^2, Ball pitch:0.65mm, Ø=0.3mm)



SYMBOL	DIMENSION (MM)		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.17	0.22	0.27
A2	0.63	0.68	0.73
b	0.25	0.30	0.35
D	7.90	8.00	8.10
E	8.90	9.00	9.10
D1	5.85 BSC		
E1	7.80 BSC.		
eD	0.65 BSC.		
eE	0.65 BSC.		
aaa	0.14		
bbb	--	--	0.1
ccc	--	--	0.1
ddd	--	--	0.08
N	130		

Figure 5-1 130 Ball VFBGA 8x9mm Package

6 MCP ORDERING INFORMATION

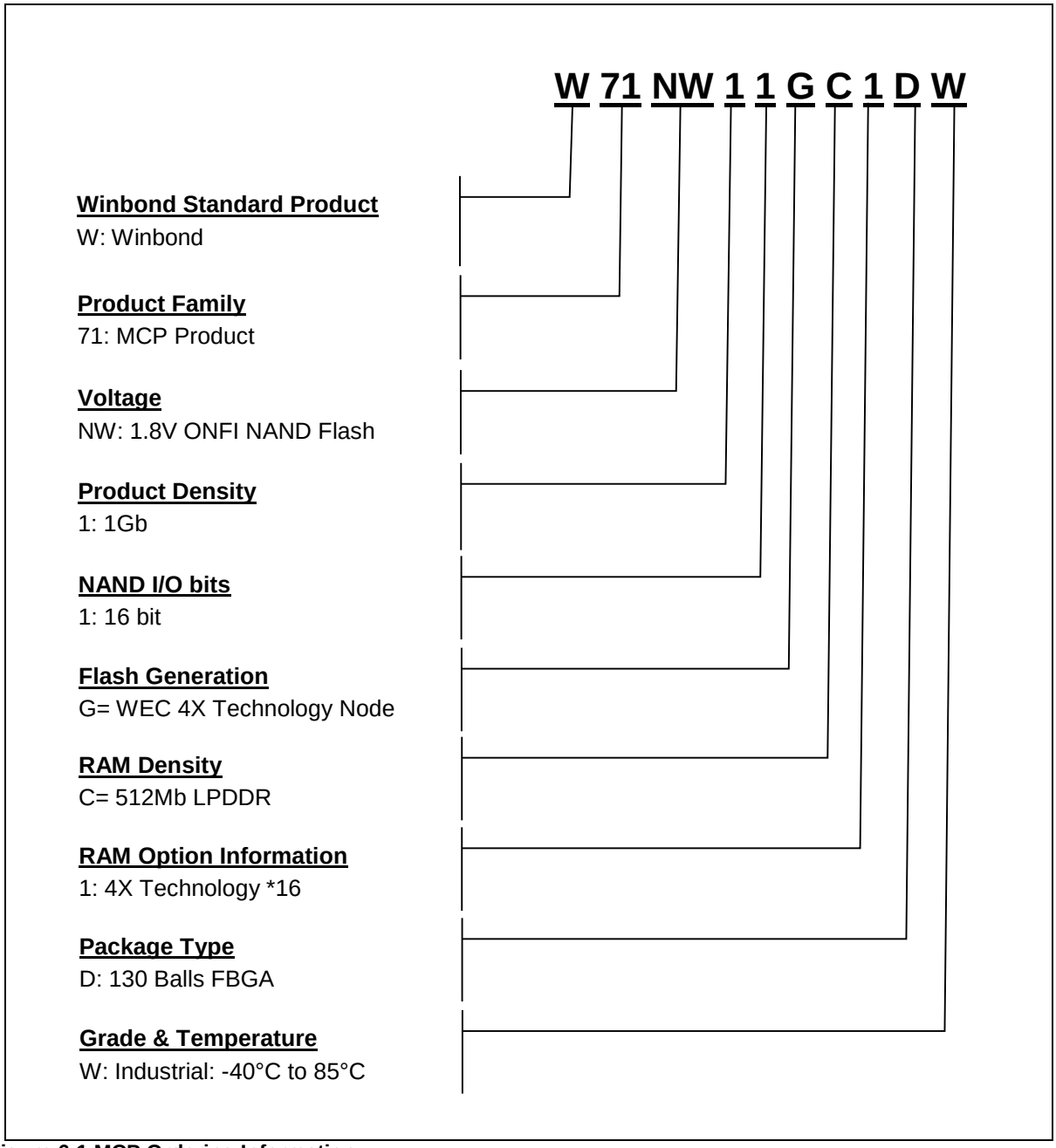


Figure 6-1 MCP Ordering Information

7 Revision History

VERSION	DATE	PAGE	DESCRIPTION
A	11/26/13		New Create Preliminary
B	02/24/14	n/a	Change DDR2 text to DDR
C	09/09/14	5	Updated NAND ball description
D	06/08/15	3 & 10	Temperature Range Correction
E	07/28/2015	9	Update POD

Table 7-1 Revision History

Preliminary Designation

The "Preliminary" designation on a *Winbond* datasheet indicates that the product is not fully characterized. The specifications are subject to change and are not guaranteed. *Winbond* or an authorized sales representative should be consulted for current information before using this product.

Trademarks

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All other marks are the property of their respective owner.

Important Notice

Winbond products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Furthermore, *Winbond* products are not intended for applications wherein failure of *Winbond* products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify *Winbond* for any damages resulting from such improper use or sales.

W29N01GW 16-BIT
W29N01GZ 8-BIT
1G-BIT 1.8V
NAND FLASH MEMORY

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1. GENERAL DESCRIPTION

The W29N01Gx (1G-bit) NAND Flash memory provides a storage solution for embedded systems with limited space, pins and power. It is ideal for code shadowing to RAM, solid state applications and storing media data such as, voice, video, text and photos. The device operates on a single 1.7V to 1.95V power supply with active current consumption as low as 25mA and 10uA for CMOS standby current.

The memory array totals 138,412,032 bytes, and organized into 1,024 erasable blocks of 135,168 bytes. Each block consists of 64 programmable pages of 2,112-bytes each. Each page consists of 2,048-bytes for the main data storage area and 64-bytes for the spare data area (The spare area is typically used for error management functions).

The W29N01GX supports the standard NAND flash memory interface using the multiplexed 8-bit bus to transfer data, addresses, and command instructions. The five control signals, CLE, ALE, #CE, #RE and #WE handle the bus interface protocol. Also, the device has two other signal pins, the #WP (Write Protect) and the RY/#BY (Ready/Busy) for monitoring the device status.

2. FEATURES

- **Basic Features**
  - Density : 1Gbit (Single chip solution)
  - Vcc : 1.7V to 1.95V
  - Bus width : x8 x16
  - Operating temperature
    - Commercial: 0°C to 70°C
    - Industrial: - 40°C to 85°C
- **Single-Level Cell (SLC) technology.**
- **Organization**
  - Density: 1G-bit/128M-byte
  - Page size
    - 2,112 bytes (2048 + 64 bytes)
    - 1,056 words(1024 +32 words)
  - Block size
    - 64 pages (128K + 4K bytes)
    - 64 pages(64K +2K words)
- **Highest Performance**
  - Read performance (Max.)
    - Random read: 25us
    - Sequential read cycle: 35ns
  - Write Erase performance
    - Page program time: 300us(typ.)
    - Block erase time: 2ms(typ.)
  - Endurance 100,000 Erase/Program Cycles(1)
  - 10-years data retention
- **Command set**
  - Standard NAND command set
  - Additional command support
    - Sequential Cache Read
    - Random Cache Read
    - Cache Program
    - Copy Back
    - OTP Data Program
    - OTP Data Lock by Page
    - OTP Data Read
  - Contact Winbond for block Lock feature
- **Lowest power consumption**
  - Read: 10mA(typ.)
  - Program/Erase: 10mA(typ.)
  - CMOS standby: 10uA(typ.)
- **Space Efficient Packaging**
  - 48-ball VFBGA
  - Contact Winbond for stacked packages/KGD

Note:

1. **Endurance specification is based on 1bit/528 byte ECC (Error Correcting Code).**

3. PIN CONFIGURATIONS

3.1 Pin Descriptions

PIN NAME	I/O	FUNCTION
#WP	I	Write Protect
ALE	I	Address Latch Enable
#CE	I	Chip Enable
#WE	I	Write Enable
RY/#BY	O	Ready/Busy
#RE	I	Read Enable
CLE	I	Command Latch Enable
I/O[0-7] I/O[0-15]	I/O	Data Input/Output (x8 x16)
Vcc	Supply	Power supply
Vss	Supply	Ground
DNU	-	Do Not Use: This pins are unconnected pins.
N.C	-	No Connect

Table 3.1 Pin Descriptions

Note:

1. **Connect all Vcc and Vss pins to power supply or ground. Do not leave Vcc or Vss disconnected.**

4. PIN DESCRIPTIONS

4.1 Chip Enable (#CE)

#CE pin enables and disables device operation. When #CE is high the device is disabled and the I/O pins are set to high impedance and enters into standby mode if not busy. When #CE is set low the device will be enabled, power consumption will increase to active levels and the device is ready for Read and Write operations.

4.2 Write Enable (#WE)

#WE pin enables the device to control write operations to input pins of the device. Such as, command instructions, addresses and data that are latched on the rising edge of #WE.

4.3 Read Enable (#RE)

#RE pin controls serial data output from the pre-loaded Data Register. Valid data is present on the I/O bus after the tREA period from the falling edge of #RE. Column addresses are incremented for each #RE pulse.

4.4 Address Latch Enable (ALE)

ALE pin controls address input to the address register of the device. When ALE is active high, addresses are latched via the I/O pins on the rising edge of #WE.

4.5 Command Latch Enable (CLE)

CLE pin controls command input to the command register of the device. When CLE is active high, commands are latched into the command register via I/O pins on the rising edge of #WE.

4.6 Write Protect (#WP)

#WP pin can be used to prevent the inadvertent program/erase to the device. When #WP pin is active low, all program/erase operations are disabled.

4.7 Ready/Busy (RY/#BY)

RY/#BY pin indicates the device status. When RY/#BY output is low, it indicates that the device is processing either a program, erase or read operations. When it returns to high, those operations have completed. RY/#BY pin is an open drain.

4.8 Input and Output (I/Ox)

I/Ox bi-directional pins are used for the following; command, address and data operations.

5. BLOCK DIAGRAM

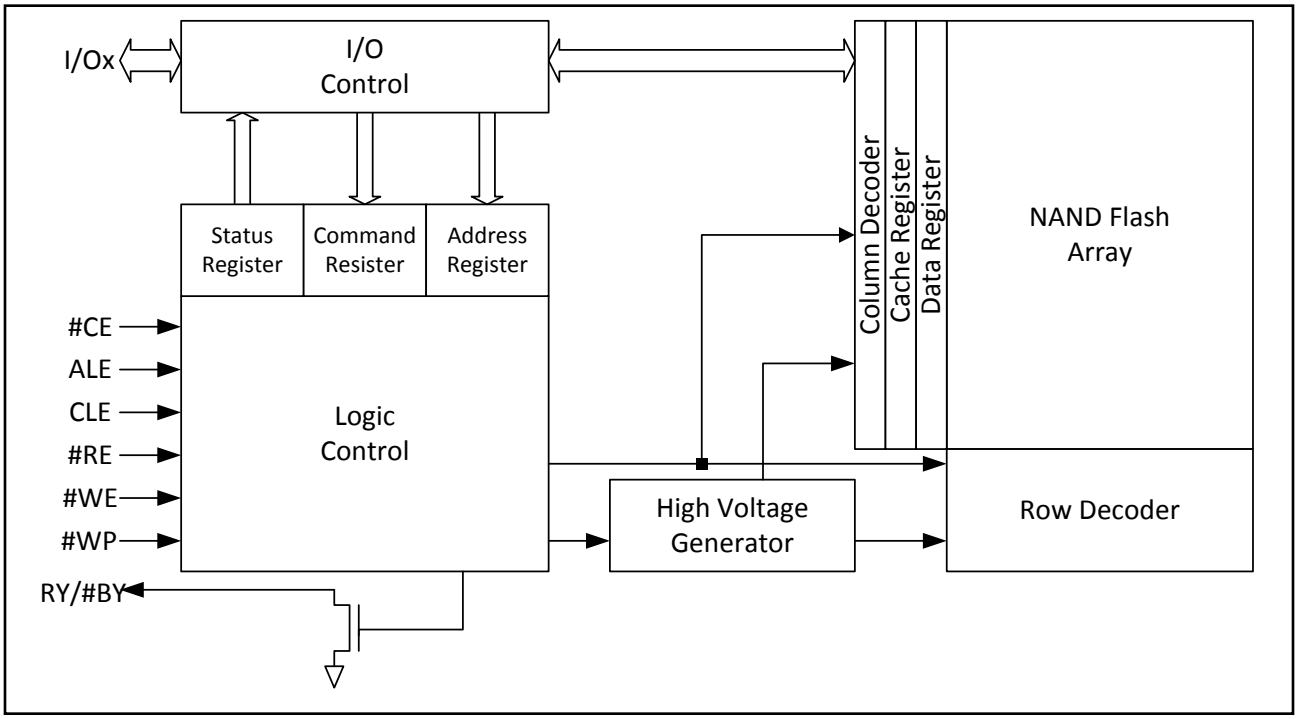


Figure 5-1 NAND Flash Memory Block Diagram

6. MEMORY ARRAY ORGANIZATION

6.1 X8 Array Organization

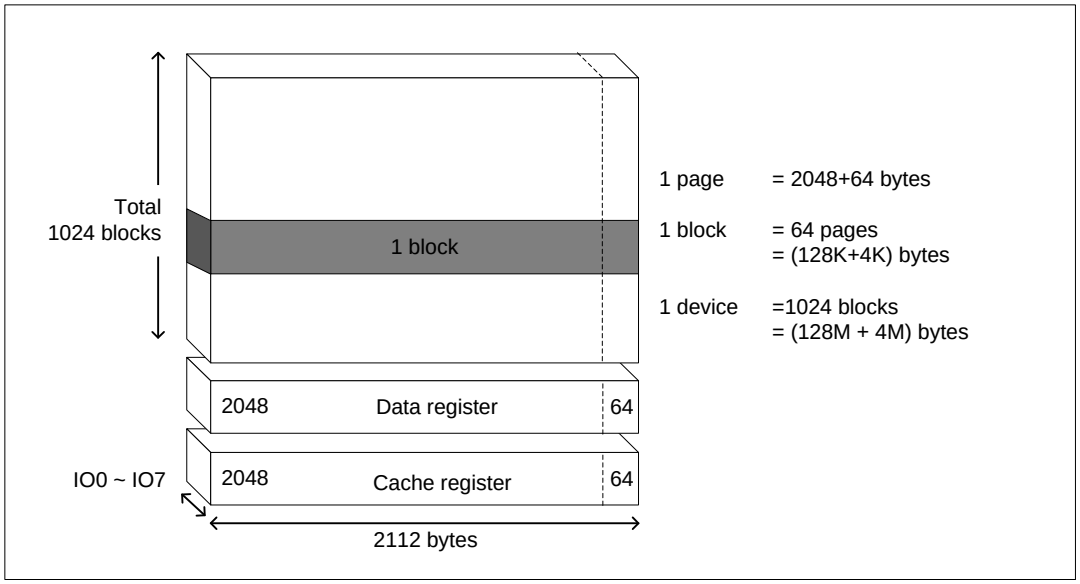


Figure 6-1 Array Organization(X8)

	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st cycle	A7	A6	A5	A4	A3	A2	A1	A0
2nd cycle	L	L	L	L	A11	A10	A9	A8
3rd cycle	A19	A18	A17	A16	A15	A14	A13	A12
4th cycle	A27	A26	A25	A24	A23	A22	A21	A20

Table 6.1 Addressing(X8)

Notes:

1. **"L" indicates a low condition, which must be held during the address cycle to insure correct processing.**
2. **A0 to A11 during the 1st and 2nd cycles are column addresses. A12 to A27 during the 3rd and 4th cycles are row addresses.**
3. **The device ignores any additional address inputs that exceed the device's requirement.**

6.2 X16 Array Organization

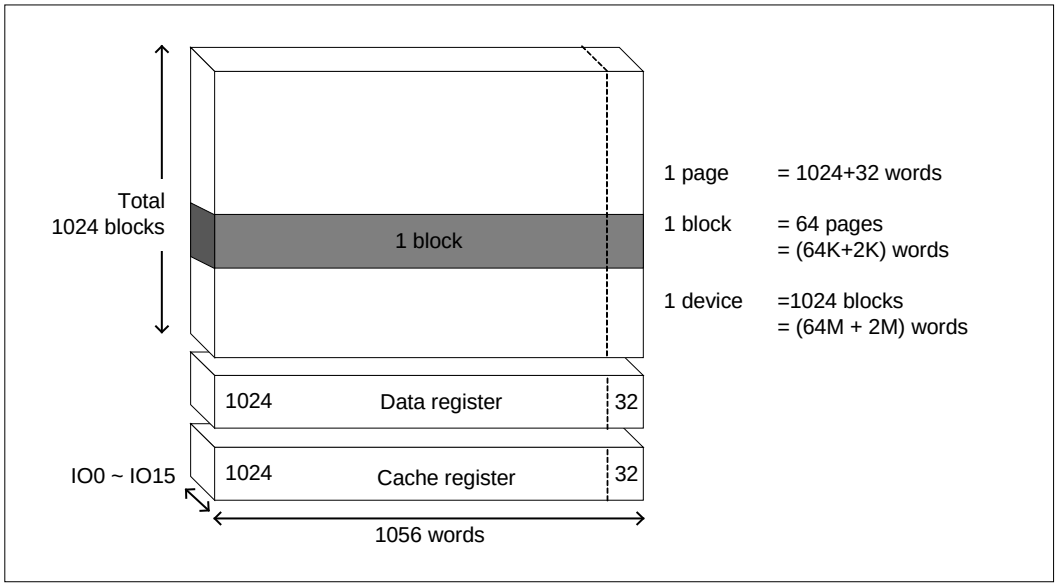


Figure 6-2 Array Organization(X16)

	I/O8~15	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st cycle	L	A7	A6	A5	A4	A3	A2	A1	A0
2nd cycle	L	L	L	L	L	L	A10	A9	A8
3rd cycle	L	A18	A17	A16	A15	A14	A13	A12	A11
4th cycle	L	A26	A25	A24	A23	A22	A21	A20	A19

Table 6.2 Addressing(X16)

NOTE

*** "L" must to be held Low during the address cycle is inputted**

*** A0 to A10 of 1st and 2nd cycle are column address, A11 to A26 of 3rd and 4th cycle are row address**

*** The device ignores any additional address input than the device is required**

7. MODE SELECTION TABLE

MODE		CLE	ALE	#CE	#WE	#RE	#WP
Read mode	Command input	H	L	L		H	X
	Address input	L	H	L		H	X
Write mode	Command input	H	L	L		H	H
	Address input	L	H	L		H	H
Data input		L	L	L		H	H
Sequential Read and Data output		L	L	L	H		X
During read (busy)		X	X	X	X	H	X
During program (busy)		X	X	X	X	X	H
During erase (busy)		X	X	X	X	X	H
Write protect		X	X	X	X	X	L
Standby		X	X	H	X	X	0V/Vcc

Table 7.1 Mode Selection

Notes:

1. **"H" indicates a HIGH input level, "L" indicates a LOW input level, and "X" indicates a Don't Care Level.**
2. **#WP should be biased to CMOS HIGH or LOW for standby.**

8. COMMAND TABLE

COMMAND	1st CYCLE	2nd CYCLE	Acceptable during busy
PAGE READ	00h	30h	
READ for COPY BACK	00h	35h	
SEQUENTIAL CACHE READ	31h		
RANDOM CACHE READ	00h	31h	
LAST ADDRESS CACHE READ	3Fh		
READ ID	90h		
READ STATUS	70h		Yes
RESET	FFh		Yes
PAGE PROGRAM	80h	10h	
PROGRAM for COPY BACK	85h	10h	
CACHE PROGRAM	80h	15h	
BLOCK ERASE	60h	D0h	
RANDOM DATA INPUT(1)	85h		
RANDOM DATA OUTPUT(1)	05h	E0h	
READ PARAMETER PAGE	ECh		
READ UNIQUE ID	EDh		
GET FEATURES	EEh		
SET FEATURES	EFh		
OTP DATA PROTECT	A5h	10h	
OTP DATA PROGRAM	A0h	10h	
OTP DATA READ	AFh	30h	

Table 8.1 Command Table

Notes:

1. **RANDOM DATA INPUT and RANDOM DATA OUTPUT command is only to be used within a page.**
2. **Any commands that are not in the above table are considered as undefined and are prohibited as inputs.**

9. DEVICE OPERATIONS

9.1 READ operation

9.1.1 PAGE READ (00h-30h)

When the device powers on, the default is READ mode. This operation can also be entered by writing 00h command to the command register, and then write four address cycles, followed by writing 30h command. After writing 30h command, the data is transferred from NAND array to Data Register during tR. Data transfer progress can be done by monitoring the status of the RY/#BY signal output. RY/#BY signal will be LOW during data transfer. Also, there is an alternate method by using the READ STATUS (70h) command. If the READ STATUS command is issued during read operation, the Read (00h) command must be re-issued to read out the data from Data Register. When the data transfer is complete, RY/#BY signal goes HIGH, and the data can be read from Data Register by toggling #RE. Read is sequential from initial column address to the end of the page. (See Figure 9-1)

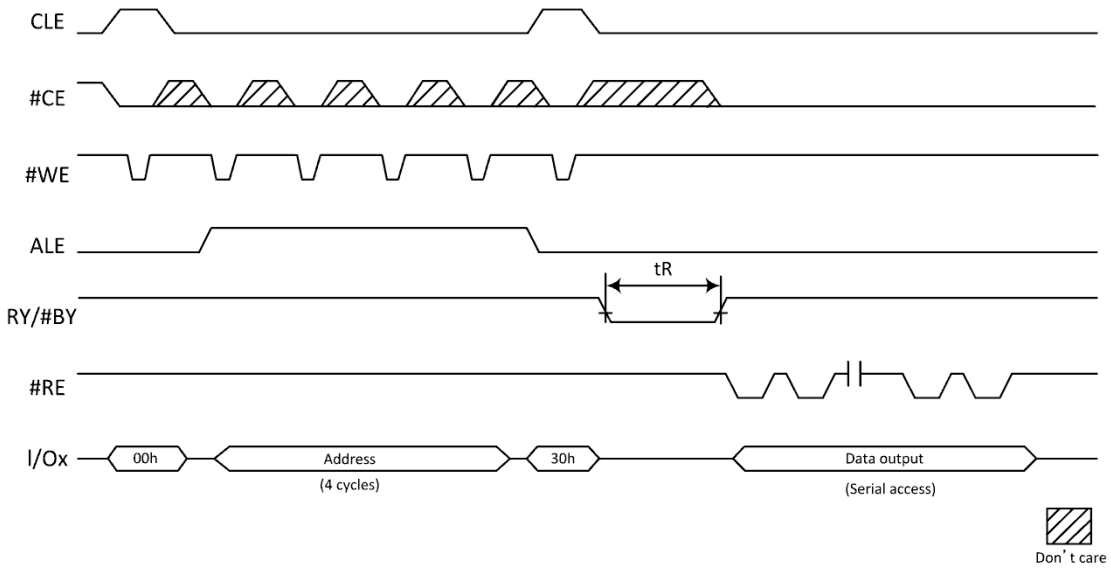


Figure 9-1 Page Read Operations

9.1.2 CACHE READ OPERATIONS

To obtain a higher degree of performance read operations, the device's Cache and Data Register can be used independent of each other. Data can be read out from the Cache Register, while array data is transferred from the NAND Array to the Data Register.

The CACHE READ mode starts with issuing a PAGE READ command (00h-30h) to transfer a page of data from NAND array to the Cache Register. RY/#BY signal will go LOW during data transfer indicating a busy status. Copying the next page of data from the NAND array to the Data Register while making the Cache Register page data available is done by issuing either a SEQUENTIAL CACHE READ (31h) or RANDOM CACHE READ (00h-31h) command. The SEQUENTIAL CACHE READ mode will copy the next page of data in sequence from the NAND array to the Data Register or use the RANDOM CACHE READ mode (00h-31h) to copy a random page of data from NAND array to the Data Register. The RY/#BY signal goes LOW for a period of tRCBSY during the page data transfer from NAND array to the Data Register. When RY/#BY goes HIGH, this means that the Cache Register data is available and can be read out of the Cache Register by toggling #RE, which starts at address column 0. If it is desired to start at a different column address, a RANDOM DATA OUTPUT (05h-E0h) command can be used to change the column address to read out the data.

At this point in the procedure when completing the read of the desired number of bytes, one of two things can be chosen. Continue CACHE READ (31h or 00h-31h) operations or end the CACHE READ mode with a LAST ADDRESS CACHE READ (3Fh) command.

To continue with the read operations, execute the CACHE READ (31h or 00h-31h) command. The RY/#BY signal goes LOW for the period of tRCBSY while data is copied from Data Register to the Cache Register and the next page of data starts being copied from the NAND array to the Data Register. When RY/#BY signal goes HIGH signifying that the Cache Register data is available, at this time #RE can start toggling to output the desired data starting at column 0 address or using the RANDOM DATA OUPUT command for random column address access.

To terminate the CACHE READ operations a LAST ADDRESS CACHE READ (3Fh) command is issued, RY/#BY signal goes LOW and the Data Register contents is copied to the Cache Register. At the completion of the Data Register to Cache Register transfer, RY/#BY goes HIGH indicating data is available at the output of the Cache Register. At this point Data can be read by toggling #RE starting at column address 0 or using the RANDOM DATA OUPUT command for random column address access. The device NAND array is ready for next command set.

9.1.2.1. SEQUENTIAL CACHE READ (31h)

The SEQUENTIAL CACHE READ (31h) copies the next page of data in sequence within block to the Data Register while the previous page of data in the Cache Register is available for output. This is done by issuing the command (31h), RY/#BY signal goes LOW and the STATUS REGISTER bits 6 and 5 = “00” for the period of tRCBSY. When RY/#BY signal goes HIGH and STATUS REGISTER bits 6 and 5 = “10”, data at the Cache Register is available. The data can be read out from the Cache Register by toggling #RE, starting address is column 0 or by using the RANDOM DATA OUPUT command for random column address access.

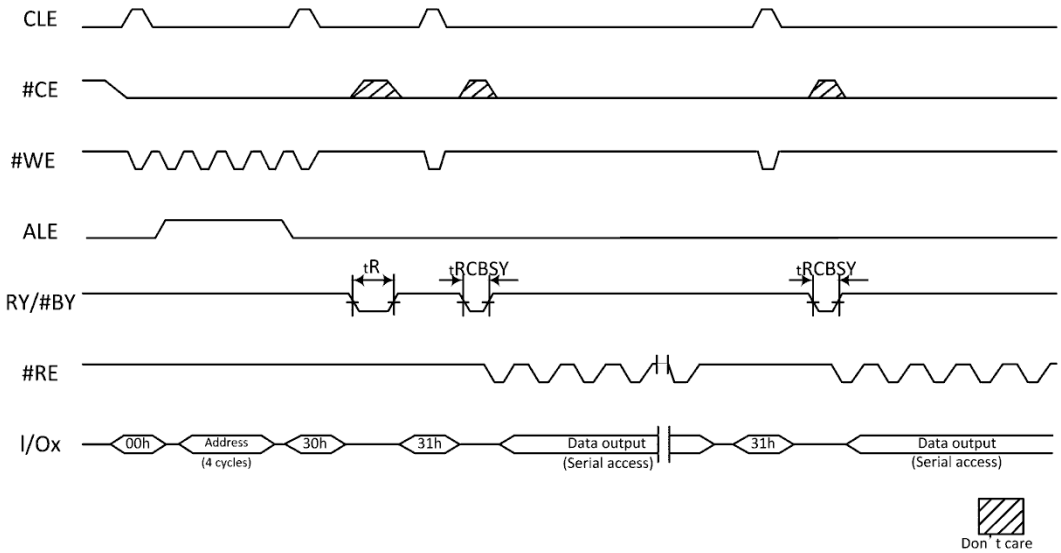


Figure 9-2 Sequential Cache Read Operations

9.1.2.2. RANDOM CACHE READ (00h-31h)

The RANDOM CACHE READ (00h-31h) will copy a particular page from NAND array to the Data Register while the previous page of data is available at the Cache Register output. Perform this function by first issuing the 00h command to the Command Register, then writing the four address cycles for the desired page of data to the Address Register. Then write the 31h command to the Command Register. Note; the column address bits are ignored.

After the RANDOM CACHE READ command is issued, RY/#BY signal goes LOW and STATUS REGISTER bits 6 and 5 equal “00” for the period of tRCBSY. When RY/#BY signal goes HIGH and STATUS REGISTER bits 6 and 5 equal “10”, the page data in the Cache Register is available. The data can read out from the Cache Register by toggling #RE, the starting column address will be 0 or use the RANDOM DATA OUTPUT (05h-E0h) command change the column address to start reading out the data.

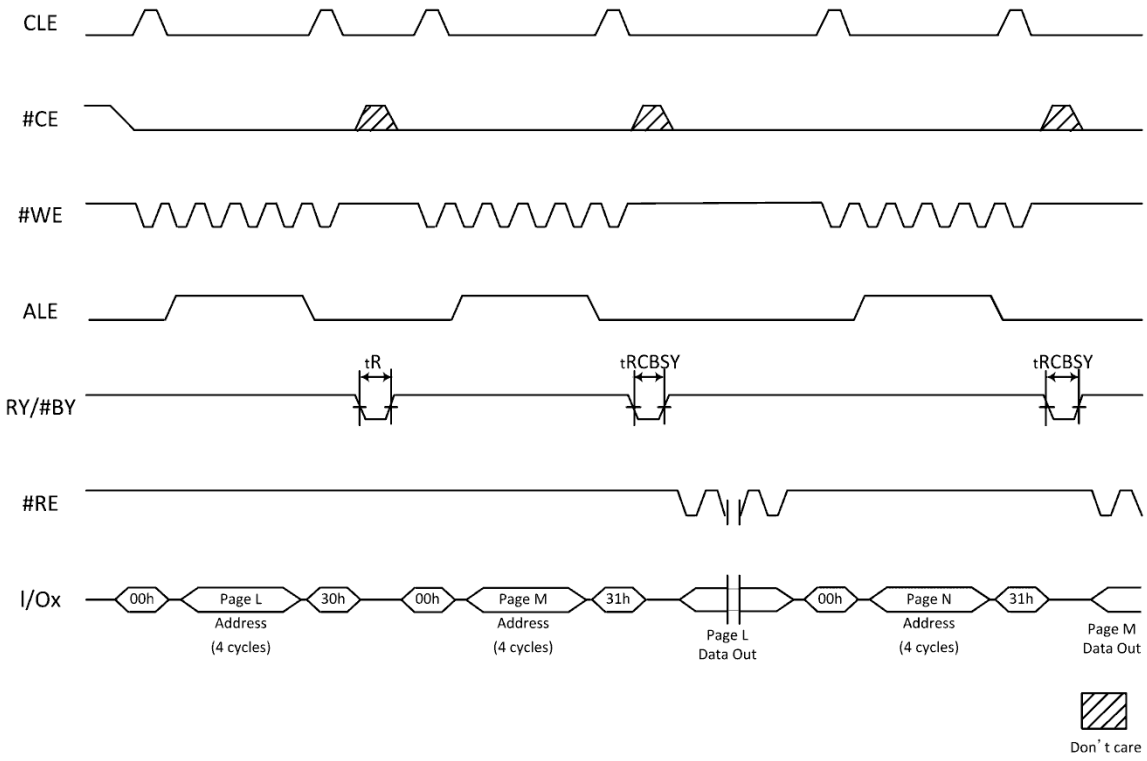


Figure 9-3 Random Cache Read Operation

9.1.2.3. LAST ADDRESS CACHE READ (3Fh)

The LAST ADDRESS CACHE READ (3Fh) copies a page of data from the Data Register to the Cache Register without starting the another cache read. After writing the 3Fh command, RY/#BY signal goes LOW and STATUS REGISTER bits 6 and 5 equals “00” for the period of tRCBSY. When RY/#BY signal goes HIGH and STATUS REGISTER bits 6 and 5 equals “11”, the Cache Register data is available, and the device NAND array is in ready state. The data can read out from the Cache Register by toggling #RE, starting at address column 0 or RANDOM DATA OUTPUT (05h-E0h) command to change the column address to read out the data.

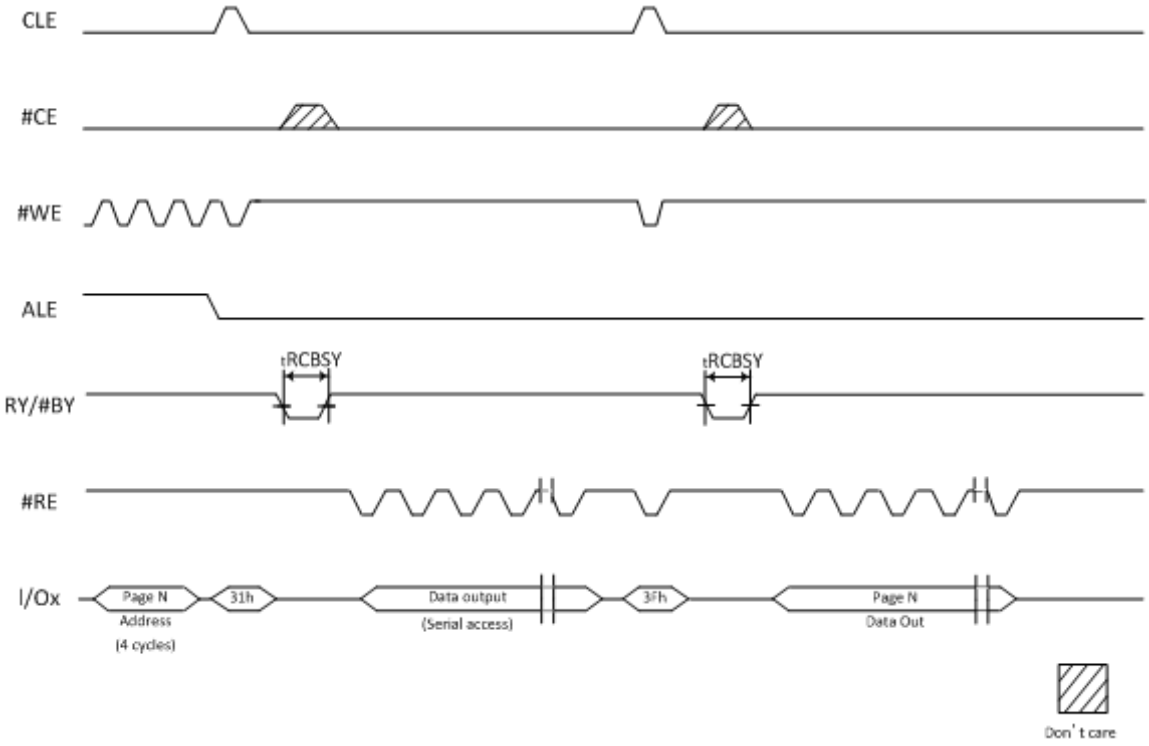


Figure 9-4 Last Address Cache Read Operation

9.1.3 RANDOM DATA OUTPUT (05h-E0h)

The RANDOM DATA OUTPUT allows the selection of random column addresses to read out data from a single or multiple of addresses. The use of the RANDOM DATA OUTPUT command is available after the PAGE READ (00h-30h) sequence by writing the 05h command following by the 2 cycle column address and then the E0h command. Toggling #RE will output data sequentially. The RANDOM DATA OUTPUT command can be issued multiple times, but limited to the current loaded page.

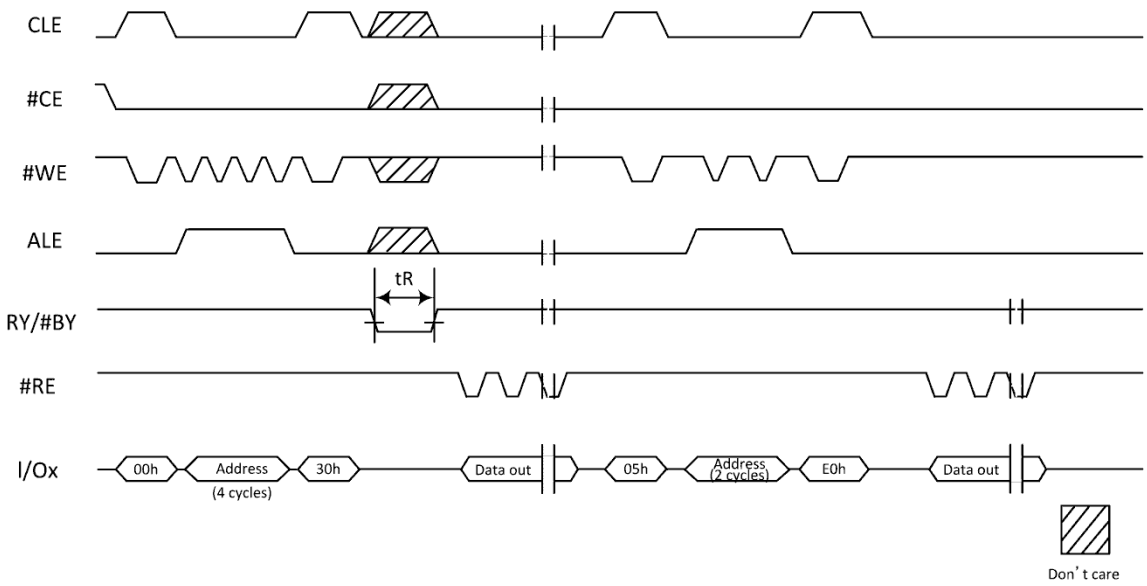


Figure 9-5 Random Data Output

9.1.4 READ ID (90h)

READ ID command is comprised of two modes determined by the input address, device (00h) or ONFI (20h) identification information. To enter the READ ID mode, write 90h to the Command Register followed by a 00h address cycle, then toggle #RE for 5 single byte cycles, the W29N01Gx pre-programmed code includes the Manufacturer ID, Device ID, and Product-Specific Information (see Table 9.1). If the READ ID command is followed by 20h address, the output code includes 4 single byte cycles of ONFI identifying information (see Table 9.2). The device remains in the READ ID mode until the next valid command is issued.

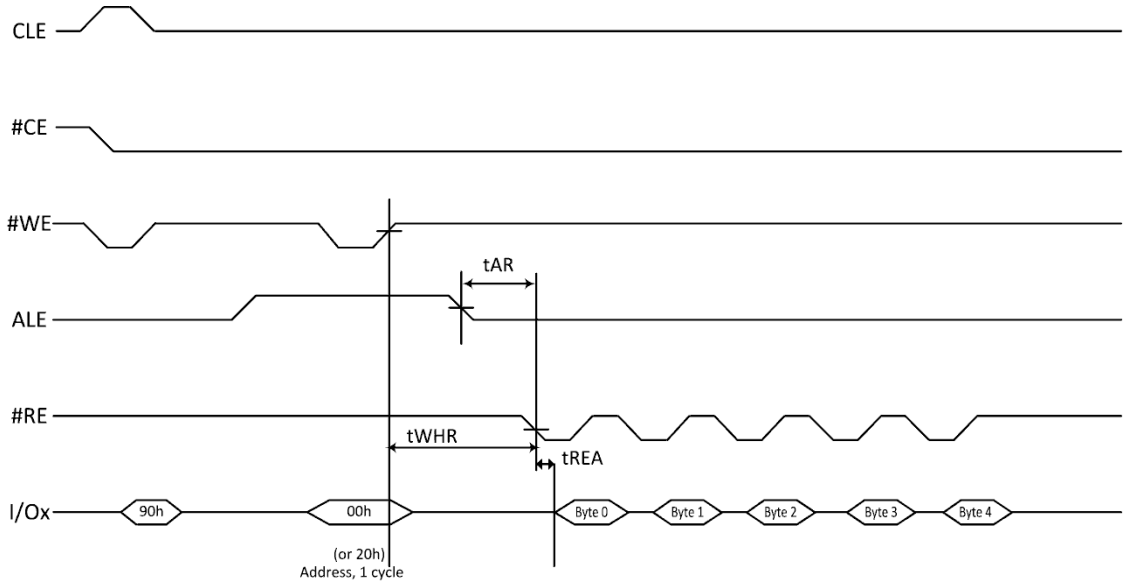


Figure 9-6 Read ID

# of Byte/Cycles	1st Byte/Cycle	2nd Byte/Cycle	3rd Byte/Cycle	4th Byte/Cycle	5th Byte/Cycle
X8	EFh	A1h	80h	15h.	00h.
X16	EFh	B1h	80h	55h	00h
Description	MFR ID	Device ID	Cache Programming Supported	Page Size:2KB Spare Area Size:64b BLK Size w/o Spare:128KB Organized:X8 X16 Serial Access:35ns	

Table 9.1 Device ID and configuration codes for Address 00h

# of Byte/Cycles	1st Byte/Cycle	2nd Byte/Cycle	3rd Byte/Cycle	4th Byte/Cycle
Code	4Fh	4Eh	46h	49h

Table 9.2 ONFI identifying codes for Address 20h

9.1.5 READ PARAMETER PAGE (ECh)

READ PARAMETER PAGE can read out the device's parameter data structure, such as, manufacturer information, device organization, timing parameters, key features, and other pertinent device parameters. The data structure is stored with at least three copies in the device's parameter page. Figure 9-7 shows the READ PARAMETER PAGE timing. The RANDOM DATA OUTPUT (05h-E0h) command is supported during data output.

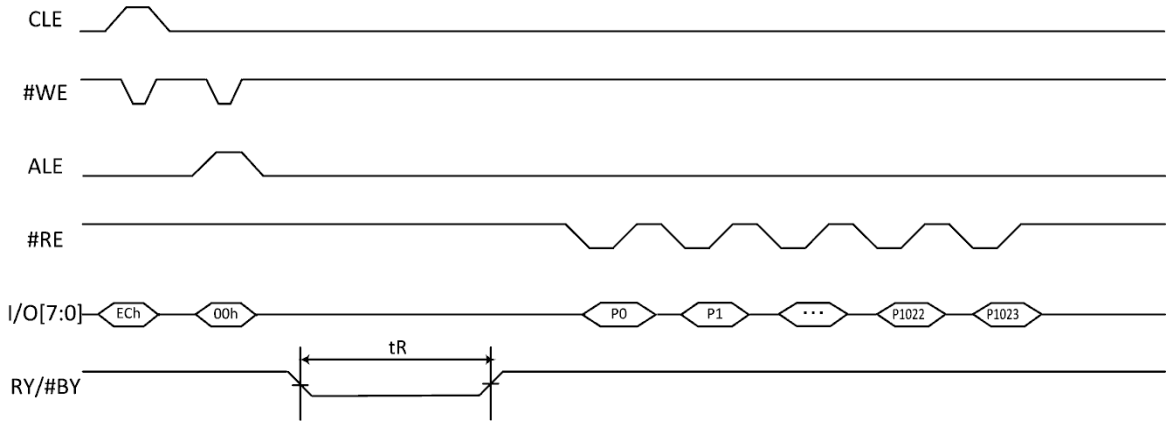


Figure 9-7 Read Parameter Page

Byte	Description		Value
0-3	Parameter page signature		4Fh, 4Eh, 46h, 49h
4-5	Revision number		02h, 00h
6-7	Features supported	W29N01GZ (x8) W29N01GW (x16)	10h, 00h 11h, 00h
8-9	Optional commands supported		37h, 00h
10-31	Reserved		00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
32-43	Device manufacturer		57h, 49h, 4Eh, 42h, 4Fh, 4Eh, 44h, 20h, 20h, 20h, 20h, 20h
44-63	Device model	W29N01GZ (x8)	57h, 32h, 39h, 4Eh, 30h, 31h, 47h, 5Ah, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
		W29N01GW(X16)	57h, 32h, 39h, 4Eh, 30h, 31h, 47h, 57h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h
64	Manufacturer ID		EFh
65-66	Date code		00h, 00h
67-79	Reserved		00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
80-83	# of data bytes per page		00h, 08h, 00h, 00h
84-85	# of spare bytes per page		40h, 00h
86-89	# of data bytes per partial page		00h, 02h, 00h, 00h
90-91	# of spare bytes per partial page		10h, 00h

Byte	Description	Value
92-95	# of pages per block	40h, 00h, 00h, 00h
96-99	# of blocks per unit	00h, 04h, 00h, 00h
100	# of logical units	01h
101	# of address cycles	22h
102	# of bits per cell	01h
103-104	Bad blocks maximum per unit	14h, 00h
105-106	Block endurance	01h, 05h
107	Guaranteed valid blocks at beginning of target	01h
108-109	Block endurance for guaranteed valid blocks	00h, 00h
110	# of programs per page	04h
111	Partial programming attributes	00h
112	# of ECC bits	01h
113	# of interleaved address bits	00h
114	Interleaved operation attributes	00h
115-127	Reserved	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
128	I/O pin capacitance	0Ah
129-130	Timing mode support	07h, 00h
131-132	Program cache timing	07h, 00h
133-134	Maximum page program time	BCh, 02h
135-136	Maximum block erase time	10h, 27h
137-138	Maximum random read time	19h, 00h
139-140	tCCS minimum	46h, 00h
141-163	Reserved	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
164-165	Vendor specific revision #	01h,00h
166-253	Vendor specific	00h
254-255	Integrity CRC	Set at shipment
256-511	Value of bytes 0-255	
512-767	Value of bytes 0-255	
>767	Additional redundant parameter pages	

Table 9.3 Parameter Page Output Value

9.1.6 READ STATUS (70h)

The W29N01GX has an 8-bit Status Register which can be read during device operation. Refer to Table 9.3 for specific Status Register definitions. After writing 70h command to the Command Register, read cycles will only read from the Status Register. The status can be read from I/O[7:0] outputs, as long as #CE and #RE are LOW. Note; #RE does not need to be toggled for Status Register read. The Command Register remains in status read mode until another command is issued. To change to normal read mode, issue the PAGE READ (00h) command. After the PAGE READ command is issued, data output starts from the initial column address.

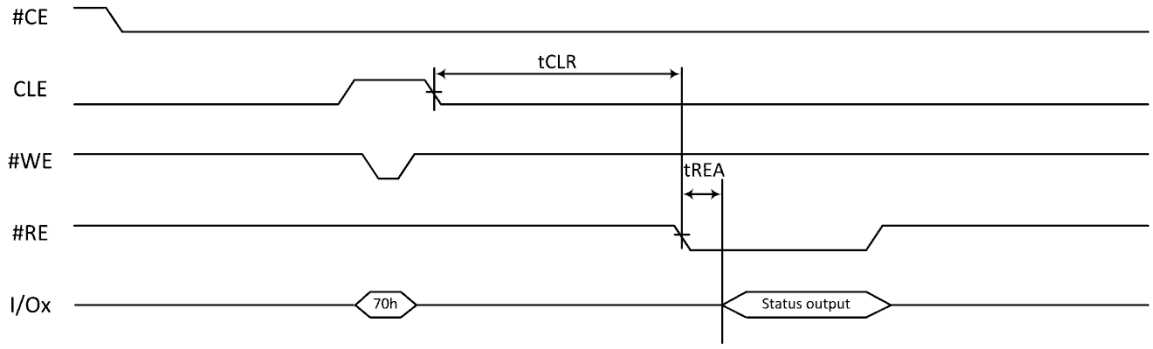


Figure 9-8 Read Status Operation

SR bit	Page Read	Cache Read	Page Program	Cache Program	Block Erase	Definition
I/O 0	Not Use	Not Use	Pass/Fail	Pass/Fail(N)	Pass/Fail	0=Successful Program/Erase 1=Error in Program/Erase
I/O 1	Not Use	Not Use	Not Use	Pass/Fail(N-1)	Not Use	0=Successful Program 1=Error in Program
I/O 2	Not Use	Not Use	Not Use	Not Use	Not Use	0
I/O 3	Not Use	Not Use	Not Use	Not Use	Not Use	0
I/O 4	Not Use	Not Use	Not Use	Not Use	Not Use	0
I/O 5	Ready/Busy	Ready/Busy[1]	Ready/Busy	Ready/Busy	Ready/Busy	Ready = 1 Busy = 0
I/O 6	Ready/Busy	Cache Ready/Busy[2]	Ready/Busy	Cache Ready/Busy	Ready/Busy	Ready = 1 Busy = 0
I/O 7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Unprotected = 1 Protected = 0

Table 9.4 Status Register Bit Definition

Notes:

1. **SR bit 5 is 0 during the actual programming operation. If cache mode is used, this bit will be 1 when all internal operations are complete.**
2. **SR bit 6 is 1 when the Cache Register is ready to accept new data. RY/#BY follows bit 6.**

9.1.7 READ UNIQUE ID (EDh)

The W29N01GX NAND Flash device has a method to uniquely identify each NAND Flash device by using the READ UNIQUE ID command. The format of the ID is limitless, but the ID for every NAND Flash device manufactured, will be guaranteed to be unique.

Numerous NAND controllers typically use proprietary error correction code (ECC) schemes. In these cases Winbond cannot protect unique ID data with factory programmed ECC. However, to ensure data reliability, Winbond will program the NAND Flash devices with 16 bytes of unique ID code, starting at byte 0 on the page, immediately followed by 16 bytes of the complement of that unique ID. The combination of these two actions is then repeated 16 times. This means the final copy of the unique ID will resides at location byte 511. At this point an XOR or exclusive operation can be performed on the first copy of the unique ID and its complement. If the unique ID is good, the results should yield all the bits as 1s. In the event that any of the bits are 0 after the XOR operation, the procedure can be repeated on a subsequent copy of the unique ID data.

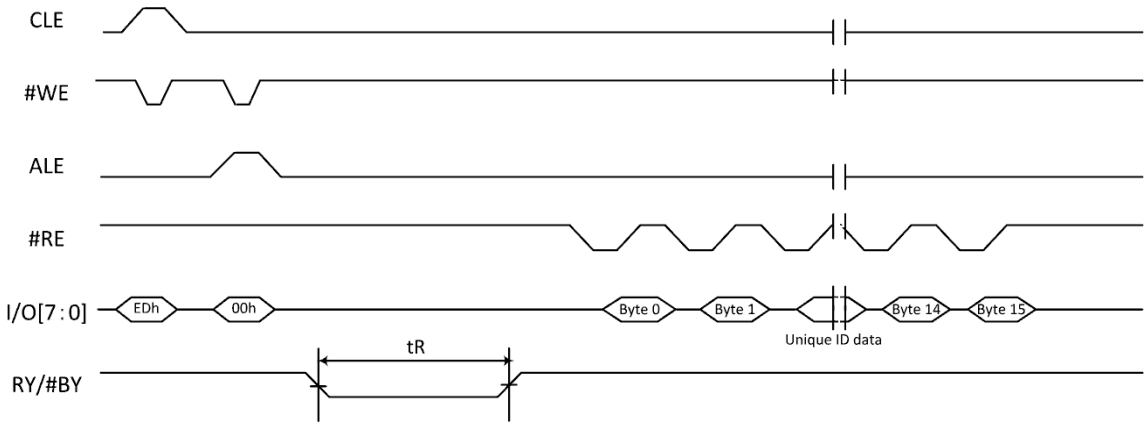


Figure 9-9 Read Unique ID

9.2 PROGRAM operation

9.2.1 PAGE PROGRAM (80h-10h)

The W29N01Gx Page Program command will program pages sequentially within a block, from the lower order page address to higher order page address. Programming pages out of sequence is prohibited. The W29N01GX supports partial-page programming operations up to 4 times before an erase is required if partitioning a page. Note; programming a single bit more than once without first erasing it is not supported.

9.2.2 SERIAL DATA INPUT (80h)

Page Program operation starts with the execution of the Serial Data Input command (80h) to the Command Register, following next by inputting four address cycles and then the data is loaded. Serial data is loaded to Cache Register with each #WE cycle. The Program command (10h) is written to the Command Register after the serial data input is finished. At this time the internal write state controller automatically executes the algorithms for program and verifies operations. Once the programming starts, determining the completion of the program process can be done by monitoring the RY/#BY output or the Status Register Bit 6, which will follow the RY/#BY signal. RY/#BY will stay LOW during the internal array programming operation during the period of (tPROG). During page program operation, only two commands are available, READ STATUS (70h) and RESET (FFh). When the device status goes to the ready state, Status Register Bit 0 (I/O0) indicates whether the program operation passed (Bit0=0) or failed (Bit0=1), (see Figure 9-10). The Command Register remains in read status mode until the next command is issued.

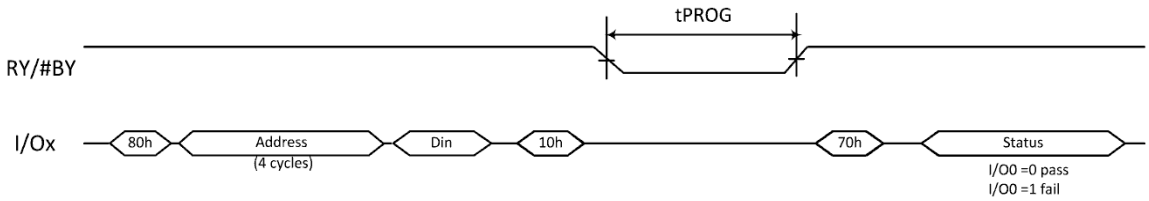


Figure 9-10 Page Program

9.2.3 RANDOM DATA INPUT (85h)

After the Page Program (80h) execution of the initial data has been loaded into the Cache Register, if the need for additional writing of data is required, using the RANDOM DATA INPUT (85h) command can perform this function to a new column address prior to the Program (10h) command. The RANDOM Data INPUT command can be issued multiple times in the same page (See Figure 9-11).

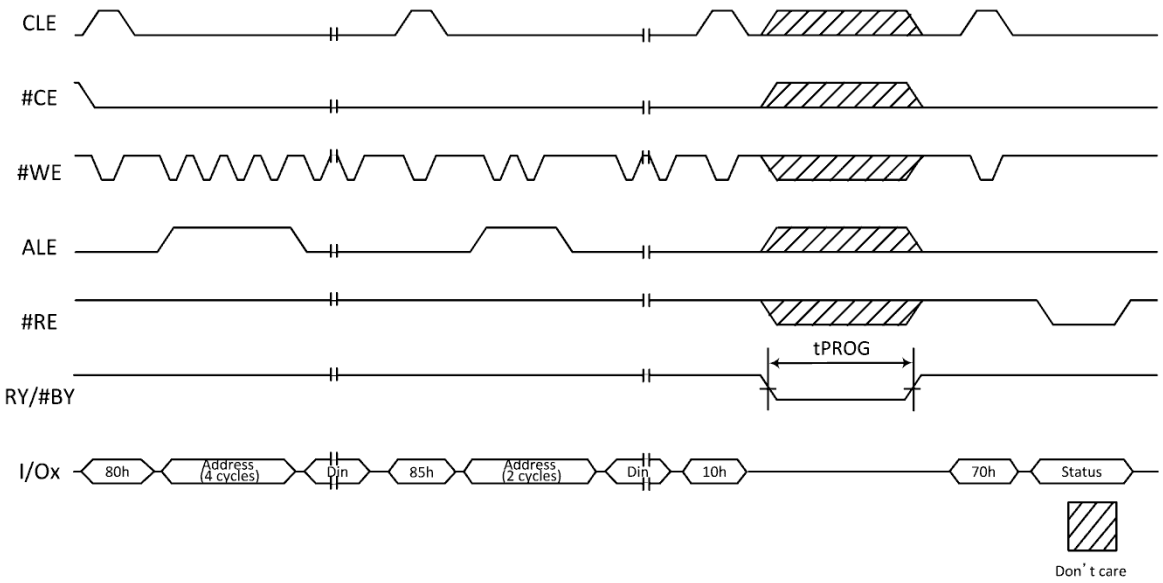


Figure 9-11 Random Data Input

9.2.4 CACHE PROGRAM (80h-15h)

CACHE PROGEAM (80h) command is started by writing the command to the Command Register. The next writes should be four cycles of address, and then either writing a full or partial page of input data into the Cache Register. Issuing the CACHE PROGRAM (15h) command to the Command Register, starting transferring data from the Cache Register to the Data Register on the rising edge of #WE and RY/#BY will go LOW. Programming to the array starts after the data has been copied into the Data Register and RY/#BY returns to HIGH.

When RY/#BY returns to HIGH, the next input data can be written to the Cache Register by issuing another CACHE PROGRAM command series. The time RY/#BY goes LOW, is typical controlled by the actual programming time. The time for the first programming pass equals the time it takes to transfer the data from the Cache Register to the Data Register. On the second and subsequent programming passes, data transfer from the Cache Register to the Data Register is held until Data Register content is programming into the NAND array.

The CACHE PROGRAM command can cross block address boundaries. RANDOM DATA INPUT (85h) commands are permitted with CACHE PROGRAM operations. Status Register's Cache RY/#BY Bit 6 (I/O6) can be read after issuing the READ STATUS (70h) command for confirming when the Cache Register is ready or busy. RY/#BY, always follows Status Register Bit 6 (I/O6). Status Register's RY/#BY Bit 5 (I/O5) can be polled to determine whether the array programming is in progress or completed for the current programming cycle.

If only RY/#BY is used for detecting programming status, the last page of the program sequence must use the PAGE PROGRAM (10h) command instead of the CACHE PROGRAM (15h) command. If the

CACHE PROGRAM (15h) command is used every time, including the last page programming, Status Register's Bit 5 (I/O5) must be used to determine when programming is complete.

Status Register's Pass/Fail, Bit 0 (I/O0) returns the pass/fail status for the previous page when Status Register's Bit 6 (I/O6) equals a "1" (ready state). The pass/fail status of the current PROGRAM operation is returned with Status Register's Bit 0 (I/O0) when Bit 5 (I/O5) of the Status Register equals a "1" (ready state) as shown in Figure 9-12 and 9-13.

Note: The CACHE PROGRAM command cannot be used on blocks 0-3 if used as boot blocks.

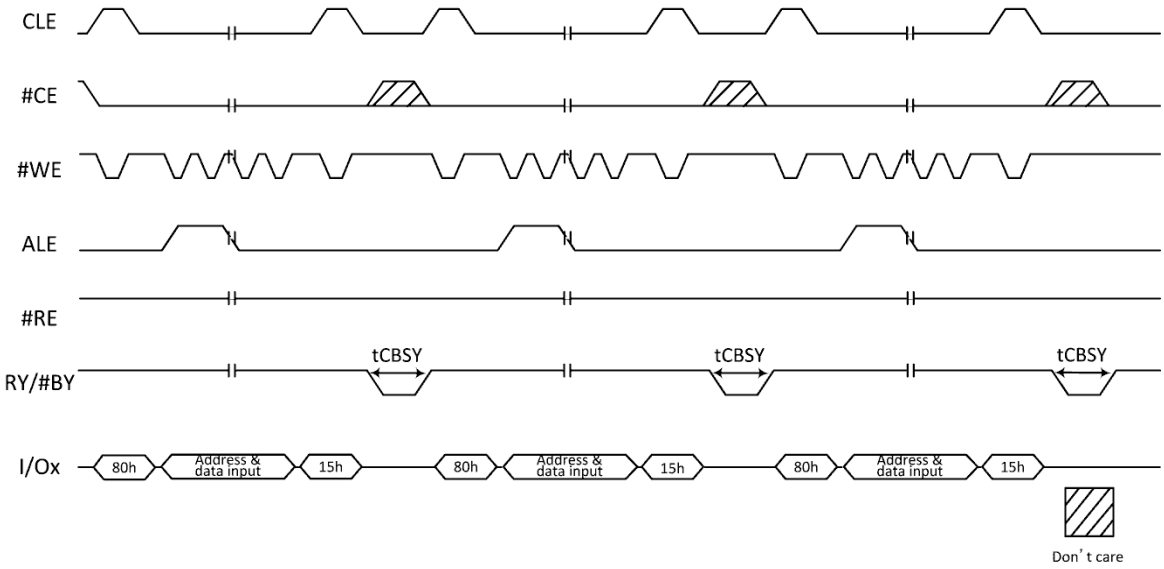


Figure 9-12 Cache Program Start

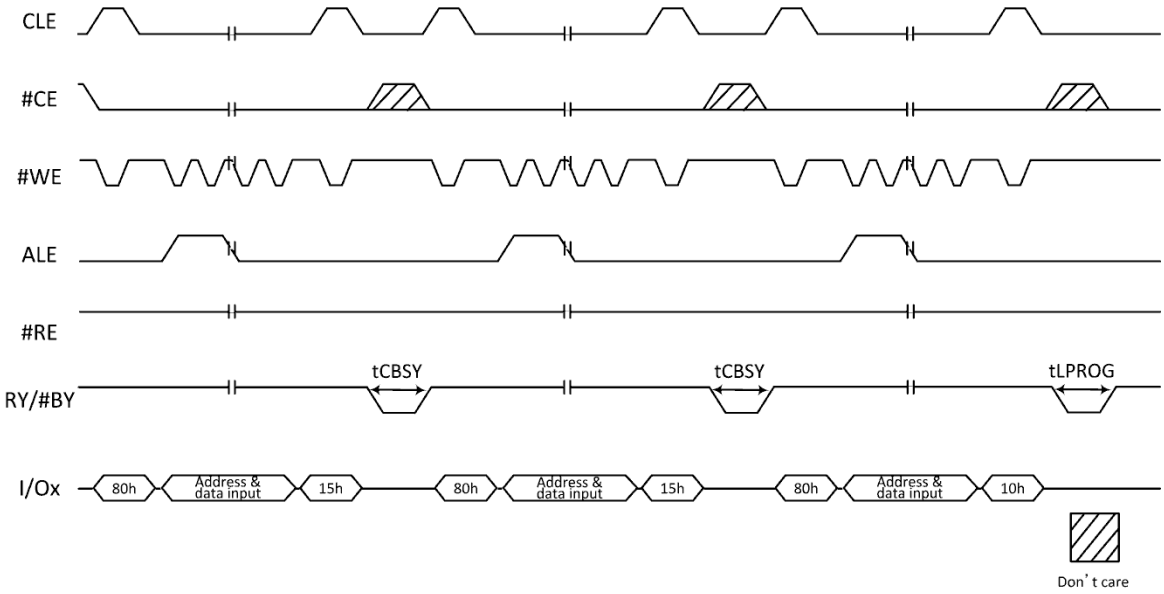


Figure 9-13 Cache Program End

9.3 COPY BACK operation

Copy Back operations require two command sets. Issue a READ for COPY BACK (00h-35h) command first, then the PROGRAM for COPY BACK (85h-10h) command.

9.3.1 READ for COPY BACK (00h-35h)

The READ for COPY BACK command is used together with the PROGRAM for COPY BACK (85h-10h) command. To start execution, READ for COPY BACK (00h) command is written to the Command Register, followed by the four cycles of the source page address. To start the transfer of the selected page data from the memory array to the Cache Register, write the 35h command to the Command Register.

After execution of the READ for COPY BACK command sequence and RY/#BY returns to HIGH marking the completion of the operation, the transferred data from the source page into the Cache Register may be read out by toggling #RE. Data is output sequentially from the column address that was originally specified with the READ for COPY BACK command. RANDOM DATA OUTPUT (05h-E0h) commands can be issued multiple times without any limitation after READ for COPY BACK command has been executed (see Figures 9-14 and 9-15).

At this point the device is in ready state to accept the PROGRAM for COPY BACK command.

9.3.2 PROGRAM for COPY BACK (85h-10h)

After the READ for COPY BACK command operation has been completed and RY/#BY goes HIGH, the PROGRAM for COPY BACK command can be written to the Command Register. The command results in the transfer of data from the Cache Register to the Data Register, then internal operations start programming of the new destination page. The sequence would be, write 85h to the Command Register, followed by the four cycle destination page address to the NAND array. Next write the 10h command to the Command Register; this will signal the internal controller to automatically start to program the data to new destination page. During this programming time, RY/#BY will go LOW. The READ STATUS command can be used instead of the RY/#BY signal to determine when the program is complete. When Status Register Bit 6 (I/O6) equals to “1”, Status Register Bit 0 (I/O0) will indicate if the operation was successful or not.

The RANDOM DATA INPUT (85h) command can be used during the PROGRAM for COPY BACK command for modifying the original data. Once the data is copied into the Cache Register using the READ for COPY BACK (00h-35h) command, follow by writing the RANDOM DATA INPUT (85h) command, along with the address of the data to be changed. The data to be changed is placed on the external data pins. This operation copies the data into the Cache Register. Once the 10h command is written to the Command Register, the original data and the modified data are transferred to the Data Register, and programming of the new page commences. The RANDOM DATA INPUT command can be issued numerous times without limitation, as necessary before starting the programming sequence with 10h command.

Since COPY BACK operations do not use external memory and the data of source page might include a bit errors, a competent ECC scheme should be developed to check the data before programming data to a new destination page.

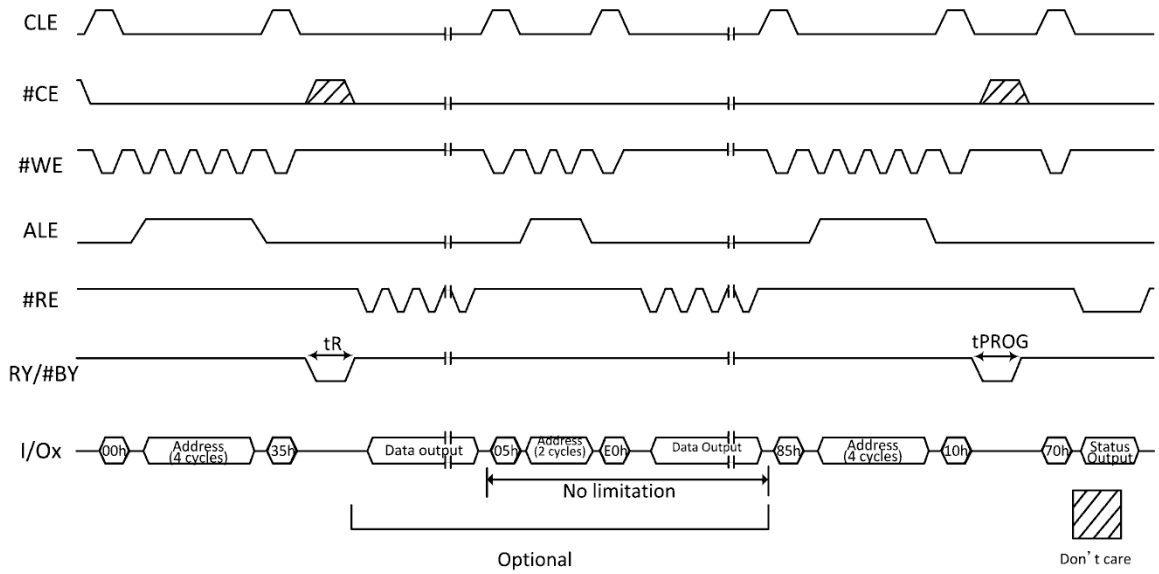


Figure 9-14 Copy Back Program Operation

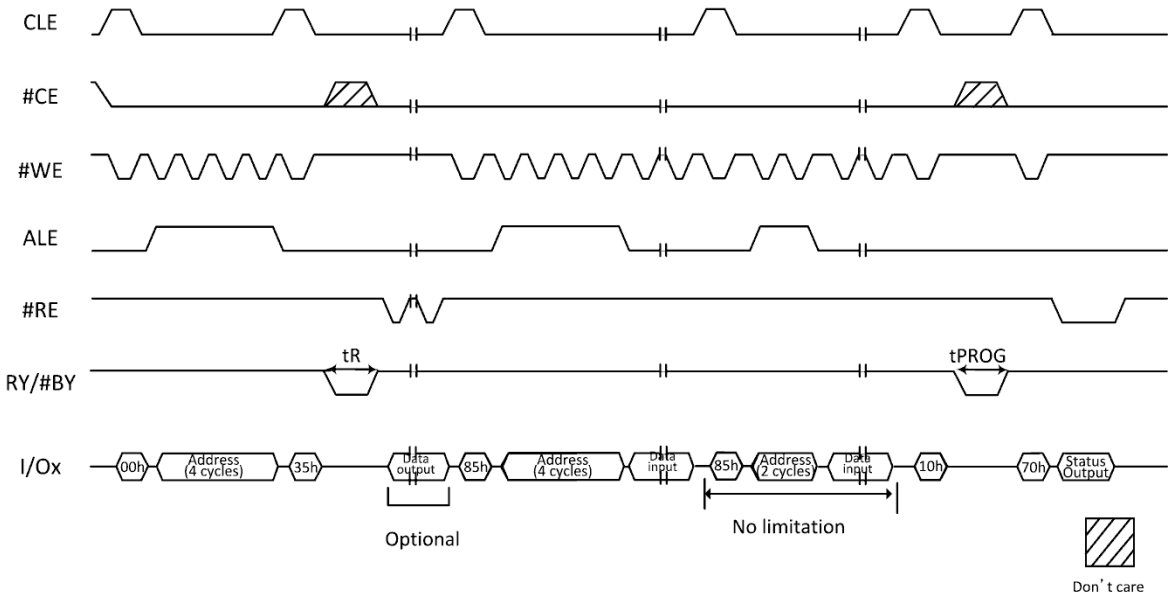


Figure 9-15 Copy Back Operation with Random Data Input

9.4 BLOCK ERASE operation

9.4.1 BLOCK ERASE (60h-D0h)

Erase operations happen at the architectural block unit. This W29N01GX has 1024 erase blocks. Each block is organized into 64 pages (2112 bytes/page,1056words/page), 132K bytes (128K + 4K bytes)/block,66Kwords(64K+2K words)/block The BLOCK ERASE command operates on a block by block basis.

Erase Setup command (60h) is written to the Command Register. Next, the two cycle block address is written to the device. The page address bits are loaded during address block address cycle, but are ignored. The Erase Confirm command (D0h) is written to the Command Register at the rising edge of #WE, RY/#BY goes LOW and the internal controller automatically handles the block erase sequence of operation. RY/#BY goes LOW during Block Erase internal operations for a period of tBERS,

The READ STATUS (70h) command can be used for confirm block erase status. When Status Register Bit6 (I/O6) becomes to “1”, block erase operation is finished. Status Register Bit0 (I/O0) will indicate a pass/fail condition (see Figure 9-16).

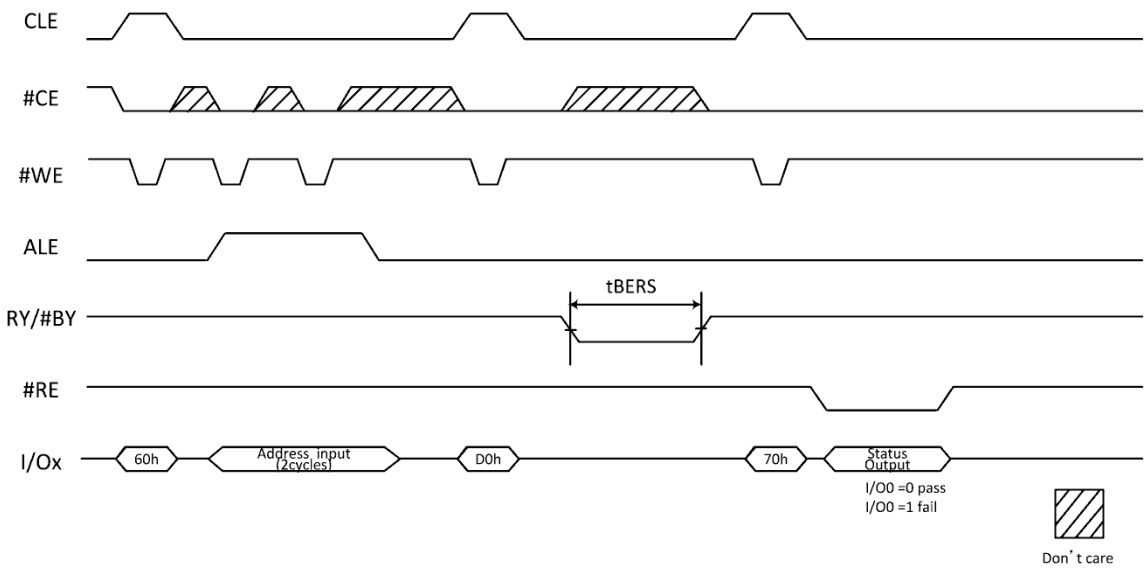


Figure 9-16 Block Erase Operation

9.5 RESET operation

9.5.1 RESET (FFh)

READ, PROGRAM, and ERASE commands can be aborted by the RESET (FFh) command during the time the W29N01GX is in the busy state. The Reset operation puts the device into a known status. The data that is processed in either the programming or erasing operations are no longer valid. This means the data can be partially programmed or erased and therefore data is invalid. The Command Register is cleared and is ready to accept next command. The Data Register and Cache Register contents are marked invalid.

The Status Register indicates a value of E0h when #WP is HIGH; otherwise a value of 60h when #WP is LOW. After RESET command is written to the command register, RY/#BY goes LOW for a period of tRST (see Figure 9-17).

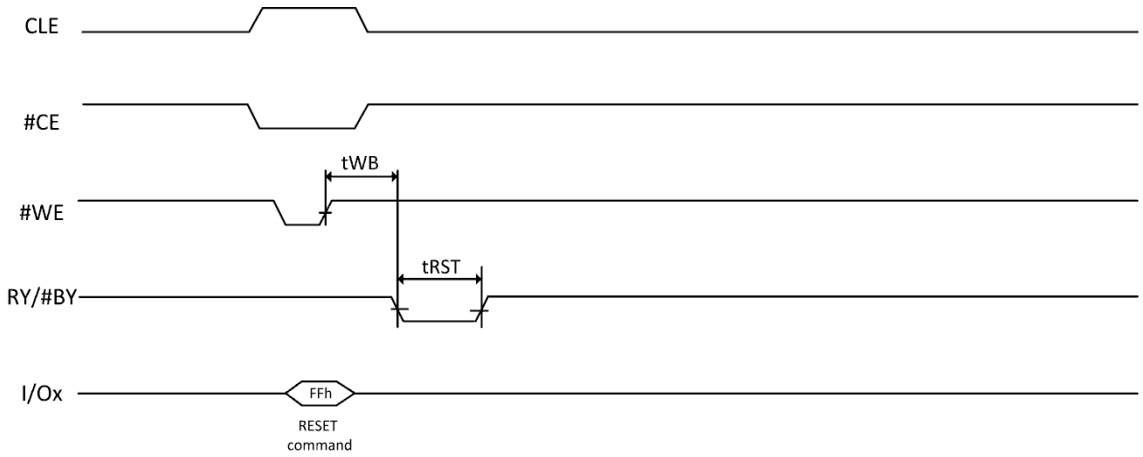


Figure 9-17 Reset Operation

9.6 FEATURE OPERATION

The GET FEATURES (EEh) and SET FEATURES (EFh) commands are used to change the NAND Flash device behavior from the default power on settings. These commands use a one-byte feature address to determine which feature is to be read or modified. A range of 0 to 255 defines all features; each is described in the features table (see Table 9.4 thru 9.7). The GET FEATURES (EEh) command reads 4-Byte parameter in the features table (See GET FEATURES function). The SET FEATURES (EFh) command places the 4-Byte parameter in the features table (See SET FEATURES function).

When a feature set is volatile, meaning it remains active by default until the device is powered off. The set feature remains the set even if a RESET (FFh) command is issued.

Feature address	Description
00h	N.A
01h	Timing mode
02h-7Fh	Reserved
80h	Vendor specific parameter : Programmable I/O drive strength
81h	Vendor specific parameter : Programmable RY/#BY pull-down strength
82h-FFh	Reserved

Table 9.5 Features

Feature Address 01h: Timing Mode

Sub feature parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
Timing mode	Mode 0 (default)	Reserved (0)					0	0	0	00h	1
	Mode 1	Reserved (0)					0	0	1	01h	1
	Mode 2	Reserved (0)					0	1	0	02h	1
	Mode 3	Reserved (0)					0	1	1	03h	2
	Mode 4	Reserved (0)					1	0	0	04h	2
	Mode 5	Reserved (0)					1	0	1	05h	2
P2											
		Reserved (0)								00h	
P3											
		Reserved (0)								00h	
P4											
		Reserved (0)								00h	

Table 9.6 Feature Address 01h

Notes:

1. **Timing mode is set to mode 0 by default. The timing mode should be selected to indicate the maximum speed at which the device will receive addresses, commands, and data cycles. The five supported settings for the timing mode are shown. The device returns to mode 0 when a power cycle has occurred. Supported timing modes are reported in the parameter page.**
2. **Not supported.**

Feature Address 80h: Programmable I/O Drive Strength

Sub feature parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
I/O drive strength	Full (default)	Reserved (0)						0	0	00h	1
	Three-quarters	Reserved (0)						0	1	01h	
	One-half	Reserved (0)						1	0	02h	
	One-quarter	Reserved (0)						1	1	03h	
P2											
		Reserved (0)								00h	
P3											
		Reserved (0)								00h	
P4											
		Reserved (0)								00h	

Table 9.7 Feature Address 80h

Note:

1. **The default drive strength setting is Full strength. The Programmable I/O Drive Strength mode is used to change from the default I/O drive strength. Drive strength should be selected based on expected loading of the memory bus. This table shows the four supported output drive-strength settings. The device returns to the default drive strength mode when a power cycle has occurred. AC timing parameters may need to be relaxed if I/O drive strength is not set to full.**

Feature Address 81h: Programmable RY/#BY Pull-down Strength

Sub feature parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
RY/#BY pull-down strength	Full (default)	Reserved (0)						0	0	00h	1
	Three-quarters	Reserved (0)						0	1	01h	
	One-half	Reserved (0)						1	0	02h	
	One-quarter	Reserved (0)						1	1	03h	
P2											
		Reserved (0)								00h	
P3											
		Reserved (0)								00h	
P4											
		Reserved (0)								00h	

Table 9.8 Feature Address 81h

Note:

1. **The default programmable RY/#BY pull-down strength is set to Full strength. The pull-down strength is used to change the RY/#BY pull-down strength. RY/#BY pull-down strength should be selected based on expected loading of RY/#BY. The four supported pull-down strength settings are shown. The device returns to the default pull-down strength when a power cycle has occurred.**

9.6.1 GET FEATURES (EEh)

The GET FEATURES command returns the device feature settings including those previously set by the SET FEATURES command. To use the Get Feature mode write the command (EEh) to the Command Register followed by the single cycle byte Feature Address. RY/#BY will goes LOW for the period of tFEAT. If Read Status (70h) command is issued for monitoring the process completion status, Read Command (00h) has to be executed to re-establish data output mode. Once, RY/#BY goes HIGH, the device feature settings can be read by toggling #RE. The device remains in Feature Mode until another valid command is issued to Command Register. See Figure 9-18.

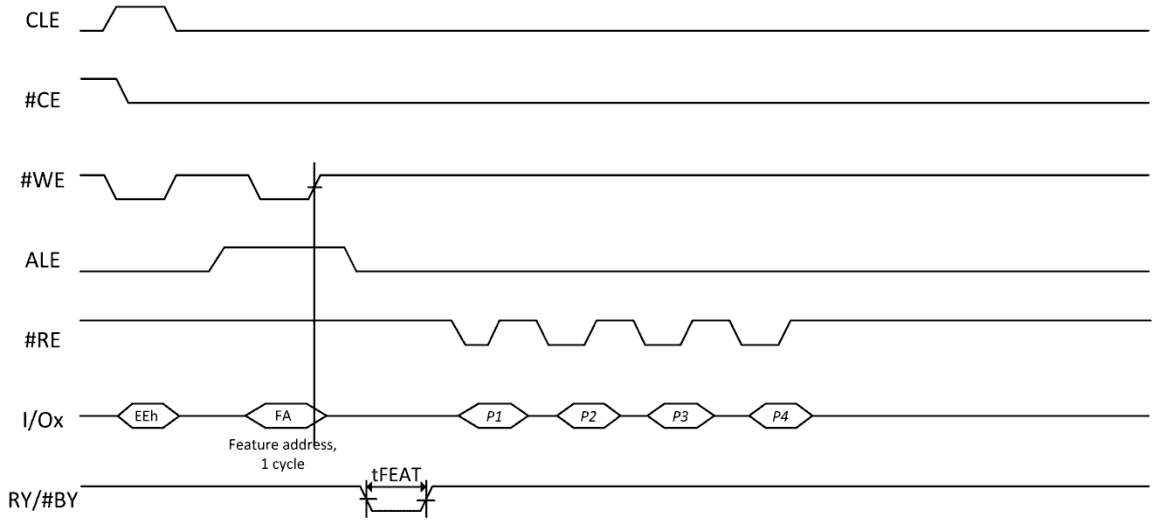


Figure 9-18 Get Feature Operation

9.6.2 SET FEATURES (EFh)

The SET FEATURES command sets the behavior parameters by selecting a specified feature address. To change device behavioral parameters, execute Set Feature command by writing EFh to the Command Register, followed by the single cycle feature address. Each feature parameter (P0-P3) is latched at the rising edge of each #WE. The RY/#BY signal will go LOW during the period of tFEAT while the four feature parameters are stored. The Read Status (70h) command can be issued for monitoring the progress status of this operation. The parameters are stored in device until the device goes through a power on cycle. The device remains in feature mode until another valid command is issued to Command Register.

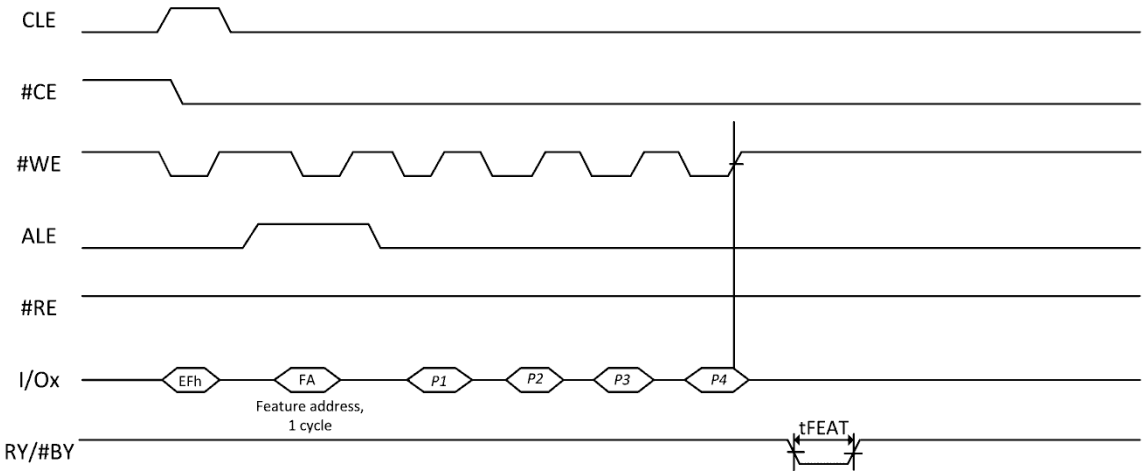


Figure 9-19 Set Feature Operation

9.7 ONE TIME PROGRAMMABLE (OTP) area

The device has One-Time Programmable (OTP) memory area comprised of ten pages (2112 bytes/page). This entire range of pages is functionally guaranteed. Only the OTP commands can access the OTP area. When the device ships from Winbond, the OTP area is in an erase state (all bits equal “1”). In the OTP area, programming or partial-page programming is done only by programming “0” bits. The OTP area cannot be erased, therefore protecting the area only prevent further programming.

OTP area programming and protection have two separate commands. The OTP DATA PROGRAM (A0h-10h) command is used to program an OTP page. Programming an entire page as one operation or up to four partial-page programming sequences is available. Programming other OTP pages can be done in the same way. The OTP DATA PROTECT (A5h-10h) command will permanently protected the OTP area from further programming operations. The OTP DATA READ command (AFh-30h) can read the OTP area with or without protection set. Note; there is no erase command for OTP area.

9.7.1 OTP DATA PROGRAM (A0h-10h)

Programming the OTP area can be done using the OTP DATA PROGRAM (A0h-10h) command. An entire page can be programmed at once or up to four partial page programming sequences per page.

This command enables programming into the offset of an OTP page by using the two bytes of Column Address [11:0]. If OTP area is protected by OTP DATA PROTECT command, the programming the OTP area will not be executed, and RY/#BY goes LOW for a period of tOBSY.

To use this command sequence, the A0h command is written to Command Register. Then issue the four address cycles that are column address of first two cycles and range page address[0B:02] of the two remaining cycles. Then write 1 to 2112 bytes of data, followed by program confirmation command (10h) is written to Command Register. At this point the internal controller automatically executes the algorithms for program and verify. The RY/#BY will go LOW during the program execution for the period of (tPROG). Program verification only detects 1’s that are not successfully programmed to 0’s.

If OTP area is not protected, RANDOM DATA INPUT commands can be used during OTP program operations.

READ STATUS (70h) command is valid during the OTP program operation. For this operation, Status Register Bit5 and Bit6 (I/O5 and I/O6, respectively) will follow same state as RY/#BY. If the OTP area is protected, Status Register Bit7 (I/O7) will equal “0”; otherwise it is a “1”. After the device is in the ready state, Status Register Bit0 (I/O0) indicates whether the operation passed or failed.

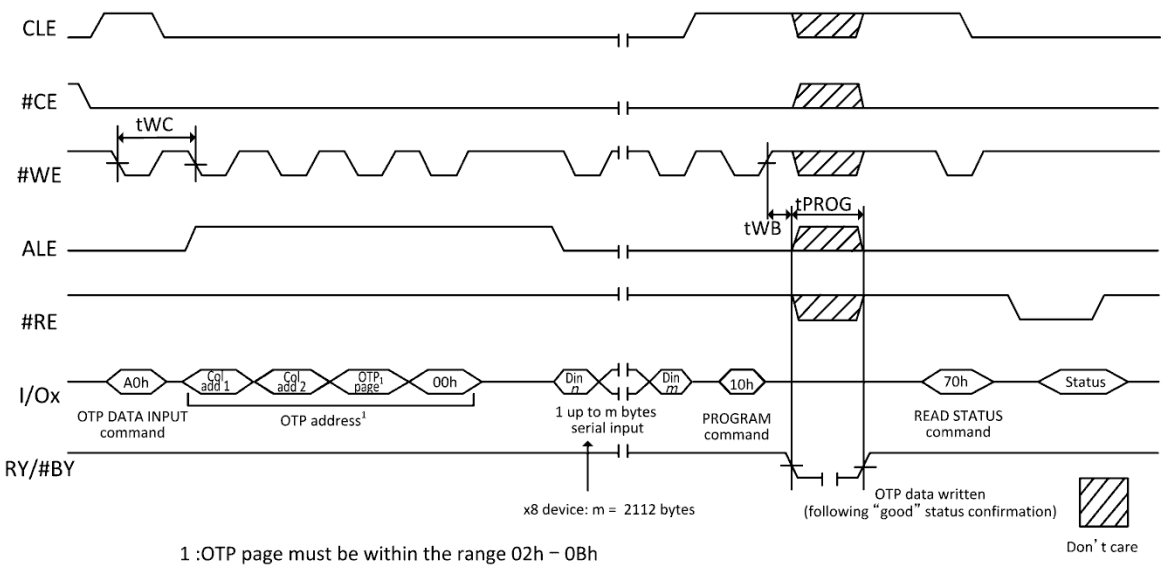


Figure 9-20 OTP Data Program

9.7.2 OTP DATA PROTECT (A5h-10h)

To protect the data in OTP area used the OTP DATA PROTECT (A5h-10h) command. After the OTP area is protected, the OTP area cannot be unprotected and no additional data can be programmed to the OTP area.

To use this command, A5h is written to the Command Register. Then issues the four address cycles with the following address code: 00h-00h-01h-00h. Finalized by writing the protect confirmation command (10h) to the Command Register. The RY/#BY signal will go LOW during this protection process, a period similar with page program time (tPROG).

READ STATUS (70h) command is valid during the OTP protect operation. For this operation, Status Register Bit5 and Bit6 (I/O5 and I/O6, respectively) will indicate same state as the RY/#BY. After the device go to the ready state, Status Register Bit0 (I/O0) indicates whether the operation passed or failed.

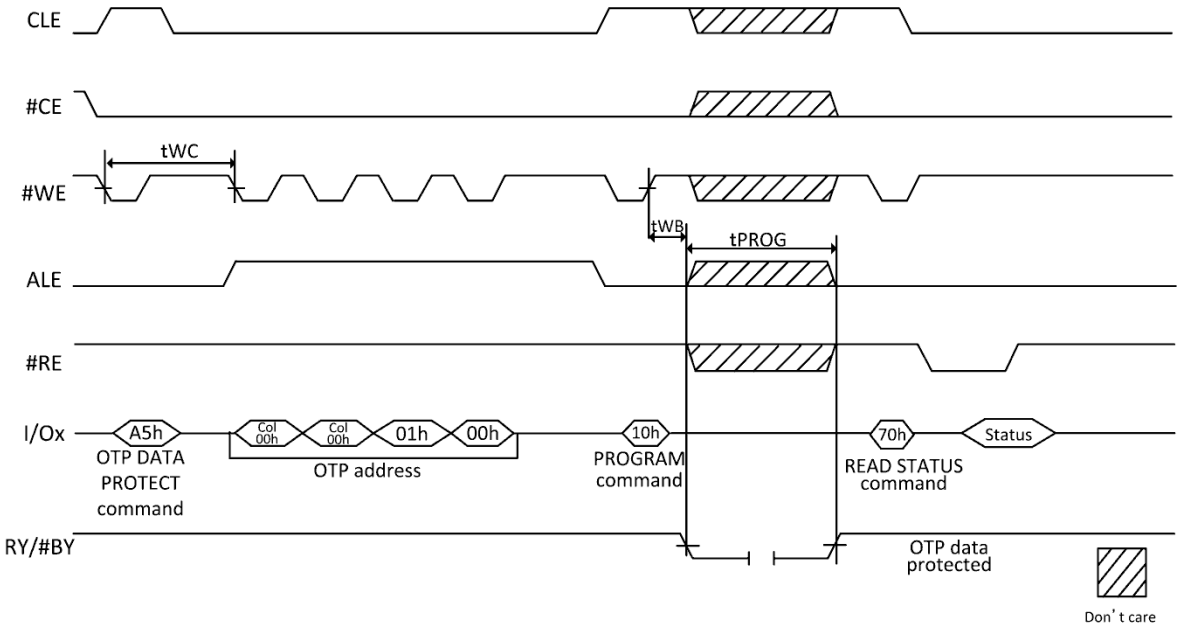


Figure 9-21 OTP Data Protect

9.7.3 OTP DATA READ (AFh-30h)

This command can read the data from OTP pages. The read capability from OTP area is available with or without OTP area protection.

To use this command sequence, AFh command is written to Command Register. Then issue four address cycles comprised of the column address (first two cycles) and the range page address [0B:02] for the remaining two cycles. Once the address is written, perform the read confirmation command (30h) to the Command Register. The RY/#BY signal will go LOW while the OTP data is transferred from OTP area to Data Register during the period of (tR). The RANDOM DATA OUTPUT command can use during OTP data read operations. Read timing of OTP data read is the same as the typical PAGE READ timing.

READ STATUS and RESET command are valid during OTP data read operation. For this operation, Status Register Bit5 and Bit6 (I/O5 and I/O6, respectively) indicate the same as the RY/#BY signal. Additional OTP pages can be read by repeating OTP DATA READ command.

If OTP DATA READ command is followed by CACHE READ operation, the RESET command has to be executed prior to issuing the CACHE READ commands. RESET time can be up to 5µs.

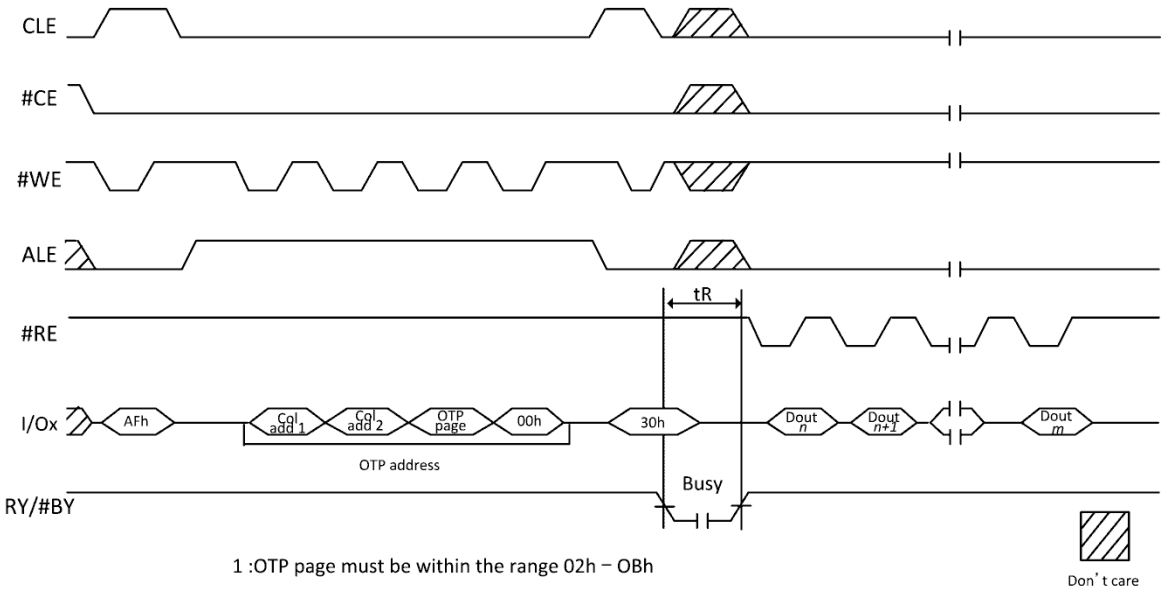


Figure 9-22 OTP Data Read

9.8 WRITE PROTECT

#WP pin can enable or disable program and erase commands preventing or allowing program and erase operations. Figure 9-23 to 9-28 shows the enabling or disabling timing with #WP setup time (tWW) that is from rising or falling edge of #WP to latch the first commands. After first command is latched, #WP pin must not toggle until the command operation is complete and the device is in the ready state. (Status Register Bit5 (I/O5) equal 1.

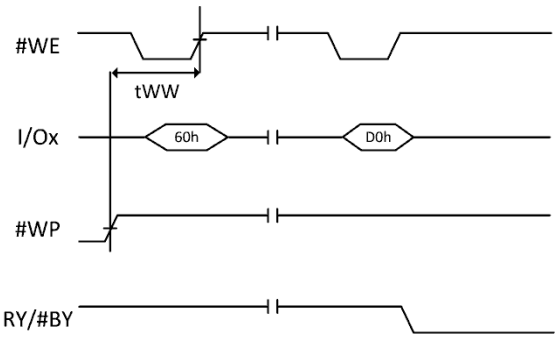


Figure 9-23 Erase Enable

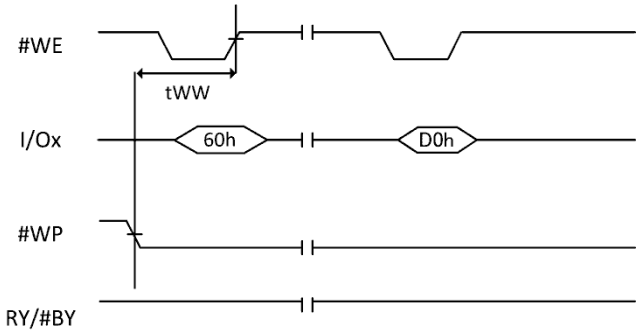


Figure 9-24 Erase Disable

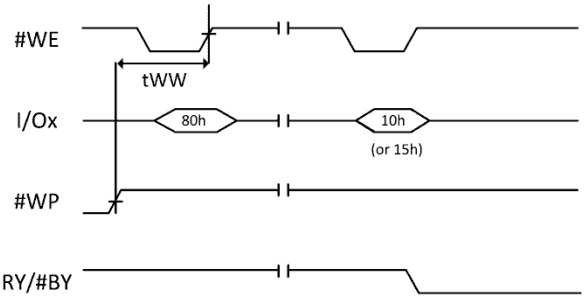


Figure 9-25 Program Enable

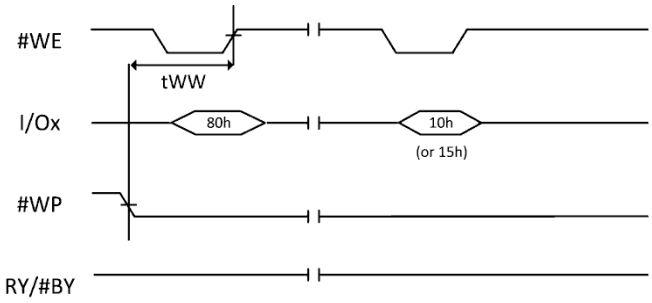


Figure 9-26 Program Disable

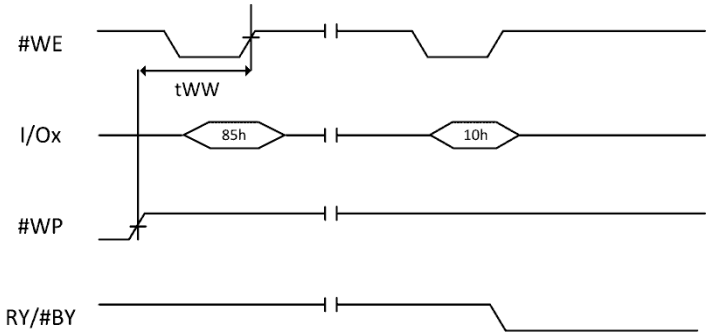


Figure 9-27 Program for Copy Back Enable

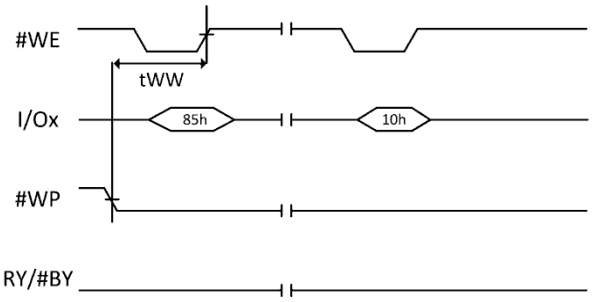


Figure 9-28 Program for Copy Back Disable

9.9 BLOCK LOCK

The device has block lock feature that can protect the entire device or user can indicate a ranges of blocks from program and erase operations. Using this feature offers increased functionality and flexibility data protection to prevent unexpected program and erase operations. Contact to Winbond for using this feature. To disable block lock feature, the LOCK pin is set to a low level.

10. ELECTRICAL CHARACTERISTICS

10.1 Absolute Maximum Ratings

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		–0.6 to +2.4	V
Voltage Applied to Any Pin	VIN	Relative to Ground	–0.6 to +2.4	V
Storage Temperature	TSTG		–65 to +150	°C
Short circuit output current, I/Os			5	mA

Table 10.1 Absolute Maximum Ratings

Notes:

1. **Specification for W29N01GX is preliminary. See preliminary designation at the end of this document.**
2. **This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.**

10.2 Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage	VCC		1.7	1.95	V
Ambient Temperature, Operating	TA	Commercial	0	+70	°C
		Industrial	-40	+85	

Table 10.2 Operating Ranges

10.3 Device power-up timing

The device is designed to avoid unexpected program/erase operations during power transitions. When the device is powered on, the system has to wait until the ready state. #WP is recommended to VIL for preventing unexpected Program and Erase operations during power-transition until Vcc is stable. The RY/#BY will become valid after 50µs from the Vcc ramp start, and at least 10µs after Vcc reaches minimum Vcc level. The first command has to be a RESET command after the device is powered on. Before issuing RESET command, the system has to wait until the RY/#BY goes HIGH, or wait at least 100µs after Vcc reaches minimum Vcc. After issuing the RESET command, the busy time is 1ms maximum. RY/#BY polling or READ STATUS command can monitor the reset busy period. After completing this procedure, the device is initialized and ready for the operation (See Figure 10-1).

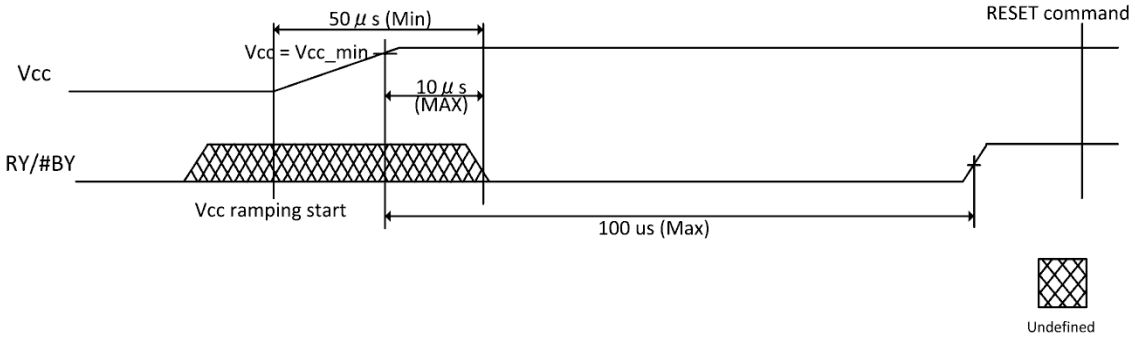


Figure 10-1 RY/#BY Behavior During Power-On

10.4 DC Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	

Sequential Read current	Icc1	tRC= tRC MIN
		#CE=VIL
		IOUT=0mA
			-	10	25	mA

Program current	Icc2	-	-	10	25	mA
Erase current	Icc3	-	-	10	25	mA
Standby current (TTL)	ISB1	#CE=VIH #WP=0V/Vcc	-	-	1	mA
Standby current (CMOS)	ISB2	#CE=Vcc – 0.2V #WP=0V/Vcc	-	10	50	µA
Input leakage current	ILI	VIN= 0 V to Vcc	-	-	±10	µA
Output leakage current	ILO	VOUT=0V to Vcc	-	-	±10	µA
Input high voltage	VIH	I/O7~0, #CE,#WE,#RE, #WP,CLE,ALE,RY/#BY,	0.8 x Vcc	-	Vcc + 0.3	V
Input low voltage	VIL	-	-0.3	-	0.2 x Vcc	V
Output high voltage(1)	VOH	IOH=--100µA	Vcc-0.1	-	-	V
Output low voltage(1)	VOL	IOL=100µA	-	-	0.1	V
Output low current	IOL(RY/#BY)	VOL=0.2V	3	4		mA

Table 10.3 DC Electrical Characteristics

Note:

1. **VOH and VOL may need to be relaxed if I/O drive strength is not set to full.**
2. **IOL (RY/#BY) may need to be relaxed if RY/#BY pull-down strength is not set to full**

10.5 AC Measurement Conditions

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Input Capacitance(1), (2)	CIN	-	10	pF
Input/Output Capacitance(1), (2)	CIO	-	10	pF
Input Rise and Fall Times	TR/TF	-	5	ns
Input Pulse Voltages	-	0 to VCC		V
Input/Output timing Voltage	-	Vcc/2		V
Output load (1)	CL	1TTL GATE and CL=30pF		-

Table 10.4 AC Measurement Conditions

Notes:

1. **Verified on device characterization , not 100% tested**
2. **Test conditions TA=25'C, f=1MHz, VIN=0V**

10.6 AC timing characteristics for Command, Address and Data Input

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
ALE to Data Loading Time	tADL	100	-	ns
ALE Hold Time	tALH	10	-	ns
ALE setup Time	tALS	15	-	ns
#CE Hold Time	tCH	10	-	ns
CLE Hold Time	tCLH	5	-	ns
CLE setup Time	tCLS	15	-	ns
#CE setup Time	tCS	25	-	ns
Data Hold Time	tDH	5	-	ns
Data setup Time	tDS	15	-	ns
Write Cycle Time	tWC	35	-	ns
#WE High Hold Time	tWH	15	-	ns
#WE Pulse Width	tWP	17	-	ns
#WP setup Time	tWW	100	-	ns

Table 10.5 AC timing characteristics for Command, Address and Data Input

Note:

1. **tADL is the time from the #WE rising edge of final address cycle to the #WE rising edge of first data cycle.**

10.7 AC timing characteristics for Operation

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
ALE to #RE Delay	tAR	10	-	ns
#CE Access Time	tCEA	-	30	ns
#CE HIGH to Output High-Z(1)	tCHZ	-	45	ns
CLE to #RE Delay	tCLR	10	-	ns
#CE HIGH to Output Hold	tCOH	15	-	ns
Cache Busy in Cache Read mode	tRCBSY	-	3	µs
Output High-Z to #RE LOW	tIR	0	-	ns
Data Transfer from Cell to Data Register	tR	-	25	µs
READ Cycle Time	tRC	35	-	ns
#RE Access Time	tREA	-	25	ns
#RE HIGH Hold Time	tREH	15	-	ns
#RE HIGH to Output Hold	tRHOH	15	-	ns
#RE HIGH to #WE LOW	tRHW	100	-	ns
#RE HIGH to Output High-Z(1)	tRHZ	-	100	ns
#RE LOW to output hold	tRLOH	5	-	ns
#RE Pulse Width	tRP	17	-	ns
Ready to #RE LOW	tRR	20	-	ns
Reset Time (READ/PROGRAM/ERASE)(2)	tRST	-	5/10/500	µs
#WE HIGH to Busy(3)	tWB	-	100	ns
#WE HIGH to #RE LOW	tWHR	80	-	ns

Table 10.6 AC timing characteristics for Operation

Notes: AC characteristics may need to be relaxed if I/O drive strength is not set to "full."

1. **Transition is measured ±200mV from steady-state voltage with load. This parameter is sampled and not 100 % tested**
2. **The first time the RESET (FFh) command is issued while the device is idle, the device will go busy for a maximum of 1ms. Thereafter, the device goes busy for a maximum of 5 μs.**
3. **Do not issue new command during tWB, even if RY/#BY is ready.**

10.8 Program and Erase Characteristics

PARAMETER	SYMBOL	SPEC		UNIT
		TYP	MAX	
Number of partial page programs	NoP	-	4	cycles
Page Program time	tPROG	300	700	µs
Busy Time for Cache program (1)	tCBSY	3	700	µs
Busy Time for SET FEATURES /GET FEATURES	tFEAT	-	1	µs
Busy Time for program/erase at locked block	tLBSY	-	3	µs
Busy Time for OTP program when OTP is protected	tOBSY	-	30	µs
Block Erase Time	tBERS	2	10	ms
Last Page Program time (2)	tLPROG	-	-	-

Table 10.7 Program and Erase Characteristics

Note:

1. **tCBSY maximum time depends on timing between internal program complete and data-in.**
2. **tLPROG = Last Page program time (tPROG) + Last -1 Page program time (tPROG) – Last page Address, Command and Data load time.**

11. TIMING DIAGRAMS

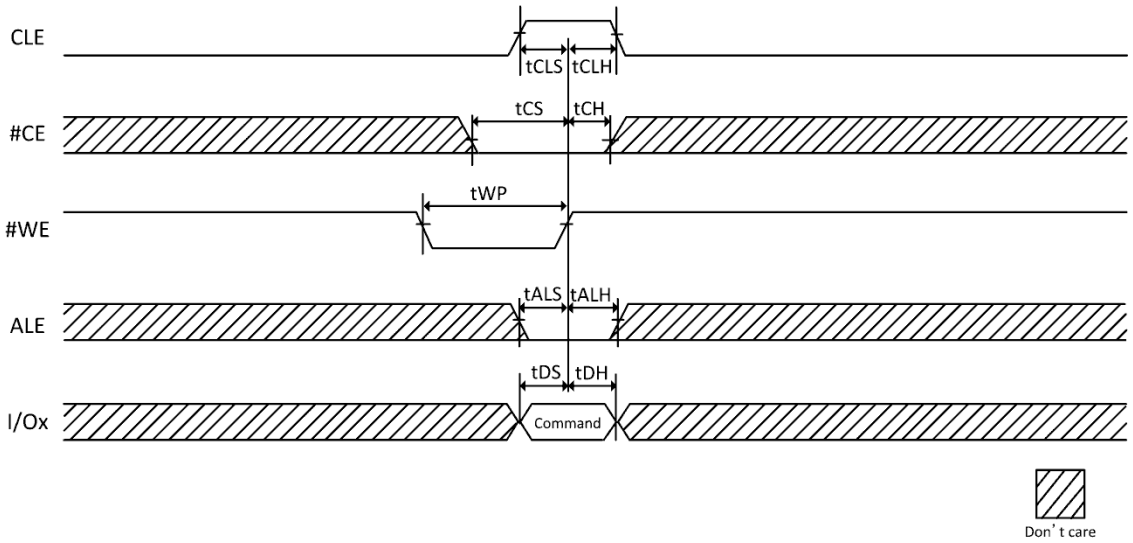


Figure 11-1 Command Latch Cycle

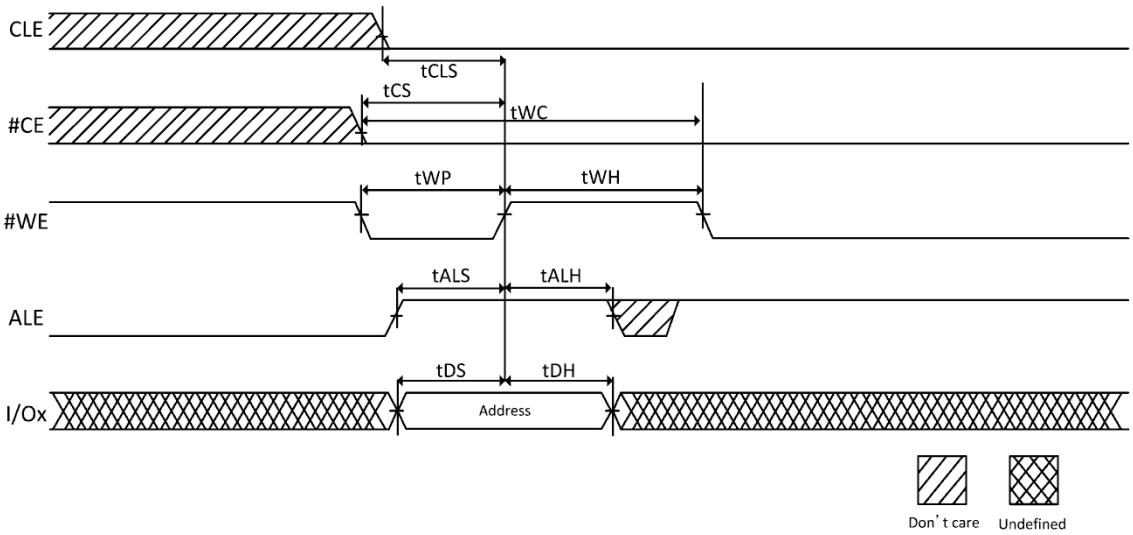


Figure 11-2 Address Latch Cycle

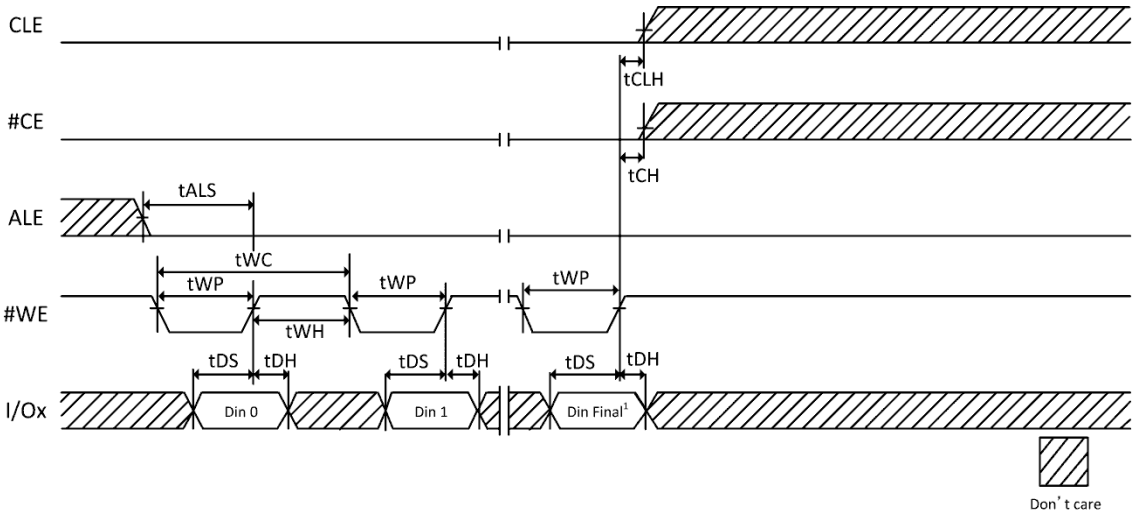


Figure 11-3 Data Latch Cycle

Note:

1. **Din Final = 2,111(x8)**

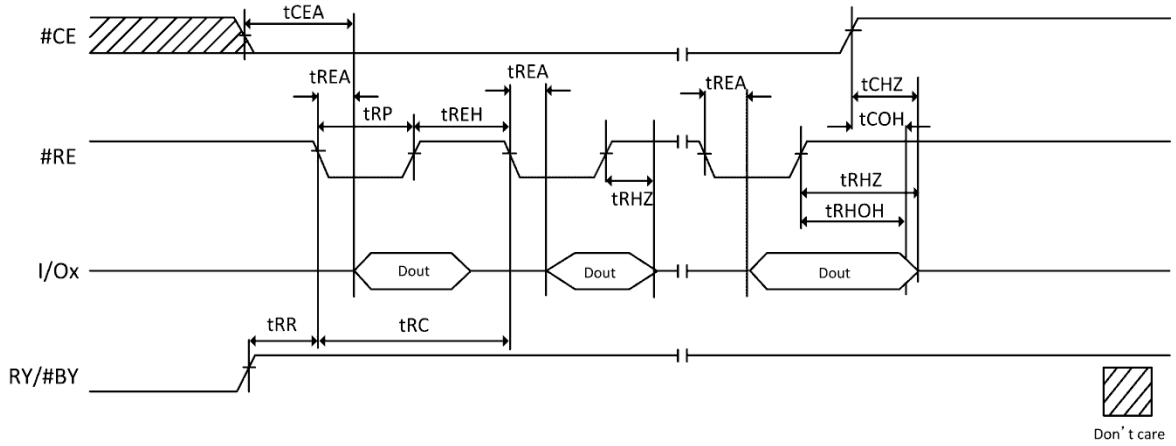


Figure 11-4 Serial Access Cycle after Read

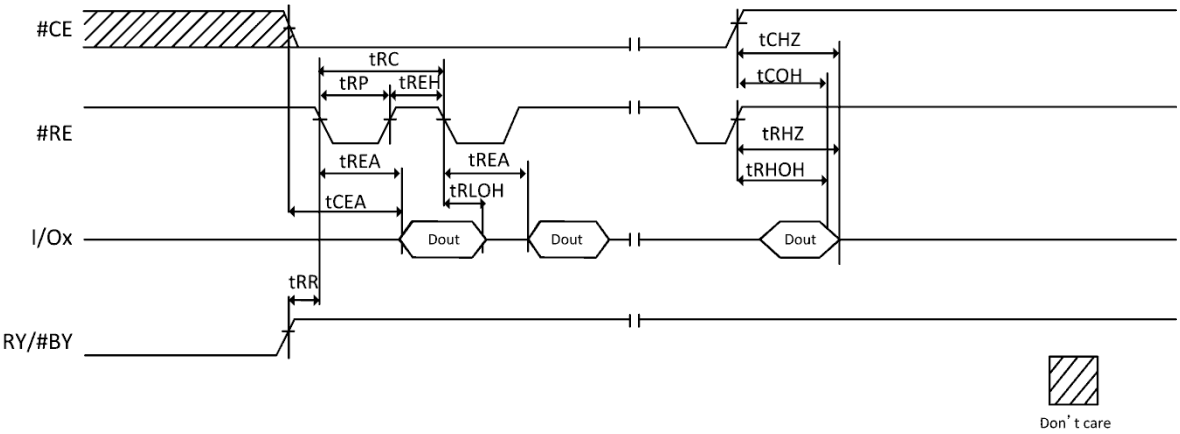


Figure 11-5 Serial Access Cycle after Read (EDO)

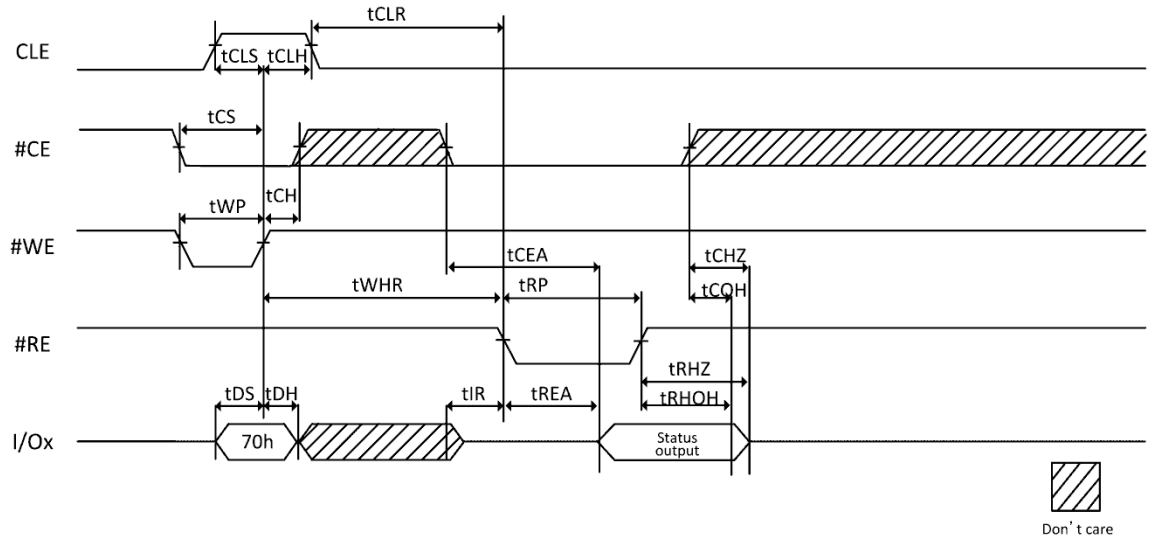


Figure 11-6 Read Status Operation

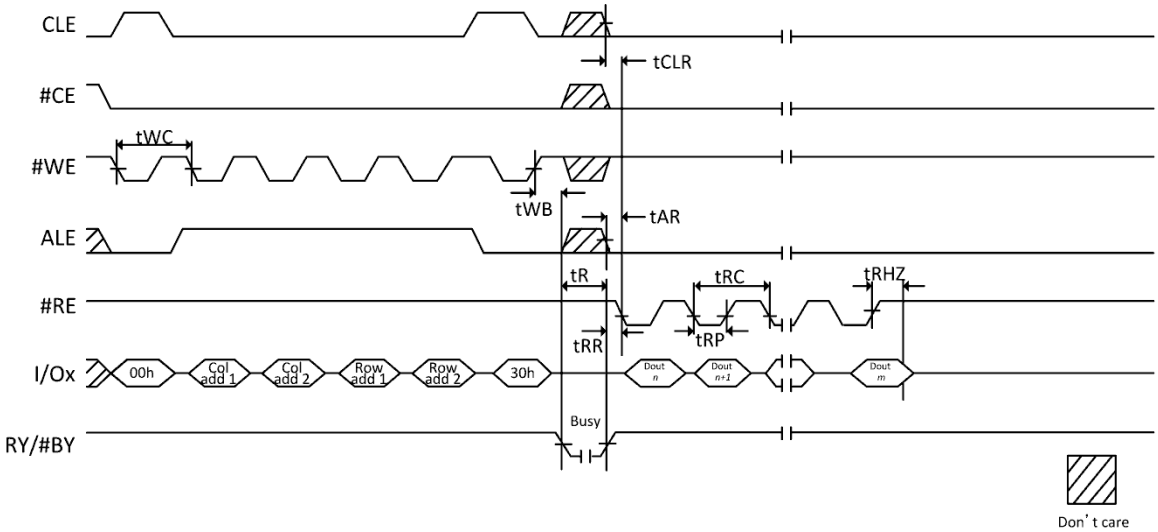


Figure 11-7 Page Read Operation

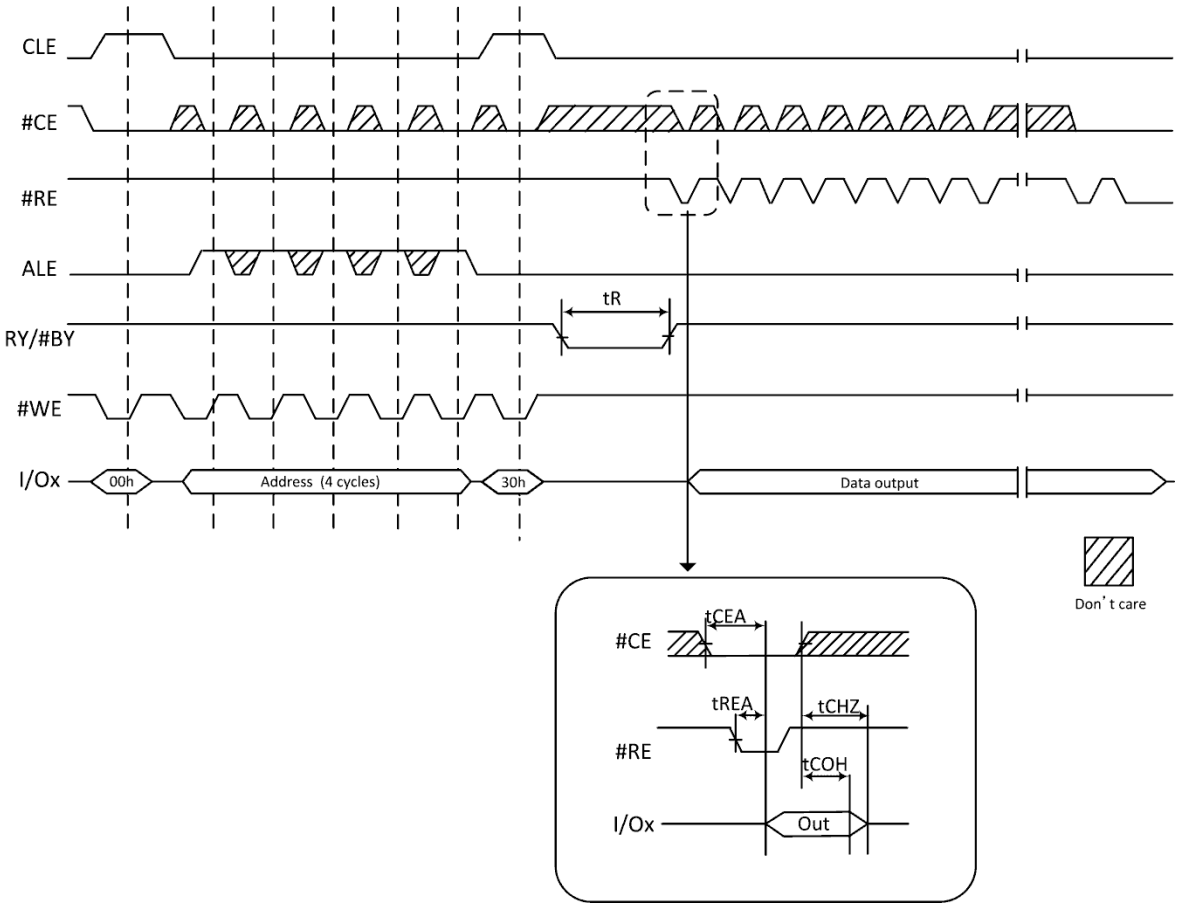


Figure 11-8 #CE Don't Care Read Operation

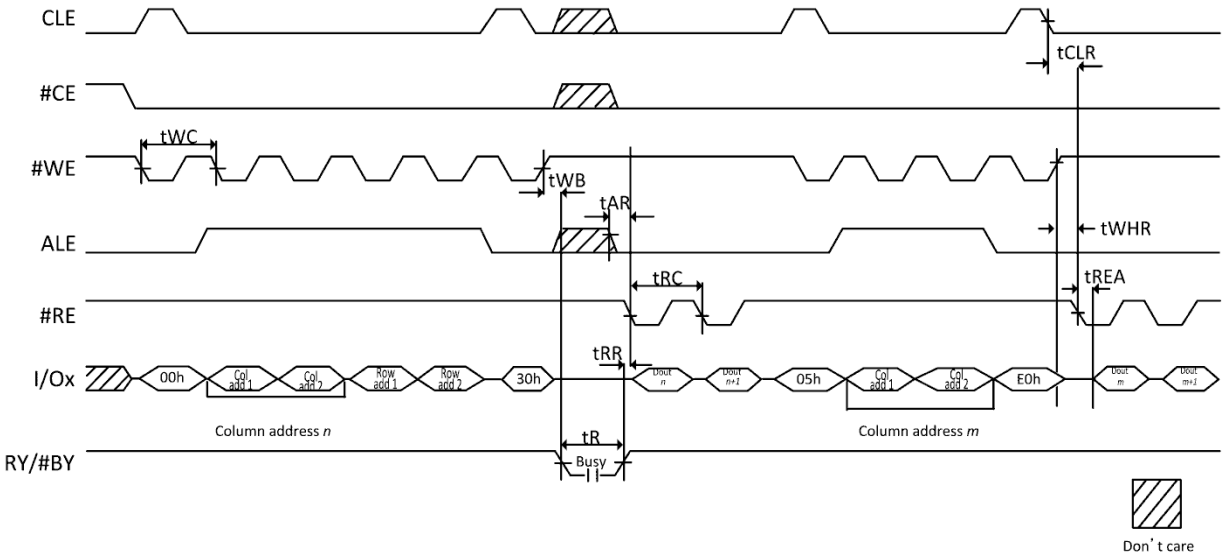


Figure 11-9 Random Data Output Operation

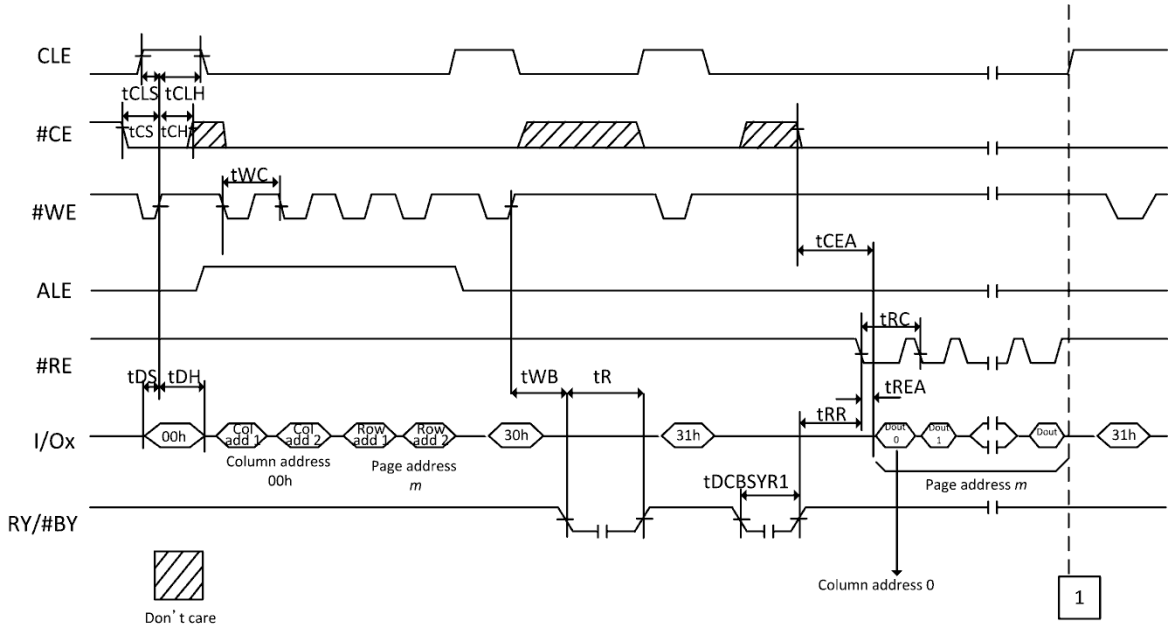


Figure 11-10 Cache Read Operation (1/2)

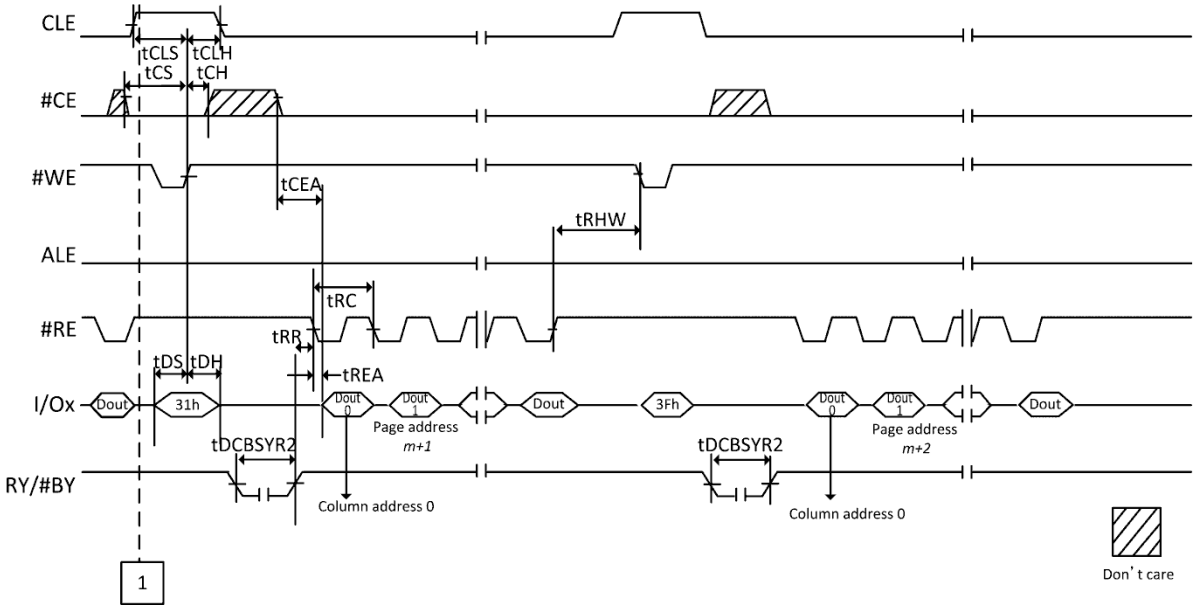


Figure 11-11 Cache Read Operation (2/2)

Note:

1. **See Table 9.1 for actual value.**

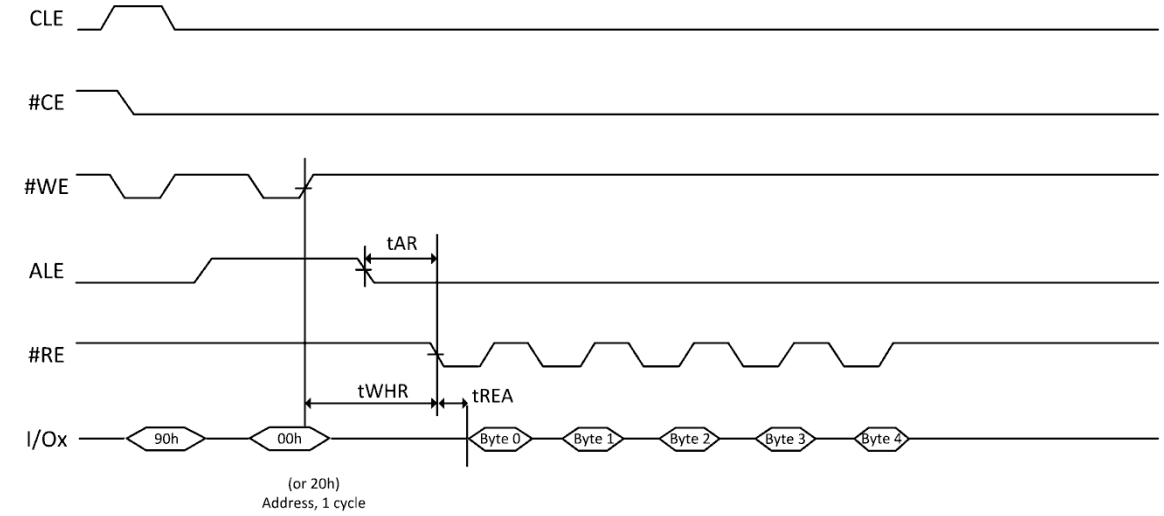


Figure 11-12 Read ID

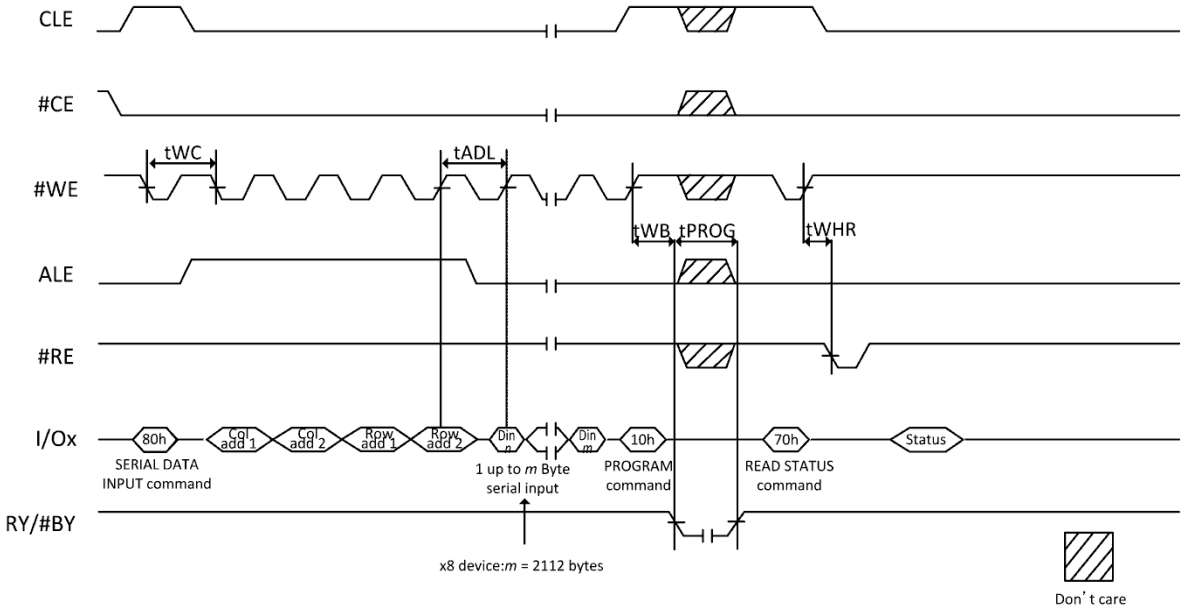


Figure 11-13 Page Program

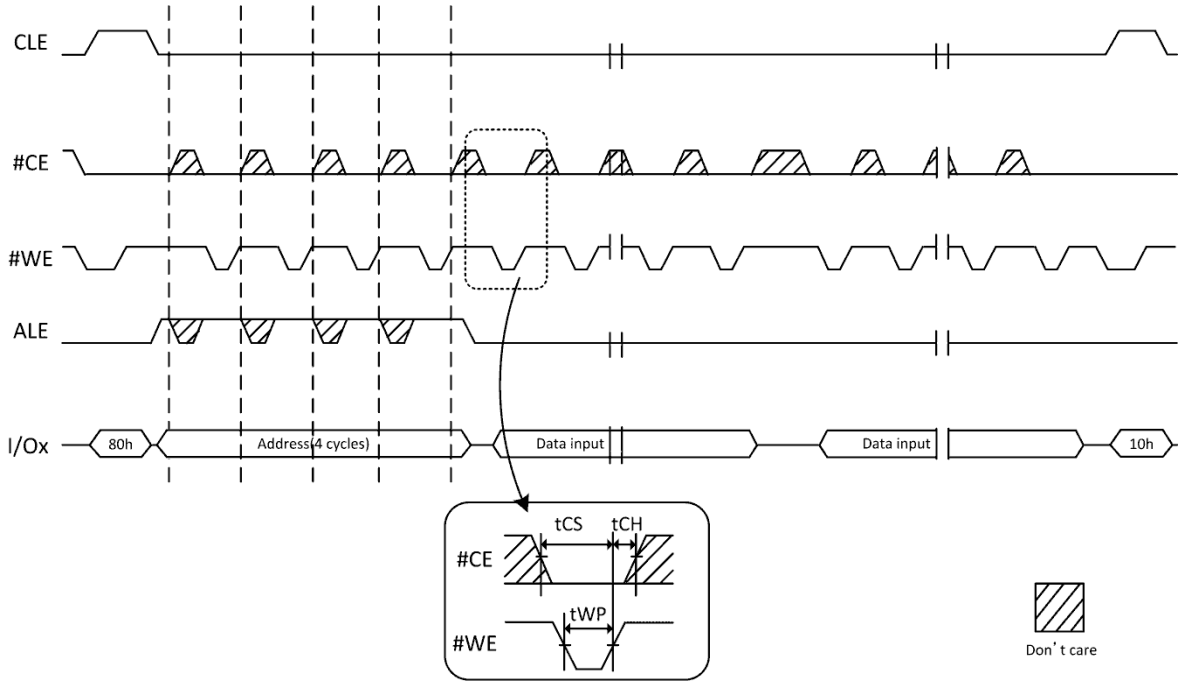


Figure 11-14 #CE Don't Care Page Program Operation

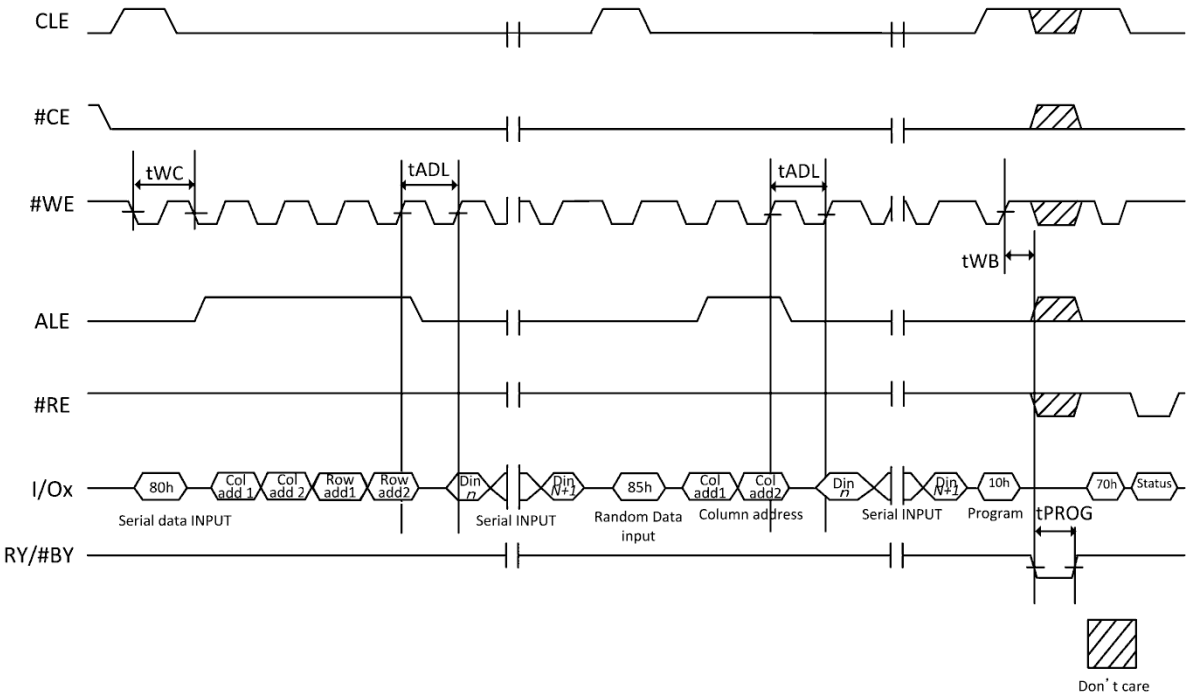


Figure 11-15 Page Program with Random Data Input

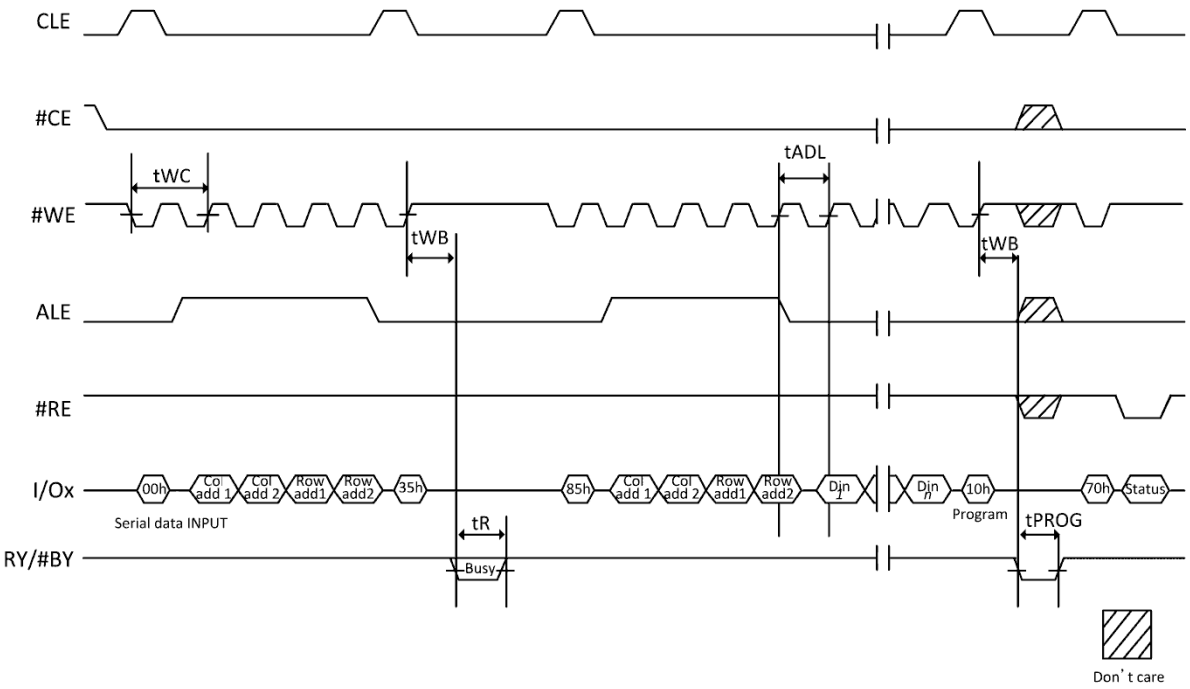


Figure 11-16 Copy Back

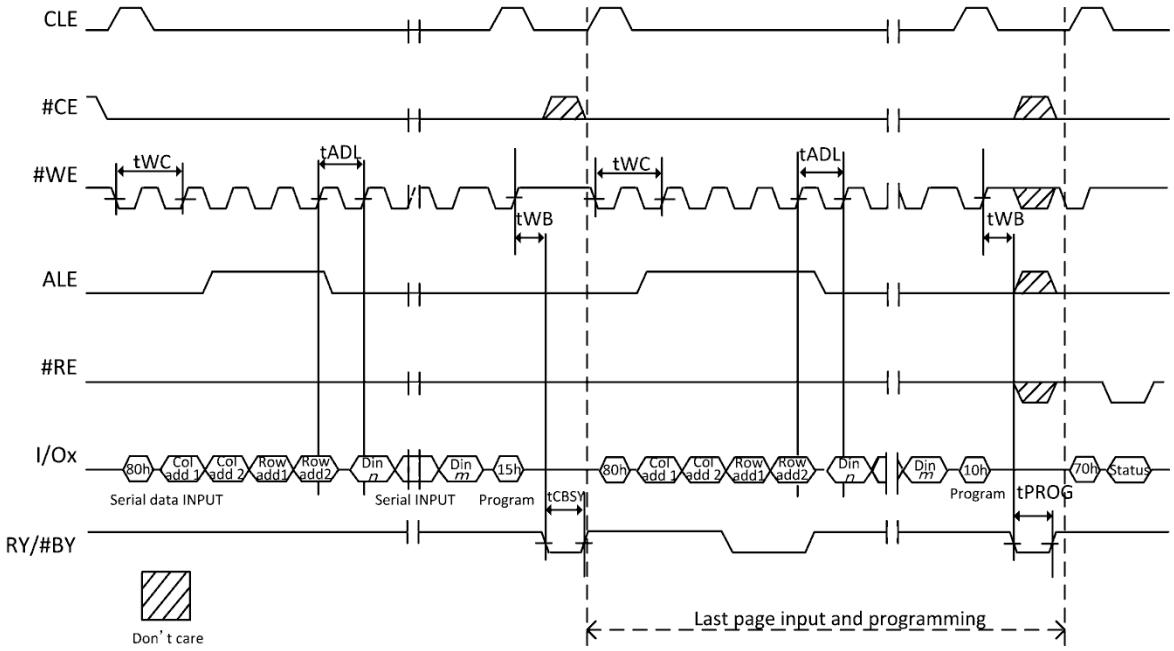


Figure 11-17 Cache Program

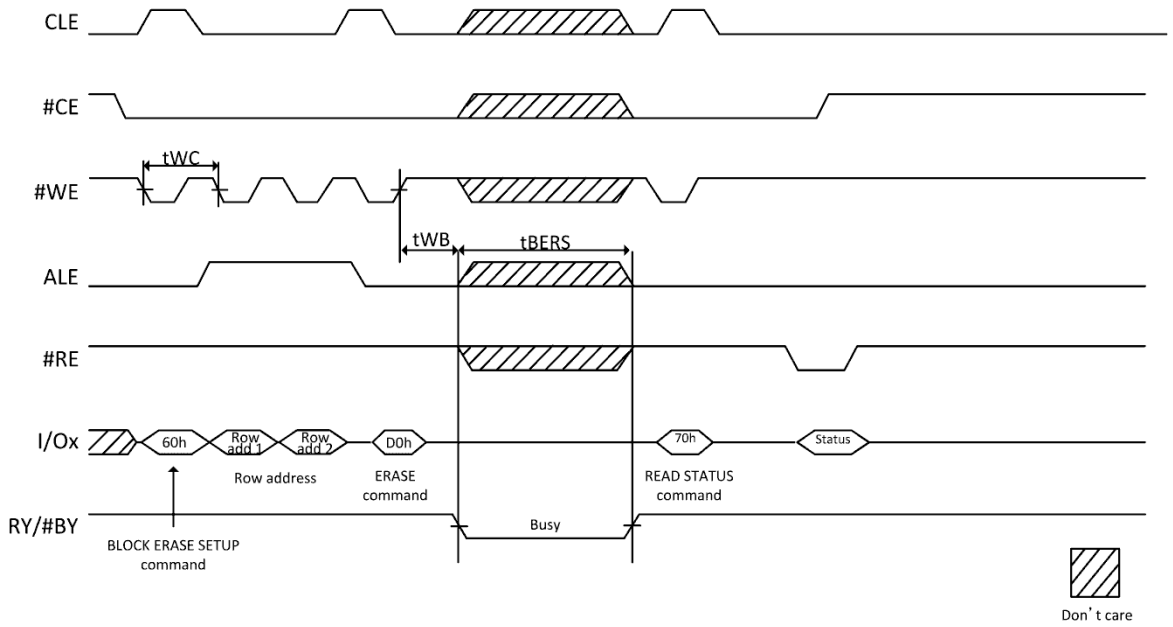


Figure 11-18 Block Erase

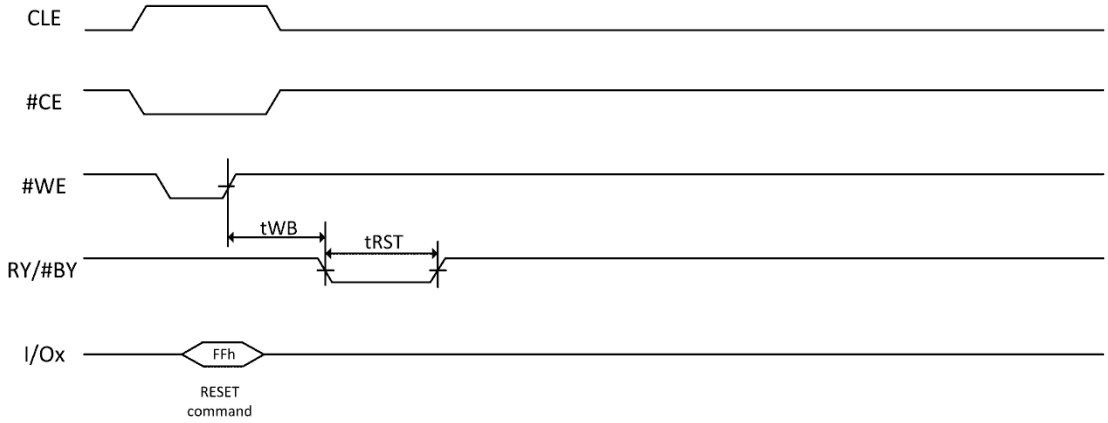


Figure 11-19 Reset

12. INVALID BLOCK MANAGEMENT

12.1 Invalid blocks

The W29N01GX may have initial invalid blocks when it ships from factory. Also, additional invalid blocks may develop during the use of the device. Nvb represents the minimum number of valid blocks in the total number of available blocks (See Table 12.1). An invalid block is defined as blocks that contain one or more bad bits. Block 0, block address 00h is guaranteed to be a valid block at the time of shipment.

Parameter	Symbol	Min	Max	Unit
Valid block number	Nvb	1004	1024	blocks

Table 12.1 Valid Block Number

12.2 Initial invalid blocks

Initial invalid blocks are defined as blocks that contain one or more invalid bits when shipped from factory.

Although the device contains initial invalid blocks, a valid block of the device is of the same quality and reliability as all valid blocks in the device with reference to AC and DC specifications. The W29N01GX has internal circuits to isolate each block from other blocks and therefore, the invalid blocks will not affect the performance of the entire device.

Before the device is shipped from the factory, it will be erased and invalid blocks are marked. All initial invalid blocks are marked with non-FFh at the first byte of spare area on the 1st or 2nd page. The initial invalid block information cannot be recovered if inadvertently erased. Therefore, software should be created to initially check for invalid blocks by reading the marked locations before performing any program or erase operation, and create a table of initial invalid blocks as following flow chart

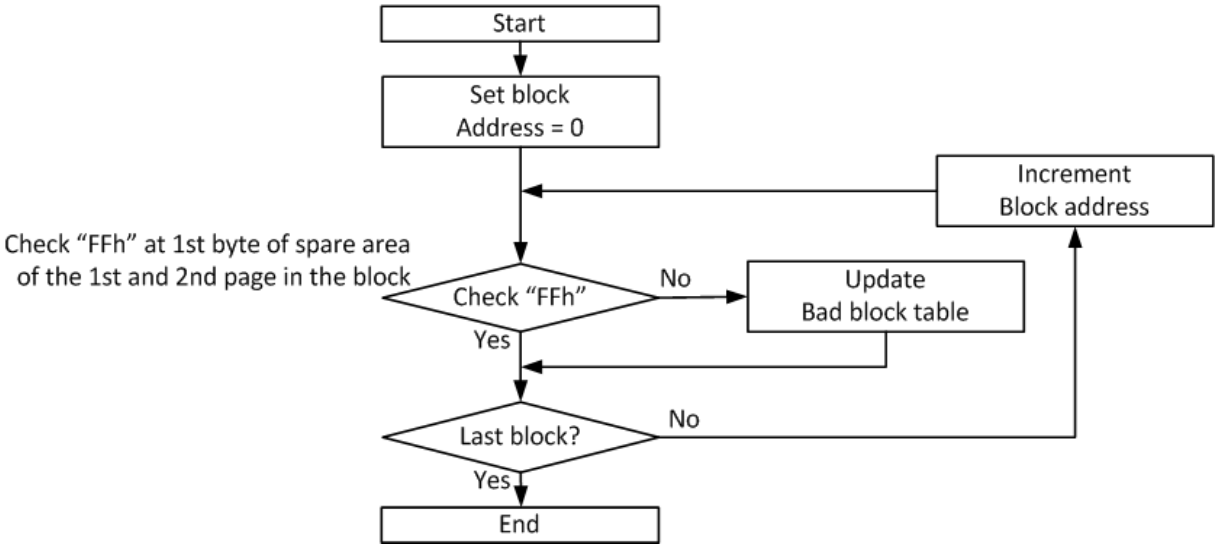


Figure 12-1 flow chart of create initial invalid block table

12.3 Error in operation

Additional invalid blocks may develop in the device during its life cycle. Following the procedures herein is required to guarantee reliable data in the device.

After each program and erase operation, check the status read to determine if the operation failed. In case of failure, a block replacement should be done with a bad-block management algorithm. The system has to use a minimum 1-bit ECC per 528 bytes of data to ensure data recovery.

Operation	Detection and recommended procedure
Erase	Status read after erase → Block Replacement
Program	Status read after program → Block Replacement
Read	Verify ECC → ECC correction

Table 12.2 Block failure

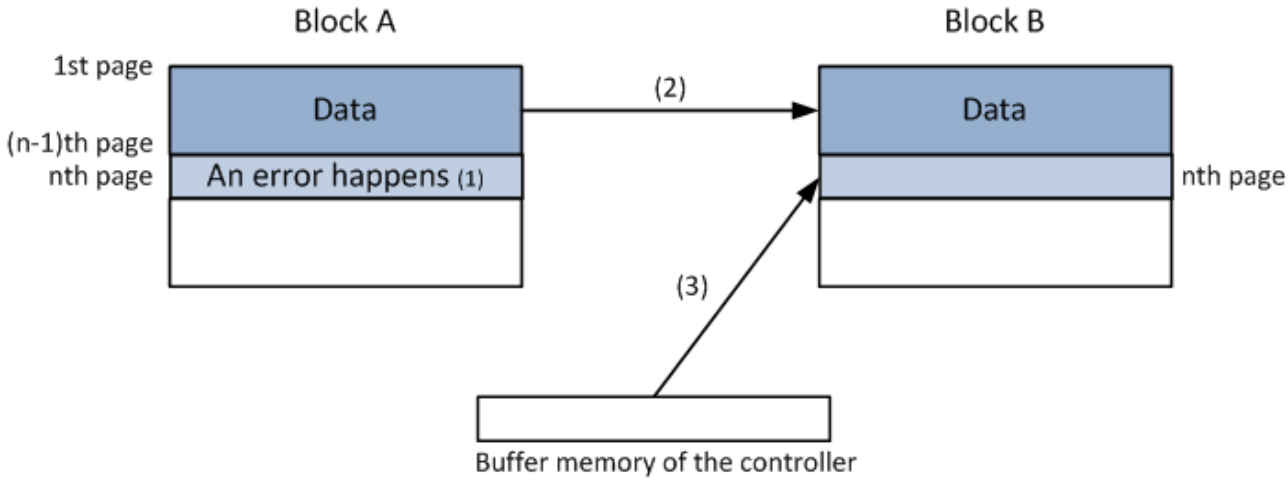


Figure 12-2 Bad block Replacement

Note:

1. **An error happens in the nth page of block A during program or erase operation.**
2. **Copy the data in block A to the same location of block B which is valid block.**
3. **Copy the nth page data of block A in the buffer memory to the nth page of block B**
4. **Creating or updating bad block table for preventing further program or erase to block A**

12.4 Addressing in program operation

The pages within the block have to be programmed sequentially from the lower order page address to the higher order page address within the block. The lower order page is defined as the start page to program, does not need to be page 0 in the block. Random page programming is prohibited.

13. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A	10/22/2013		New Create Preliminary

Table 16.1 History Table

Preliminary Designation

The "Preliminary" designation on a *Winbond* datasheet indicates that the product is not fully characterized. The specifications are subject to change and are not guaranteed. *Winbond* or an authorized sales representative should be consulted for current information before using this product.

Trademarks

Winbond is trademark of *Winbond Electronics Corporation.*
All other marks are the property of their respective owner.

Important Notice

Winbond products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Furthermore, Winbond products are not intended for applications wherein failure of Winbond products could result or lead to a situation where in personal injury, death or severe property or environmental damage could occur.

Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

512Mb Mobile LPDDR

1. GENERAL DESCRIPTION

W949D6KB / W949D2KB is a high-speed Low Power double data rate synchronous dynamic random access memory (LPDDR SDRAM), An access to the LPDDR SDRAM is burst oriented. Consecutive memory location in one page can be accessed at a burst length of 2, 4, 8 and 16 when a bank and row is selected by an ACTIVE command. Column addresses are automatically generated by the LPDDR SDRAM internal counter in burst operation. Random column read is also possible by providing its address at each clock cycle. The multiple bank nature enables interleaving among internal banks to hide the pre-charging time. By setting programmable Mode Registers, the system can change burst length, latency cycle, interleave or sequential burst to maximize its performance. The device supports special low power functions such as Partial Array Self Refresh (PASR) and Automatic Temperature Compensated Self Refresh (ATCSR).

2. FEATURES

- VDD = 1.7~1.95V
- VDDQ = 1.7~1.95V;
- Data width: x16 / x32
- Clock rate: 200MHz (-5),166MHz (-6)
- Standard Self Refresh Mode
- Partial Array Self-Refresh(PASR)
- Auto Temperature Compensated Self-Refresh(ATCSR)
- Power Down Mode
- Deep Power Down Mode (DPD Mode)
- Programmable output buffer driver strength
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- Clock Stop capability during idle periods
- Auto Pre-charge option for each burst access
- Double data rate for data output
- Differential clock inputs (CK and $\overline{CK}$)
- Bidirectional, data strobe (DQS)
- $\overline{CAS}$ Latency: 2 and 3
- Burst Length: 2, 4, 8 and 16
- Burst Type: Sequential or Interleave
- 64 ms Refresh period
- Interface: LVCMOS compatible
- Support package:
  - 60 balls VFBGA (x16)
  - 90 balls VFBGA (x32)
- Operating Temperature Range :
  - Extended (-25°C ~ +85°C)
  - Industrial (-40°C ~ +85°C)

TABLE OF CONTENTS

3. PIN DESCRIPTION

3.1 Ball Assignment : LPDDR X16

60 BALL VFBGA									
	1	2	3	4	5	6	7	8	9
A	VSS	DQ15	VSSQ				VDDQ	DQ0	VDD
B	VDDQ	DQ13	DQ14				DQ1	DQ2	VSSQ
C	VSSQ	DQ11	DQ12				DQ3	DQ4	VDDQ
D	VDDQ	DQ9	DQ10				DQ5	DQ6	VSSQ
E	VSSQ	UDQS	DQ8				DQ7	LDQS	VDDQ
F	VSS	UDM	NC				NC	LDM	VDD
G	CKE	CK	$\overline{CK}$				$\overline{WE}$	$\overline{CAS}$	$\overline{RAS}$
H	A9	A11	A12				$\overline{CS}$	BA0	BA1
J	A6	A7	A8				A10/AP	A0	A1
K	VSS	A4	A5				A2	A3	VDD

(Top View) Pin Configuration

3.2 Ball Assignment : LPDDR X32

90 BALL VFBGA									
	1	2	3	4	5	6	7	8	9
A	VSS	DQ31	VSSQ				VDDQ	DQ16	VDD
B	VDDQ	DQ29	DQ30				DQ17	DQ18	VSSQ
C	VSSQ	DQ27	DQ28				DQ19	DQ20	VDDQ
D	VDDQ	DQ25	DQ26				DQ21	DQ22	VSSQ
E	VSSQ	DQS3	DQ24				DQ23	DQS2	VDDQ
F	VDD	DM3	NC				NC	DM2	VSS
G	CKE	CK	$\overline{CK}$				$\overline{WE}$	$\overline{CAS}$	$\overline{RAS}$
H	A9	A11	A12				$\overline{CS}$	BA0	BA1
J	A6	A7	A8				A10/AP	A0	A1
K	A4	DM1	A5				A2	DM0	A3
L	VSSQ	DQS1	DQ8				DQ7	DQS0	VDDQ
M	VDDQ	DQ9	DQ10				DQ5	DQ6	VSSQ
N	VSSQ	DQ11	DQ12				DQ3	DQ4	VDDQ
P	VDDQ	DQ13	DQ14				DQ1	DQ2	VSSQ
R	VSS	DQ15	VSSQ				VDDQ	DQ0	VDD

(Top View) Pin Configuration

4. PIN DESCRIPTION

4.1 Signal Descriptions

Signal Name	Type	Function	Description
A [n : 0]	Input	Address	Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. The address inputs also provide the opcode during a MODE REGISTER SET command. A10 is used for Auto Pre-charge Select.
BA0, BA1	Input	Bank Select	Define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
DQ0~DQ15 (×16) DQ0~DQ31 (×32)	I/O	Data Input/ Output	Data bus: Input / Output.
$\overline{CS}$	Input	Chip Select	$\overline{CS}$ enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$	Input	Row Address Strobe	$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
$\overline{CAS}$	Input	Column Address Strobe	Referred to $\overline{RAS}$.
$\overline{WE}$	Input	Write Enable	Referred to $\overline{RAS}$.
UDM / LDM(x16); DM0 to DM3 (x32)	Input	Input Mask	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading matches the DQ and DQS loading. x16: LDM: DQ0 - DQ7, UDM: DQ8 – DQ15 x32: DM0: DQ0 - DQ7, DM1: DQ8 – DQ15, DM2: DQ16 – DQ23, DM3: DQ24 – DQ31.
CK / $\overline{CK}$	Input	Clock Inputs	CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$.Input and output data is referenced to the crossing of CK and $\overline{CK}$ (both directions of crossing). Internal clock signals are derived from CK/ $\overline{CK}$.

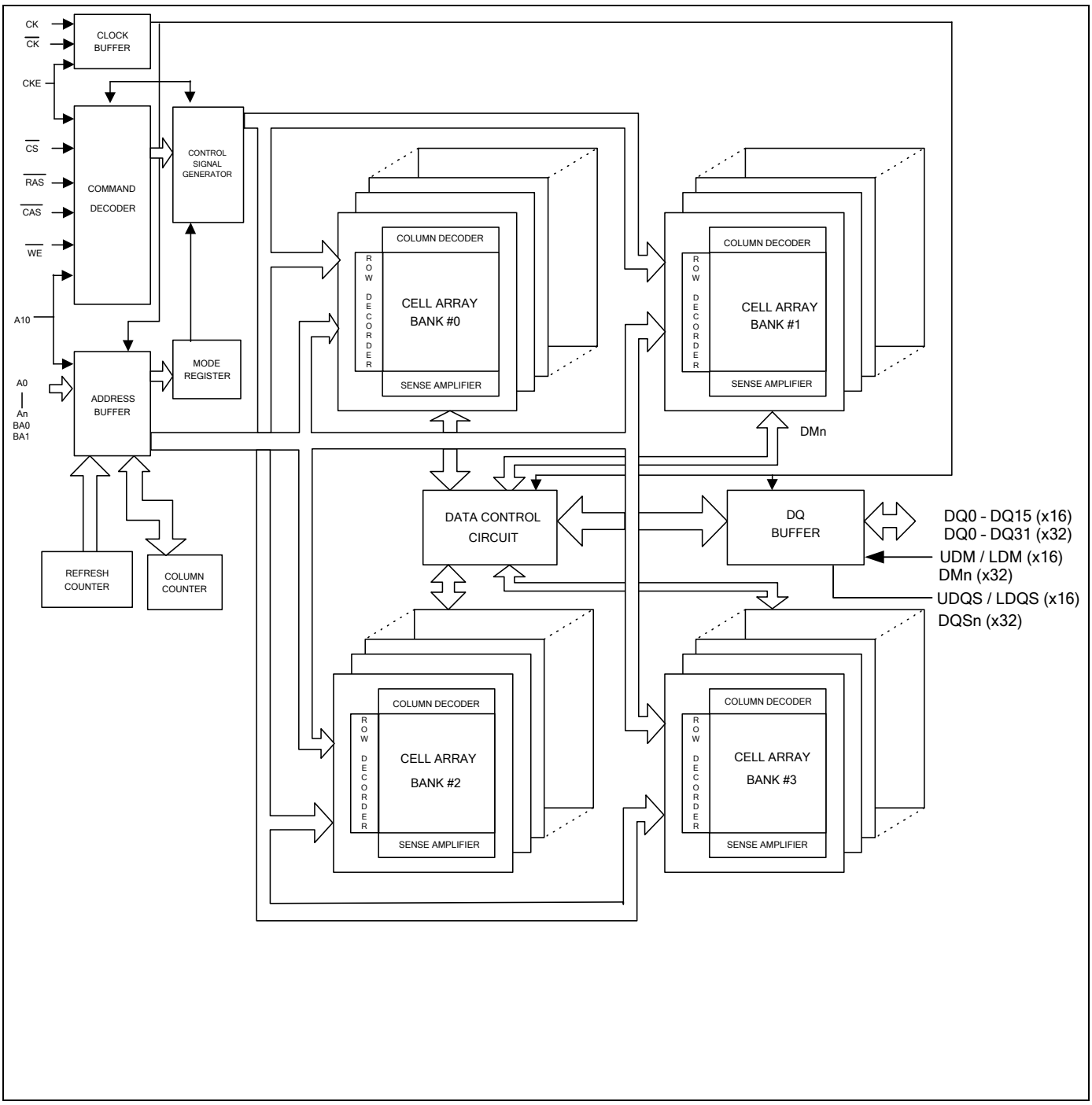
Signal Name	Type	Function	Description
CKE	Input	Clock Enable	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE, POWER DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank). CKE is synchronous for all functions except for SELF REFRESH EXIT, which is achieved asynchronously. Input buffers, excluding CK, $\overline{CK}$ and CKE, are disabled during power down and self refresh mode which are contrived for low standby power consumption.
LDQS, UDQS(x16); DQS0~DQS3 (x32)	I/O	Data Strobe	Output with read data, input with write data. Edge-aligned with read data, centered with write data. Used to capture write data. x16: LDQS: DQ0~DQ7; UDQS: DQ8~DQ15. x32: DQS0: DQ0~DQ7; DQS1: DQ8~DQ15; DQS2: DQ16~DQ23; DQS3: DQ24~DQ31.
VDD	Supply	Power	Power supply for input buffers and internal circuit.
VSS	Supply	Ground	Ground for input buffers and internal circuit.
VDDQ	Supply	Power for I/O Buffer	Power supply separated from VDD, used for output drivers to improve noise.
VSSQ	Supply	Ground for I/O Buffer	Ground for output drivers.
NC	-	No Connect	No internal electrical connection is present.

4.2 Addressing Table

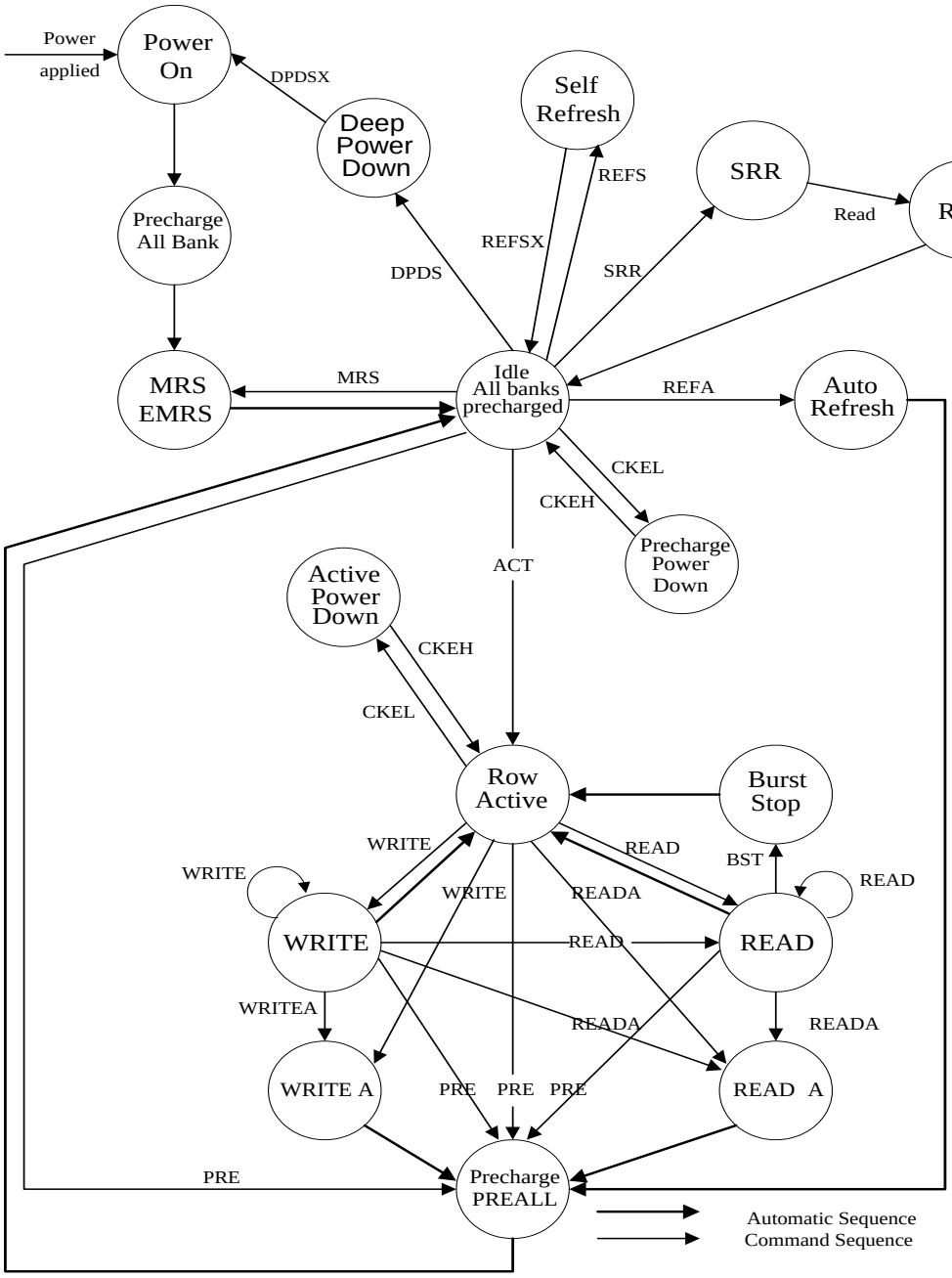
Item		512 Mb
Number of banks		4
Bank address pins		BA0,BA1
Auto precharge pin		A10/AP
Type		**Package**
X16	Row addresses	A0-A12
	Column addresses	A0-A9
	tREFI(µs)	7.8
x32	Row addresses	A0-A12
	Column addresses	A0-A8
	tREFI(µs)	7.8

5. BLOCK DIAGRAM

5.1 Block Diagram



5.2 Simplified State Diagram



ACT = Active
BST = Burst Terminate
CKEL= Enter Power-Down
CKEH=Exit Power - Down
DPDS= Enter Deep Power Down
DPDSX= Exit Deep Power Down
EMRS= Ext . Mode Reg . Set
MRS = Mode Register Set
PRE = Precharge
PREALL= Precharge All Bank
REFA = Auto Refresh
REFS = Enter Self Refresh
REFSX= Exit Self Refresh
READ = Read w/o Auto Precharge
READA = Read with Auto Precharge
WRITE = Write w/o Auto Precharge
WRITEA = Write with Auto Precharge
SRR = Status Register Read

Note: Use caution with this diagram . It is indented to provide a floorplan of the possible state transitions and commands to control them , not all details.In particular situations involving more than one bank are not captured in full detall.

6. FUNCTION DESCRIPTION

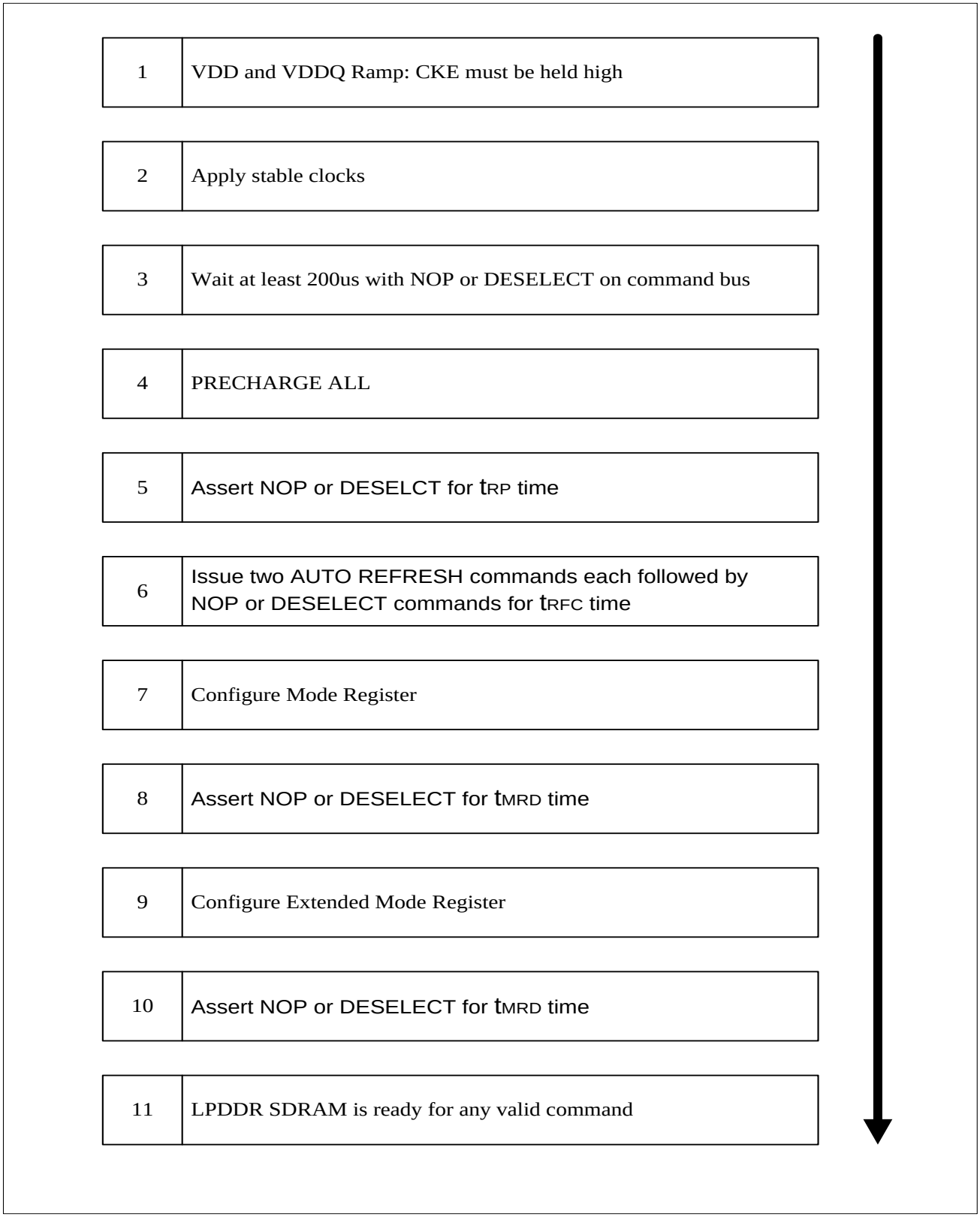
6.1 Initialization

LPDDR SDRAM must be powered up and initialized in a predefined manner. Operations procedures other than those specified may result in undefined operation. If there is any interruption to the device power, the initialization routine should be followed. The steps to be followed for device initialization are listed below.

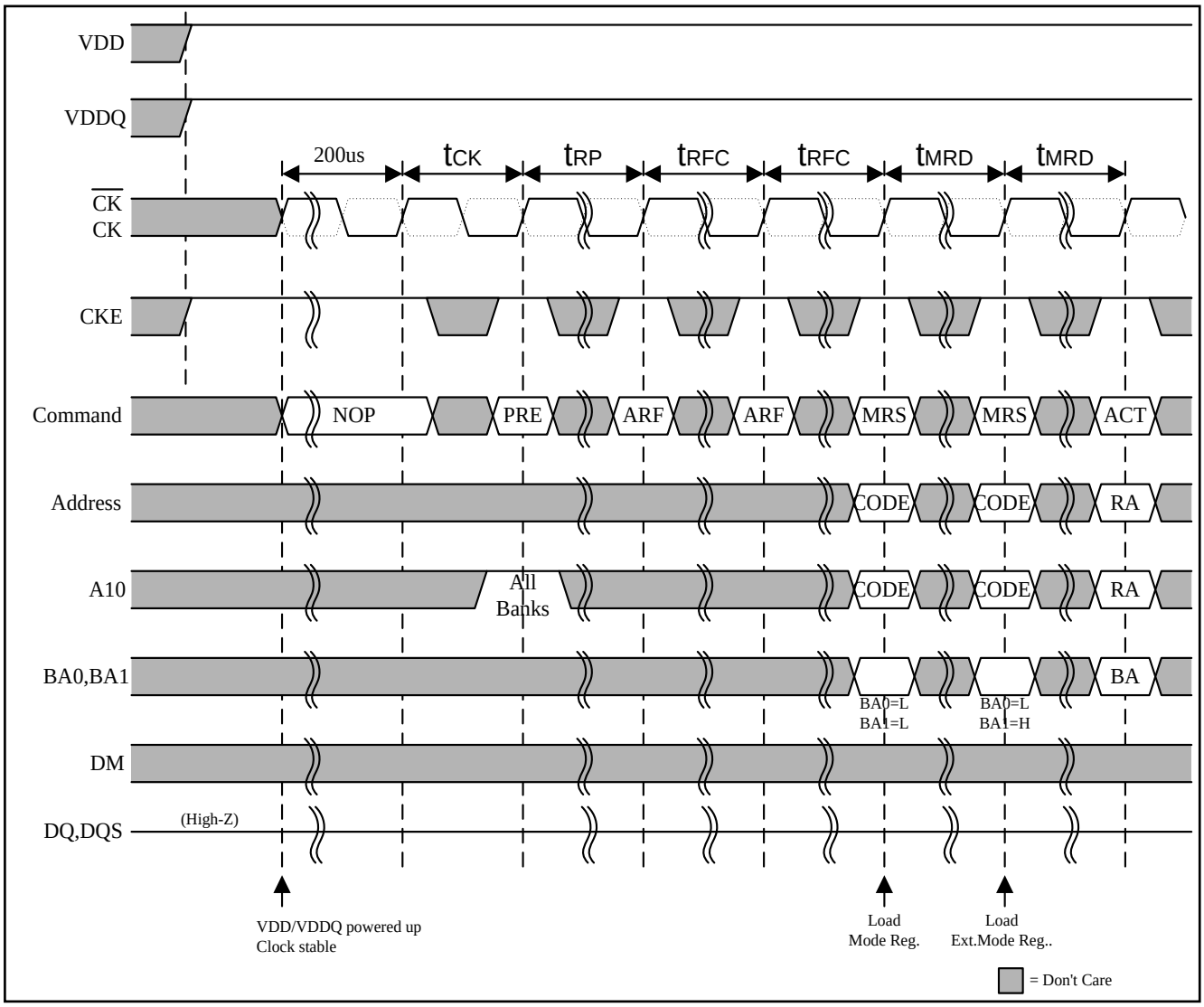
The Mode Register and Extended Mode Register do not have default values. If they are not programmed during the initialization sequence, it may lead to unspecified operation. The clock stop feature is not available until the device has been properly initialized from Step 1 through 11.

- Step 1: Provide power, the device core power (VDD) and the device I/O power (VDDQ) must be brought up simultaneously to prevent device latch-up. Although not required, it is recommended that VDD and VDDQ are from the same power source. Also Assert and hold Clock Enable (CKE) to a LVCMOS logic high level
- Step 2: Once the system has established consistent device power and CKE is driven high, it is safe to apply stable clock.
- Step 3: There must be at least 200μs of valid clocks before any command may be given to the DRAM. During this time NOP or DESELECT commands must be issued on the command bus.
- Step 4: Issue a PRECHARGE ALL command.
- Step 5: Provide NOPs or DESELECT commands for at least tRP time.
- Step 6: Issue an AUTO REFRESH command followed by NOPs or DESELECT command for at least tRFC time. Issue the second AUTO REFRESH command followed by NOPs or DESELECT command for at least tRFC time. Note as part of the initialization sequence there must be two Auto Refresh commands issued. The typical flow is to issue them at Step 6, but they may also be issued between steps 10 and 11.
- Step 7: Using the MRS command, program the base mode register. Set the desired operation modes.
- Step 8: Provide NOPs or DESELECT commands for at least tMRD time.
- Step 9: Using the MRS command, program the extended mode register for the desired operating modes. Note the order of the base and extended mode register programmed is not important.
- Step 10: Provide NOP or DESELECT commands for at least tMRD time.
- Step 11: The DRAM has been properly initialized and is ready for any valid command.

6.1.1 Initialization Flow Diagram



6.1.2 Initialization Waveform Sequence



6.2 Mode Register Set Operation

The Mode Register is used to define the specific mode of operation of the LPDDR SDRAM. This definition includes the definition of a burst length, a burst type, a CAS latency as shown in the following figure.

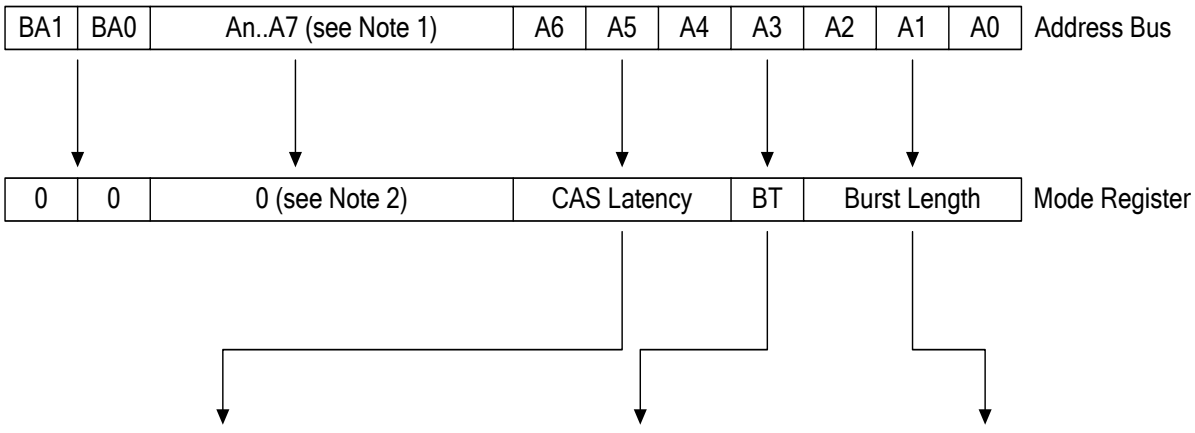
The Mode Register is programmed via the MODE REGISTER SET command (with BA0=0 and BA1=0) and will retain the stored information until it is reprogrammed, the device goes into Deep Power Down mode, or the device loses power.

Mode Register bits A0-A2 specify the burst length, A3 the type of burst (sequential or interleave), A4-A6 the CAS latency. A logic 0 should be programmed to all the undefined addresses bits to ensure future compatibility.

The Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time tMRD before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

6.3 Mode Register Definition



A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A3	Burst Type
0	Sequential
1	Interleave

A2	A1	A0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

NOTE:
1.MSB depends on LPDDR SDRAM density.
2.Alogic 0 should be programmed to all unused / undefined address bits to future compatibility.

6.3.1 Burst Length

Read and write accesses to the LPDDR SDRAM are burst oriented, with the burst length and burst type being programmable.

The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within the block, meaning that the burst will wrap within the block if a boundary is reached.

The block is uniquely selected by A1−An when the burst length is set to two, by A2−An when the burst length is set to 4, by A3−An when the burst length is set to 8 (where An is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both read and write bursts.

6.3.2 Burst Definition

Burst Length	Starting Column Address				Order Of Accesses Within A Burst (Hexadecimal Notation)	
	A3	A2	A1	A0	Sequential	Interleaved
2				0	0 – 1	0 – 1
				1	1 – 0	1 – 0
4			0	0	0 – 1 – 2 – 3	0 – 1 – 2 – 3
			0	1	1 – 2 – 3 – 0	1 – 0 – 3 – 2
			1	0	2 – 3 – 0 – 1	2 – 3 – 0 – 1
			1	1	3 – 0 – 1 – 2	3 – 2 – 1 – 0
8		0	0	0	0 – 1 – 2 – 3 – 4 – 5 – 6 – 7	0 – 1 – 2 – 3 – 4 – 5 – 6 – 7
		0	0	1	1 – 2 – 3 – 4 – 5 – 6 – 7 – 0	1 – 0 – 3 – 2 – 5 – 4 – 7 – 6
		0	1	0	2 – 3 – 4 – 5 – 6 – 7 – 0 – 1	2 – 3 – 0 – 1 – 6 – 7 – 4 – 5
		0	1	1	3 – 4 – 5 – 6 – 7 – 0 – 1 – 2	3 – 2 – 1 – 0 – 7 – 6 – 5 – 4
		1	0	0	4 – 5 – 6 – 7 – 0 – 1 – 2 – 3	4 – 5 – 6 – 7 – 0 – 1 – 2 – 3
		1	0	1	5 – 6 – 7 – 0 – 1 – 2 – 3 – 4	5 – 4 – 7 – 6 – 1 – 0 – 3 – 2
		1	1	0	6 – 7 – 0 – 1 – 2 – 3 – 4 – 5	6 – 7 – 4 – 5 – 2 – 3 – 0 – 1
		1	1	1	7 – 0 – 1 – 2 – 3 – 4 – 5 – 6	7 – 6 – 5 – 4 – 3 – 2 – 1 – 0
16	0	0	0	0	0-1-2-3-4-5-6-7-8-9-A-B-C-D-E-F	0-1-2-3-4-5-6-7-8-9-A-B-C-D-E-F
	0	0	0	1	1-2-3-4-5-6-7-8-9-A-B-C-D-E-F-0	1-0-3-2-5-4-7-6-9-8-B-A-D-C-F-E
	0	0	1	0	2-3-4-5-6-7-8-9-A-B-C-D-E-F-0-1	2-3-0-1-6-7-4-5-A-B-8-9-E-F-C-D
	0	0	1	1	3-4-5-6-7-8-9-A-B-C-D-E-F-0-1-2	3-2-1-0-7-6-5-4-B-A-9-8-F-E-D-C
	0	1	0	0	4-5-6-7-8-9-A-B-C-D-E-F-0-1-2-3	4-5-6-7-0-1-2-3-C-D-E-F-8-9-A-B
	0	1	0	1	5-6-7-8-9-A-B-C-D-E-F-0-1-2-3-4	5-4-7-6-1-0-3-2-D-C-F-E-9-8-B-A
	0	1	1	0	6-7-8-9-A-B-C-D-E-F-0-1-2-3-4-5	6-7-4-5-2-3-0-1-E-F-C-D-A-B-8-9
	0	1	1	1	7-8-9-A-B-C-D-E-F-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0-F-E-D-C-B-A-9-8
	1	0	0	0	8-9-A-B-C-D-E-F-0-1-2-3-4-5-6-7	8-9-A-B-C-D-E-F-0-1-2-3-4-5-6-7
	1	0	0	1	9-A-B-C-D-E-F-0-1-2-3-4-5-6-7-8	9-8-B-A-D-C-F-E-1-0-3-2-5-4-7-6
	1	0	1	0	A-B-C-D-E-F-0-1-2-3-4-5-6-7-8-9	A-B-8-9-E-F-C-D-2-3-0-1-6-7-4-5
	1	0	1	1	B-C-D-E-F-0-1-2-3-4-5-6-7-8-9-A	B-A-9-8-F-E-D-C-3-2-1-0-7-6-5-4
	1	1	0	0	C-D-E-F-0-1-2-3-4-5-6-7-8-9-A-B	C-D-E-F-8-9-A-B-4-5-6-7-0-1-2-3
	1	1	0	1	D-E-F-0-1-2-3-4-5-6-7-8-9-A-B-C	D-C-F-E-9-8-B-A-5-4-7-6-1-0-3-2
	1	1	1	0	E-F-0-1-2-3-4-5-6-7-8-9-A-B-C-D	E-F-C-D-A-B-8-9-6-7-4-5-2-3-0-1
	1	1	1	1	F-0-1-2-3-4-5-6-7-8-9-A-B-C-D-E	F-E-D-C-B-A-9-8-7-6-5-4-3-2-1-0

Notes:

1. For a burst length of two, A1-An selects the two data element block; A0 selects the first access within the block.
2. For a burst length of four, A2-An selects the four data element block; A0-A1 selects the first access within the block.
3. For a burst length of eight, A3-An selects the eight data element block; A0-A2 selects the first access within the block.
4. For the optional burst length of sixteen, A4-An selects the sixteen data element block; A0-A3 selects the first access within the block.
5. Whenever a boundary of the block is reached within a given sequence, the following access wraps within the block.

   When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within the block, meaning that the burst will wrap within the block if a boundary is reached.

   The block is uniquely selected by A1-An when the burst length is set to two, by A2-An when the burst length is set to 4, by A3-An when the burst length is set to 8 and A4-An when the burst length is set to 16(where An is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both read and write bursts.

6.3.3 Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3. The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in the previous table.

6.3.4 Read Latency

The READ latency is the delay between the registration of a READ command and the availability of the first piece of output data. The latency should be set to 2 or 3 clocks.

If a READ command is registered at a clock edge n and the latency is 3 clocks, the first data element will be valid at n + 2 tCK + tAC. If a READ command is registered at a clock edge n and the latency is 2 clocks, the first data element will be valid at n + tCK + tAC.

6.4 Extended Mode Register Description

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include output drive strength selection and Partial Array Self Refresh (PASR). PASR is effective in Self Refresh mode only.

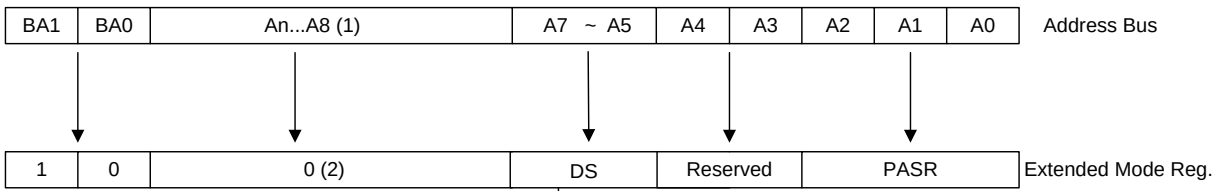
The Extended Mode Register is programmed via the MODE REGISTER SET command (with BA1=1 and BA0=0) and will retain the stored information until it is reprogrammed, the device is put in Deep Power Down mode, or the device loses power.

The Extended Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time tMRD before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

Address bits A0-A2 specify PASR, A5-A7 the Driver Strength. A logic 0 should be programmed to all the undefined addresses bits to ensure future compatibility.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

6.4.1 Extended Mode Register Definition



A7	A6	A5	Drive Strength
0	0	0	Full Strength Driver (default)
0	0	1	Half Strength Driver
0	1	0	Quarter Strength Driver
0	1	1	Octant Strength Driver
1	0	0	Three-Quarters Strength Driver

A2	A1	A0	PASR
0	0	0	All banks
0	0	1	1/2 array (BA1=0)
0	1	0	1/4 array (BA1=BA0=0)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

NOTES:
1.MSB depends on mobile DDR SDRAM density.
2.A logic 0 should be programmed to all unused / undefined bits to ensure future compatibility.

6.4.2 Partial Array Self Refresh

With partial array self refresh (PASR), the self refresh may be restricted to a variable portion of the total array. The whole array (default), 1/2 array, or 1/4 array could be selected. Data outside the defined area will be lost. Address bits A0 to A2 are used to set PASR.

6.4.3 Automatic Temperature Compensated Self Refresh

The device has an Automatic Temperature Compensated Self Refresh feature. It automatically adjusts the refresh rate based on the device temperature without any register update needed.

6.4.4 Output Drive Strength

The drive strength could be set to full, half, quarter, three-quarter, octant strength via address bits A5 and A6. The half drive strength option is intended for lighter loads or point-to-point environments.

6.5 Status Register Read

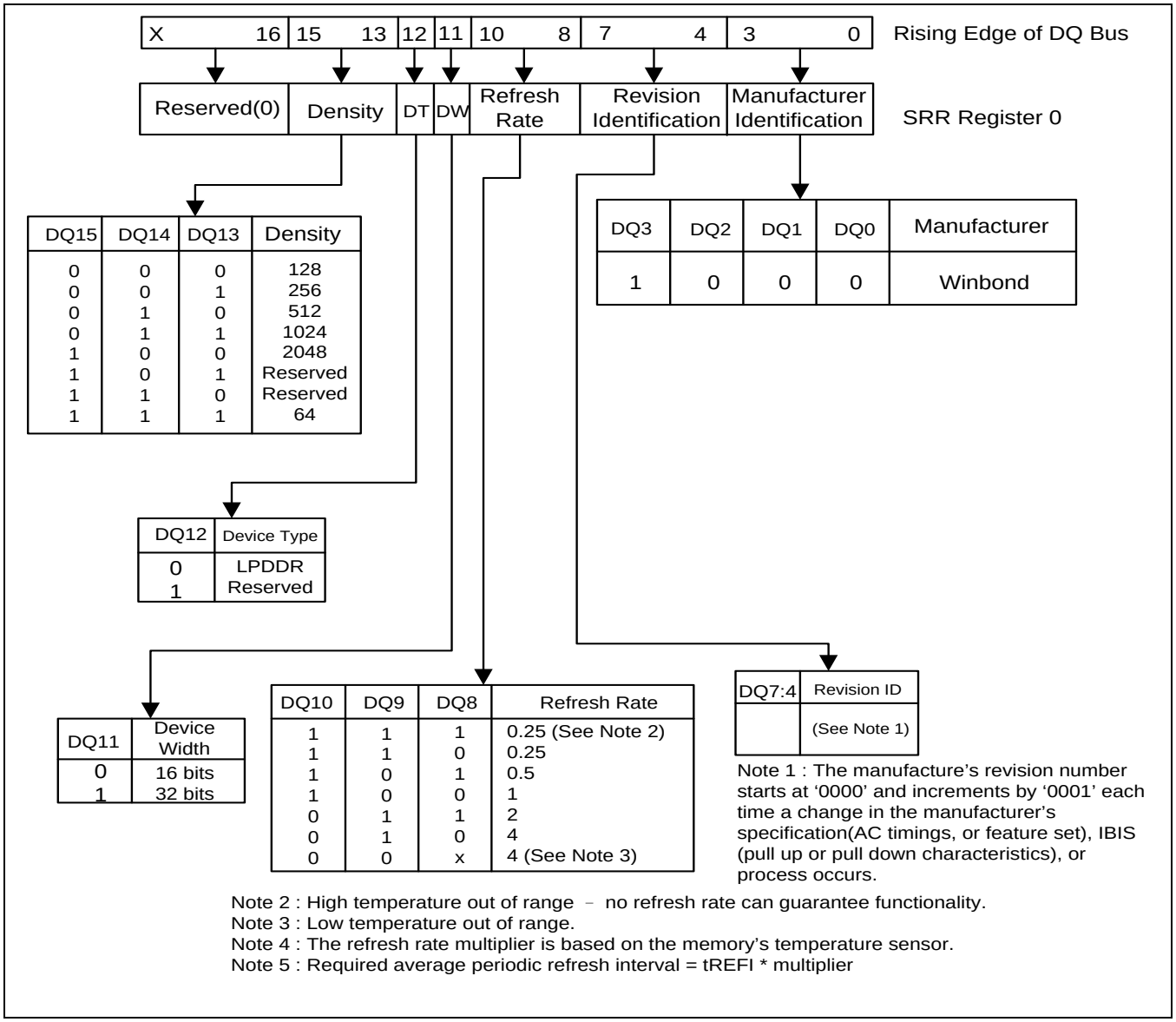
Status Register Read (SRR) is an optional feature in JEDEC, and it is implemented in this device. With SRR, a method is defined to read registers from the device. The encoding for an SRR command is the same as a MRS with BA[1:0]=”01”. The address pins (A[n:0]) encode which register is to be read. Currently only one register is defined at A[n:0]=0. The sequence to perform an SRR command is as follows:

- All reads/writes must be completed
- All banks must be closed
- MRS with BA=01 is issued (SRR)
- Wait tSRR
- Read issued to any bank/page
- CAS latency cycles later the device returns the registers data as it would a normal read
- The next command to the device can be issued tSRC after the Read command was issued.

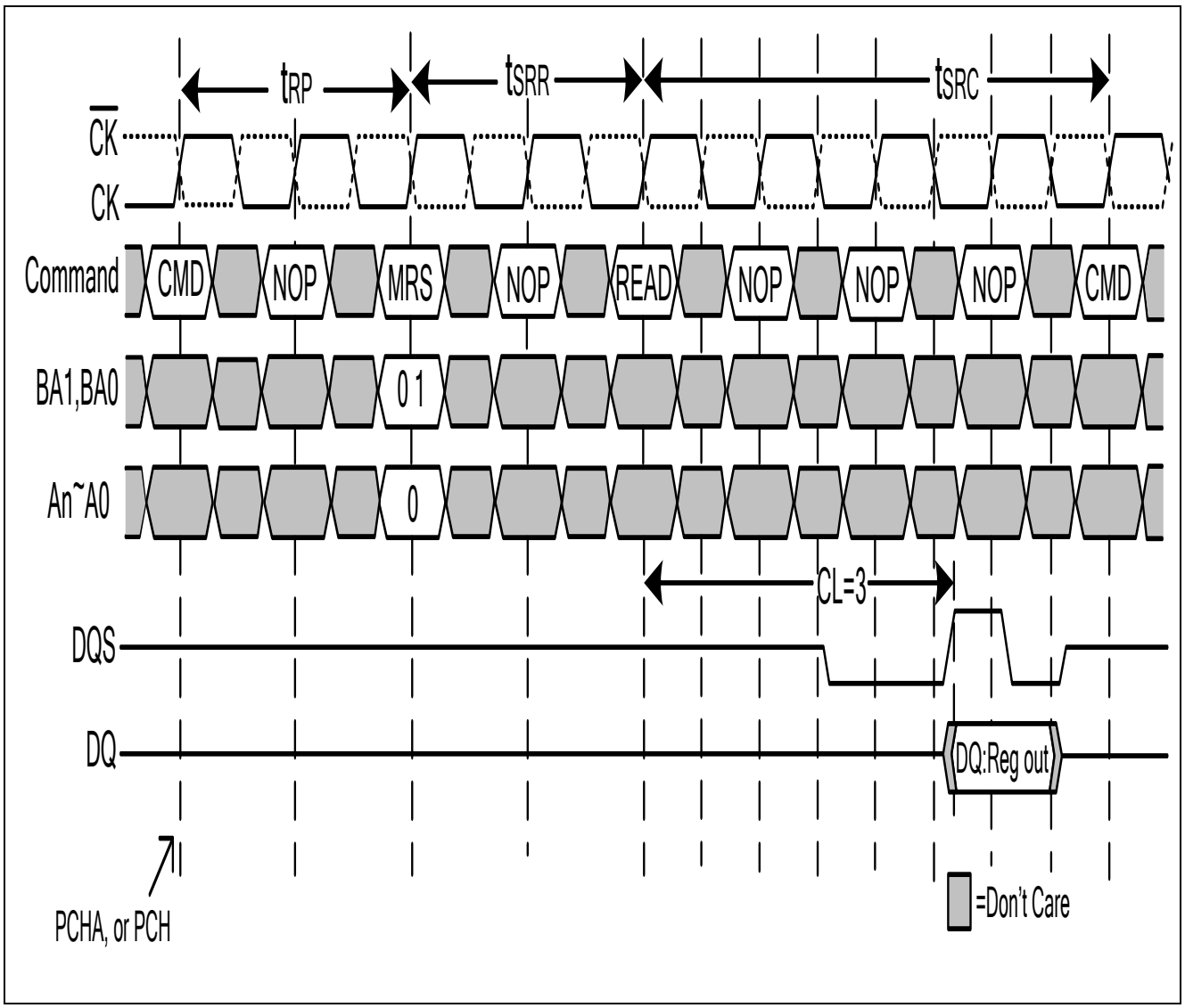
The burst length for the SRR read is always fixed to length 2.

6.5.1 SRR Register Definition

Default: (A[n:0] = 0)



6.5.2 Status Register Read Timing Diagram



Notes :

1.SRR can only be issued after power-up sequence is complete.

2.SRR can only be issued with all banks precharged.

3.SRR CL is unchanged from value in the mode register.

4.SRR BL is fixed at 2.

5.tSRR = 2 (min).

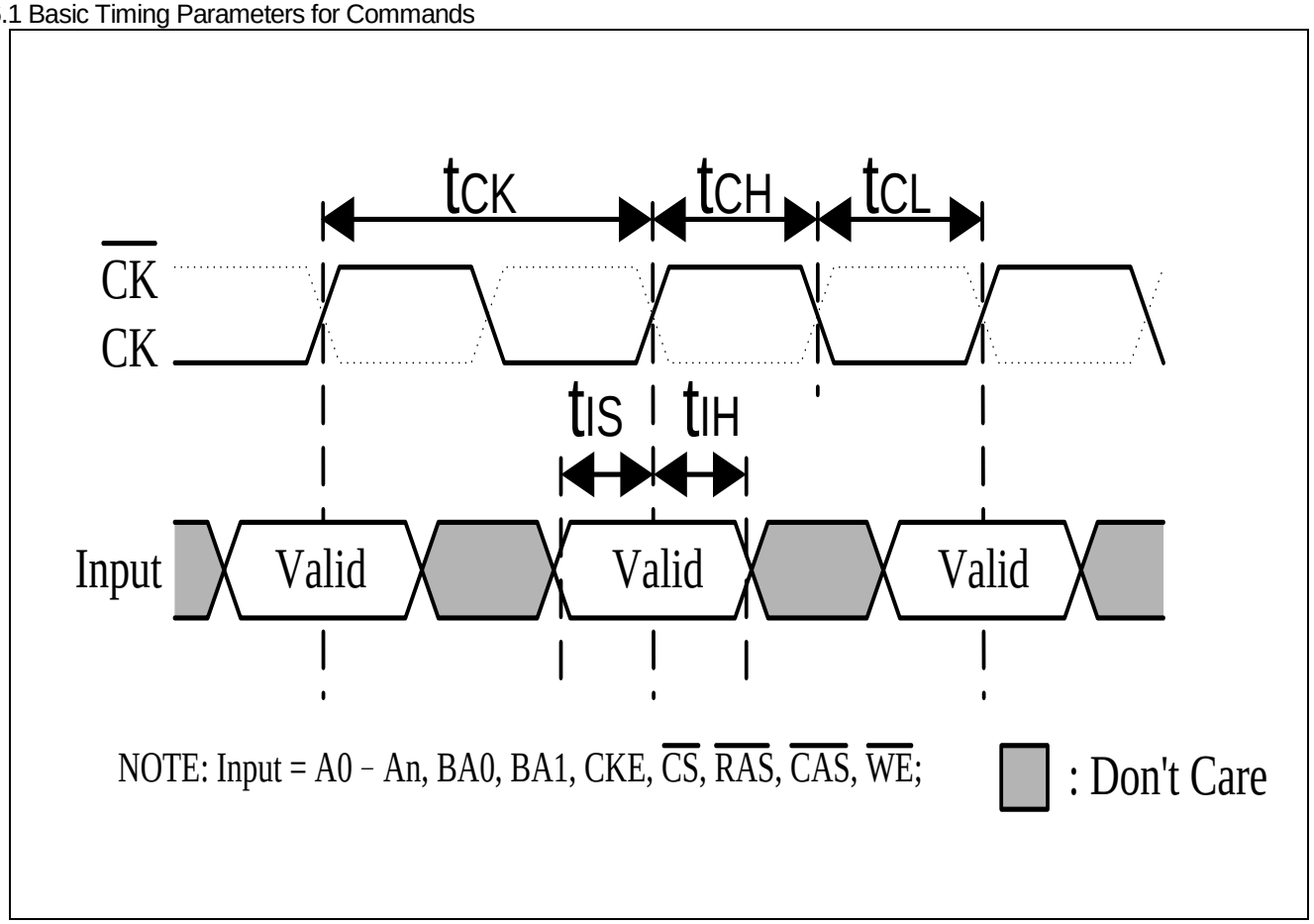
6.tSRC = CL + 1; (min time between read to next valid command)

6.No commands other than NOP and DES are allowed between the SRR and the READ.

6.6 Commands

All commands (address and control signals) are registered on the positive edge of clock (crossing of CK going high and $\overline{CK}$ going low).

6.6.1 Basic Timing Parameters for Commands



6.6.2 Truth Table - Commands

Name (Function)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A10/AP	Addr	Notes
DESELECT (NOP)	H	X	X	X	X	X	X	2
NO OPERATION (NOP)	L	H	H	H	X	X	X	2
ACTIVE (Select Bank and activate row)	L	L	H	H	Valid	Row	Row	
READ (Select bank and column and start read burst)	L	H	L	H	Valid	L	Col	
READ with AP (Read Burst with Auto Precharge)	L	H	L	H	Valid	H	Col	3
WRITE (Select bank and column and start write burst)	L	H	L	L	Valid	L	Col	
WRITE with AP (Write Burst with Auto Precharge)	L	H	L	L	Valid	H	Col	3
BURST TERMINATE or enter DEEP POWER DOWN	L	H	H	L	X	X	X	4, 5
PRECHARGE (Deactivate Row in selected bank)	L	L	H	L	Valid	L	X	6
PRECHARGE ALL (Deactivate rows in all banks)	L	L	H	L	X	H	X	6
AUTO REFRESH or enter SELF REFRESH	L	L	L	H	X	X	X	7, 8, 9
MODE REGISTER SET	L	L	L	L	Valid	Op-code		10

Notes:

1.All states and sequences not shown are illegal or reserved.
2.DESELECT and NOP are functionally interchangeable.
3.Auto precharge is non-persistent. A10 High enables Auto precharge, while A10 Low disables Auto precharge.
4.Burst Terminate applies to only Read bursts with Autoprecharge disabled. This command is undefined and should not be used for Read with Auto precharge enabled, and for Write bursts.
5.This command is BURST TERMINATE if CKE is High and DEEP POWER DOWN entry if CKE is Low.
6.If A10 is low, bank address determines which bank is to be precharged. If A10 is high, all banks are precharged and BA0~BA1 are don't care.
7.This command is AUTO REFRESH if CKE is High and SELF REFRESH if CKE is low.
8.All address inputs and I/O are 'don't care' except for CKE. Internal refresh counters control bank and row addressing.
9.All banks must be precharged before issuing an AUTO-REFRESH or SELF REFRESH command.
10.BA0 and BA1 value select between MRS and EMRS.
11.CKE is HIGH for all commands shown except SELF REFRESH and DEEP POWER-DOWN.

6.6.3 Truth Table - DM Operations

Function	DM	DQ	Notes
Write Enable	L	Valid	1
Write Inhibit	H	X	1

Notes:Used to mask write data, provided coincident with the corresponding data.

6.6.4 Truth Table - CKE

CKEn-1	CKEn	Current State	COMMANDn	ACTIONn	Notes
L	L	Power Down	X	Maintain Power Down	
L	L	Self Refresh	X	Maintain Self Refresh	
L	L	Deep Power Down	X	Maintain Deep Power Down	
L	H	Power Down	NOP or DESELECT	Exit Power Down	5, 6, 9
L	H	Self Refresh	NOP or DESELECT	Exit Self Refresh	5, 7, 10
L	H	Deep Power Down	NOP or DESELECT	Exit Deep Power Down	5, 8
H	L	All Banks Idle	NOP or DESELECT	Precharge Power Down Entry	5
H	L	Bank(s) Active	NOP or DESELECT	Active Power Down Entry	5
H	L	All Banks Idle	AUTO REFRESH	Self Refresh Entry	
H	L	All Banks Idle	BURST TERMINATE	Enter Deep Power Down	
H	H	See the other Truth Tables			

Notes:

1.CKEn is the logic state of CKE at clock edge n; CKEn-1 was the state of CKE at the previous clock edge.
2.Current state is the state of LPDDR immediately prior to clock edge n.
3.COMMANDn is the command registered at clock edge n, and ACTIONn is the result of COMMANDn.
4.All states and sequences not shown are illegal or reserved.
5.DESELECT and NOP are functionally interchangeable.
6.Power Down exit time (tXP) should elapse before a command other than NOP or DESELECT is issued.
7.SELF REFRESH exit time (tXSR) should elapse before a command other than NOP or DESELECT is issued.
8.The Deep Power-Down exit procedure must be followed as discussed in the Deep Power-Down section of the Functional Description.
9.The clock must toggle at least once during the tXP period.
10.The clock must toggle at least once during the tXSR time.

6.6.5 Truth Table - Current State BANKn - Command to BANKn

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command	Action	Notes
Any	H	X	X	X	DESELECT	NOP or Continue previous operation	
	L	H	H	H	No Operation	NOP or Continue previous operation	
Idle	L	L	H	H	ACTIVE	Select and activate row	
	L	L	L	H	AUTO REFRESH	Auto refresh	10
	L	L	L	L	MRS	Mode register set	10
Row Active	L	H	L	H	READ	Select column & start read burst	
	L	H	L	L	WRITE	Select column & start write burst	
	L	L	H	L	PRECHARGE	Deactivate row in bank (or banks)	4
Read (Auto precharge Disabled)	L	H	L	H	READ	Select column & start new read burst	5, 6
	L	H	L	L	WRITE	Select column & start write burst	5, 6, 13
	L	L	H	L	PRECHARGE	Truncate read burst, start precharge	
	L	H	H	L	BURST TERMINATE	Burst terminate	11
Write (Auto precharge Disabled)	L	H	L	H	READ	Select column & start read burst	5, 6, 12
	L	H	L	L	WRITE	Select column & start new write burst	5, 6
	L	L	H	L	PRECHARGE	Truncate write burst & start precharge	12

Notes:

1. The table applies when both CKEn-1 and CKEn are HIGH, and after tXSR or tXP has been met if the previous state was Self Refresh or Power Down.
2. DESELECT and NOP are functionally interchangeable.
3. All states and sequences not shown are illegal or reserved.
4. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
5. A command other than NOP should not be issued to the same bank while a READ or WRITE burst with Auto Precharge is enabled.
6. The new Read or Write command could be Auto Prechrge enabled or Auto Precharge disabled.
7. Current State Definitions:
   Idle: The bank has been precharged, and tRP has been met.
   Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A READ burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Write: A WRITE burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
8. The following states must not be interrupted by a command issued to the same bank. DESEDECT or NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and this table, and according to next table.
   Precharging: Starts with the registration of a PRECHARGE command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.
   Row Activating: Starts with registration of an ACTIVE command and ends when tRCD is met. Once tRCD is met, the bank will be in the 'row active' state.
   Read with AP Enabled: Starts with the registration of the READ command with Auto Precharge enabled and ends when tRP has been met. Once tRP has been met, the bank will be in the idle state.
   Write with AP Enabled: Starts with registration of a WRITE command with Auto Precharge enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.
9. The following states must not be interrupted by any executable command; DESEDECT or NOP commands must be applied to each positive clock edge during these states.
   Refreshing: Starts with registration of an AUTO REFRESH command and ends when tRFC is met. Once tRFC is met, the LPDDR will be in an 'all banks idle' state.
   Accessing Mode Register: Starts with registration of a MODE REGISTER SET command and ends when tMRD has been met. Once tMRD is met, the LPDDR will be in an 'all banks idle' state.

Precharging All: Starts with the registration of a PRECHARGE ALL command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.

10.Not bank-specific; requires that all banks are idle and no bursts are in progress.
11.Not bank-specific. BURST TERMINATE affects the most recent READ burst, regardless of bank.
12.Requires appropriate DM masking.
13.A WRITE command may be applied after the completion of the READ burst; otherwise, a BURST TERMINATE must be used to end the READ prior to asserting a WRITE command.

6.6.6 Truth Table - Current State BANKn, Command to BANKm

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command	Action	Notes
Any	H	X	X	X	DESELECT	NOP or Continue previous Operation	
	L	H	H	H	NOP	NOP or Continue previous Operation	
Idle	X	X	X	X	ANY	Any command allowed to bank m	
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE	Select and activate row	
	L	H	L	H	READ	Select column & start read burst	8
	L	H	L	L	WRITE	Select column & start write burst	8
	L	L	H	L	PRECHARGE	Precharge	
Read with Auto Precharge disabled	L	L	H	H	ACTIVE	Select and activate row	
	L	H	L	H	READ	Select column & start new read burst	8
	L	H	L	L	WRITE	Select column & start write burst	8,10
	L	L	H	L	PRECHARGE	Precharge	
Write with Auto Precharge disabled	L	L	H	H	ACTIVE	Select and activate row	
	L	H	L	H	READ	Select column & start read burst	8, 9
	L	H	L	L	WRITE	Select column & start new write burst	8
	L	L	H	L	PRECHARGE	Precharge	
Read with Auto Precharge	L	L	H	H	ACTIVE	Select and activate row	
	L	H	L	H	READ	Select column & start new read burst	5, 8
	L	H	L	L	WRITE	Select column & start write burst	5, 8, 10
	L	L	H	L	PRECHARGE	Precharge	
Write with Auto Precharge	L	L	H	H	ACTIVE	Select and activate row	
	L	H	L	H	READ	Select column & start read burst	5, 8
	L	H	L	L	WRITE	Select column & start new write burst	5, 8
	L	L	H	L	PRECHARGE	Precharge	

Notes:
1.The table applies when both CKEn-1 and CKEn are HIGH, and after tXSR or tXP has been met if the previous state was Self Refresh or Power Down.
2.DESELECT and NOP are functionally interchangeable.
3.All states and sequences not shown are illegal or reserved.
4.Current State Definitions:
Idle: The bank has been precharged, and tRP has been met.
Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
Read: A READ burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
Write: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
5.Read with AP enabled and Write with AP enabled: The read with Auto Precharge enabled or Write with Auto Precharge enabled states can be broken into two parts: the access period and the precharge period. For Read with AP, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all the data in the burst. For Write with Auto precharge, the precharge period begins when tWR ends, with tWR measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or tRP) begins. During the precharge period, of the Read with Auto Precharge enabled or Write with Auto Precharge enabled states, ACTIVE, PRECHARGE, READ, and WRITE commands to the other bank may be applied; during the access period, only ACTIVE and PRECHARGE commands to the other banks may be applied. In either case, all other related limitations apply (e.g. contention between READ data and WRITE data must be avoided).
6.AUTO REFRESH, SELF REFRESH, and MODE REGISTER SET commands may only be issued when all bank are idle.
7.A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
8.READs or WRITEs listed in the Command column include READs and WRITEs with Auto Precharge enabled and READs and WRITEs with Auto Precharge disabled.
9.Requires appropriate DM masking.
10.A WRITE command may be applied after the completion of data output, otherwise a BURST TERMINATE command must be issued to end the READ prior to asserting a WRITE command.

7. OPERATION

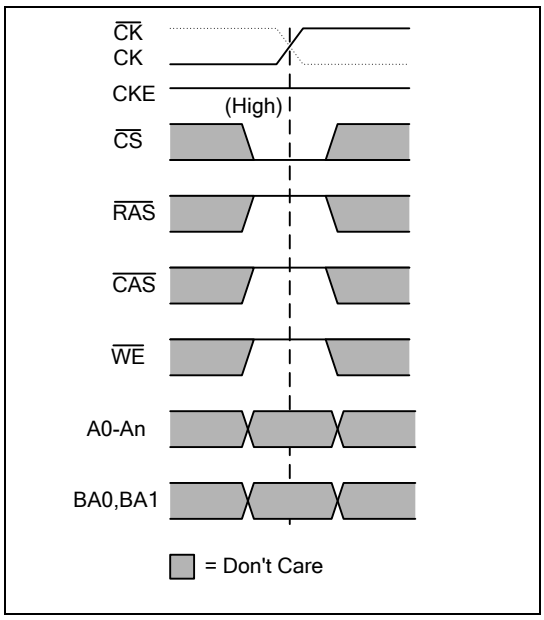
7.1. Deselect

The DESELECT function ($\overline{CS}$ = high) prevents new commands from being executed by the LPDDR SDRAM. The LPDDR SDRAM is effectively deselected. Operations already in progress are not affected.

7.2. No Operation

The NO OPERATION (NOP) command is used to perform a NOP to a LPDDR SDRAM that is selected ($\overline{CS}$=Low). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

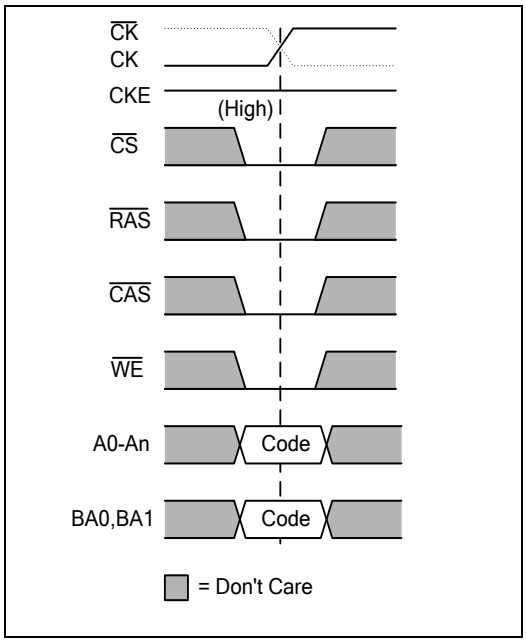
7.2.1 NOP Command



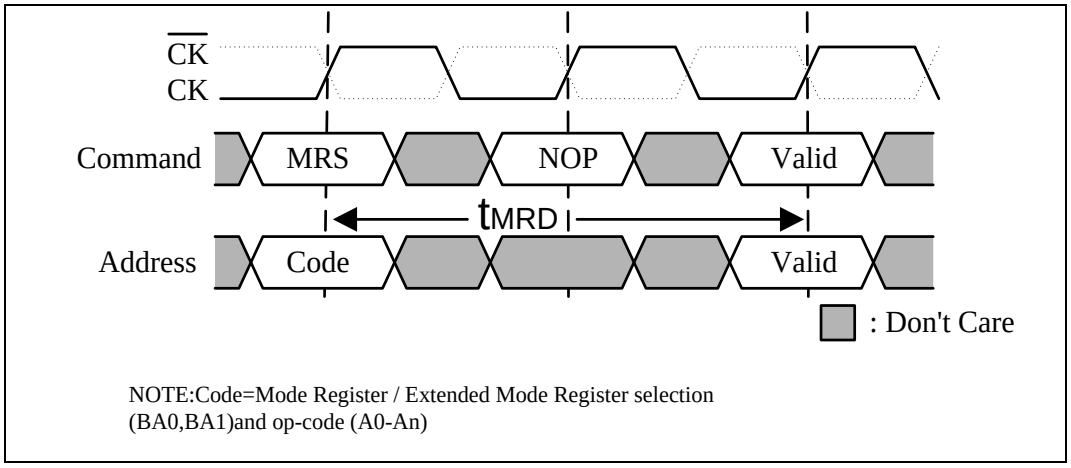
7.3 Mode Register Set

The Mode Register and the Extended Mode Register are loaded via the address inputs. The MODE REGISTER SET command can only be issued when all banks are idle and no bursts are in progress, and a subsequent executable command cannot be issued until tMRD is met.

7.3.1 Mode Register Set Command



7.3.2 Mode Register Set Command Timing



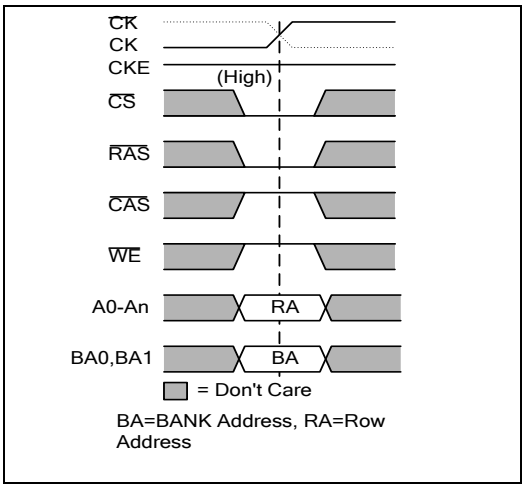
7.4. Active

Before any READ or WRITE commands can be issued to a bank in the LPDDR SDRAM, a row in that bank must be opened. This is accomplished by the ACTIVE command: BA0 and BA1 select the bank, and the address inputs select the row to be activated. More than one bank can be active at any time.

Once a row is open, a READ or WRITE command could be issued to that row, subject to the tRCD specification.

A subsequent ACTIVE command to another row in the same bank can only be issued after the previous row has been closed. The minimum time interval between two successive ACTIVE commands on the same bank is defined by tRC.

7.4.1 Active Command

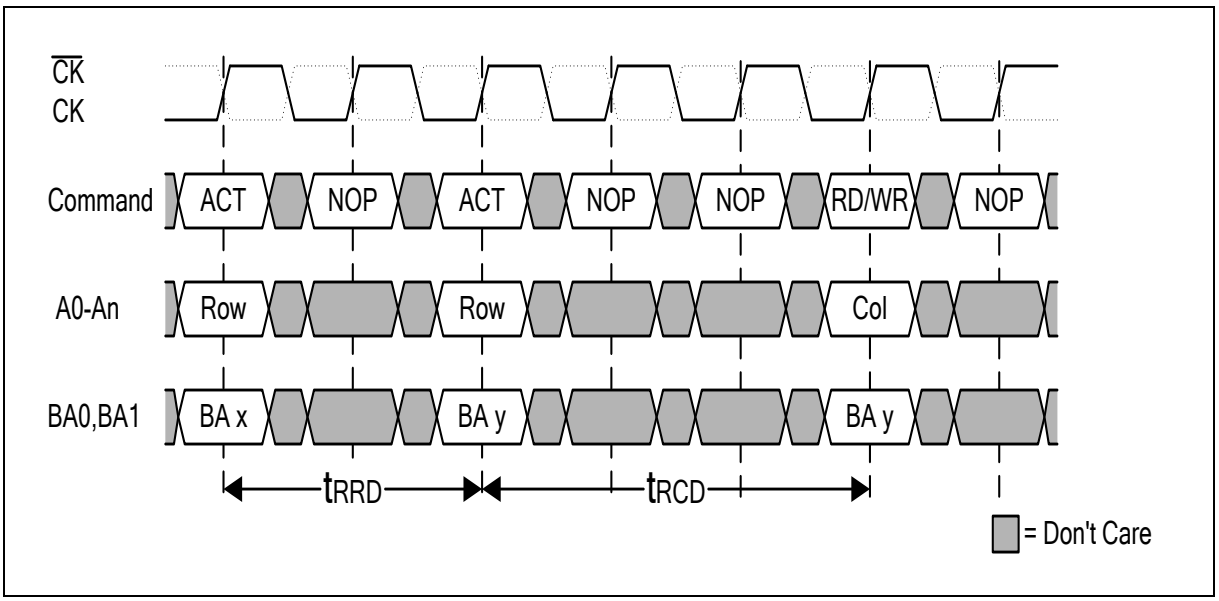


A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between two successive ACTIVE commands on different banks is defined by tRRD.

The row remains active until a PRECHARGE command (or READ or WRITE command with Auto Precharge) is issued to the bank.

A PRECHARGE (or READ with Auto Precharge or Write with Auto Precharge) command must be issued before opening a different row in the same bank.

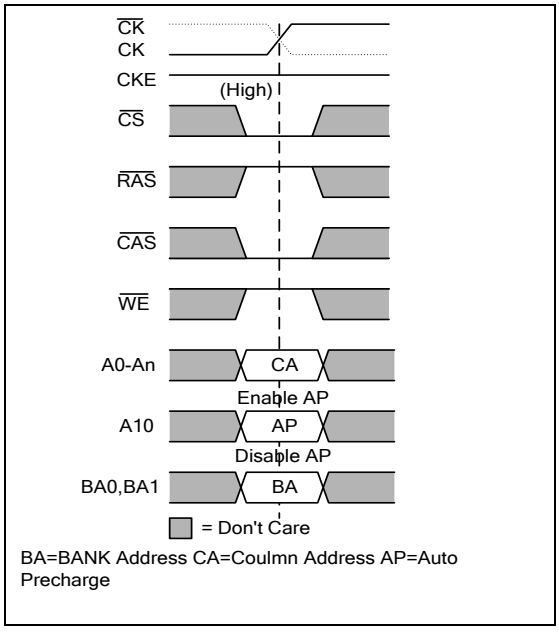
7.4.2 Bank Activation Command Cycle



7.5. Read

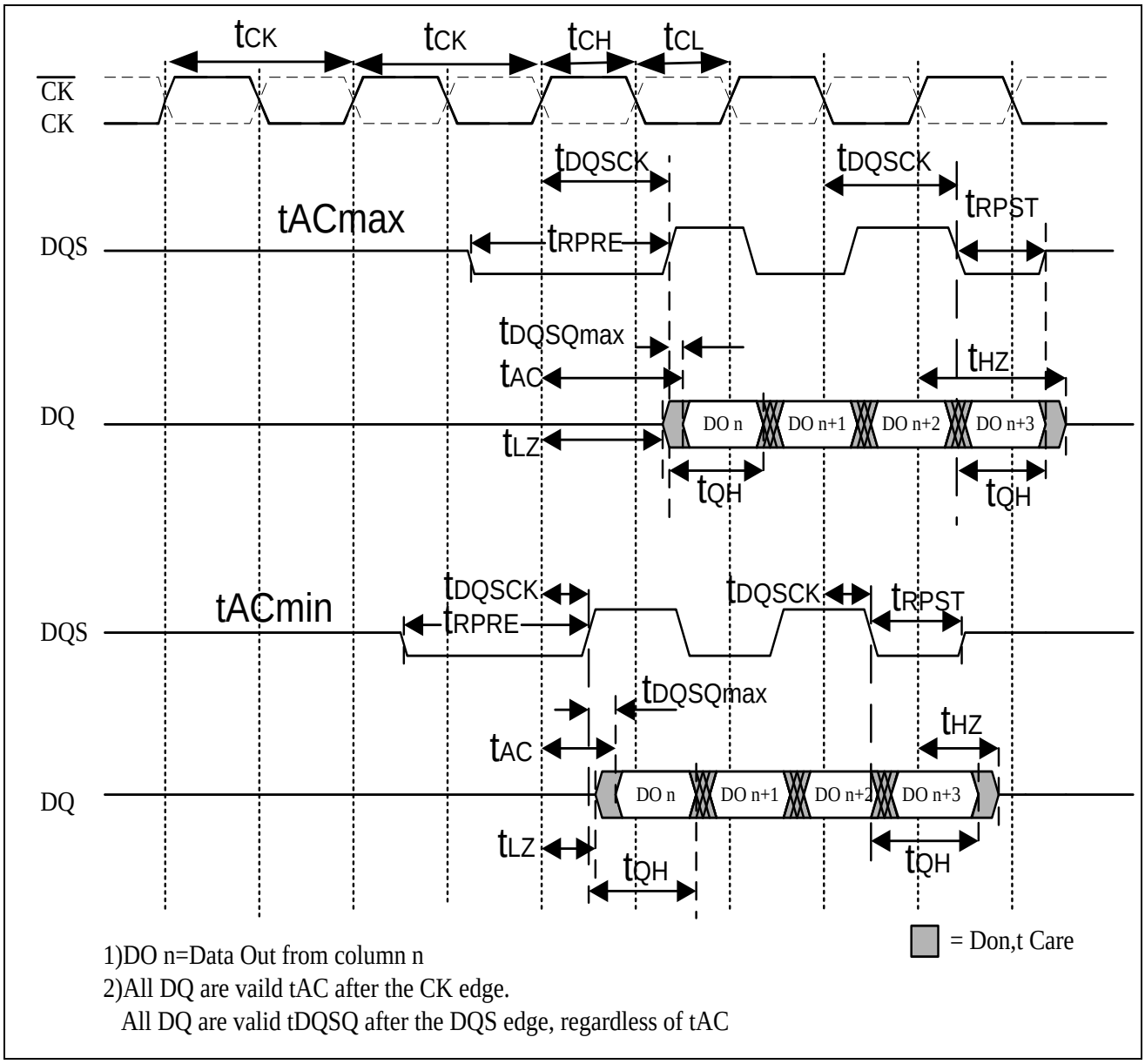
The READ command is used to initiate a burst read access to an active row, with a burst length as set in the Mode Register. BA0 and BA1 select the bank, and the address inputs select the starting column location. The value of A10 determines whether or not Auto Pre-charge is used. If Auto Pre-charge is selected, the row being accessed will be pre-charged at the end of the read burst; if Auto Pre-charge is not selected, the row will remain open for subsequent accesses.

7.5.1 Read Command



The basic Read timing parameters for DQs are shown in following figure; they apply to all Read operations.

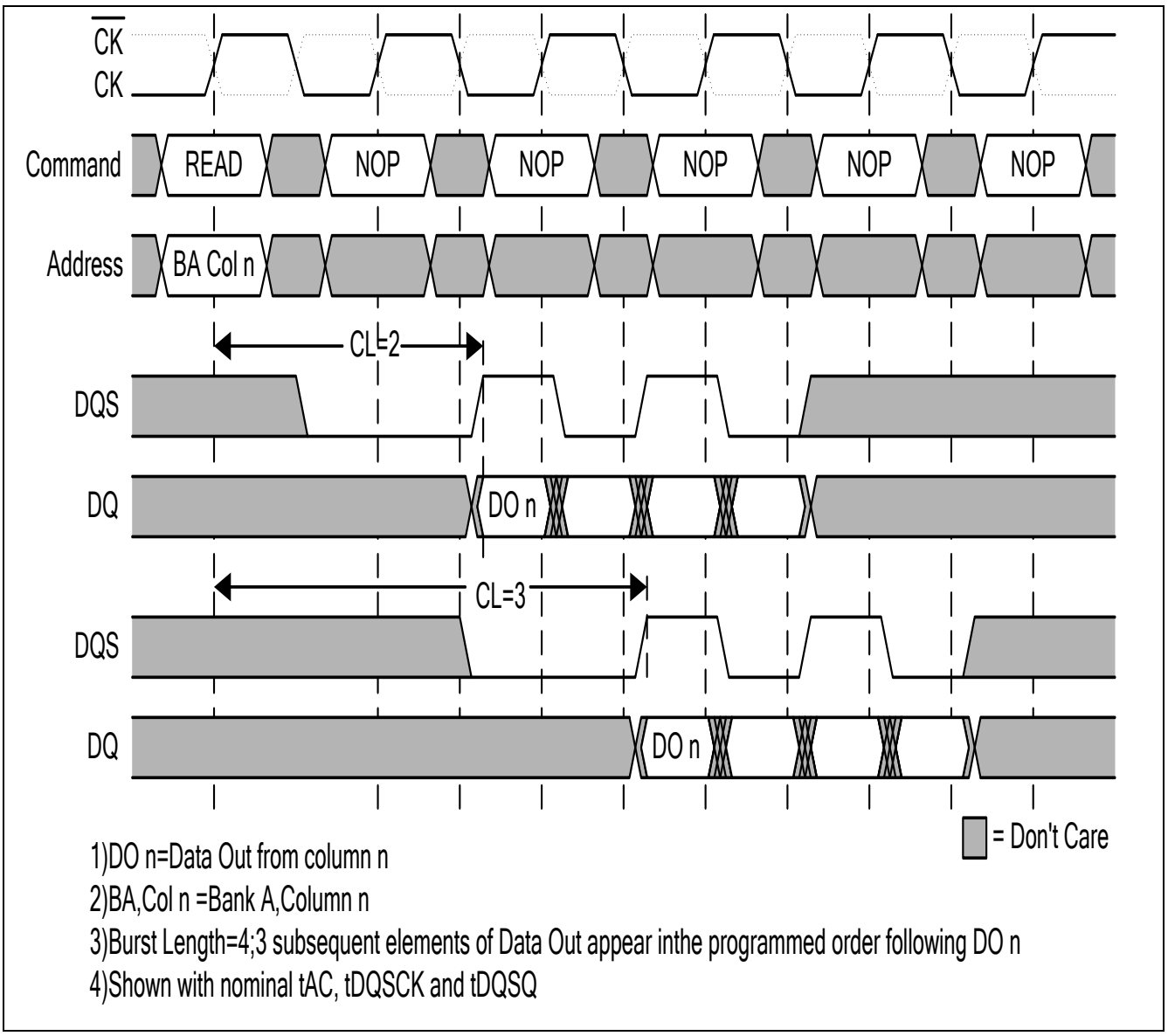
7.5.2 Basic Read Timing Parameters



During Read bursts, DQS is driven by the LPDDR SDRAM along with the output data. The initial Low state of the DQS is known as the read preamble; the Low state coincident with last data-out element is known as the read post-amble. The first data-out element is edge aligned with the first rising edge of DQS and the successive data-out elements are edge aligned to successive edges of DQS. This is shown in following figure with a CAS latency of 2 and 3.

Upon completion of a read burst, assuming no other READ command has been initiated, the DQs will go to High-Z.

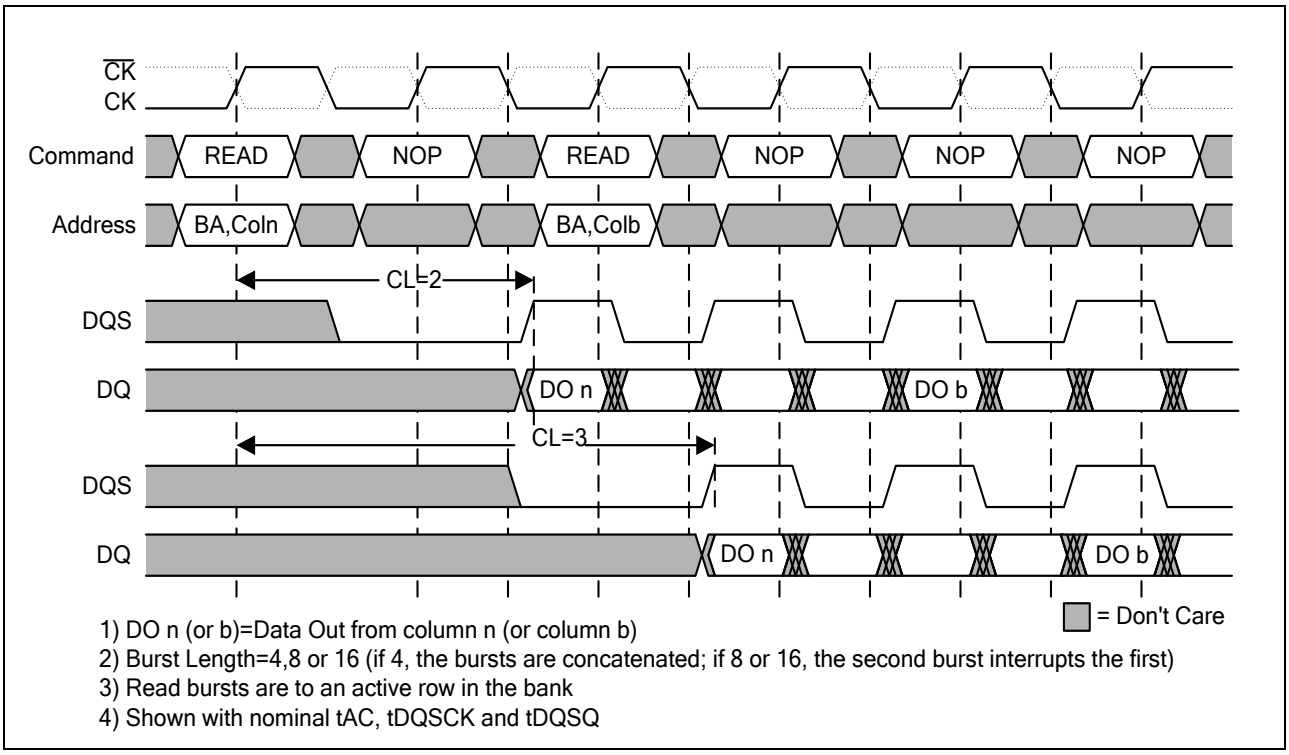
7.5.3 Read Burst Showing CAS Latency



7.5.4 Read to Read

Data from a read burst may be concatenated or truncated by a subsequent READ command. The first data from the new burst follows either the last element of a completed burst or the last desired element of a longer burst that is being truncated. The new READ command should be issued X cycles after the first READ command, where X equals the number of desired data-out element pairs (pairs are required by the 2n-prefetch architecture). This is shown in following figure.

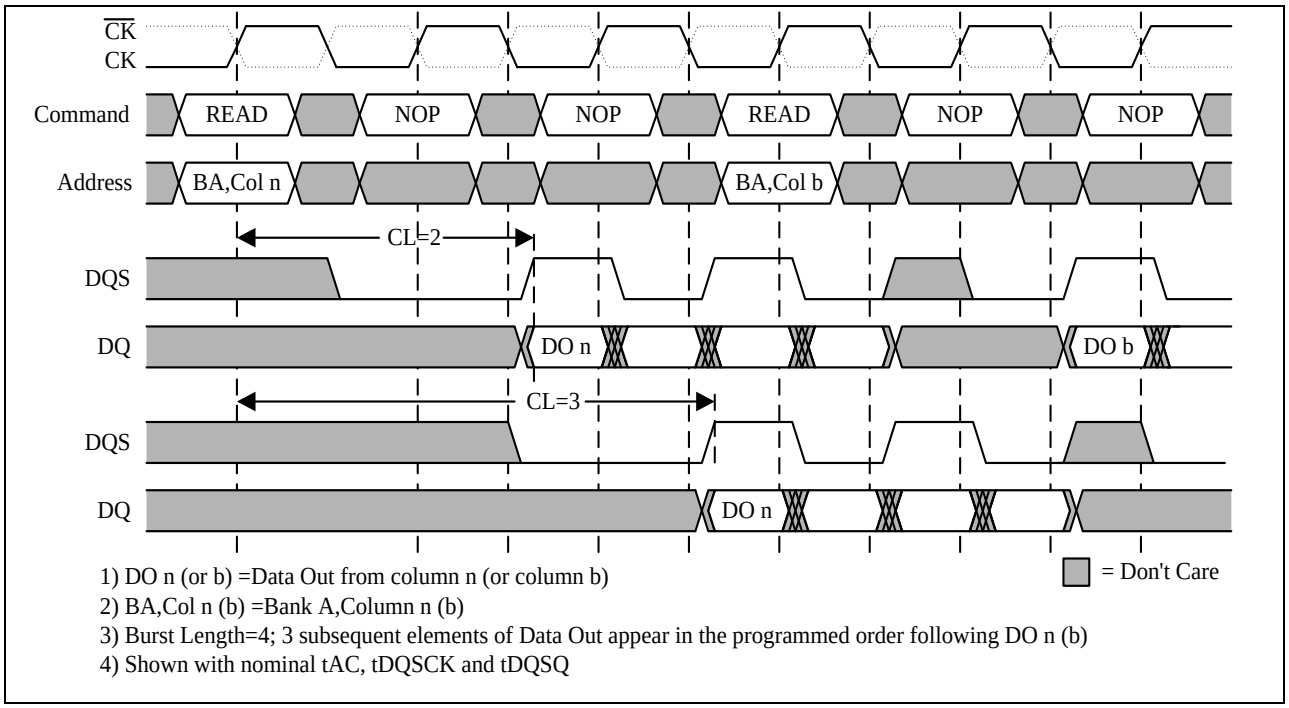
7.5.5 Consecutive Read Bursts



1) DO n (or b)=Data Out from column n (or column b)
2) Burst Length=4,8 or 16 (if 4, the bursts are concatenated; if 8 or 16, the second burst interrupts the first)
3) Read bursts are to an active row in the bank
4) Shown with nominal tAC, tDQSCK and tDQSQ

7.5.6 Non-Consecutive Read Bursts

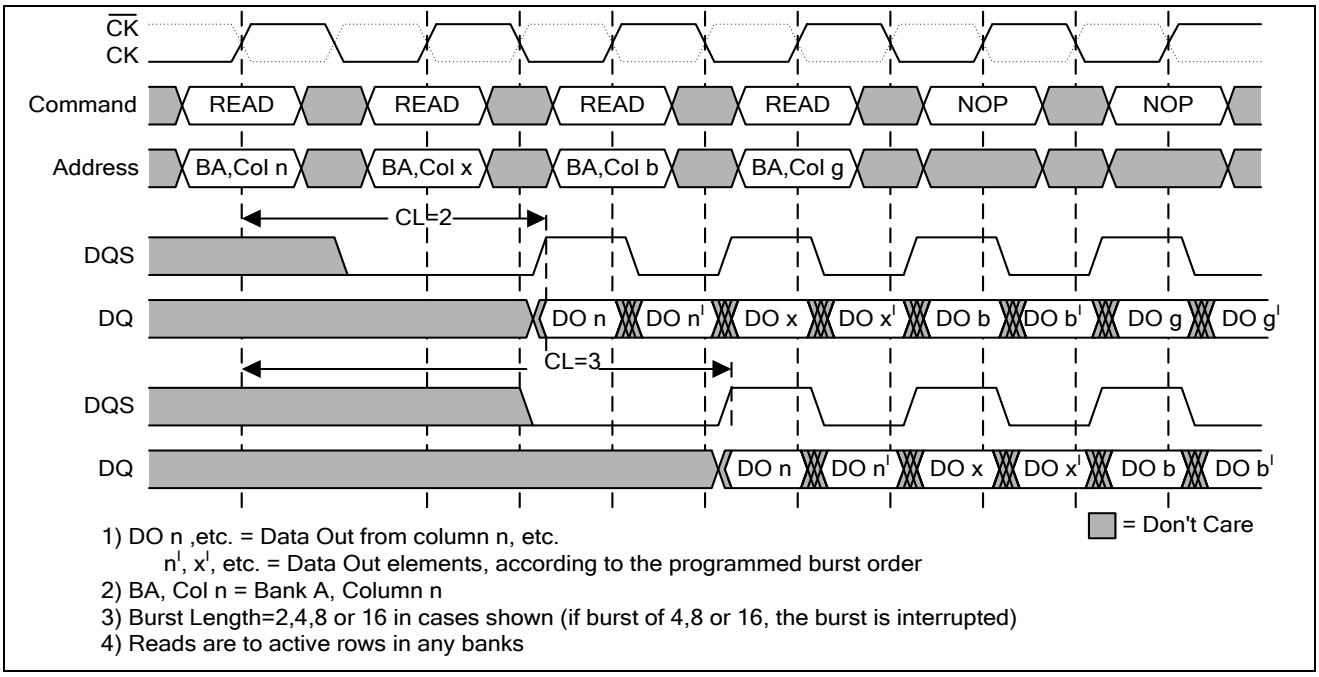
A READ command can be initiated on any clock cycle following a previous READ command. Non-consecutive Reads are shown in following figure.



1) DO n (or b) =Data Out from column n (or column b)
2) BA,Col n (b) =Bank A,Column n (b)
3) Burst Length=4; 3 subsequent elements of Data Out appear in the programmed order following DO n (b)
4) Shown with nominal tAC, tDQSCK and tDQSQ

7.5.7 Random Read Bursts

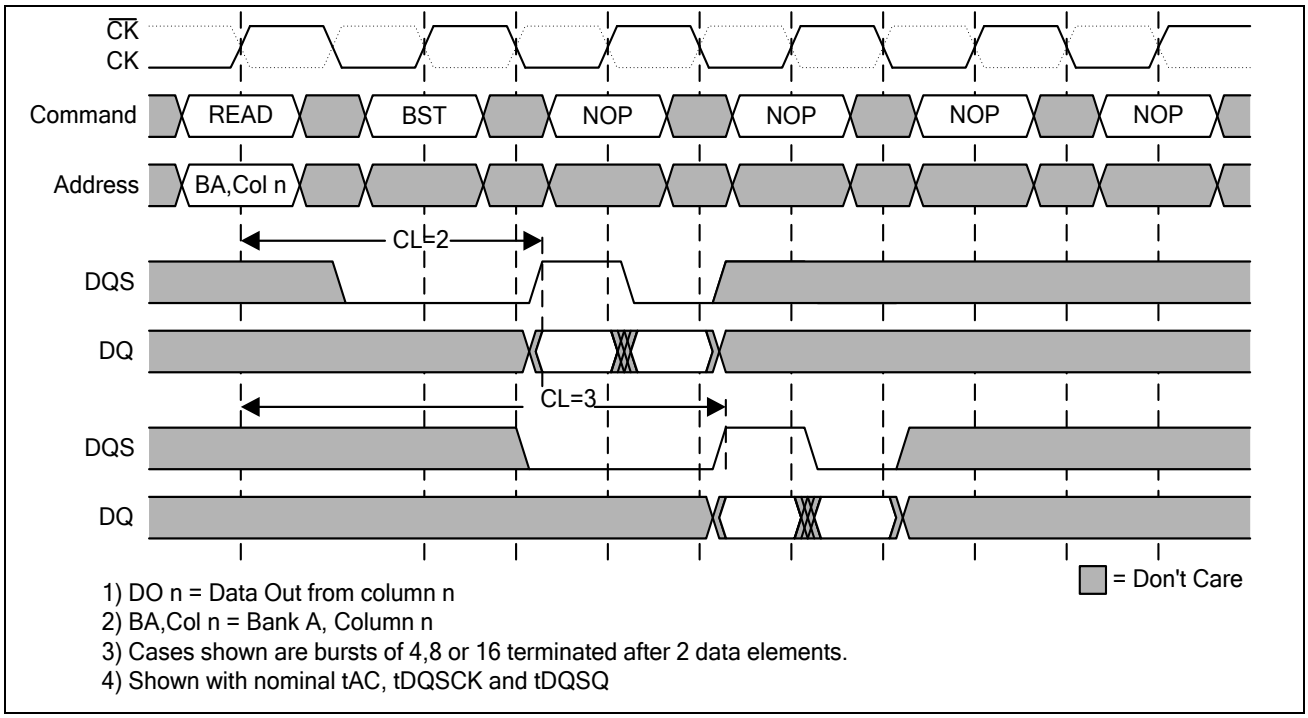
Full-speed random read accesses within a page or pages can be performed as shown in following figure.



1) DO n ,etc. = Data Out from column n, etc.
   n^{I}, x^{I}, etc. = Data Out elements, according to the programmed burst order
2) BA, Col n = Bank A, Column n
3) Burst Length=2,4,8 or 16 in cases shown (if burst of 4,8 or 16, the burst is interrupted)
4) Reads are to active rows in any banks

7.5.8 Read Burst Terminate

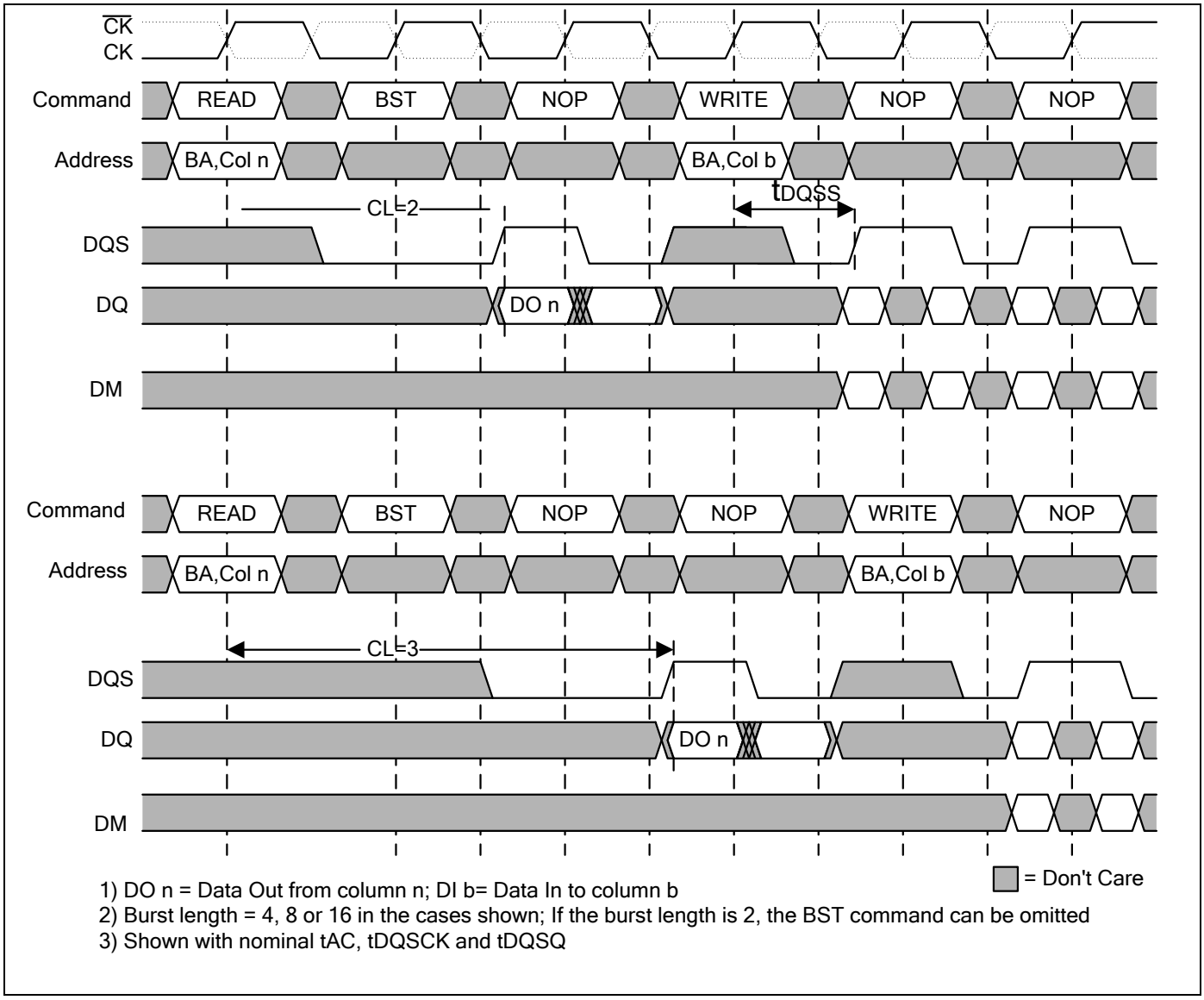
Data from any READ burst may be truncated with a BURST TERMINATE command, as shown in figure. The BURST TERMINATE latency is equal to the read (CAS) latency, i.e., the BURST TERMINATE command should be issued X cycles after the READ command where X equals the desired data-out element pairs.



1) DO n = Data Out from column n
2) BA,Col n = Bank A, Column n
3) Cases shown are bursts of 4,8 or 16 terminated after 2 data elements.
4) Shown with nominal tAC, tDQSCK and tDQSQ

7.5.9 Read to Write

Data from READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used, as shown in following figure for the case of nominal tDQSS

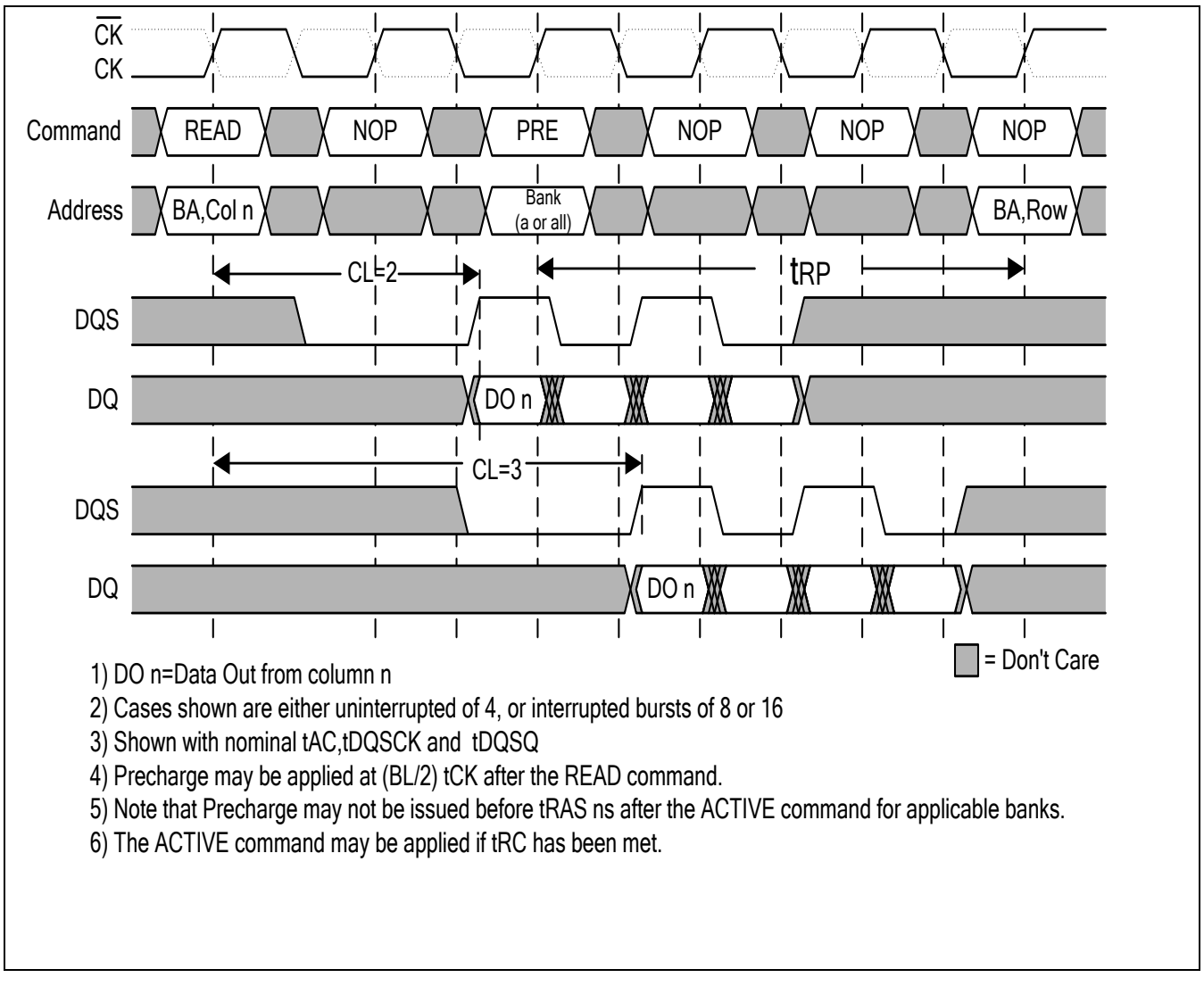


1) DO n = Data Out from column n; DI b= Data In to column b
2) Burst length = 4, 8 or 16 in the cases shown; If the burst length is 2, the BST command can be omitted
3) Shown with nominal tAC, tDQSCK and tDQSQ

7.5.10 Read to Pre-charge

A Read burst may be followed by or truncated with a PRECHARGE command to the same bank (provided Auto Pre-charge was not activated). The PRECHARGE command should be issued X cycles after the READ command, where X equal the number of desired data-out element pairs. This is shown in following figure. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until t_{RP} is met. Note that part of the row pre-charge time is hidden during the access of the last data-out elements.

In the case of a Read being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from Read burst with Auto Pre-charge enabled. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command. The advantage of the PRECHARGE command is that it can be used to truncate bursts.

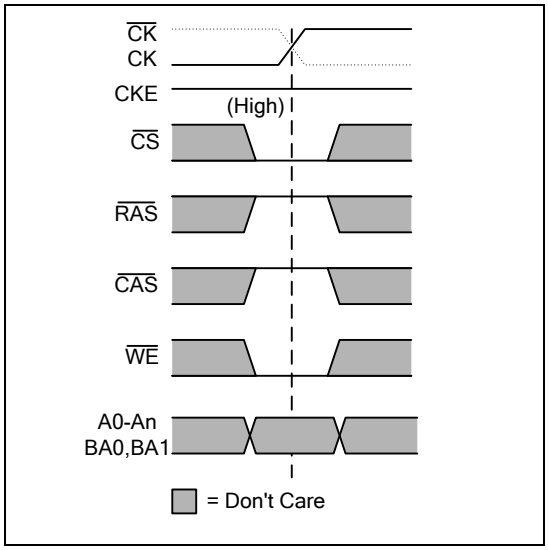


1) DO n=Data Out from column n
2) Cases shown are either uninterrupted of 4, or interrupted bursts of 8 or 16
3) Shown with nominal tAC,tDQSCK and tDQSQ
4) Precharge may be applied at (BL/2) tCK after the READ command.
5) Note that Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks.
6) The ACTIVE command may be applied if tRC has been met.

7.5.11 Burst Terminate of Read

The BURST TERMINATE command is used to truncate read bursts (with Auto Pre-charge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated. Note that the BURST TERMINATE command is not bank specific.

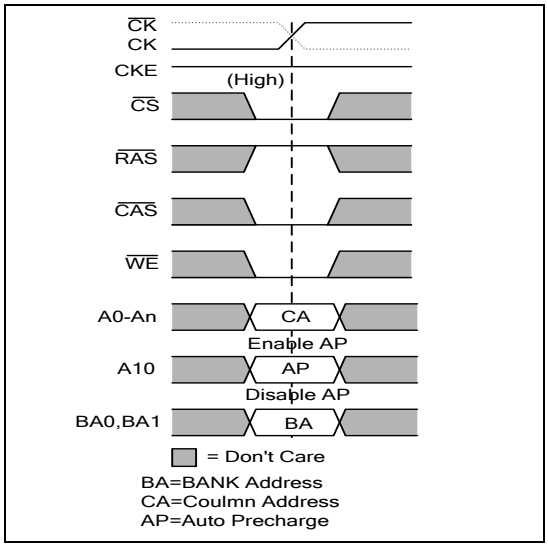
This command should not be used to terminate write bursts.



7.6 Write

The WRITE command is used to initiate a burst write access to an active row, with a burst length as set in the Mode Register. BA0 and BA1 select the bank, and the address inputs select the starting column location. The value of A10 determines whether or not Auto Pre-charge is used. If Auto Pre-charge is selected, the row being accessed will be pre-charged at the end of the write burst; if Auto Pre-charge is not selected, the row will remain open for subsequent accesses.

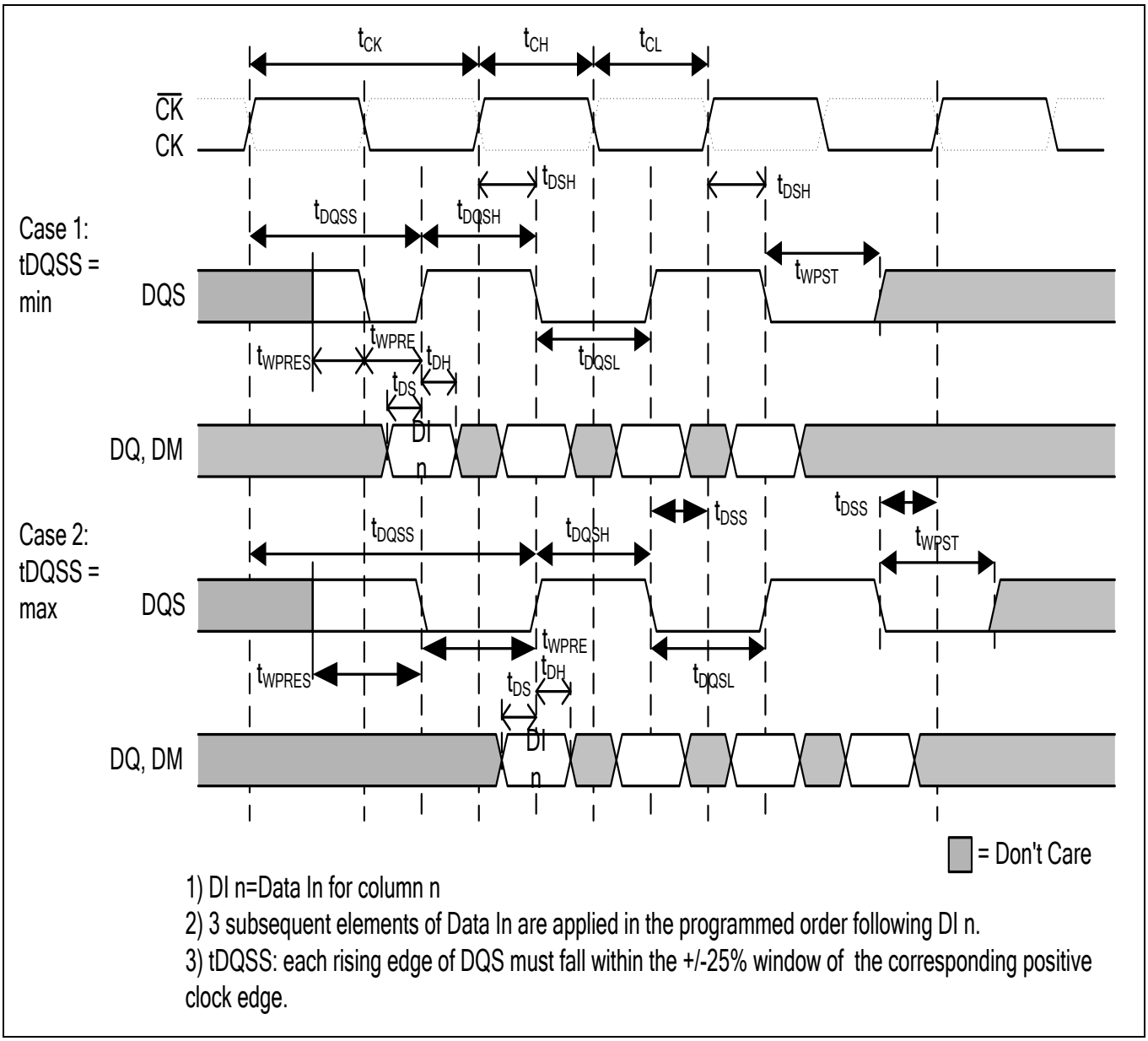
7.6.1 Write Command



7.6.2 Basic Write Timing Parameters

Basic Write timing parameters for DQs are shown in figure below; they apply to all Write operations.

Input data appearing on the data bus, is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered Low, the corresponding data will be written to the memory; if the DM signal is registered High, the corresponding data inputs will be ignored, and a write will not be executed to that byte / column location.



1) DI n=Data In for column n

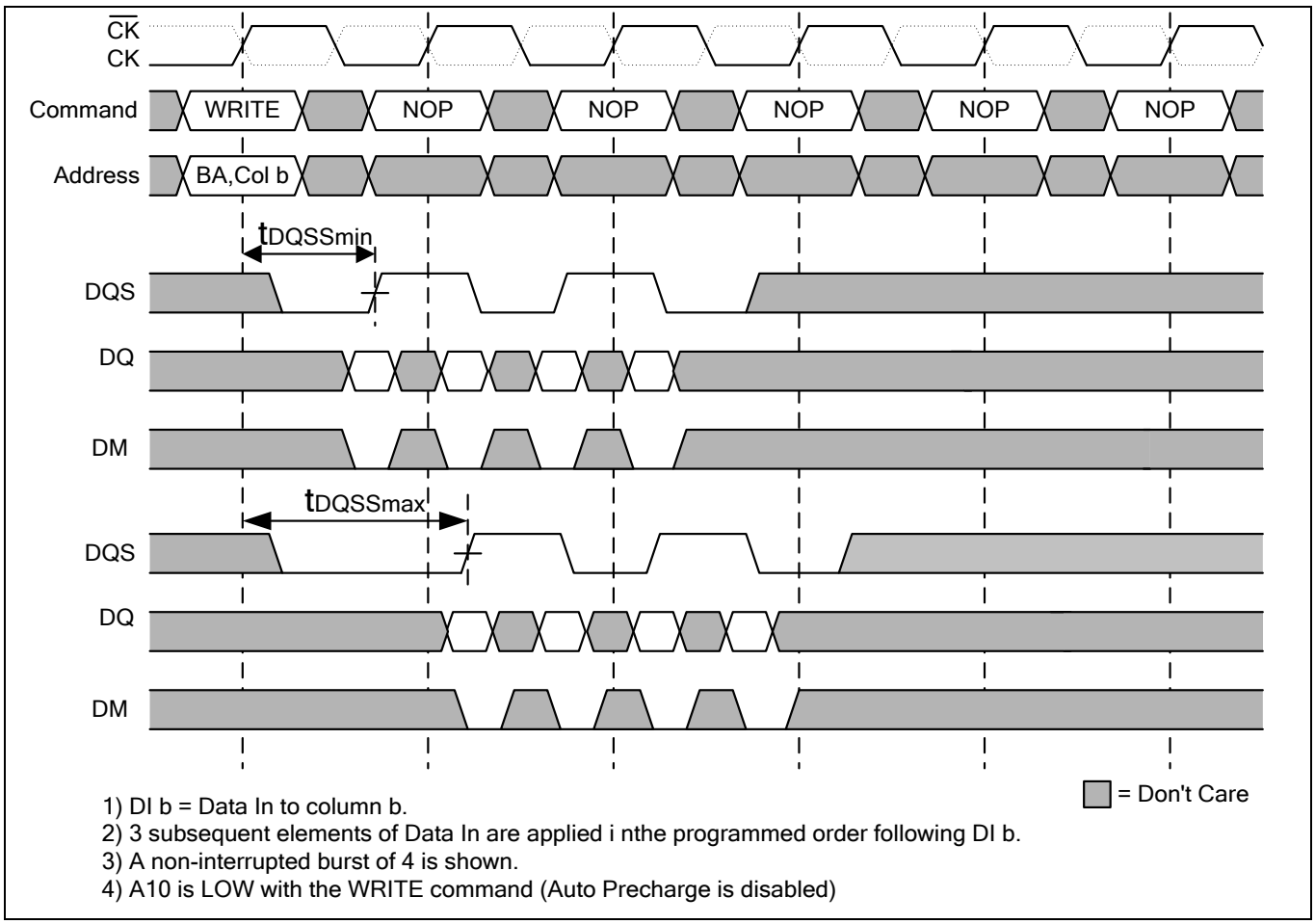
2) 3 subsequent elements of Data In are applied in the programmed order following DI n.

3) tDQSS: each rising edge of DQS must fall within the +/-25% window of the corresponding positive clock edge.

7.6.3 Write Burst (min. and max. tDQSS)

During Write bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and the subsequent data elements will be registered on successive edges of DQS. The Low state of DQS between the WRITE command and the first rising edge is called the write preamble, and the Low state on DQS following the last data-in element is called the write post-amble.

The time between the WRITE command and the first corresponding rising edge of DQS (t_{DQSS}) is specified with a relatively wide range - from 75% to 125% of a clock cycle. Following figure shows the two extremes of t_{DQSS} for a burst of 4, upon completion of a burst, assuming no other commands have been initiated, the DQs will remain high-Z and any additional input data will be ignored.



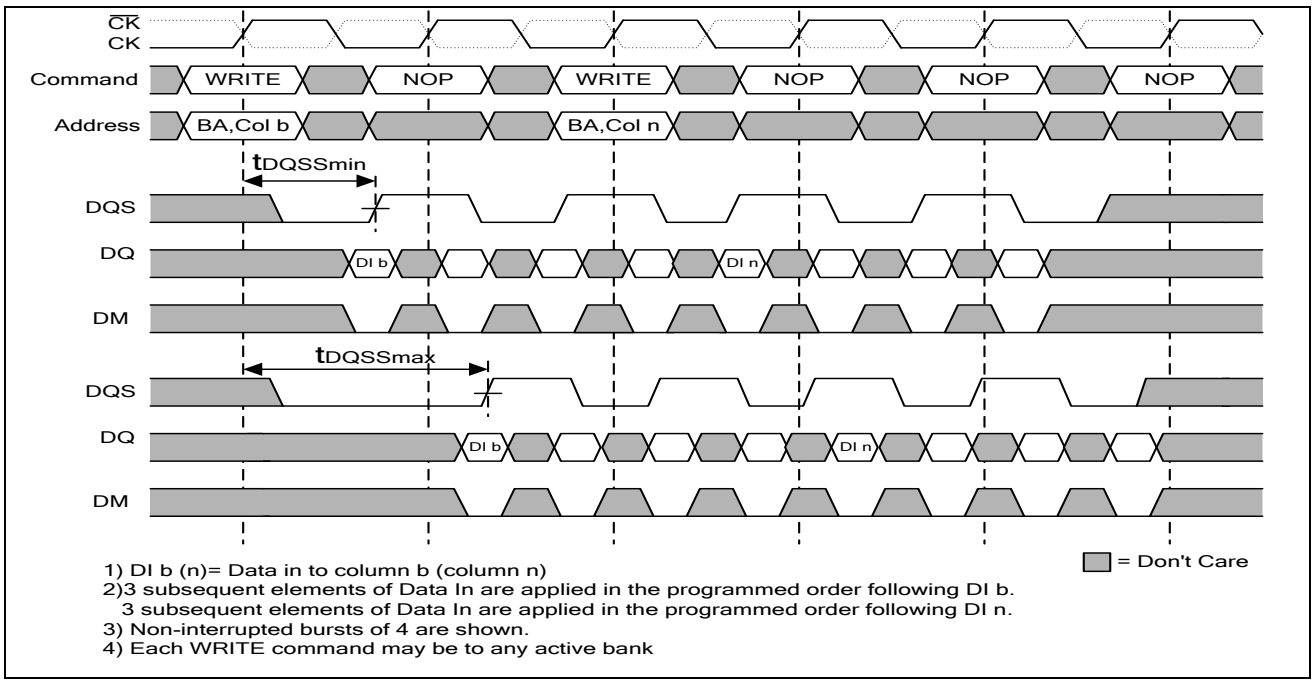
7.6.4 Write to Write

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data, can be maintained. The new WRITE command can be issued on any positive edge of the clock following the previous WRITE command.

The first data-in element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new WRITE command should be issued X cycles after the first WRITE command, where X equals the number of desired data-in element pairs.

7.6.5 Concatenated Write Bursts

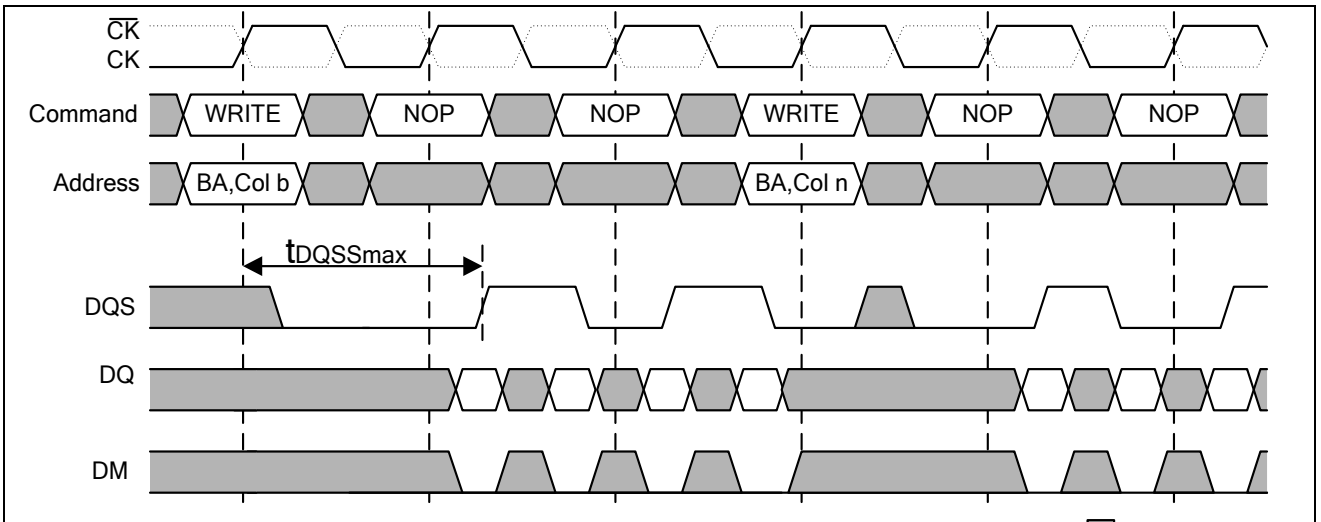
An example of concatenated write bursts is shown in figure below.



1) DI b (n)= Data in to column b (column n)
2)3 subsequent elements of Data In are applied in the programmed order following DI b.
3 subsequent elements of Data In are applied in the programmed order following DI n.
3) Non-interrupted bursts of 4 are shown.
4) Each WRITE command may be to any active bank

7.6.6 Non-Consecutive Write Bursts

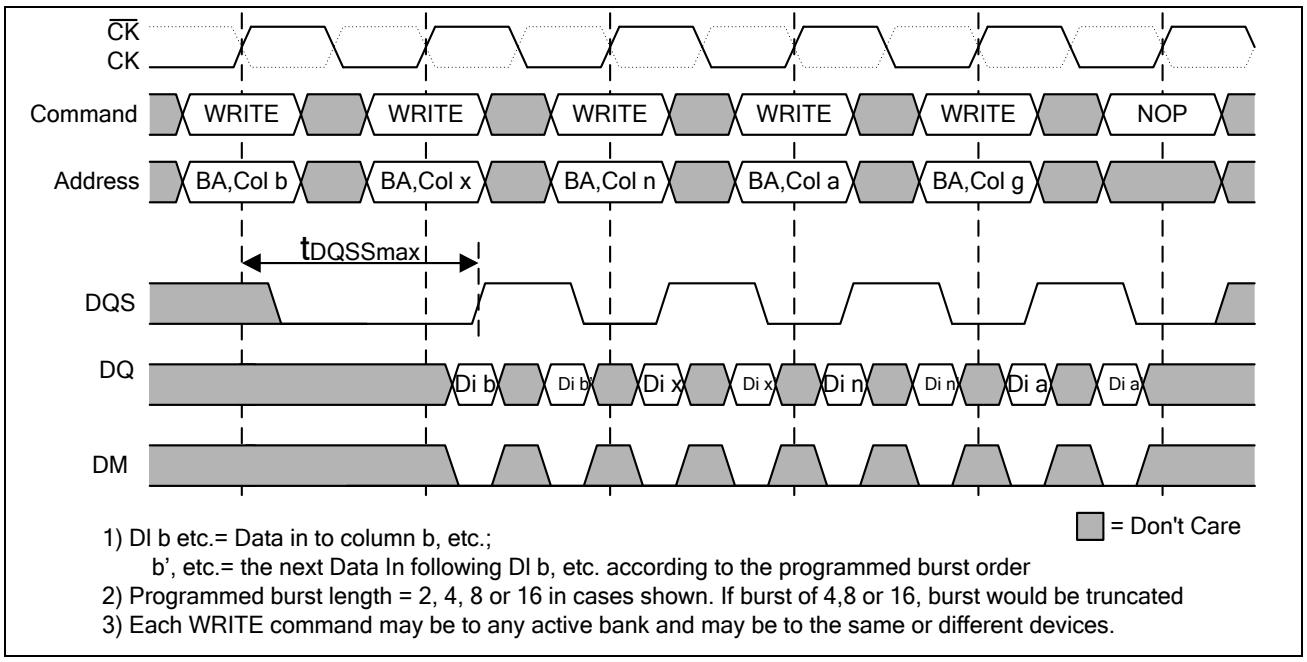
An example of non-consecutive write bursts is shown in figure below.



1) DI b (n)= Data in to column b (or column n)
2) 3 subsequent elements of Data In are applied in the programmed order following DI b.
3 subsequent elements of Data In are applied in the programmed order following DI n.
3) Non-interrupted bursts of 4 are shown.
4) Each WRITE command may be to any active bank and may be to the same or different devices.

7.6.7 Random Write Cycles

Full-speed random write accesses within a page or pages can be performed as shown in figure below.



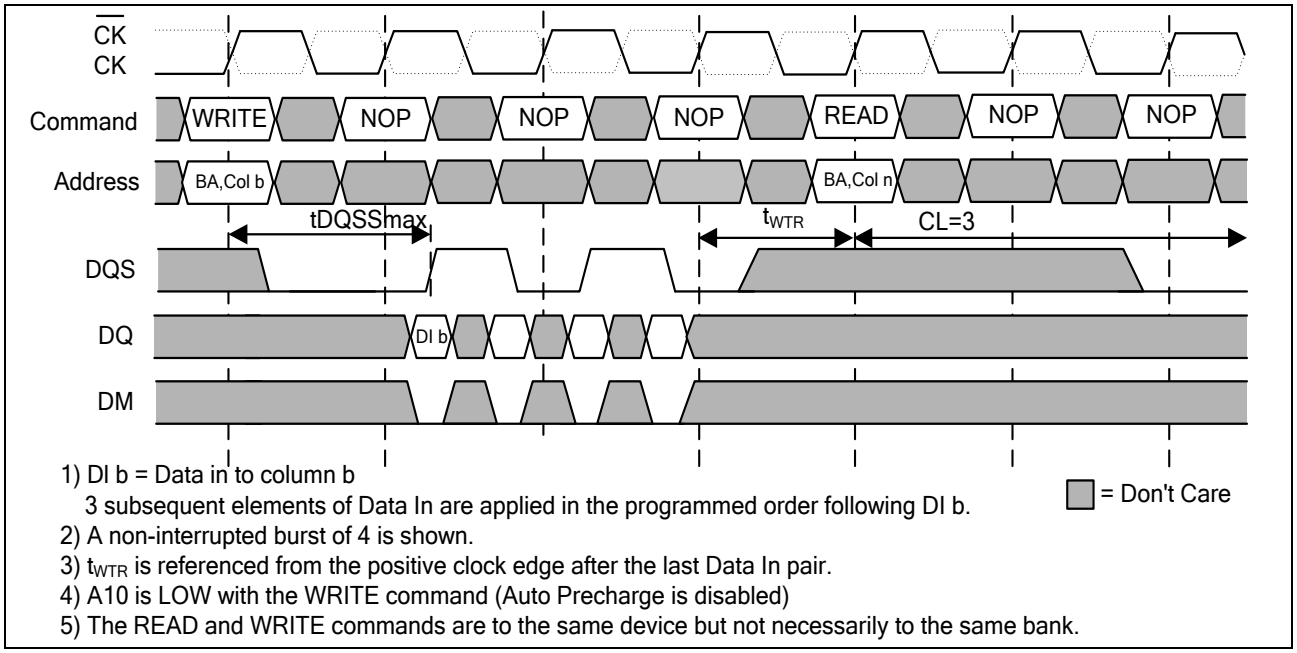
1) DI b etc.= Data in to column b, etc.;
b', etc.= the next Data In following DI b, etc. according to the programmed burst order
2) Programmed burst length = 2, 4, 8 or 16 in cases shown. If burst of 4,8 or 16, burst would be truncated
3) Each WRITE command may be to any active bank and may be to the same or different devices.

7.6.8 Write to Read

Data for any Write burst may be followed by a subsequent READ command.

7.6.9 Non-Interrupting Write to Read

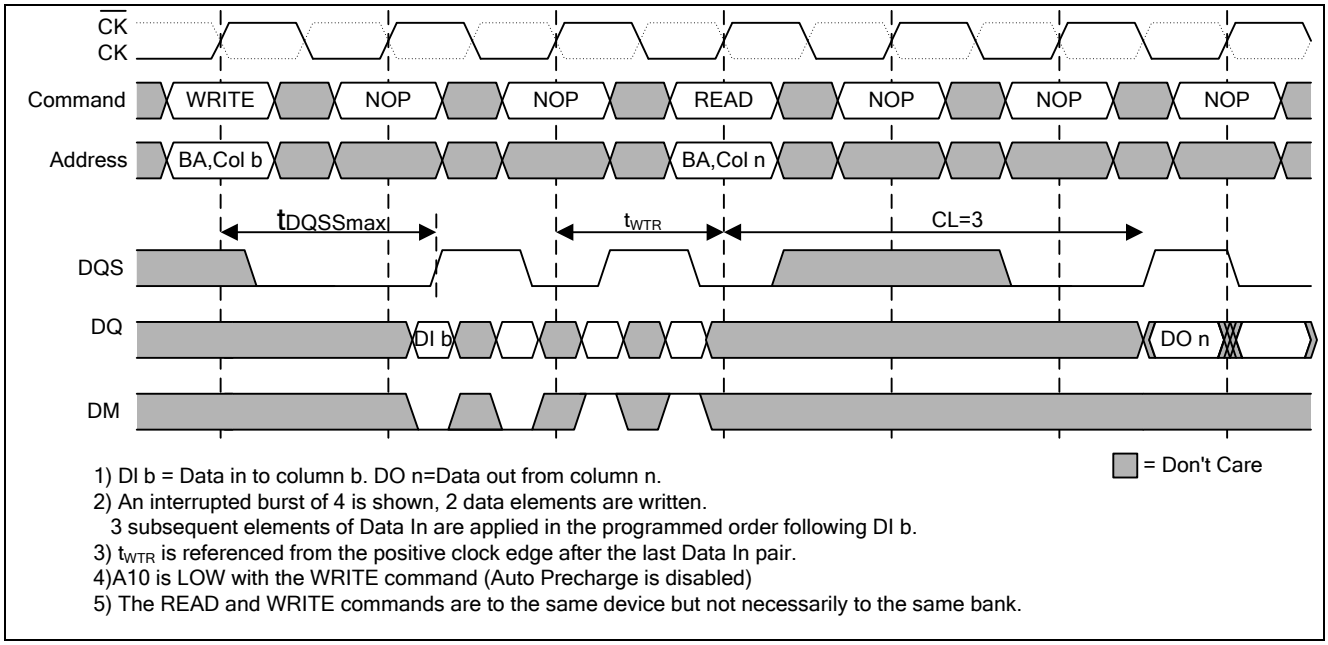
To follow a Write without truncating the write burst, tWTR should be met as shown in the figure below.



1) DI b = Data in to column b
3 subsequent elements of Data In are applied in the programmed order following DI b.
2) A non-interrupted burst of 4 is shown.
3) t_{WTR} is referenced from the positive clock edge after the last Data In pair.
4) A10 is LOW with the WRITE command (Auto Precharge is disabled)
5) The READ and WRITE commands are to the same device but not necessarily to the same bank.

7.6.10 Interrupting Write to Read

Data for any Write burst may be truncated by a subsequent READ command as shown in the figure below. Note that the only data-in pairs that are registered prior to the tWTR period are written to the internal array, and any subsequent data-in must be masked with DM.

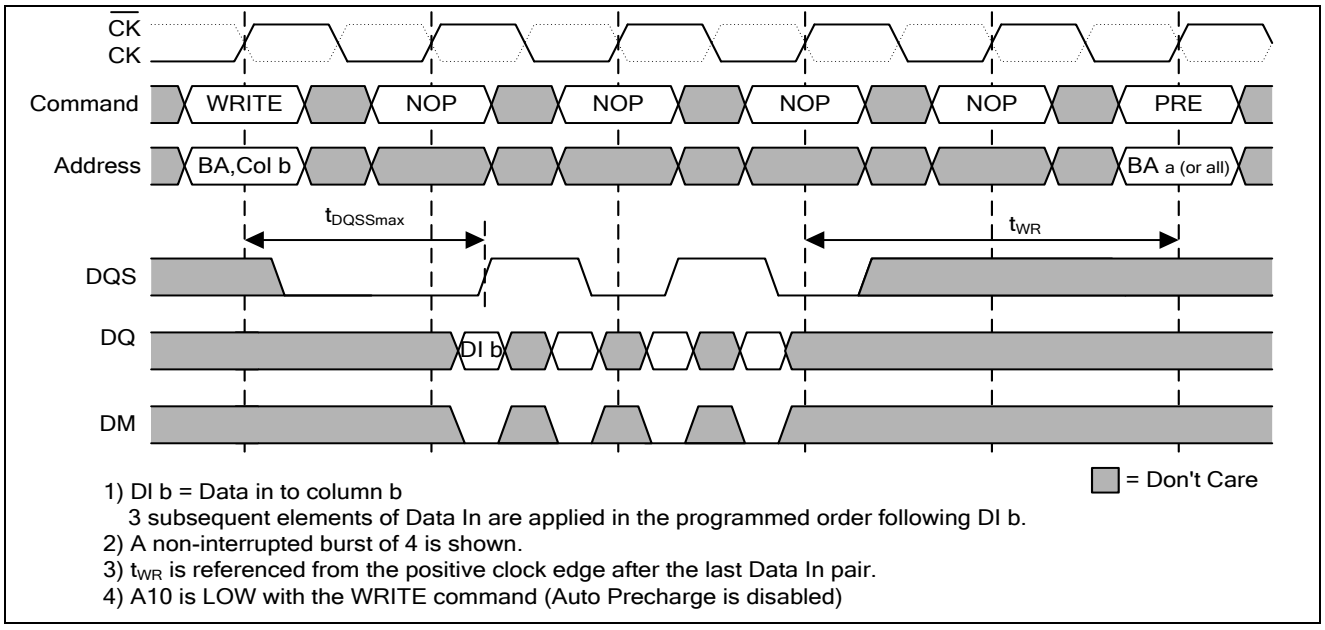


1) DI b = Data in to column b. DO n=Data out from column n.
2) An interrupted burst of 4 is shown, 2 data elements are written.
   3 subsequent elements of Data In are applied in the programmed order following DI b.
3) t_{WTR} is referenced from the positive clock edge after the last Data In pair.
4)A10 is LOW with the WRITE command (Auto Precharge is disabled)
5) The READ and WRITE commands are to the same device but not necessarily to the same bank.

7.6.11 Write to Precharge

Data for any WRITE burst may be followed by a subsequent PRECHARGE command to the same bank (provided Auto Precharge was not activated). To follow a WRITE without truncating the WRITE burst, tWR should be met as shown in the figure below.

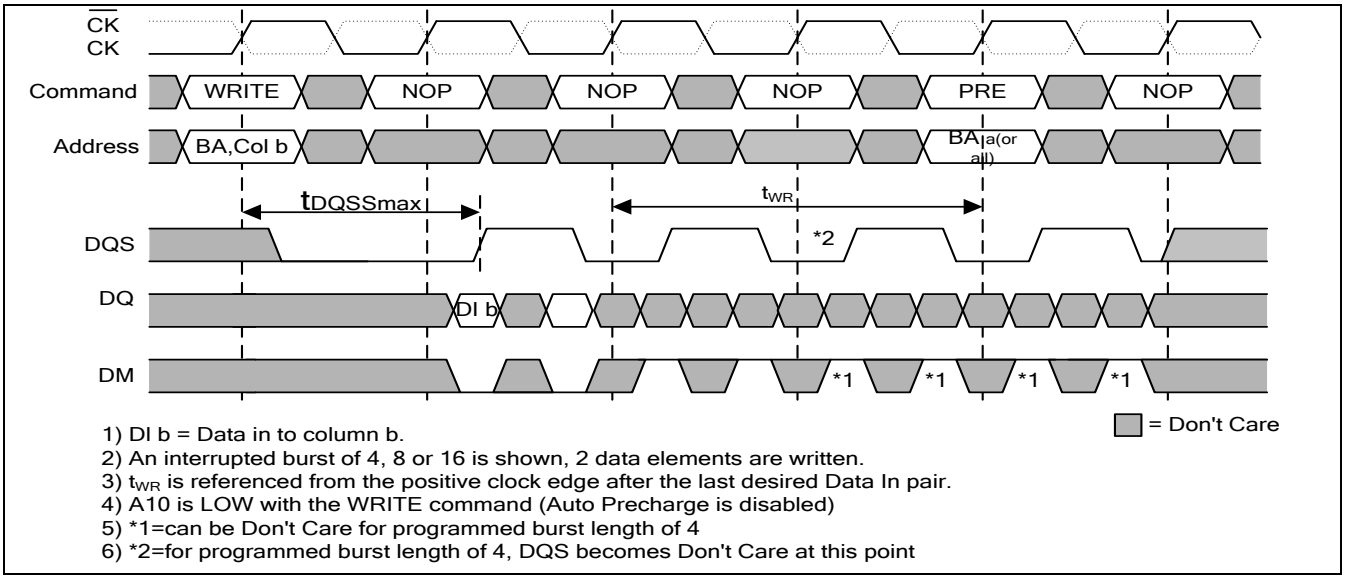
7.6.12 Non-Interrupting Write to Precharge



1) DI b = Data in to column b
   3 subsequent elements of Data In are applied in the programmed order following DI b.
2) A non-interrupted burst of 4 is shown.
3) t_{WR} is referenced from the positive clock edge after the last Data In pair.
4) A10 is LOW with the WRITE command (Auto Precharge is disabled)

7.6.13 Interrupting Write to Precharge

Data for any WRITE burst may be truncated by a subsequent PRECHARGE command as shown in figure below. Note that only data-in pairs that are registered prior to the tWR period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in figure. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met.



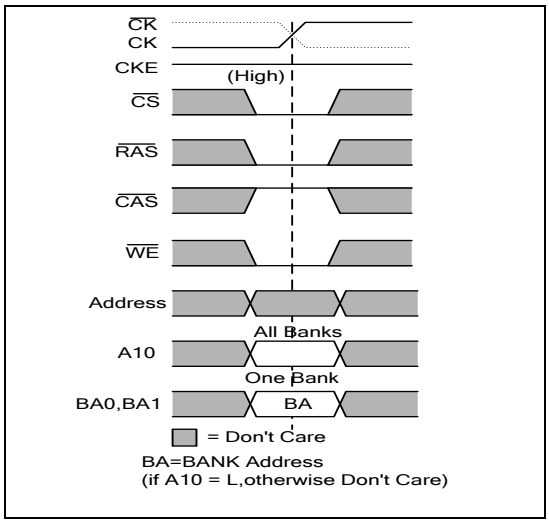
7.7 Precharge

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the PRECHARGE command is issued.

Input A10 determines whether one or all banks are to be precharged. In case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as “Don’t Care”.

Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE command being issued. A PRECHARGE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.

7.7.1 Precharge Command



7.8 Auto Precharge

Auto Precharge is a feature which performs the same individual bank precharge function as described above, but without requiring an explicit command. This is accomplished by using A10 (A10 = High), to enable Auto Precharge in conjunction with a specific READ or WRITE command. A precharge of the bank / row that is addressed with the READ or WRITE command is automatically performed upon completion of the read or write burst. Auto Precharge is non persistent in that it is either enabled or disabled for each individual READ or WRITE command.

Auto Precharge ensures that a precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharing time (t_{RP}) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in the Operation section of this specification.

7.9 Refresh Requirements

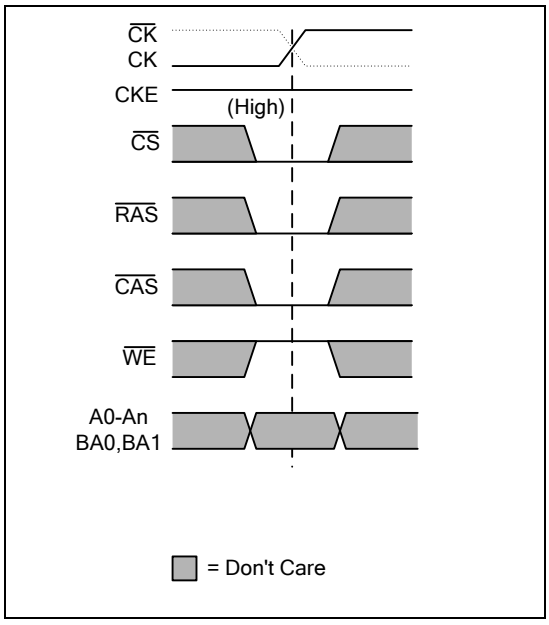
LPDDR SDRAM devices require a refresh of all rows in any rolling 64ms interval. Each refresh is generated in one of two ways: by an explicit AUTO REFRESH command, or by an internally timed event in SELF REFRESH mode. Dividing the number of device rows into the rolling 64ms interval defines the average refresh interval (t_{REFI}), which is a guideline to controllers for distributed refresh timing.

7.10 Auto Refresh

AUTO REFRESH command is used during normal operation of the LPDDR SDRAM. This command is non persistent, so it must be issued each time a refresh is required.

The refresh addressing is generated by the internal refresh controller. The LPDDR SDRAM requires AUTO REFRESH commands at an average periodic interval of t_{REFI}.

7.10.1 Auto Refresh Command



7.11 Self Referesh

The SELF REFRESH command can be used to retain data in the LPDDR SDRAM, even if the rest of the system is powered down. When in the Self Refresh mode, the LPDDR SDRAM retains data without external clocking. The LPDDR SDRAM device has a built-in timer to accommodate Self Refresh operation. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is LOW. Input signals except CKE are “Don’t Care” during Self Refresh. The user may halt the external clock one clock after the SELF REFRESH command is registered.

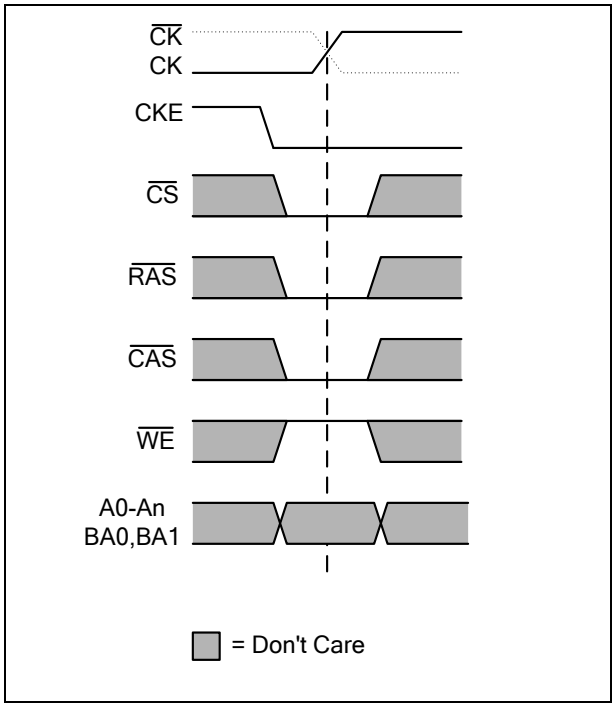
Once the command is registered, CKE must be held low to keep the device in Self Refresh mode. The clock is internally disabled during Self Refresh operation to save power. The minimum time that the device must remain in Self Refresh mode is t_{RFC}.

The procedure for exiting Self Refresh requires a sequence of commands. First, the clock must be stable prior to CKE going back High. Once Self Refresh Exit is registered, a delay of at least t_{XS} must be satisfied before a valid command can be issued to the device to allow for completion of any internal refresh in progress.

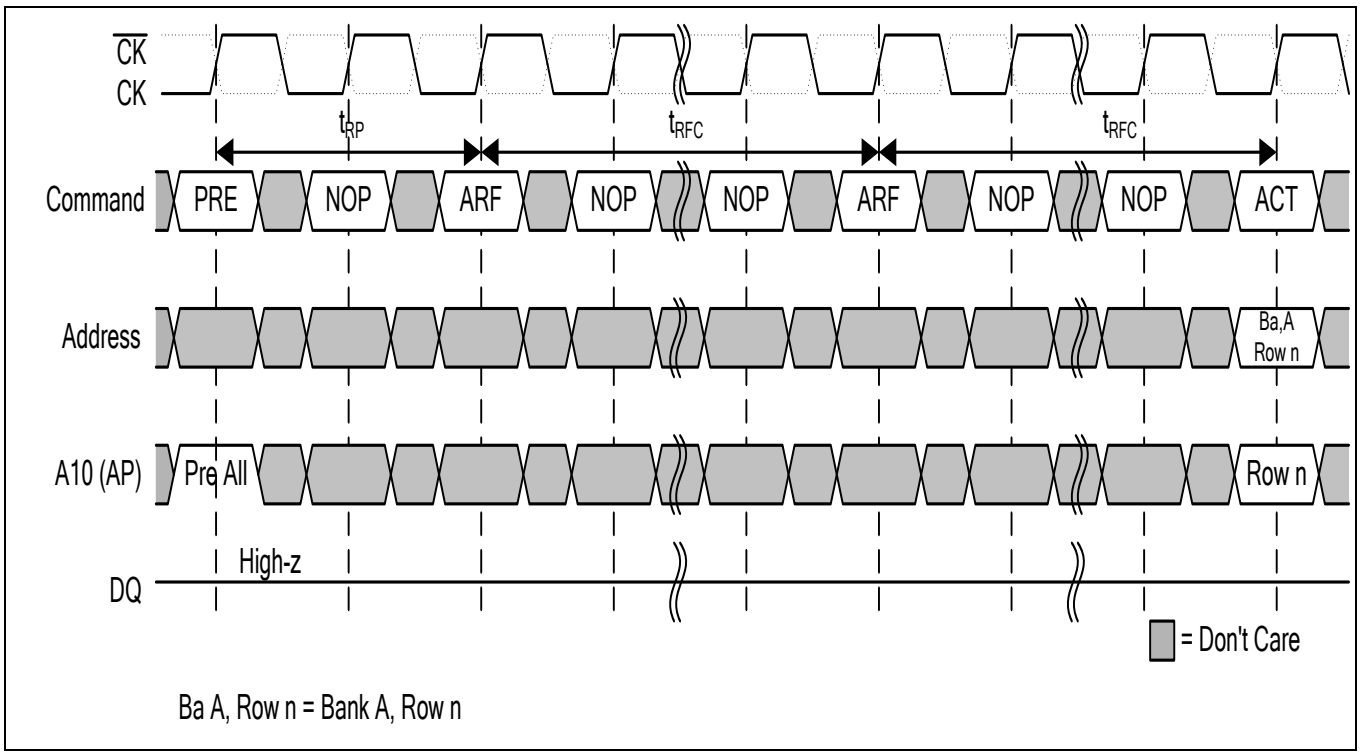
The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh an extra AUTO REFRESH command is recommended.

In the Self Refresh mode, Partial Array Self Refresh (PASR) function is described in the Extended Mode Register section.

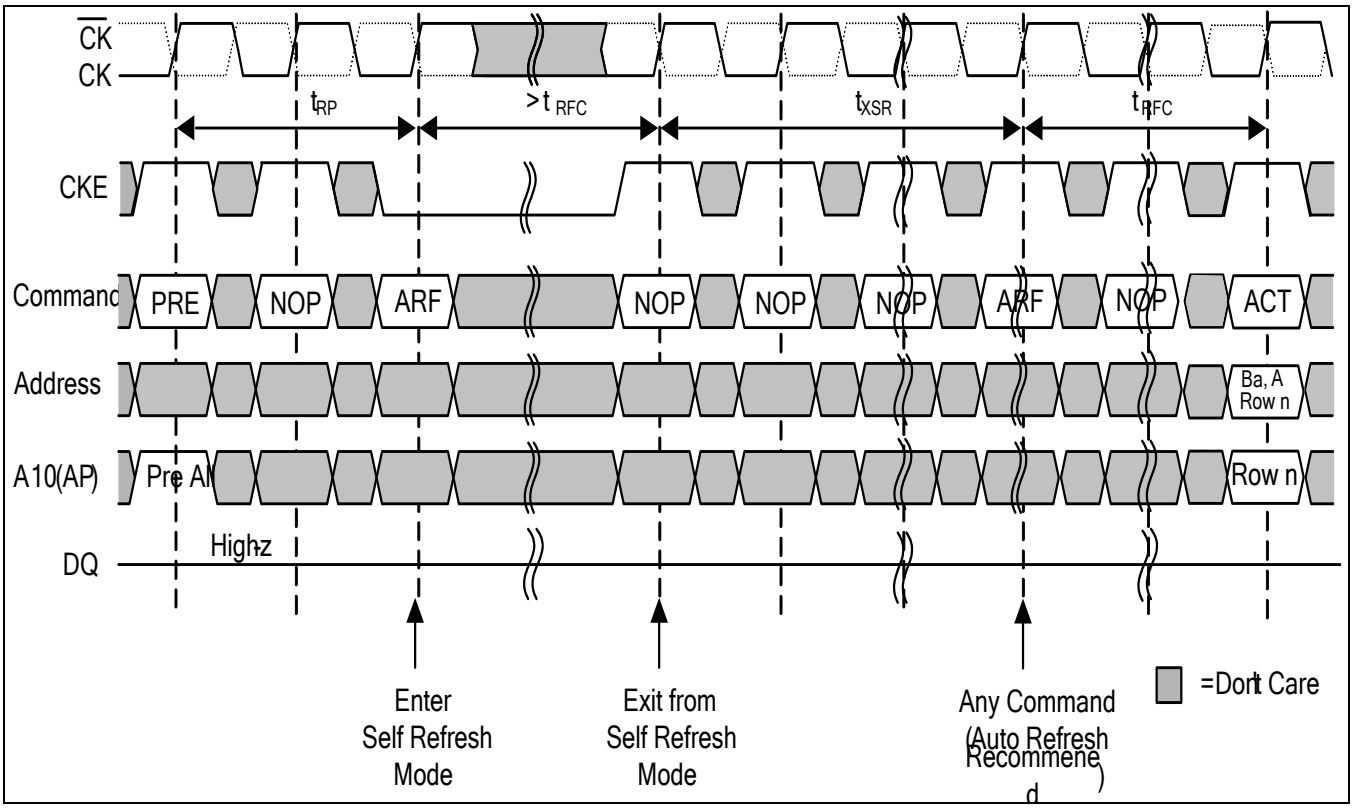
7.11.1 Self Refresh Command



7.11.2 Auto Refresh Cycles Back-to-Back



7.11.3 Self Refresh Entry and Exit



7.12 Power Down

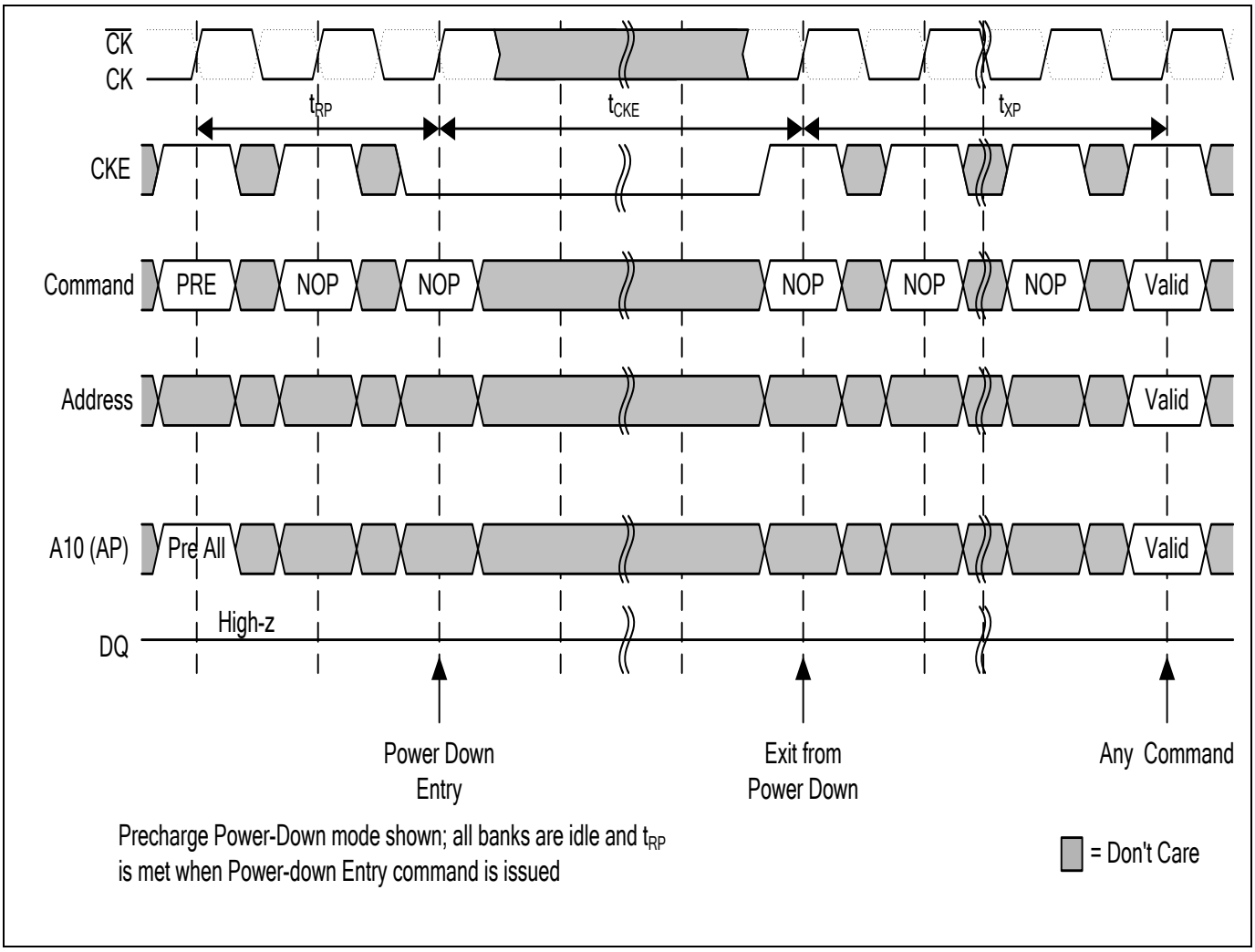
Power-down is entered when CKE is registered Low (no accesses can be in progress). If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down.

Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$ and CKE. In power-down mode, CKE Low must be maintained, and all other input signals are “Don’t Care”. The minimum power-down duration is specified by t_{CKE}. However, power-down duration is limited by the refresh requirements of the device.

The power-down state is synchronously exited when CKE is registered High (along with a NOP or DESELECT command). A valid command may be applied t_{XP} after exit from power-down.

For Clock Stop during Power-Down mode, please refer to the Clock Stop subsection in this specification.

7.12.1 Power-Down Entry and Exit



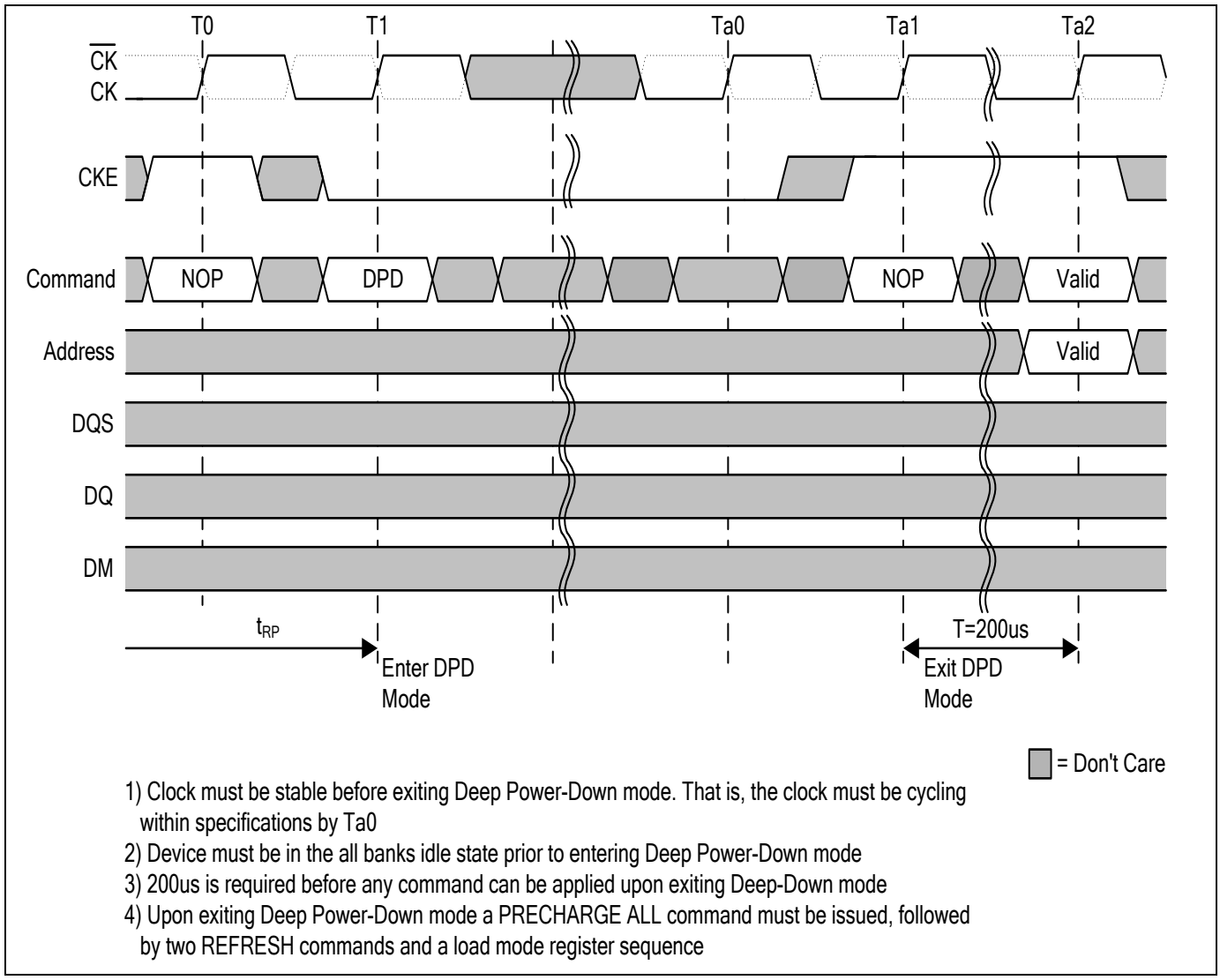
7.13 Deep Power Down

The Deep Power-Down (DPD) mode enables very low standby currents. All internal voltage generators inside the LPDDR SDRAM are stopped and all memory data is lost in this mode. All the information in the Mode Register and the Extended Mode Register is lost.

Deep Power-Down is entered using the BURST TERMINATE command except that CKE is registered Low. All banks must be in idle state with no activity on the data bus prior to entering the DPD mode. While in this state, CKE must be held in a constant Low state.

To exit the DPD mode, CKE is taken high after the clock is stable and NOP commands must be maintained for at least 200µs. After 200µs a complete re-initialization is required following steps 4 through 11 as defined for the initialization sequence.

7.13.1 Deep Power-Down Entry and Exit



1) Clock must be stable before exiting Deep Power-Down mode. That is, the clock must be cycling within specifications by Ta0
2) Device must be in the all banks idle state prior to entering Deep Power-Down mode
3) 200us is required before any command can be applied upon exiting Deep-Down mode
4) Upon exiting Deep Power-Down mode a PRECHARGE ALL command must be issued, followed by two REFRESH commands and a load mode register sequence

7.14 Clock Stop

Stopping a clock during idle periods is an effective method of reducing power consumption.

The LPDDR SDRAM supports clock stop under the following conditions:

- the last command (ACTIVE, READ, WRITE, PRECHARGE, AUTO REFRESH or MODE REGISTER SET) has executed to completion, including any data-out during read bursts; the number of clock pulses per access command depends on the device's AC timing parameters and the clock frequency;
- the related timing conditions (t_{RCD}, t_{WR}, t_{RP}, t_{RFC}, t_{MRD}) has been met;
- CKE is held High

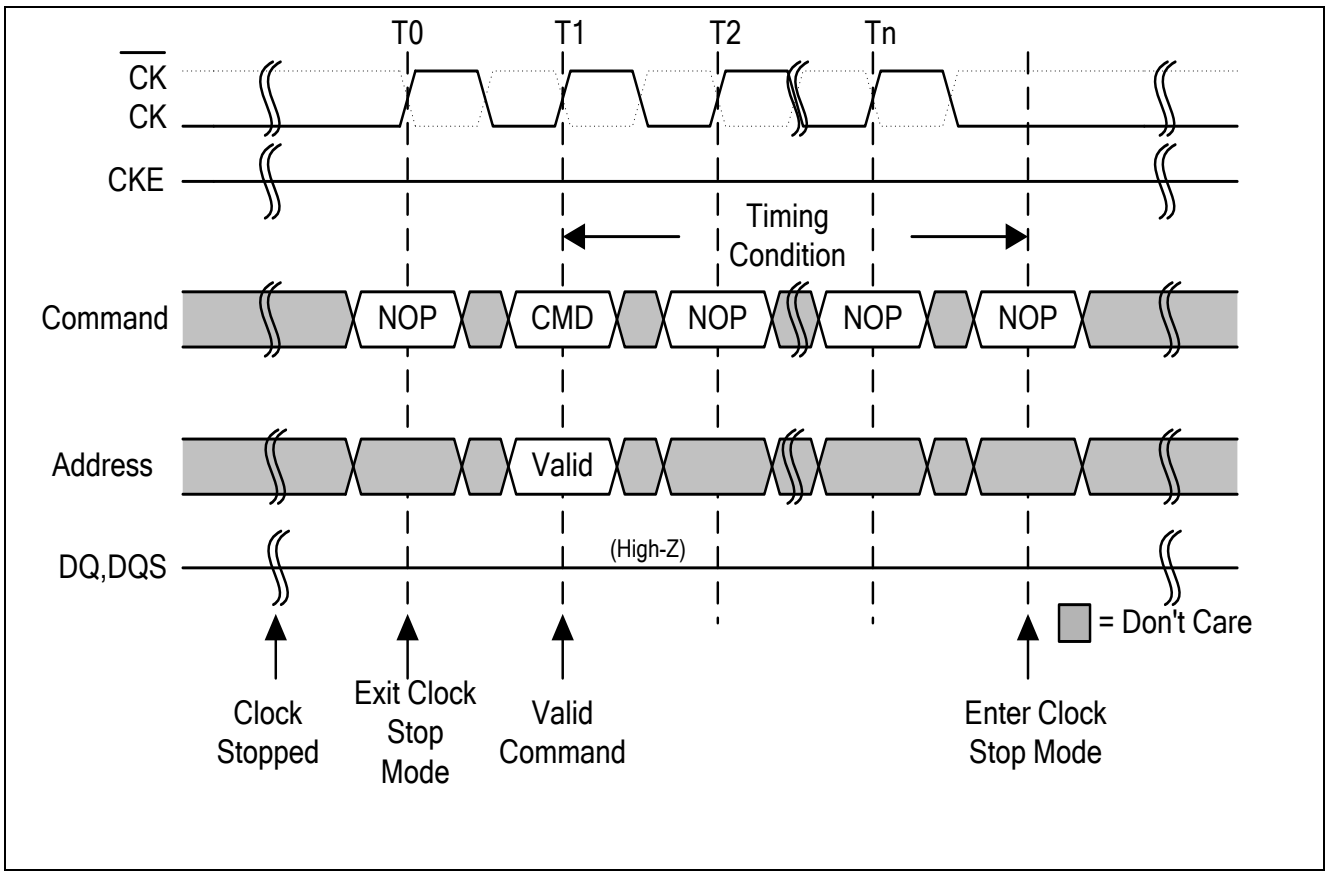
When all conditions have been met, the device is either in "idle state" or "row active state" and clock stop mode may be entered with CK held Low and $\overline{CK}$ held High.

Clock stop mode is exited by restarting the clock. At least one NOP command has to be issued before the next access command may be applied. Additional clock pulses might be required depending on the system characteristics.

The following Figure shows clock stop mode entry and exit.

- Initially the device is in clock stop mode
- The clock is restarted with the rising edge of T0 and a NOP on the command inputs
- With T1 a valid access command is latched; this command is followed by NOP commands in order to allow for clock stop as soon as this access command is completed
- Tn is the last clock pulse required by the access command latched with T1
- The clock can be stopped after Tn

7.14.1 Clock Stop Mode Entry and Exit



8. ELECTRICAL CHARACTERISTIC

8.1 Absolute Maximum Ratings

Parameter	Symbol	Values		Units
		Min	Max	
Voltage on VDD relative to VSS	VDD	−0.5	2.3	V
Voltage on VDDQ relative to VSS	VDDQ	−0.5	2.3	V
Voltage on any pin relative to VSS	VIN, VOUT	−0.5	2.3	V
Operation Case Temperature	Tc	-25 -40	85 85	°C
Storage Temperature	TSTG	−55	150	°C
Short Circuit Output Current	IOUT		±50	mA
Power Dissipation	PD		1.0	W

Notes:

Stresses greater than those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

8.2 Input/Output Capacitance

Parameter	Symbol	Min	Max	Units	Notes
Input capacitance, CK, $\overline{CK}$	CCK	1.5	3.0	pF	
Input capacitance delta, CK, $\overline{CK}$	CDCK		0.25	pF	
Input capacitance, all other input-only pins	CI	1.5	3.0	pF	
Input capacitance delta, all other input-only pins	CDI		0.5	pF	
Input/ output capacitance, DQ,DM,DQS	CIO	3.0	5.0	pF	3
Input/output capacitance delta, DQ, DM, DQS	CDIO		0.50	pF	3

Notes:

1.These values are guaranteed by design and are tested on a sample base only.
2.These capacitance values are for single monolithic devices only. Multiple die packages will have parallel capacitive loads.
3.Although DM is an input-only pin, the input capacitance of this pin must model the input capacitance of the DQ and DQS pins. This is required to match signal propagation times of DQ, DQS and DM in the system

8.3 Electrical Characteristics and AC/DC Operating Conditions

All values are recommended operating conditions unless otherwise noted.

8.3.1 Electrical Characteristics and AC/DC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units	Notes
Supply Voltage	VDD	1.70	1.95	V	
I/O Supply Voltage	VDDQ	1.70	1.95	V	
Address And Command Inputs (A0~An, BA0,BA1,CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)					
Input High Voltage	VIH	0.8*VDDQ	VDDQ + 0.3	V	
Input Low Voltage	VIL	−0.3	0.2*VDDQ	V	
Clock Inputs (CK, $\overline{CK}$)					
DC Input Voltage	VIN	−0.3	VDDQ + 0.3	V	
DC Input Differential Voltage	VID (DC)	0.4*VDDQ	VDDQ + 0.6	V	2
AC Input Differential Voltage	VID (AC)	0.6*VDDQ	VDDQ + 0.6	V	2
AC Differential Crossing Voltage	VIX	0.4*VDDQ	0.6*VDDQ	V	3
Data Inputs (DQ, DM, DQS)					
DC Input High Voltage	VIHD (DC)	0.7*VDDQ	VDDQ + 0.3	V	
DC Input Low Voltage	VILD (DC)	−0.3	0.3*VDDQ	V	
AC Input High Voltage	VIHD (AC)	0.8*VDDQ	VDDQ + 0.3	V	
AC Input Low Voltage	VILD (AC)	−0.3	0.2*VDDQ	V	
Data Outputs (DQ, DQS)					
DC Output High Voltage (IOH=−0.1mA)	VOH	0.9*VDDQ	-	V	
DC Output Low Voltage (IOL=0.1mA)	VOL	-	0.1*VDDQ	V	
Leakage Current					
Input Leakage Current	IiL	-1	1	uA	4
Output Leakage Current	IoL	-5	5	uA	5

Notes:

1.All voltages referenced to VSS and VSSQ must be same potential.

2. VID (DC) and VID (AC) are the magnitude of the difference between the input level on CK and $\overline{CK}$.

3. The value of VIX is expected to be 0.5*VDDQ and must track variations in the DC level of the same.

4. Any input 0V ≤ VIN ≤ VDD. All other pins are not tested under VIN=0V.

5. Any output 0V ≤ VOUT ≤ VDDQ. DOUT is disabled.

8.4 IDD Specification Parameters and Test Conditions

8.4.1 IDD Specification and Test Conditions (x16)

[Recommended Operating Conditions; Notes 1-4]

Parameter	Symbol	Test Condition	- 5	- 6	Unit
Operating one bank active-precharge current	IDD0	tRC = tRCmin ; tCK = tCKmin ; CKE is HIGH; $\overline{CS}$ is HIGH between valid commands; address inputs are SWITCHING; data bus inputs are STABLE	40	38	mA
Precharge power-down standby current	IDD2P	all banks idle, CKE is LOW; $\overline{CS}$ is HIGH, tCK = tCKmin ; address and control inputs are SWITCHING; data bus inputs are STABLE	0.3	0.3	mA
Precharge power-down standby current with clock stop	IDD2PS	all banks idle, CKE is LOW; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	0.3	0.3	mA
Precharge non power-down standby current	IDD2N	all banks idle, CKE is HIGH; $\overline{CS}$ is HIGH, tCK = tCKmin; address and control inputs are SWITCHING; data bus inputs are STABLE	10	10	mA
Precharge non power-down standby current with clock stop	IDD2NS	all banks idle, CKE is HIGH; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	3	3	mA
Active power-down standby current	IDD3P	one bank active, CKE is LOW; $\overline{CS}$ is HIGH, tCK = tCKmin;address and control inputs are SWITCHING; data bus inputs are STABLE	3	3	mA
Active power-down standby current with clock stop	IDD3PS	one bank active, CKE is LOW; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	3	3	mA
Active non power-down standby current	IDD3N	one bank active, CKE is HIGH; $\overline{CS}$ is HIGH, tCK = tCKmin; address and control inputs are SWITCHING; data bus inputs are STABLE	25	25	mA
Active non power-down standby current with clock stop	IDD3NS	one bank active, CKE is HIGH; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	15	15	mA
Operating burst read current	IDD4R	one bank active; BL = 4; CL = 3; tCK = tCKmin ; continuous read bursts; IOUT = 0 mA; address inputs are SWITCHING; 50% data change each burst transfer	75	70	mA
Operating burst write current	IDD4W	one bank active; BL = 4; t CK = t CKmin ; continuous write bursts; address inputs are SWITCHING; 50% data change each burst transfer	55	50	mA
Auto-Refresh Current	IDD5	tRC = tRFCmin ; tCK = tCKmin ; burst refresh; CKE is HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	75	75	mA
Deep Power-Down current	IDD8(4)	Address and control inputs are STABLE; data bus inputs are STABLE	10	10	uA

8.4.2 IDD Specification and Test Conditions (x32)

[Recommended Operating Conditions; Notes 1-4]

Parameter	Symbol	Test Condition	- 5	- 6	Unit
Operating one bank active-precharge current	IDD0	tRC = tRCmin ; tCK = tCKmin ; CKE is HIGH; $\overline{CS}$ is HIGH between valid commands; address inputs are SWITCHING; data bus inputs are STABLE	40	38	mA
Precharge power-down standby current	IDD2P	all banks idle, CKE is LOW; $\overline{CS}$ is HIGH, tCK = tCKmin ; address and control inputs are SWITCHING; data bus inputs are STABLE	0.3	0.3	mA
Precharge power-down standby current with clock stop	IDD2PS	all banks idle, CKE is LOW; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	0.3	0.3	mA
Precharge non power-down standby current	IDD2N	all banks idle, CKE is HIGH; $\overline{CS}$ is HIGH, tCK = tCKmin; address and control inputs are SWITCHING; data bus inputs are STABLE	10	10	mA
Precharge non power-down standby current with clock stop	IDD2NS	all banks idle, CKE is HIGH; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	3	3	mA
Active power-down standby current	IDD3P	one bank active, CKE is LOW; $\overline{CS}$ is HIGH, tCK = tCKmin; address and control inputs are SWITCHING; data bus inputs are STABLE	3	3	mA
Active power-down standby current with clock stop	IDD3PS	one bank active, CKE is LOW; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	3	3	mA
Active non power-down standby current	IDD3N	one bank active, CKE is HIGH; $\overline{CS}$ is HIGH, tCK = tCKmin; address and control inputs are SWITCHING; data bus inputs are STABLE	25	25	mA
Active non power-down standby current with clock stop	IDD3NS	one bank active, CKE is HIGH; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	15	15	mA
Operating burst read current	IDD4R	one bank active; BL = 4; CL = 3; tCK = tCKmin ; continuous read bursts; IOUT = 0 mA; address inputs are SWITCHING; 50% data change each burst transfer	75	70	mA
Operating burst write current	IDD4W	one bank active; BL = 4; t CK = t CKmin ; continuous write bursts; address inputs are SWITCHING; 50% data change each burst transfer	55	50	mA
Auto-Refresh Current	IDD5	tRC = tRFCmin ; tCK = tCKmin ; burst refresh; CKE is HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	75	75	mA
Deep Power-Down current	IDD8(4)	Address and control inputs are STABLE; data bus inputs are STABLE	10	10	uA

Notes:
1.IDD specifications are tested after the device is properly initialized.
2.Input slew rate is 1V/ns.
3.Definitions for IDD:
LOW is defined as VIN ≤ 0.1 * VDDQ;
HIGH is defined as VIN ≥ 0.9 * VDDQ;
STABLE is defined as inputs stable at a HIGH or LOW level;
SWITCHING is defined as:
- Address and command: inputs changing between HIGH and LOW once per two clock cycles;
- Data bus inputs: DQ changing between HIGH and LOW once per clock cycle; DM and DQS are STABLE.
4.IDD8 is a typical value at 25°C.

IDD6 Conditions :

Self Refresh Current	IDD6	CKE is LOW; CK = LOW, $\overline{CK}$ = HIGH; Extended Mode Register set to all 0's; address and control inputs are STABLE; data bus inputs are STABLE	PASR Range	85°C	Units
			Full Array	450	uA
			1/2 Array	350	
			1/4 Array	300	

8.5 AC Timings

[Recommended Operating Conditions: Notes 1-9]

Parameter		Symbol	- 5		- 6		Unit	Notes
			Min	Max	Min	Max		
DQ output access time from CK/ $\overline{CK}$	CL=3	tAC	2.0	5.0	2.0	5.0	ns	
	CL=2		2.0	6.5	2.0	6.5		
DQS output access time from CK	CL=3	tDQSCK	2.0	5.0	2.0	5.0	ns	
	CL=2		2.0	6.5	2.0	6.5		
Clock high-level width		tCH	0.45	0.55	0.45	0.55	tCK	
Clock low-level width		tCL	0.45	0.55	0.45	0.55	tCK	
Clock half period		tHP	Min (tCL, tCH)		Min (tCL, tCH)		ns	10,11
Clock cycle time	CL=3	tCK	5		6		ns	12
	CL=2		12		12		ns	12
DQ and DM input setup time	fast	tDS	0.48		0.6		ns	13,14,15
	slow		0.58		0.7		ns	13,14,16
DQ and DM input hold time	fast	tDH	0.48		0.6		ns	13,14,15
	slow		0.58		0.7		ns	13,14,16
DQ and DM input pulse width		tDIPW	1.4		1.6		ns	17
Address and control input setup time	fast	tIS	0.9		1.1		ns	15,18
	slow		1.1		1.3		ns	16,18
Address and control input hold time	fast	tIH	0.9		1.1		ns	15,18
	slow		1.1		1.3		ns	16,18
Address and control input pulse width		tIPW	2.3		2.6		ns	17
DQ & DQS low-impedance time from CK/ $\overline{CK}$		tLZ	1.0		1.0		ns	19
DQ & DQS high-impedance time from CK/ $\overline{CK}$	CL=3	tHZ		5.0		5.0	ns	19
	CL=2			6.5		6.5		
DQS-DQ skew		tDQSQ		0.4		0.5	ns	20
DQ/DQS output hold time from DQS		tQH	tHP-tQHS		tHP-tQHS		ns	11
Data hold skew factor		tQHS		0.5		065	ns	11
Write command to 1st DQS latching transition		tDQSS	0.75	1.25	0.75	1.25	tCK	
DQS input high-level width		tDQSH	0.4	0.6	0.4	0.6	tCK	
DQS input low-level width		tDQSL	0.4	0.6	0.4	0.6	tCK	
DQS falling edge to CK setup time		tDSS	0.2		0.2		tCK	
DQS falling edge hold time from CK		tDSH	0.2		0.2		tCK	

Parameter		Symbol	- 5		- 6		Unit	Notes
			Min	Max	Min	Max		
MODE REGISTER SET command period		tMRD	2		2		tCK	
Write preamble setup time		tWPRES	0		0		ns	21
Write postamble		tWPST	0.4	0.6	0.4	0.6	tCK	22
Write preamble		tWPRE	0.25		0.25		tCK	
Read preamble	CL = 3	tRPRE	0.9	1.1	0.9	1.1	tCK	23
	CL = 2		0.5	1.1	0.5	1.1	tCK	23
Read postamble		tRPST	0.4	0.6	0.4	0.6	tCK	
ACTIVE to PRECHARGE command period		tRAS	40	70,000	42	70,000	ns	
ACTIVE to ACTIVE command period		tRC	tRAS+ tRP		tRAS+ tRP		ns	
AUTO REFRESH to ACTIVE/AUTO REFRESH command period		tRFC	72		72		ns	
ACTIVE to READ or WRITE delay		tRCD	15		18		ns	
PRECHARGE command period		tRP	3		3		tCK	
ACTIVE bank A to ACTIVE bank B delay		tRRD	10		12		ns	
WRITE recovery time		tWR	15		15		ns	24
Auto precharge write recovery + precharge time		tDAL	-		-		tCK	25
Internal write to Read command delay		tWTR	1		1		tCK	
Self Refresh exit to next valid command delay		tXSR	120		120		ns	26
Exit power down to next valid command delay		tXP	2		1		tCK	27
CKE min. pulse width (high and low pulse width)		tCKE	1		1		tCK	
Refresh Period		tREF		64		64	ms	
Average periodic refresh interval		tREFI		7.8		7.8	µs	28,29
MRS for SRR to READ		tSRR	2		2		tCK	
READ of SRR to next valid command		tSRC	CL+1		CL+1		tCK	

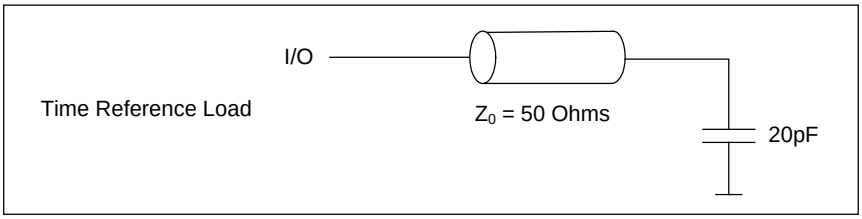
Notes:

1.All voltages referenced to VSS.

2.All parameters assume proper device initialization.

3.Tests for AC timing may be conducted at nominal supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage and temperature range specified.

4.The circuit shown below represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics). For the half strength driver with a nominal 10pF load parameters tAC and tQH are expected to be in the same range. However, these parameters are not subject to production test but are estimated by design / characterization. Use of IBIS or other simulation tools for system design validation is suggested.



5.The CK/$\overline{CK}$ input reference voltage level (for timing referenced to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross; the input reference voltage level for signals other than CK/$\overline{CK}$ is VDDQ/2.

6.The timing reference voltage level is VDDQ/2.

7.AC and DC input and output voltage levels are defined in the section for Electrical Characteristics and AC/DC operating conditions.

8.A CK/$\overline{CK}$ differential slew rate of 2.0 V/ns is assumed for all parameters.

9. $\overline{CAS}$ latency definition: with CL = 3 the first data element is valid at (2 * tCK + tAC) after the clock at which the READ command was registered ; with CL = 2 the first data element is valid at (tCK + tAC) after the clock at which the READ command was registered

10.Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits of tCL and tCH)

11.tQH = tHP - tQHS, where tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCL, tCH). tQHS accounts for 1) the pulse duration distortion of on-chip clock circuits; and 2) the worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.

12.The only time that the clock frequency is allowed to change is during clock stop, power-down or self-refresh modes.

13.The transition time for DQ, DM and DQS inputs is measured between VIL(DC) to VIH(AC) for rising input signals, and VIH(DC) to VIL(AC) for falling input signals.

14.DQS, DM and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.

15.Input slew rate ≥ 1.0 V/ns.

16.Input slew rate ≥ 0.5 V/ns and < 1.0 V/ns.

17.These parameters guarantee device timing but they are not necessarily tested on each device.

18.The transition time for address and command inputs is measured between VIH and VIL.

19.tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).

20.tDQSQ consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.

21.The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before the corresponding CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.

22.The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

23.A low level on DQS may be maintained during High-Z states (DQS drivers disabled) by adding a weak pull-down element in the system. It is recommended to turn off the weak pull-down element during read and write bursts (DQS drivers enabled).

24.At least one clock cycle is required during tWR time when in auto precharge mode.

25.tDAL = (tWR/tCK) + (tRP/tCK): for each of the terms, if not already an integer, round to the next higher integer.

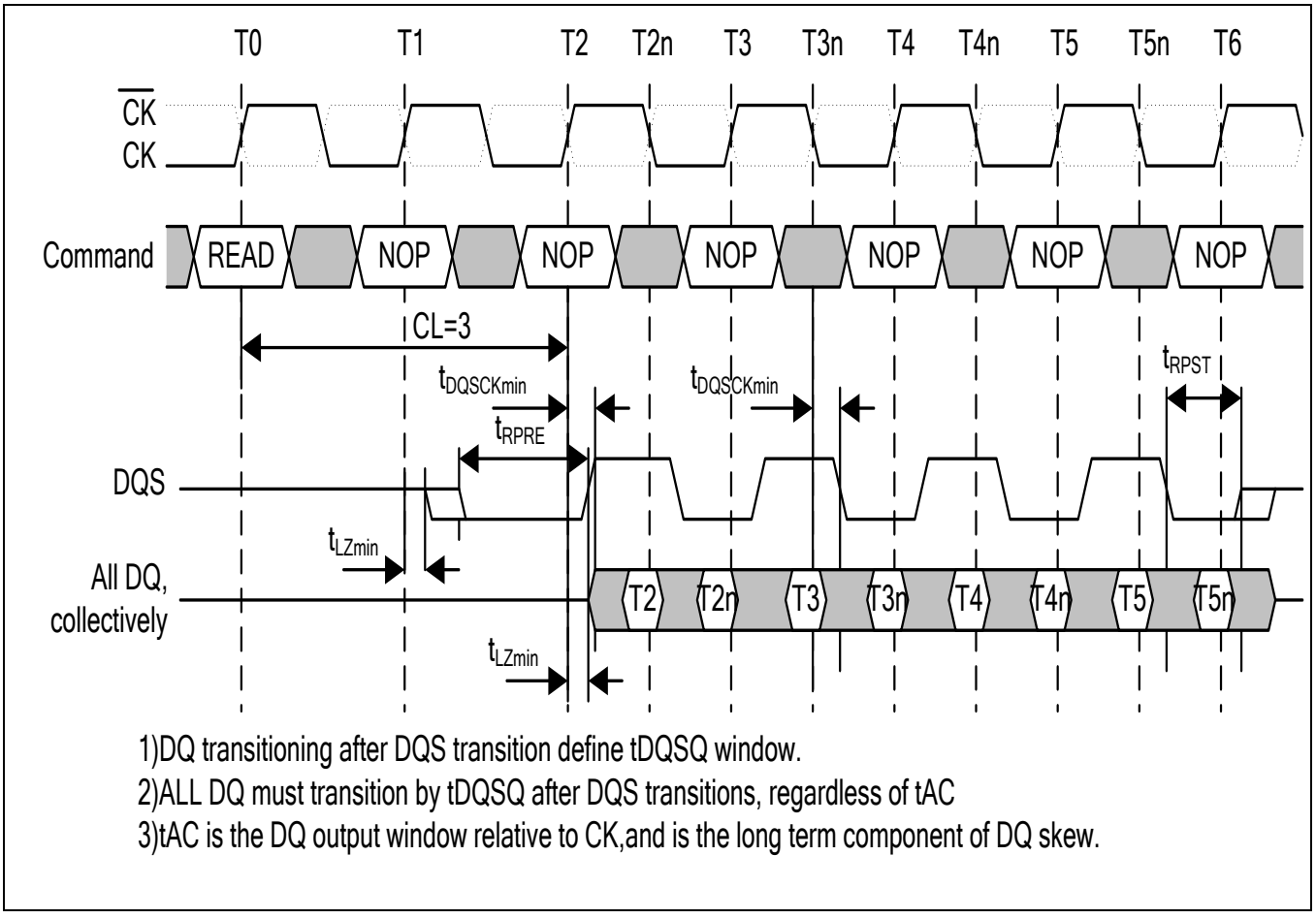
26.There must be at least two clock pulses during the tXSR period.

27.There must be at least one clock pulse during the tXP period.

28.tREFI values are dependent on density and bus width.

29.A maximum of 8 Refresh commands can be posted to any given LPDDR, meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 8*tREFI.

8.5.1 CAS Latency Definition (With CL=3)



8.5.2 Output Slew Rate Characteristics

Parameter	Min	Max	Unit	Notes
Pull-up and Pull-Down Slew Rate for Full Strength Driver	0.7	2.5	V/ns	1,2
Pull-up and Pull-Down Slew Rate for Three-Quarter Strength Driver	0.5	1.75	V/ns	1,2
Pull-up and Pull-Down Slew Rate for Half Strength Driver	0.3	1.0	V/ns	1,2
Output Slew rate Matching ratio (Pull-up to Pull-down)	0.7	1.4	-	3

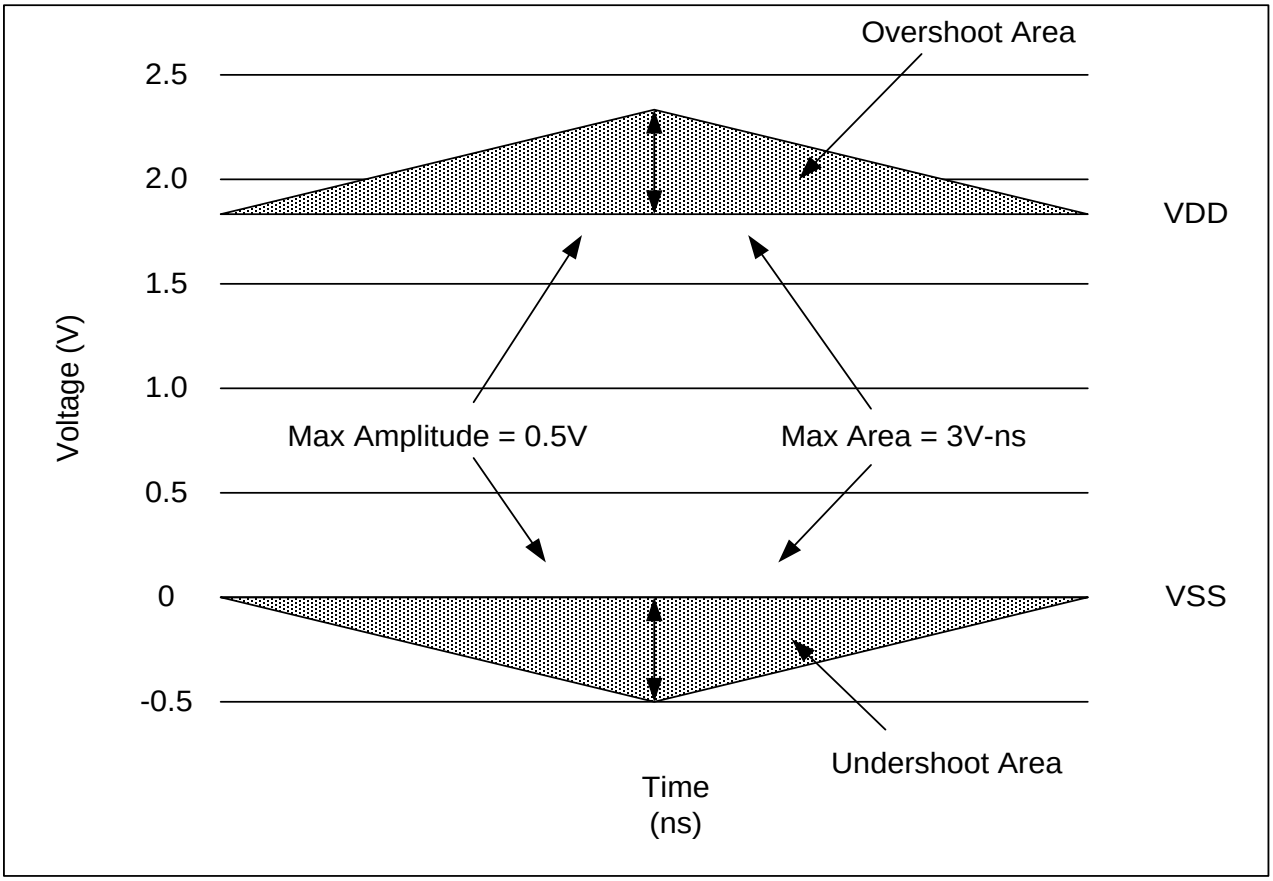
Notes:

1.Measured with a test load of 20 pF connected to V_{SSQ}.
2.Output slew rate for rising edge is measured between VILD(DC) to VIHD(AC) and for falling edge between VIHD(DC) to VILD(AC).
3.The ratio of pull-up slew rate to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.

8.5.3 AC Overshoot/Undershoot Specification

Parameter	Specification
Maximum peak amplitude allowed for overshoot	0.5 V
Maximum peak amplitude allowed for undershoot	0.5 V
The area between overshoot signal and VDD must be less than or equal to	3 V-ns
The area between undershoot signal and GND must be less than or equal to	3 V-ns

8.5.4 AC Overshoot and Undershoot Definition



9. REVISION HISTORY

Version	Date	Page	Description
P01-001	03/27/2012	All	First preliminary release.
P01-002	07/31/2012	2 18 50,51	Add ordering information. Update SRR[10:8]. Update IDDx value.
A01-001	09/21/2012	2 All 48 52	Update ordering information. Remove text “Preliminary”. Add note in section 8.1. Update IDD6 value.

Important Notice

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