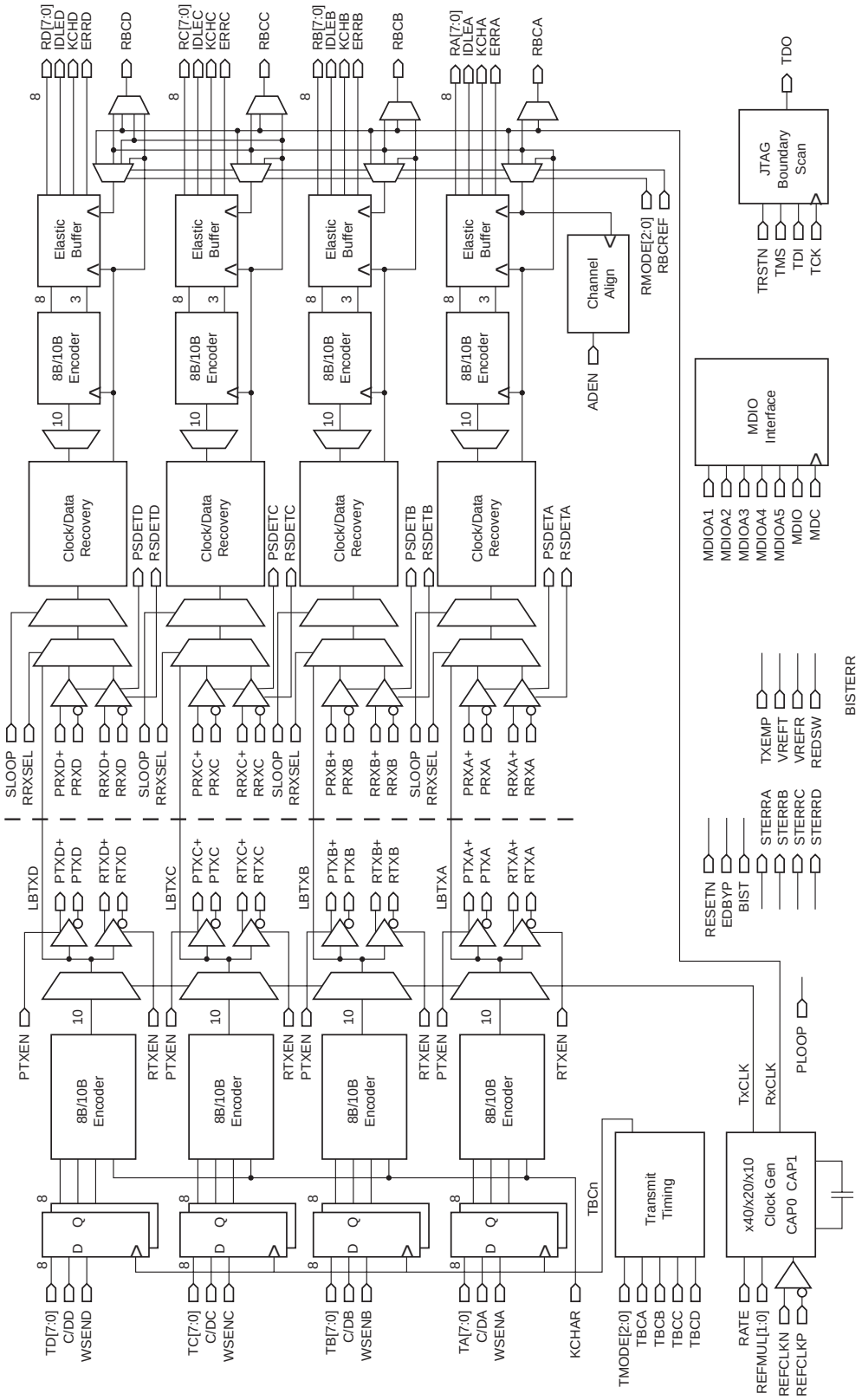
when describing common behavior, specifications, and requirements; references to individual variants will be used only where necessary and appropriate for clarity.

Notation

For purposes of this document, the VSC7226's four channels are identified as channel A, B, C or D. When discussing a signal on any specific channel, the signal will have the channel letter used as part of the name; for example, TA[7:0]. When referring to the common behavior of a signal which is used on each of the four channels, a lower case "n" is used in the signal name; for example, Tn[7:0]. Differential signals, such as PTXA+ and PTXA-, may be referred to as a single signal (for example, PTXA) by dropping reference to the "+" and "-". REFCLK refers either to the PECL/TTL input pair REFCLKP/REFCLKN, which can be differential PECL (using both REFCLKP and REFCLKN), or to single-ended TTL (using REFCLKP only).

VSC7226 Block Diagram



Clock Synthesizer

Depending on the state of the REFMUL[1:0] inputs, the VSC7226 clock synthesizer multiplies the reference frequency provided on the REFCLK input by 10, 20, or 40. A serial baud rate clock between 2.4GHz and 3.125GHz is thus obtained for the VSC7226-01 and between 1.9GHz and 2.52GHz for the VSC7226-02. The TBCn inputs are used to generate the data transfer clock for the parallel data lines. The on-chip Phase-Lock Loop (PLL) uses a single external 0.1µF capacitor to control the Loop Filter (see "External Capacitors" on page 21).

Further control of the serial baud rate and parallel data transfer rate is provided by the RATE pin. When RATE is HIGH, the transceiver functions at full rate, and when LOW, both rates are halved. The resulting serial baud rate ranges, when RATE is LOW, become 1.2Gb/s to 1.56Gb/s for the VSC7226-01, and 0.95Gb/s to 1.26Gb/s for the VSC7226-02, and the corresponding parallel data transfer rates are 120MByte/s to 156MByte/s, and 95MByte/s to 120MByte/s, respectively. The control of serial and parallel data rates by the REFMUL[1:0] and RATE pins is shown in Table 1 for the VSC7226-01. Similar relationships hold for the VSC7226-02. The RATE pin provides global rate control. All four channels are affected simultaneously by this control pin. When RATE is HIGH, the Management Data Input/Output (MDIO) interface may be used to access registers controlling the rates of each individual channel. Tx rates and Rx rates can also be controlled separately through the MDIO interface (see "Register Definitions" on page 25 for MDIO register definitions). When the MDIO register interface is used for individual channel control, the data rates of those channels operating in half rate mode differ from those in full rate mode by precisely a factor of one-half. Note that power to an operating device should be cycled when changing the REFMUL[1:0] or RATE pin settings to ensure proper operation.

Table 1. Use of the REFMUL[1:0] and RATE Pins for VSC7226-01 (3.125Gb/s example)

REFMUL[1:0]	Rate	REFCLK (MHz)	REFCLK Multiplier	Serial Baud Rate (Gb/s)	Parallel Transfer Rate (MByte/s)
00	1	312.5	x10	3.125	312.5
01	1	156.25	x20	3.125	312.5
10	1	78.125	x40	3.125	312.5
00	0	156.25	x10	1.5625	156.25
01	0	78.125	x20	1.5625	156.25
10	0	39.06	x40	1.5625	156.25
11	x	Reserved			

TRANSMITTER FUNCTIONAL DESCRIPTION

Transmitter Data Bus

Each VSC7226 transmit channel has an 8-bit, SSTL_2 input transmit data character, Tn[7:0], and two control inputs, C/Dn and WSENn. The C/Dn input determines whether a normal data character or a special "K-character" is transmitted, and the WSENn input initiates transmission of a 16-character "word sync sequence" used to align the receive channels.

The data to clock phasing can be chosen in either of two modes. The data may be clocked on the rising and falling edges of TBCn in the standard Double Data Rate (DDR) mode, or within the data eye formed by TBCn in a mode referred to as "ASIC Friendly." Which TBCn is used for clocking each channel is also controllable. There are three possible combinations. In the first mode, TBCA is used for all four channels. In the second mode, TBCA is used for channels A and B, and TBCC is used for channels C and D. In the third mode, each channel uses its own TBCn.

Both the data to clock phasing and the selection of TCBn are controlled by the TMODE[2:0] pins. Table 2 shows the relationships between these pin settings and the data to clock phasing and the clock source selection for each channel.

The TBCn inputs must be frequency-locked to REFCLK. No phase relationship is assumed. An internal phase detector is used to monitor and compensate for phase drift between TBCn and REFCLK.

Figure 1 shows the possible relationships between data and control inputs and TBCn.

Note that the TBCn input is not used directly to clock the input data. Instead, an internal PLL generates an input sampling clock that is phase-locked to TBCn.

Table 2. TBCn Timing Mode Selection with TMODE[2:0] Pins

TMODE[2:0]	CHAN A Clock	CHAN B Clock	CHAN C Clock	CHAN D Clock	TBC Mode
000	TBCA	TBCB	TBCC	TBCD	Data Eye
001	TBCA	TBCA	TBCC	TBCC	Data Eye
010	TBCA	TBCA	TBCA	TBCA	Data Eye
100	TBCA	TBCB	TBCC	TBCD	DDR
101	TBCA	TBCA	TBCC	TBCC	DDR
110	TBCA	TBCA	TBCA	TBCA	DDR
x11	Reserved				

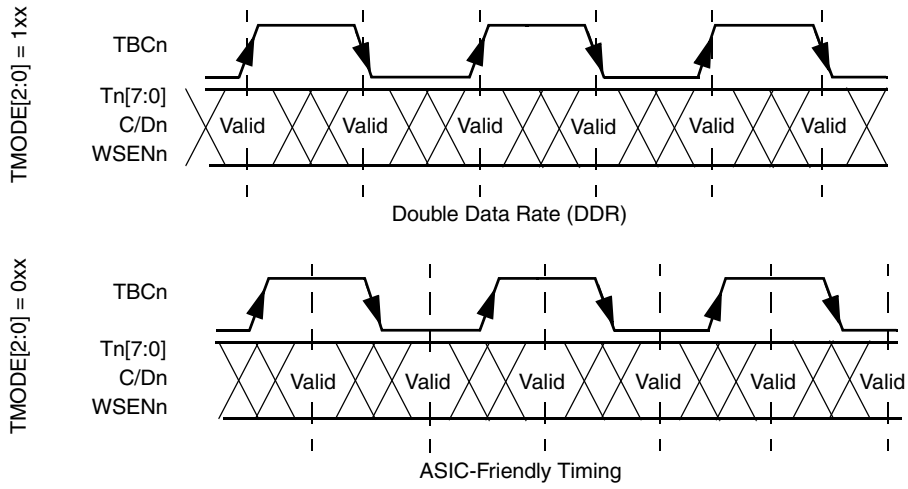


Figure 1. TBC Timing Modes

8B/10B Encoder

Each channel contains an 8B/10B encoder that translates the 8-bit input data on Tn[7:0] into a 10-bit encoded data character. C/Dn inputs are also provided in each channel which, along with KCHAR, allow the transmission of special Fibre Channel (FC) Kxx.x characters (see Table 3). Note that KCHAR is a static input, and does *not* have the same input timing as Tn[7:0], C/Dn and WSENn. Normally, C/Dn is LOW in order to transmit data. If C/Dn is HIGH and KCHAR is LOW, then a Fibre Channel defined IDLE Character (K28.5 = 0011111010 or 1100000101, depending on disparity) is transmitted and Tn[7:0] is ignored. If C/Dn is HIGH and KCHAR is HIGH, a Kxx.x character is transmitted as determined by the data pattern on Tn[7:0] (see Table 4).

When in the K-character transmission mode, 8-bit data patterns other than those defined in Table 4 produce undefined 10B encodings. Should such an invalid encoding occur, the VSC7226 will output either of two specific 10B characters, depending upon the current running disparity. For current RD-, 001111 0001 will be output and for RD+, 110000 1110 will be output. Optionally, the transmitter may be configured to output the K30.7 of the appropriate disparity instead of the above two characters. This is accomplished through the MDIO interface (see "Register Definitions" on page 25 for MDIO register definitions).

Table 3. Transmit Data Controls

WSENn	C/Dn	KCHAR	Encoded 10-Bit Output
0	0	X	Data Character
0	1	0	IDLE Character (K28.5)
0	1	1	Special Kxx.x Character
1	x	x	16-Character Word Sync Sequence

Table 4. Special Characters (selected when C/Dn and KCHAR are HIGH)

Code	Tn[7:0]	Comment	Code	Tn[7:0]	Comment
K28.0	000 11100	User Defined	K28.5–	101 01101	User Defined
K28.1	001 11100	User Defined	K28.6	110 11100	User Defined
K28.2	010 11100	User Defined	K28.7	111 11100	Test Only
K28.3	011 11100	User Defined	K23.7	111 10111	User Defined
K28.4	100 11100	User Defined	K27.7	111 11011	User Defined
K28.5	101 11100	IDLE	K29.7	111 11101	User Defined
K28.5+	101 01100	User Defined	K30.7	111 11110	User Defined

Encoder Bypass Mode

If Encoder/Decoder Bypass (EDBYP) is HIGH, the 8B/10B encoder is bypassed. In this case, Tn[7:0] operates normally, but C/Dn is equivalent to Tn8, WSENn is equivalent to Tn9, and the KCHAR input becomes ENCDET which, when HIGH, enables comma detection in all four receivers. Note that, as in the case of KCHAR, ENCDET is a static input and does not have the same input timing as Tn[9:0]. Comma detection is always enabled when EDBYP is LOW (see "Deserializer and Character Alignment" on page 10 for a description of comma detection). The latency through the transmitter is reduced when EDBYP is HIGH. This mode of operation is equivalent to a 10-bit interface commonly found in SerDes for Fibre Channel and Gigabit Ethernet (GbE) applications (VSC7123 and VSC7139). The effect of the EDBYP pin is global. All four channels are affected simultaneously by this pin. When EDBYP is LOW, encoder/decoder bypassing on a per-channel basis is possible. The MDIO interface may then be used to access

internal registers controlling each individual channel. Independent Tx and Rx bypassing can also be controlled (see "Register Definitions" on page 25 for MDIO register definitions).

Word Sync Generation

The VSC7226 can perform channel alignment (also referred to as word alignment or word sync). Word sync means that the selected receive data output streams are aligned such that the same N-byte word (N = 2 or 4) presented to the N transmit channel inputs for serialization will be transferred on the receive channel parallel outputs. The word sync sequence provides a unique synchronization point in the serial data stream that is used to align the receive channels. This sequence consists of 16 consecutive K28.5 IDLE characters with disparity reversals on the second and fourth characters. The word sync sequence is sent either as I+ I+ I- I- I+ I- I+ I- I+ I- I+ I- I+ I- I+ I- or I- I- I+ I+ I- I+ I- I+ I- I+ I- I+ I- I+ I- I+, depending on the transmitter's running disparity at the time the first IDLE character is serialized.

Alternatively, a different alignment character may be defined for this purpose. The MDIO management interface is used to enable this feature and to define the alternate 8-bit K-character to be used (see "MDIO/MDC Serial Interface" on page 21 for MDIO register definitions).

Transmission of the word sync sequence is initiated independently in each channel when the WSENn input is asserted HIGH for one character time (see Figure 2 on page 7). When WSENn is HIGH, the C/Dn and Tn[7:0] inputs are ignored. The WSENn, C/Dn and Tn[7:0] inputs are also ignored for the subsequent 15 character times. In Figure 2 on page 7, the word sync sequence is initiated in cycle W1 and transmitted through cycle W16. Normal data transmission (or the transmission of another word sync sequence) resumes in cycle D3. As long as WSENn remains asserted, another word sync sequence will be generated.

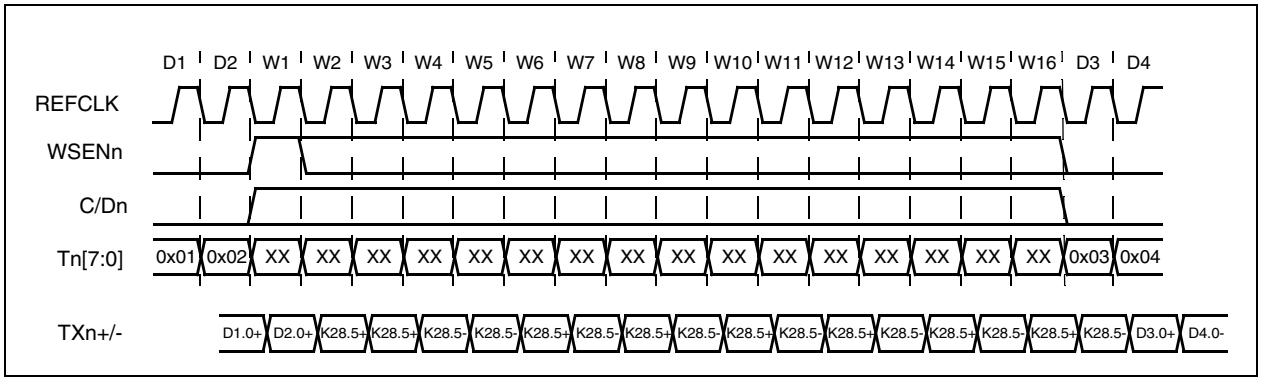


Figure 2. Word Sync Sequence Generation

Serializer

The 10-bit output from the 8B/10B encoder (or from the input buffer if EDBYP is HIGH) is fed into a multiplexer which serializes the parallel data using the synthesized transmit clock. The least significant bit (LSB) of the 10B data is transmitted first. Each channel has both primary and redundant serial output ports, PTXn and RTXn, respectively, which consist of differential PECL output buffers operating at either 10, 20 or 40 times the REFCLK frequency (depending on REFMUL[1:0] settings). All four primary PECL outputs (PTXn) are enabled when the PTXEN input is HIGH, and the redundant PECL outputs RTXn are enabled when the RTXEN input is HIGH. When a PECL output is disabled, the associated output buffers do not consume power and the associated output pins are not driven. PTXEN and RTXEN are global control pins, simultaneously affecting the status of all four channels' primary and redundant

PECL outputs. When PTXEN and RTXEN are HIGH, independent control of all four channels is possible, and the MDIO interface may be used to access internal registers controlling each individual channel (see "Register Definitions" on page 25 for MDIO register definitions).

Transmitter Pre-Emphasis

High-speed digital waveforms are subject to "skin-effect phenomena" such as velocity dispersion and frequency-dependent attenuation of their Fourier components. These effects cause the signal to become increasingly distorted with increasing propagation distance along a transmission medium. The situation is exacerbated with increasing frequency. Recognizing this, the VSC7226 provides the capability of signal predistortion, or pre-emphasis in its transmitter section. When used, transmit pre-emphasis will cause the PECL transmitter outputs to compensate for the skin effect distortion. When signal pre-emphasis is chosen, the effects of predistortion and skin effect distortion will offset and a high quality waveform will be seen at the input of the receiving device.

Control of the pre-emphasis feature on a global basis is provided through the TXEMP pin. When HIGH, pre-emphasis is enabled on all four channels. When set LOW, transmitter pre-emphasis is disabled on all four channels. Also, when LOW, the allocated MDIO interface registers may be set such that pre-emphasis may be enabled on each individual channel (see "Register Definitions" on page 25 for details on using the MDIO interface and registers.)

Reduced Transmitter Serial Output Swing

The VSC7226 provides a mode of operation in which the high-speed PECL transmitter output voltage swing is reduced by approximately one-half. This mode may be useful driving signals over short distances. It carries the benefit of a reduction in the total power consumption of the device. Refer to "DC Characteristics" on page 41 for power consumption specifications.

Control of this function is provided on a global basis with the REDSW pin and on a per-channel basis through the MDIO interface. When REDSW is HIGH, all channels operate in the reduced swing mode and swing in full power on individual channels may be selected through the MDIO registers (see "Register Definitions" on page 25 for details on using the MDIO interface and registers). When REDSW is LOW, full output swing is always enabled on all channels and per-channel register programmable output swing is not accessible.

On-Chip Transmit and Receive Terminations

The VSC7226 features on-chip terminations for all high-speed serial PECL inputs and outputs.

On the receive side the on-chip input termination value is controllable by means of the RREF pin. A single external reference resistor, when connected between RREF and ground, will control the value of differential input resistance for all channels. The range of control is between values of 100Ω and 150Ω. The ratio of external RREF resistance to PECL termination resistance is approximately 1:1. For example, to obtain a differential input termination resistance of approximately 100Ω, use an external resistor of 100Ω. Placing the external resistor physically close to the VSC7226 is not required. RREF is a global configuration pin affecting the primary and redundant PECL inputs for all four channels. Control of the termination values on a per-channel basis is not provided.

On the transmit side, the output termination value is fixed. External control of this value is not provided.

Receiver Functional Description

Serial Data Source

Each receive channel has both primary and redundant serial input ports, PRXn and RRXn, respectively, which consist of differential PECL input buffers. Simultaneous control of primary/redundant serial inputs for all four channels is provided by the RRXSEL pin. When RRXSEL is HIGH, the redundant inputs are selected and the primary inputs are deselected. The reverse is true for RRXSEL LOW. When RRXSEL is HIGH, each channel can also be controlled individually via the MDIO interface. If independent control of all four channels is required, the MDIO interface must be used to access internal registers controlling each individual channel (see "Register Definitions" on page 25 for MDIO register definitions).

When serial loopback is enabled (SLOOP is HIGH), the channel's transmitter is looped back and becomes the serial data source regardless of the state of RRXSEL. See "Loopback Operation" on page 18 for details on this mode of operation.

Signal Detection and Output Squelching

Each channel's primary and redundant PECL input buffers have an associated signal detect status output, PSDETn and RSDETn. All eight outputs are available for continuous monitoring of both the selected and non-selected input. Each signal detect output is asserted HIGH when transitions are detected on the associated PECL input and the differential signal peak-to-peak swing exceeds approximately 270mV differential. A LOW indicates that either no transitions are detected or the signal amplitude is below approximately 65mV differential. The signal detect outputs are considered undefined when the signal swing is in the 65mV to 270mV differential range. The signal detect circuitry behaves like a re-triggerable one-shot that is triggered by signal transitions, and whose time-out interval ranges from 40 bit to 80 bit times. The transition density is not checked to make sure that it corresponds to a valid Fibre Channel data stream. The PSDETn and RSDETn output timing is identical to the low-speed receiver outputs, as selected by RMODE[2:0] in Table 6 on page 13.

The VSC7226 features a receiver output squelching capability, selectable on a per-channel basis. This capability can only be enabled through the MDIO interface (see "MDIO/MDC Serial Interface" on page 21 for MDIO register definitions). When squelching is enabled, the selected channel's parallel outputs will be driven HIGH when the detected differential signal voltage is less than 65mV differential on either PRXn+/- or RRXn+/-, whichever is in use for that channel. There is no external pin providing global control of this function. Control is only provided through the settings of these MDIO register bits. The default condition for all channels is output squelch disabled.

Receiver Equalization

Incoming data on the Rx inputs typically contains a substantial amount of Inter Symbol Interference (ISI) or deterministic jitter that reduces the ability of the receiver to recover data without errors. An equalizer has been added to each of the receiver's input buffers in order to compensate for this deterministic jitter. This circuit has been designed to effectively reduce the ISI commonly found in copper cables or backplane traces due to low frequencies being attenuated less than high frequencies as a result of the skin effect. The equalizer boosts high frequency edge response in order to reduce the adverse effects of ISI. This feature is especially important with 3.125Gb/s signals when using long copper cable or PCB traces.

Clock and Data Recovery

At the receiver, each channel contains an independent Clock Recovery Unit (CRU) that accepts the selected serial input source, extracts the high-speed clock, and retimes the data. Each CRU automatically locks on data and if the data is not present, will automatically lock to the REFCLK.

The CRU must perform bit synchronization, which occurs when the CRU locks onto and properly samples the incoming serial data as described in the previous paragraph. When the CRU is not locked onto the serial data, the 10-bit data out of the decoder is invalid, which results in numerous 8B/10B decoding errors or disparity errors. In the absence of data at the input, noise present at the serial inputs may be interpreted as "data" and may appear as random data bits with REFCLK-based timing at the receiver's parallel outputs. The squelching feature, described in "Signal Detection and Output Squelching" on page 9, can be used to ignore the noise and force the parallel outputs to the HIGH state. When the link is disturbed (the cable is disconnected or the serial data source is switched), the CRU will then require a certain amount of time to lock onto data. The CRU in the VSC7226 is designed with a fast-locking feature, permitting high-speed data transmission in the presence of frequent serial switching. The time required for CRU lock is specified as 290 data transitions. See "General Receive AC Characteristics" on page 46 for details on CRU lock time.

The CRUs for all four channels operate in full-speed mode if RATE is HIGH or at half-speed mode if RATE is LOW. When RATE is set HIGH, the MDIO interface may be used to access internal registers controlling each individual channel (see "MDIO/MDC Serial Interface" on page 21 for MDIO register definitions).

Deserializer and Character Alignment

The retimed serial data stream is converted into 10-bit characters by the deserializer. A special 7-bit "comma" pattern (0011111xxx or 1100000xxx) is recognized by the receiver and allows it to identify the 10-bit character boundary. Note that this pattern is found in three special characters, K28.1, K28.5 and K28.7; however, K28.5 is chosen as the unique IDLE character. Only K28.1 and K28.5 should be used in normal operation. The K28.7 character should be reserved for test and characterization use.

Character alignment occurs when the deserializer synchronizes the 10-bit character framing boundary to a comma pattern in the incoming serial data stream. If the receiver identifies a comma pattern in the incoming data stream, which is misaligned to the current framing boundary, the receiver will resynchronize the recovered data in order to align the data to the new comma pattern. In this process, RBC is neither stretched nor slivered; character alignment is achieved by adjusting the latency through the elastic buffers. Resynchronization ensures that the comma character is output on the internal 10-bit bus so that bits 0 through 9 equal 0011111xxx or 1100000xxx. If the comma pattern is aligned with the current framing boundary, then resynchronization will not change the current alignment. Resynchronization is always enabled and is not turned off when EDBYP is LOW. After character resynchronization the VSC7226 ensures that within a channel, the 8-bit data sent to the transmitting VSC7226 will be recovered by the receiving VSC7226 in the same bit locations as the transmitter (Tn[7:0] = Rn[7:0]).

It is possible to enable comma detection only when in the Loss of Synchronization (LOS) state, rather than at all times. This may be desirable to prevent character realignment due to false commas resulting from single-bit errors. LOS-only comma detection may be enabled on a per-channel basis through the MDIO interface (see "Register Definitions" on page 25 for MDIO register definitions).

10B/8B Decoder

The 10-bit character from the deserializer is decoded in the 8B/10B decoder, which outputs the 8-bit data byte and three bits of status information. If the 10-bit character does not match any valid value, an out-of-band error is generated, which is output on the receiver status bus. Additionally, the VSC7226 may be configured to output K30.7 at the parallel interface when such a condition occurs. This is achieved through the MDIO interface (see "Register Definitions" on page 25 for details).

Similarly, if the running disparity of the character does not match the expected value, a disparity error is generated. For diagnostic purposes, internal 32-bit counters are provided that keep a separate running count of the number of 10-bit code errors and disparity errors. Access to these registers is through the MDIO port (see "MDIO/MDC Serial Interface" on page 21 for a description of MDIO registers). Unless disabled, the counters will function when the VSC7226 is operating in Built-in Self-Test (BIST) mode as well as in normal mode. The decoder also reports when a K-character is received, and distinguishes the K28.5 (IDLE) character from other K-characters. This status information is combined with Loss of Synchronization State Machine (LSSM) status and FIFO error status to produce the prioritized per-character link status output information (see Table 9 on page 18).

Decoder Bypass Mode

If EDBYP is HIGH, the 8B/10B decoder is bypassed. In this case, Rn[7:0] operates normally, but KCHn is equivalent to Rn8, ERRn is equivalent to Rn9, and IDLEn is equivalent to Comma Detect (COMDET). The KCHAR input is equivalent to ENCDET, which when LOW, always disables Comma Detection in all four channels. When KCHAR is HIGH, it enables Comma Detection in all four receivers. In TBI mode, the Comma Detection function CANNOT be accessed through MDIO register. The latency through the receiver is reduced when EDBYP is HIGH. This mode of operation is equivalent to a 10-bit interface commonly found in SerDes for the Fibre Channel and Gigabit Ethernet markets (VSC7123 and VSC7139). If encoder/decoder bypassing on a per-channel basis is required, the MDIO interface must be used to access internal registers controlling each individual channel. Independent Tx and Rx bypassing can also be controlled (see "MDIO/MDC Serial Interface" on page 21 for MDIO register definitions).

Comma Alignment

The VSC7226 defines which edge of RBC is used for comma alignment. This allows for the setting of the alignment of comma only to a desirable edge by stretching RBC. When comma is detected on the opposite edge of the desirable clock edge, the RBC will be stretched to make the comma aligned with the desirable clock edge. When this alignment occurs, there will be no latency change. If consecutive comma characters are present in the data stream, the re-alignment only occurs at the last comma.

This feature can be enabled on per-channel basis through MDIO register 23. It is independent of other mode controls such as RMODE2 and EDBYP. The default value is to be backward-compatible, so that the comma can be aligned to either the rising or the falling edge of RBC.

Elastic Buffer

An elastic buffer is incorporated into each of the four receive channels. Decoded data and status information is written into these buffers on each channel's recovered clock and is read on the selected output clock. In addition to allowing decoded data to easily cross from a channel's recovered clock domain to its output clock domain, the elastic buffers facilitate channel alignment (the reconstruction of a multi-byte word as presented to the transmitting devices). Data skew of up to 90 bit times can be accommodated when the word synchronization points are separated sufficiently in time. See "Word Alignment and Channel-to-Channel Deskew" on page 14. The elastic buffers also facilitate rate

matching via IDLE character insertion/deletion when the channel's recovered clock is not frequency-locked to its output clock.

There are three conditions that cause adjustment of the FIFO read pointer in a receive channel's elastic buffer: the RESETN input, when asserted, readjusts the read/write pointers in each elasticity buffer's FIFO; whenever a comma character is received that changes the receive character's framing boundary, the pointer is adjusted; and lastly, it is also adjusted whenever the receiver detects the synchronization point in the word sync sequence. All three of these events are associated with chip initialization or link initialization and would not occur during normal data transfer. Note that readjustment can result in the loss or duplication of decoded character data and status information.

Receiver Output Timing

The VSC7226 presents recovered data on Rn[7:0] and status on IDLEn, KCHn and ERRn. The recovered data for channels A through D may be word aligned (or word synchronized), in three selectable modes. Control of word alignment is accomplished by choosing the appropriate timing references via the RMODE([2:0] pins. In 32-bit mode (RMODE[2:0] = x10), all four channels are aligned. In this mode, RBCA serves as the timing reference for Rn[7:0]. In 16-bit mode (RMODE[2:0] = x01), channels A and B are aligned and channels C and D are aligned. The recovered byte clock used for channels A and B is RBCA, and the clock for channels C and D is RBCC. When RMODE[2:0] = x00, the four channels function independently and each channel's recovered byte clock is derived from its own data.

In addition to timing the receiver's parallel outputs according to one or more of the recovered byte clocks, the data output timing may be derived from REFCLK. It is derived in the same manner as the transmitter input timing reference is obtained from REFCLK through the PLL circuitry. This mode of operation is globally enabled by using the RBCREF pin. When RBCREF is HIGH, all four channels' output timing is derived from REFCLK, regardless of the state of the RMODE0 and RMODE1. When RBCREF is LOW, the recovered byte clocks are used, or the MDIO interface may be used to select REFCLK based timing on a per-channel basis (see "MDIO/MDC Serial Interface" on page 21 for MDIO register definitions).

Regardless of which output timing source is selected for each channel with RBCREF or MDIO register settings, the corresponding output clock will also appear at the RBCn output pin.

The RMODE[2:0] pins are also used to specify one of two possible clock to data phase relationships, DDR or the ASIC Friendly (data eye). When RMODE[2:0] = 0xx, RBCn is centered approximately in the output data valid window, with clock edges occurring during data transition periods. When RMODE[2:0]=1xx, RBCn slightly leads the data valid window so that clock edges occur during the data valid periods. These relationships are shown in Figure 3 on page 12 and Figure 4 on page 13.

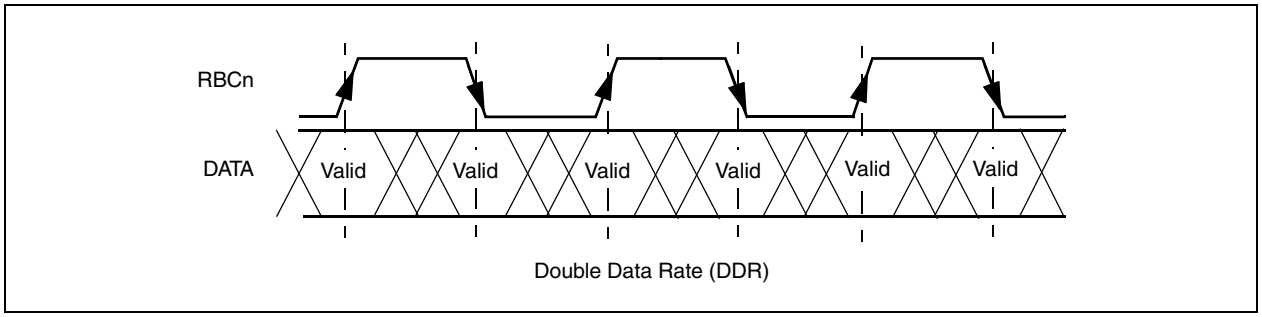


Figure 3. Receive Timing, RMODE[2:0] = 1xx

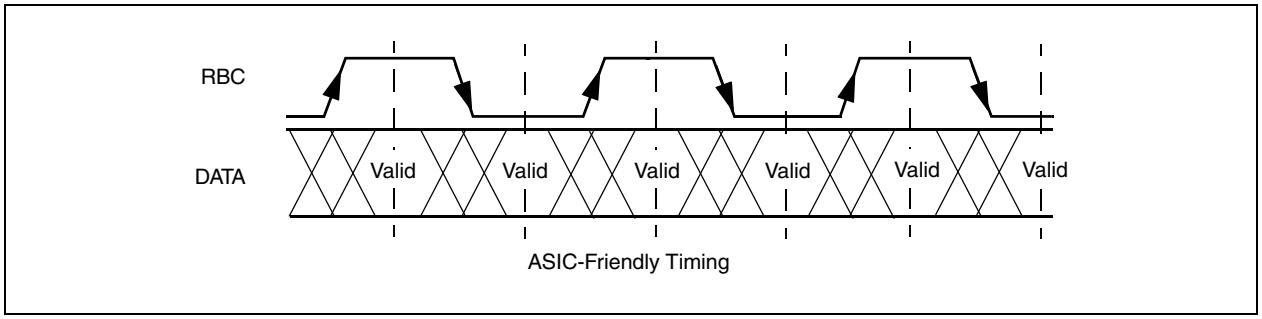


Figure 4. Receive Timing, RMODE[2:0] = 0xx

The correspondence between RBCREF and RMODE[2:0] settings and the resulting timing parameters is shown in Table 5, Table 6, and Table 7.

Table 5. Relationships Between RBCREF and Parallel Data Output Timing

RBCREF	FIFO Read Timing Source
1	REFCLK Based
0	Recovered Byte Clock

Table 6. Relationships Between RMODE[1:0] and Recovered Byte Clocks for Each Channel

RMODE[1:0]	RBCA Clock	RBCB Clock	RBCC Clock	RBCD Clock
00	CHAN A	CHAN B	CHAN C	CHAN D
01	CHAN A	CHAN A	CHAN C	CHAN C
10	CHAN A	CHAN A	CHAN A	CHAN A
11	Reserved			

Table 7. Relationship Between RMODE2 and Parallel Data Output Timing Mode

RMODE2	Data Timing Mode
1	Double Data Rate (DDR)
0	Data Eye (ASIC style)

The term “word clock” is used to describe the receiver’s parallel output clock. The recovered clock or REFCLK may be selected as this output timing reference. The word clock in use for each channel is output on RBCn. Data at the four output ports is synchronously clocked out on both positive and negative edges of the selected word clock whose frequency is 1/20th the baud rate. Timing waveforms for the output data and status are shown in Figures 3 and 4.

The data coming from the 8B/10B decoder is clocked into the elastic buffer by the recovered clock from the channel’s CRU. The data is clocked out of the elastic buffers with the word clock. If the transmitting device’s REFCLK is not precisely frequency-locked to a receive channel’s word clock, the channel’s elastic buffer will tend to gradually fill or empty as the recovered clock (which, by definition, is frequency-locked to the transmitter’s REFCLK) steadily drifts relative to the word clock.

Tx/Rx Rate Matching

In order to accommodate frequency differences between a transmitter's REFCLK and the receiver's word clock, the VSC7226 can automatically perform rate matching by either deleting one or inserting up to two IDLE characters. The IDLE character used for this purpose may be redefined to be a valid K-character other than K28.5 by using the appropriate MDIO register (see "MDIO/MDC Serial Interface" on page 21 for MDIO register definitions). The ADEN input must be LOW to enable rate matching, which can either be performed in each channel individually, or can be performed in parallel across a group of channels that are word-aligned. This is discussed in detail in the following section. When ADEN is set HIGH, IDLE insertion/deletion on an individual channel basis may be enabled via the MDIO register interface (see "MDIO/MDC Serial Interface" on page 21 for details).

It is the user's responsibility to ensure that the frequency at which IDLEs are simultaneously transmitted on each channel accommodates the frequency differences, if any, in their system architecture. Not meeting the IDLE density requirements could result in FIFO underrun or overrun errors. Note that if the user has the receiver configured in independent channel mode (RMODE[2:0] = x00), it is not required that the IDLEs be sent simultaneously.

The elastic buffer is designed to allow a maximum phase drift of +10 or -10 serial clock bit times (one character time) between resynchronizations, which sets a limit on the maximum data "packet" length allowed between IDLEs. This maximum packet length depends on the frequency difference between the transmitting and receiving devices REFCLKs. Let $\Delta\phi$ represent phase drift in bit times, and let 2π represent one full 10-bit character of phase drift. Limiting phase drift to two bit times means the following inequality must be satisfied:

$$\Delta\phi \leq (2\pi) \quad \textbf{(EQ 1)}$$

Let L be the number of 10-bit characters transmitted, and let Δf be the frequency offset in ppm. The total phase drift in bit times is given by:

$$(\Delta\phi = (\Delta f / 10^6) \times 2\pi L) \quad \textbf{(EQ 2)}$$

A simple expression for maximum packet length as a function of frequency offset is derived by substituting (EQ2) in (EQ1) and solving for L:

$$L \leq (10^6) / \Delta f \quad \textbf{(EQ 3)}$$

As an example, if the frequency offset is 200ppm, then the maximum packet length should not be more than 5K bytes. To increase the maximum packet length L, decrease the frequency offset, Δf.

Word Alignment and Channel-to-Channel Deskew

The VSC7226 performs channel-to-channel word alignment. In this mode of operation, if the data from all four channels on the transmitting VSC7226 (the four Tn[7:0] busses) is viewed as a 32-bit word, then the receiving VSC7226 will recover an identical word. For example, if a transmit pattern were "ABCD", "EFGH", "IJKL", and so on, the receiver should recover data words in the correct order as "ABCD", "EFGH", "IJKL", and so on.

Similarly, word alignment can be selected in a dual 16-bit mode, where channels A and B are aligned to each other and channels C and D are aligned to each other. See Table 5 for 16-bit and 32-bit RMODE[2:0] settings.

Within the receiver there are elastic buffers used to deskew the dual channels in 16-bit mode or quad channels in 32-bit mode and align them to a common word clock. With sufficient separation between alignment points, the elastic buffer allows the channels' input to be skewed up to 90 bit times in order to accommodate circuit imperfections, differences in transmission delay, and jitter. To achieve this maximum skew tolerance, the alignment point separation must be a minimum of 220 bit times.

With an alignment point separation of less than 220 bit times, this separation will limit the amount of skew the VSC7226 can tolerate. Theoretically, lane skew in excess of one-half the separation in alignment points cannot be interpreted unambiguously. The amount of bit times of correctable skew (t_{SKEW}) as a function of alignment point separation (t_{SEP}) is given by:

$$t_{SKEW} < (t_{SEP}/2) - 20 \quad \textbf{(EQ 4)}$$

For example, when sending the 16-character (160 bits) word synchronization sequence, the time separation of alignment points is 160 bit times, and the resulting maximum correctable skew is 60 bit times.

In order to perform word alignment, a synchronization point must be seen across all aligned receive channels. The VSC7226 receiver recognizes the first four characters of the word sync sequence (either K28.5+ K28.5+ K28.5- K28.5- or K28.5- K28.5- K28.5+ K28.5+) as the synchronization point. At the user's discretion, an alternative alignment character may be assigned (see "MDIO/MDC Serial Interface" on page 21 for MDIO register definitions). When an alignment character is defined, one alignment character marks the synchronization point. As a model for understanding, consider the case where a VSC7226 transmitter sends 32 bits of data to the receiver via copper media, which has small cable length differences causing a channel-to-channel skew. All transmit channels that are to be word aligned transmit the word sync sequence in parallel. On detection of the synchronization point, the receivers will reposition the recovered data within their elastic buffers in order to align all four channels and remove any channel-to-channel skew. All normal data characters following the word sync sequence will be properly word aligned. In the process of channel alignment, one or two of the final twelve Kxx.x characters in the word sync sequence may be deleted or duplicated. This ensures that each transmitted 32-bit word is recovered correctly.

The VSC7226 performs rate matching in word-aligned applications by inserting or deleting add/drop characters in parallel across the aligned receive channels. This requires that the word-aligned data streams contain add or drop characters inserted in parallel on all transmit channels (an add or drop "word") according to the density requirement previously described. Otherwise, word alignment cannot be maintained.

Word alignment is enabled by selecting the appropriate RMODE[2:0] settings. The ADEN input state determines whether or not rate matching (add/drop insertion or deletion) will be performed. Table 8 shows the relationship between these settings.

Table 8. Word Alignment and Rate Matching Control

RMODE[2:0]	ADEN	Word Alignment	Rate Matching
x00	1	Off	Off
x01	1	16-bit	Off
x10	1	32-bit	Off
x00	0	Off	On
x01	0	16-bit	On
x10	0	32-bit	On
x11	x	Reserved	

With word alignment off and rate matching on, each channel operates independently with each channel individually rate matched. With 16-bit word alignment selected and rate matching on, the aligned channels A and B are rate-matched and the aligned channels C and D are rate-matched. The A and B rate may differ from the C and D rate. With 32-bit word alignment, all four channels are aligned and rate-matched.

Receiver State Machine

Each channel contains two possible LSSMs are responsible for detecting and handling loss of bit, channel, word and word clock synchronization in a controlled manner. The state diagram shown in Figure 5A is in effect for all channels unless the MDIO interface is used to select, on a per-channel basis, the alternate state diagram shown in Figure 5B (see "MDIO/MDC Serial Interface" on page 21 for details).

There are three states in the LSSM depicted in Figure 5A: LOSS_OF_SYNC, RESYNC, and SYNC_ACQUIRED, as shown in the state diagram. The RESYNC state is entered when a 10-bit word has been received which contains the 7-bit comma pattern (for example, a K28.5 IDLE character). After entering the RESYNC state, the VSC7226 will stay in it until a valid, non-comma transmission is received, then it transitions to the SYNC_ACQUIRED state indicating a normal operating condition. The RESYNC state is re-entered if four consecutive commas are received or if a single comma is received that changes the 10B character framing boundary. The LOSS_OF_SYNC state is entered whenever four consecutive invalid transmissions have been detected or when the occurrences of invalid transmission outnumber those of valid transmission by four. The relative occurrences of invalid vs. valid transmissions are monitored with a simple up/down counter that increments when an invalid transmission is detected and decrements otherwise. The LSSM transitions to the LOSS_OF_SYNC state when the counter reaches four, and the counter is reset. A state diagram for the invalid transmission counter is shown in Figure 6. The VSC7226 receiver will stay in the LOSS_OF_SYNC state until a valid comma pattern is detected. Note that the RESYNC state is entered whenever the 10B framing boundary is changed, and whenever the word sync sequence is received.

There are two states in the LSSM shown in Figure 5B: LOSS_OF_SYNC and SYNC_ACQUIRED. In the LOSS_OF SYNC state, the appearance of a valid comma pattern will cause the VSC7226 to move to the SYNC_ACQUIRED state. Movement from the SYNC_ACQUIRED state to the LOSS_OF_SYNC state is mediated by the invalid transmission counter.

When using either of the LSSMs shown in Figure 5, additional control of the invalid transmission counter on a per-channel basis is provided through the MDIO interface. Two parameters pertaining to this counter may be varied independently, giving control over the rate of data errors required to drive the device into the LOSS_OF_SYNC state. The number of valid transmissions required to progress one state lower in the counter (state 3 to state 2 to state 1 to state 0) may be set at 1, 2, 3, or 4. Higher numbers cause lower error rates to drive the device into the LOS state. The default setting is 1.

A second variable parameter available for either LSSM is the code block size that is examined for valid/invalid transmissions. The code block size may be varied from one to eight characters in length. The default setting is a code block size of one character. Larger code block sizes cause lower data error rates to drive the device into the LOS state. See "MDIO/MDC Serial Interface" on page 21 for details on how to control these two parameters.

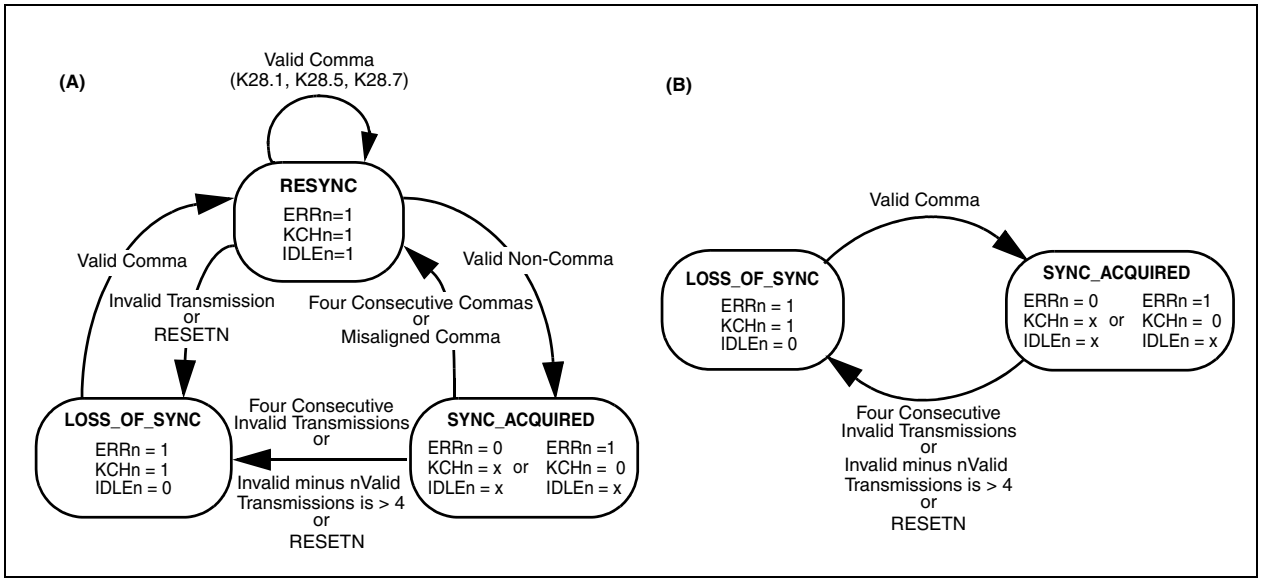


Figure 5. State Diagrams of Loss of Synchronization State Machine

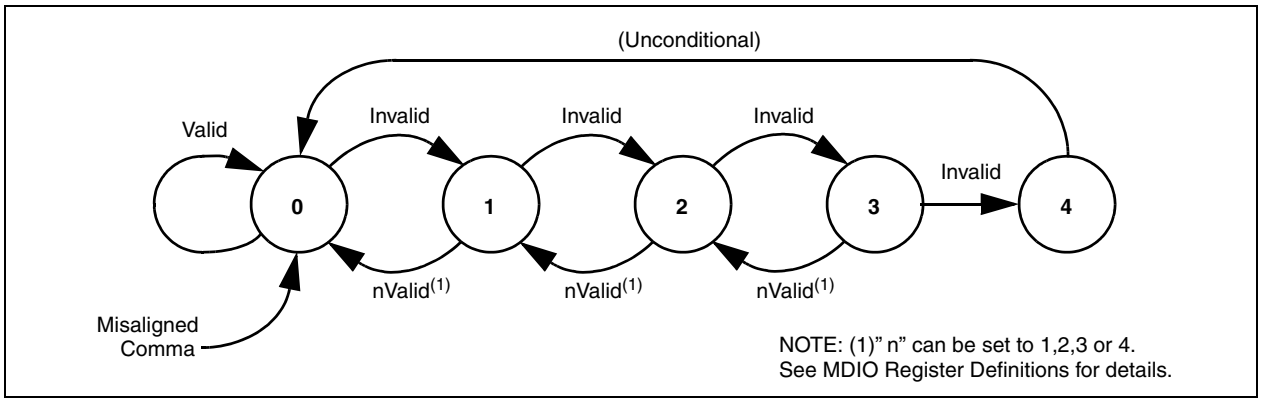


Figure 6. State Diagram of Invalid Transmission Counter

Link Status Outputs

On the receiver output bus, the ERRn, KCHn and IDLEn outputs indicate status for each channel as shown in Table 9. Because this status is encoded, multiple conditions could occur simultaneously so the states are prioritized as indicated (1 being highest priority). For example, if both out-of-band and disparity errors occur, only an out-of-band error is reported because it has higher priority.

The ERRn, KCHn and IDLEn status signals apply to the data on Rn[7:0] on a per-character basis. The only exception to this is the underrun/overrun indication, which is asserted coincident with the duplicated character when an underrun occurs, and is asserted following the deleted character (on the cycle where the deleted character should have appeared) when an overrun occurs.

Table 9. Receiver Status Signals

ERRn	KCHn	IDLEn	Priority	Link Status
0	0	0	7	**Valid Data Transmission:** A valid 10B data character with correct disparity was received. The correctly decoded version of this character is on Rn[7:0]**.**
0	0	1	1	**Underrun/Overrun Error**(1)**:** The elastic buffer has not been able to add/drop an IDLE when required. Data on Rn[7:0] is invalid.
0	1	0	6	**Kxx.x Special Character Detected (not IDLE):** A valid 10B special character with correct disparity was received. The correctly decoded version of this character, per Table 4 is on Rn[7:0]
0	1	1	5	**IDLE Detected:** A valid IDLE character(K28.5) with correct disparity was received. The correctly decoded version of this character, per Table 4, is on Rn[7:0].
1	0	0	3	**Out-of-Band Error Detected**(1): A character was received that was not a valid 10B data or control character. Data on Rn[7:0] is invalid.
1	0	1	4	**Disparity Error Detected**(1)**:** A valid 10B character was received that did not have the expected disparity. Rn[7:0] is invalid.
1	1	0	2	**Loss of Synchronization:** The receiver state machine is in the Loss-of-Sync state. Data on Rn[7:0] is invalid.
1	1	1	2	**RESYNC (**when using the LSSM of 5a**):** The receiver state machine is in the Re-Synchronization state. Data on **Rn[7:0]** is a decoded version of K28.1, K28.5 or K28.7. **Channel Re-alignment (**when using the LSSM of 5b**):** FIFO read pointer has been re-adjusted.

1. An internal 32-bit register is provided to serve as a counter for this type of error. Errors may be accumulated either in BIST mode or normal operating mode. Access to all counter registers is through the MDIO interface port. See "MDIO/MDC Serial Interface" on page 21 for definitions of all MDIO registers.

Loopback Operation

Loopback control pins, SLOOP and PLOOP, are provided to internally loopback serial and parallel data paths.

Table 10. Loopback Mode Selection

SLOOP	PLOOP	Loopback Mode
0	0	Normal operation
0	1	Internal parallel loopback
1	0	Internal serial loopback
1	1	Reserved

When SLOOP is HIGH and PLOOP is LOW, serial loopback mode is selected. The transmitter's serial transmit data is internally connected to the receiver's CRU input. The serial loopback paths are labeled LBTXn in the VSC7226 block diagram. This allows parallel data on Tn[7:0] to be encoded, serialized, looped back, deserialized and decoded. This mode is intended for the system to verify functionality of the local VSC7226 prior to attempting to establish an external serial link. The PTXn and RTXn outputs are unaffected by the state of PLOOP and SLOOP.

When SLOOP is LOW and PLOOP is HIGH, parallel loopback mode is selected. The Rn[7:0] outputs are looped back to the Tn[7:0] inputs, and the KCHn output is looped back to the C/Dn input (see Figure 7 on page 19). WSENn does not have a loopback source and is internally connected to a logic LOW. KCHAR does not have a loopback source when EDBYP is low and it is internally connected to a logic HIGH; when EDBYP is high, KCHAR is not

connected high. Connecting KCHn to C/Dn and setting KCHAR HIGH means that the character to be retransmitted will depend not only on the received character, but also on the state of the LSSM. The specific K-character received will be transmitted when the receiver is in the RESYNC or SYNC_ACQUIRED states. When in the LOSS_OF_SYNC state, however, the transmitted character must be considered undefined since Rn[7:0] does not necessarily specify a valid K-character as defined in Table 4 on page 6.

The PLOOP and SLOOP pins provide global loopback control. All four channels are affected simultaneously by these control pins. When PLOOP and SLOOP are set LOW, parallel and serial loopback control on a per-channel basis is possible. The MDIO interface may, then be used to access registers controlling the loopback mode of each individual channel (see "MDIO/MDC Serial Interface" on page 21 for MDIO register definitions).

In parallel loopback mode the receiver could use either REFCLK or recovered clock as the word clock and the RMODE[1:0] could be set independently to the clock selected. The user must set the RMODE2 pin, or DDR or data eye timing. This data is looped back to the transmitter with TBC being equivalent to RBC. This internal loopback configuration also allows rate matching to be performed in the receivers' elastic buffers. Rate matching is controlled and operates exactly the same way that it does in normal mode. This is needed to avoid receiver overrun/underrun errors in the loopback device if the remote transmitting device's REFCLK is not frequency-locked. PLOOP, SLOOP, RRXSEL, PTXEN, RTXEN and BIST inputs must all be configured appropriately in order for end-to-end parallel loopback to function correctly in a user environment. Parallel loopback mode is internally disabled when BIST mode is enabled.

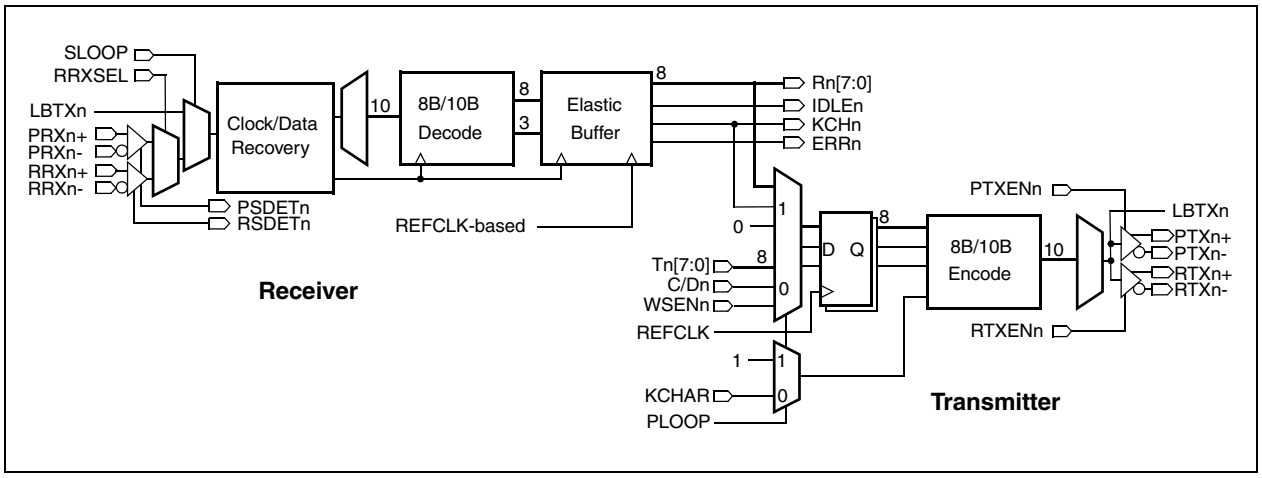


Figure 7. Parallel Loopback Mode Operation

Built-In Self Test Operation

Built-In Self Test operation is enabled when the BIST input is HIGH, which causes TMODE[2:0] to be internally set to 000. Upon entering BIST mode, each transmitter will issue a word sync sequence in order to re-center the elasticity buffers in the receive channel. Each transmitter then repeatedly sends a simple 256-byte incrementing data pattern (prior to 8B/10B encoding) followed by three IDLE characters (K28.5). Note that this incrementing pattern plus three IDLEs will cause both disparities of each data character and the IDLE character to be transmitted, and contains a sufficient IDLE density for any application requiring IDLE insertion/deletion. It is up to the user to enable IDLE insertion/deletion if the receiver's word clock is not frequency-locked to the transmitter's REFCLK.

Each receiver monitors incoming data for this pattern and indicates if any errors are detected. Correct reception of the pattern is reported on each receiver's STERRn output; a LOW means the pattern is being received correctly and a HIGH means that errors are detected. When BIST transitions from LOW to HIGH, each STERRn output is initialized HIGH. It will be cleared LOW whenever one or more IDLE characters followed by all 256 data characters are sequentially received without error, and set HIGH whenever a pattern mismatch is encountered. Since each channel functions independently, no attempt is made to word-align the receive channels. Received data and associated status will be output as in normal operation. Please note that serial loopback mode and receiver output timing mode selection via RMODE[2:0] operate independently of BIST mode, but BIST mode disables parallel loopback mode.

When BIST is HIGH, all four channels are placed in BIST mode, and control of individual channels through the MDIO interface is not possible. When BIST is set LOW, individual channel control is possible (see"MDIO/MDC Serial Interface" on page 21 for a description of the MDIO registers.)

BIST Monitoring

Two 32-bit counters are provided internal to the VSC7226 which allow the accumulation of BIST cycles and BIST errors. Depending on the status of SLOOP, the VSC7226 transceiver or a complete data link may be monitored for BIST performance. In addition, 32-bit registers are allocated for counting 8B/10B coding violations, disparity errors and FIFO overflow/underflow conditions (see "MDIO/MDC Serial Interface" on page 21 for a description of the MDIO registers).

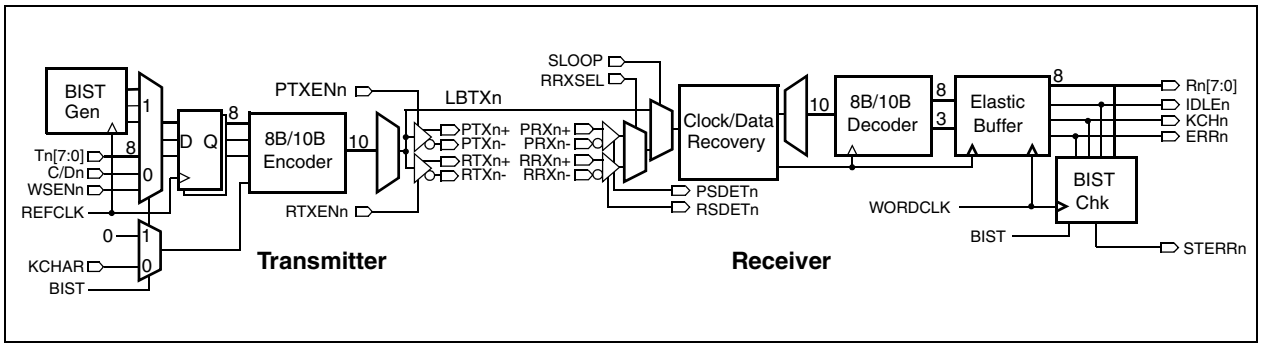


Figure 8. BIST Mode Operation

External Capacitors

The on-chip PLL uses a single external 0.1µF capacitor (connected between CAP0 and CAP1) to control the loop filter. This capacitor should be a multilayer ceramic dielectric, or better, with at least a 5V working voltage rating and a good temperature coefficient (NPO is preferred but X7R may be acceptable). These capacitors are used to minimize the impact of common-mode noise on the Clock Multiplier Unit (CMU), especially power supply noise. Higher value capacitors provide better robustness in systems. NPO is preferred over an X7R capacitor since the power supply noise sensitivity will vary with temperature. For best noise immunity, the designer may use a three-capacitor circuit with one differential capacitor between CAP0 and CAP1(C1), a capacitor from CAP0 to ground (C2), and a capacitor from CAP1 to ground (C3). Larger values are better but 0.1µF is adequate. However, if the designer cannot use a three-capacitor circuit, a single differential capacitor (C1) is adequate. These components should be isolated from noisy traces.

The VSC7226 contains an internal voltage regulator used to obtain a 1.8V supply. The output of this regulator is accessible from either of two pins labeled VDD18. A capacitance of 4.7 µF or greater is required to be connected from one of these leads to digital ground (VSSD).

MDIO/MDC Serial Interface

The VSC7226 provides a IEEE-802.3u MDIO/MDC serial interface to allow enhanced register-based management of the control and status resources of the VSC7226. Normal operation of the VSC7226 is possible without the use of the MDIO/MDC serial interface since all essential control and status signals for operation are accessible through the device pins. However, some additional features are accessible only through the MDIO/MDC serial interface. Features such as add/drop enable, primary/redundant serial port select, transmit signal pre-emphasis and loopback modes, can all be controlled on a per-channel basis via the MDIO/MDC serial interface.

The MDIO/MDC serial interface consists of two pins, Management Data Input/Output (MDIO) and Management Data Clock (MDC). MDC has a maximum clock rate of 2.5MHz and no minimum rate. The MDIO line is bi-directional and may be shared by up to 32 devices. The MDIO/MDC serial frame format is shown in Table 11.

Table 11. MDIO/MDC Serial Frame Format

	Start	Op Code	Device Addr	Register Addr	Turnaround	Register Data	Idle
Read	01	10	AAAAA	AAAAA	Z00	D[15:0]	Z
Write	01	01	AAAAA	AAAAA	10	D[15:0]	Z

The MDIO pin requires a pull-up resistor (1.5kΩ) which, during IDLE and turnaround, will pull MDIO HIGH. In order to initialize the MDIO interface, the Station Management Entity (SME) sends 32 consecutive logic 1s on MDIO to provide the VSC7226 with a sequence that can be used to establish synchronization. This preamble may be generated either by driving MDIO HIGH for 32 consecutive MDC clock cycles or by simply allowing the MDIO pull-up resistor to pull MDIO HIGH during which time 32 MDC clock cycles are provided. In addition, 32 MDC clock cycles should be used if an invalid start, op code or turnaround bit is detected.

The VSC7226 waits until it has received this preamble sequence before responding to any other transaction. Once the VSC7226 MDIO/MDC serial interface has been initialized with this preamble, no further preamble is required until after a power-on/reset has occurred.

The start code is indicated by a <01> pattern which assures the MDIO line transitions from the default idle line state. Turnaround (TA) is an idle bit time inserted between the register address field and the data field. To avoid contention, no device actively drives the MDIO signal during the first bit of TA during read transactions. Depending on the path delay between the MDC and MDIO, the TA could be captured as Z0 or Z00. When MDIO bus shows more delay, it will be viewed as Z00 and followed by the required data. Figures 9, 10, and 11 show the timing relationship between MDC and MDIO as driven/received by the SME and the VSC7226 for a typical register read access. For both the device address and register address, the first address bit transmitted is the most significant bit (MSB) of the address field.

In order to make the MDIO Read Operation compatible to IEEE, another option is provided to have the TA (turnaround) be captured as Z0 only. To provide sufficient setup and hold time, instead of rising edge, the falling edge of the MDC is used to clock out the data from VSC7226. To maintain backward compatibility, a RESERVED pin (15B) is now called MRS (MDIO READ SELECT) and setting it HIGH will be backward compatible to previous versions of the VSC7226. To make it IEEE compatible, TA=Z0, this pin MRS, should be pulled LOW.

There are a number of 32-bit counters which span two 16-bit registers. When reading the contents of such a counter, the register with the lower number must be read first, followed immediately by a read transaction on the higher numbered register, with no other transactions between.

For write transactions, the SME writes data to an addressed VSC7226 eliminating the requirement for MDIO turnaround. The TA time is filled by the SME inserting <10> for these two bits. Figures 9, 10, and 11 show the timing relationship for a typical MDIO/MDC serial interface register write access.

The VSC7226 MDIO/MDC serial interface supports a preamble suppression mode which eliminates the need to generate a preamble for each read or write transaction. The 32 bits of preamble are only required following a power-on/hardware reset condition. A minimum of one idle bit between a read or write transaction is required as specified by IEEE 802.3u.

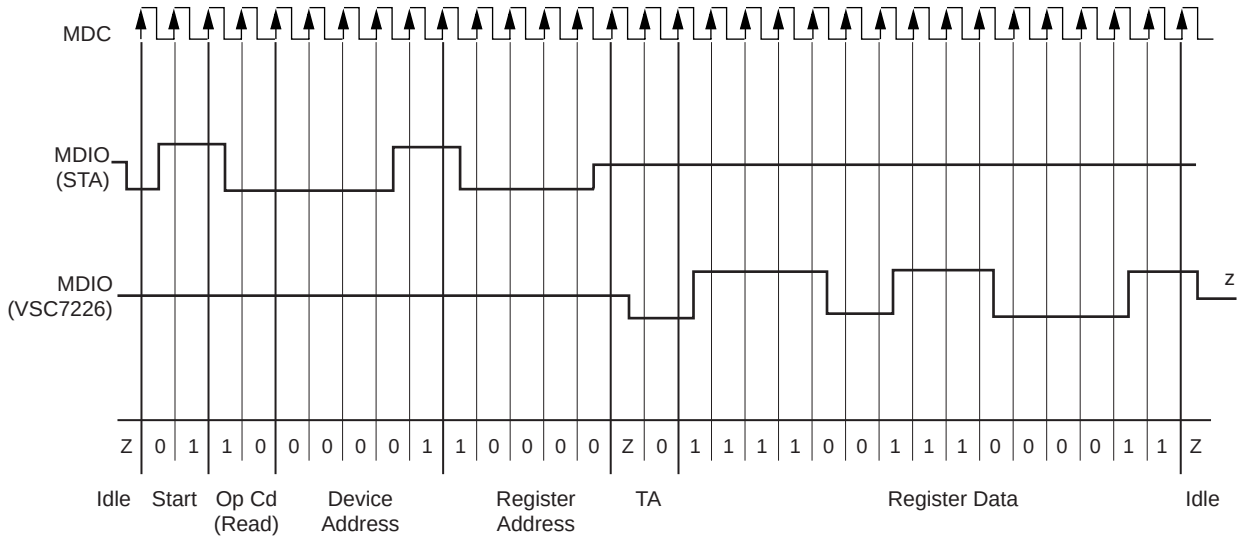


Figure 9. MDIO/MDC Read Operation with MRS=0, TA=Z0

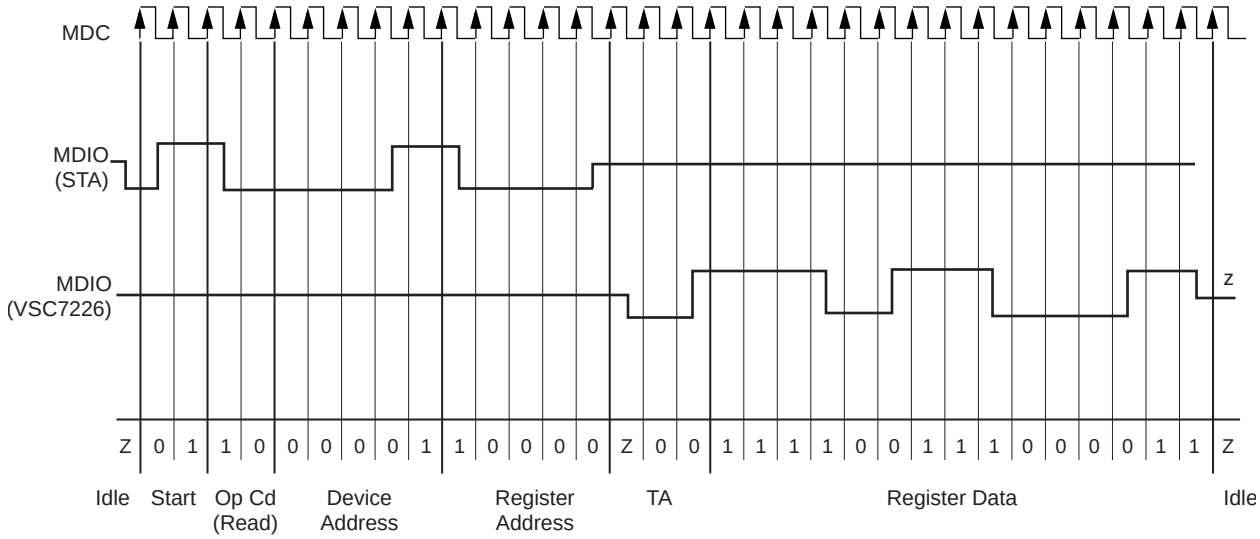


Figure 10. MIDO/MDC Read Operation with MRS=1, TA=Z00

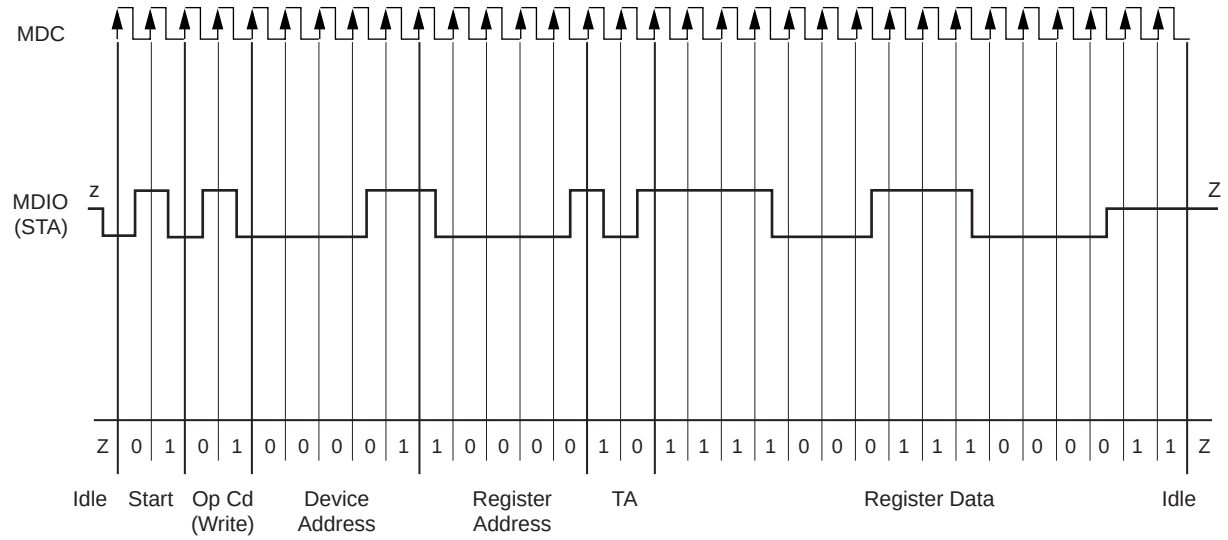


Figure 11. MDIO/MDC Write Operation

REGISTER DEFINITIONS

There are sixteen register blocks each consisting of sixteen 16-bit registers available via the VSC7226 MDIO/MDC serial interface. By writing a 4-bit value to the register block index register, any of the sixteen register blocks can be selected for read or write access. Presently, the VSC7226 uses only the first five register blocks with the remaining eleven register blocks undefined. The register block index register is always located at register address 31, independent of the currently selected register block. The register maps for the five defined register blocks are shown in Table 12.

Table 12. VSC7226 MDIO/MDC Register Map

Register Address	Register Block 0 (Block Index = 0)	Register Block 1 (Block Index = 1)	Register Block 2 (Block Index = 2)	Register Block 3 (Block Index = 3)	Register Block 4 (Block Index = 4)
16	Device ID	Channel A BIST Cycle Counter	Channel B BIST Cycle Counter	Channel C BIST Cycle Counter	Channel D BIST Cycle Counter
17	Device ID	Channel A BIST Cycle Counter	Channel B BIST Cycle Counter	Channel C BIST Cycle Counter	Channel D BIST Cycle Counter
18	Global Config	Channel A BIST Error Counter	Channel B BIST Error Counter	Channel C BIST Error Counter	Channel D BIST Error Counter
19	Global Config	Channel A BIST Error Counter	Channel B BIST Error Counter	Channel C BIST Error Counter	Channel D BIST Error Counter
20	Loopback and BIST Control	Channel A Rx 8B/10B Error Counter	Channel B Rx 8B/10B Error Counter	Channel C Rx 8B/10B Error Counter	Channel D Rx 8B/10B Error Counter
21	Redundant I/O Control	Channel A Rx 8B/10B Error Counter	Channel B Rx 8B/10B Error Counter	Channel C Rx 8B/10B Error Counter	Channel D Rx 8B/10B Error Counter
22	Tx/Rx Rate and Rate Matching Control	Channel A Rx Disparity Error Counter	Channel B Rx Disparity Error Counter	Channel C Rx Disparity Error Counter	Channel D Rx Disparity Error Counter
23	8B/10B and Out-of-Band Character Control	Channel A Rx Disparity Error Counter	Channel B Rx Disparity Error Counter	Channel C Rx Disparity Error Counter	Channel D Rx Disparity Error Counter
24	LOS Comma Detect and Invalid/Valid Counter Disparity	Channel A Rx FIFO Error Counter	Channel B Rx FIFO Error Counter	Channel C Rx FIFO Error Counter	Channel D Rx FIFO Error Counter
25	Alternate LSSM and Counter Code Block Size	Channel A Rx FIFO Error Counter	Channel B Rx FIFO Error Counter	Channel C Rx FIFO Error Counter	Channel D Rx FIFO Error Counter
26	Tx Pre-Emphasis Control	Reserved	Reserved	Reserved	Reserved
27	RBC Control/Signal Detect Status	Reserved	Reserved	Reserved	Reserved
28	Rx Squelch Control/ PECL Output Power	Reserved	Reserved	Reserved	Reserved
29	Add/Drop Character Definition	Reserved	Reserved	Reserved	Reserved
30	Word Sync Character Definition	Channel A Counter Control	Channel B Counter Control	Channel C Counter Control	Channel D Counter Control
31	Register Block Index	Register Block Index	Register Block Index	Register Block Index	Register Block Index

Upon power-on/hardware reset, the register block index register is loaded with 0. Consequently, any accesses to the VSC7226 MDIO/MDC serial interface will access register block 0 until the register block index register is modified to a value other than 0. A decription of the individual registers located within a register block and associated control/status bits within those registers is listed in Table 13 and Table 14. When the bits of the read registers are not defined, the values of these bits could be read back as 0 or 1, and should not bear any meaning to the user. For those bits that are undefined in write registers, the user should assign them to 1.

Table 13. Register Block 0

Register Address	Register Type	Access	Description
16	Device ID	Read Only	Lower 16 bits of a 32-bit device ID
17	Device ID	Read Only	Upper 16 bits of a 32-bit device ID
18	Global Config	Read Only	Status of VSC7226 mode pins
19	Global Config	Read Only	Status of VSC7226 mode pins
20	Loopback and BIST Control	R/W	Per channel parallel and serial loopback and BIST enables Possible with PLOOP = LOW, SLOOP = LOW, BIST = LOW
21	Redundant I/O Control	R/W	Per channel Tx and Rx redundant I/O control Possible with PTXEN = HIGH, RTXEN = HIGH, RRXSEL = HIGH
22	Tx/Rx Rate and Rate Matching Control	R/W	Per channel Tx and Rx half-rate speed enables and rate matching enable Possible with RATE = HIGH, ADEN = HIGH
23	8B/10B and Out-of-Band Character Control Comma Alignment Control	R/W	Per channel Tx and Rx 8B/10B encoder bypass enables and global control of out-of-band character outputs Possible with EDBYP = LOW Enable comma alignment with selectable rising or falling edge of RBC
24	LOS Comma Detect and Valid/Invalid Counter Disparity	R/W	Per channel enable of comma detect in LOS state only, and valid/invalid
25	Alternate LSSM and Code Block Size for Valid/Invalid Counter	R/W	Per channel enable of alternate LSSM, and specification of code block size for valid/invalid transmission counter
26	Tx Pre-Emphasis Control	R/W	Per channel Tx pre-emphasis control Possible with TXEMP = LOW
27	RBC Control/Signal Detect Status	R/W	Per channel recovered byte clock control and PSDET/RSDET status reporting Possible with RBCREF = LOW
28	Rx Squelch Control and PECL Output Power	R/W	Per channel receiver output squelching control and per channel PECL output power control Possible with REDSW = HIGH
29	Add/Drop Character Definition	R/W	Defines an alternate K-character for add/drop rate matching
30	Word Sync Character Definition	R/W	Defines an alternate K-character for word synchronization
31	Register Block Index	R/W	4-bit register block index

Table 14. Register Blocks 1-4

Register Address	Register Type	Access	Description
16	BIST Cycle Counter	R/W	Lower 16 bits of a 32-bit BIST cycle counter
17	BIST Cycle Counter	R/W	Upper 16 bits of a 32-bit BIST cycle counter
18	BIST Error Counter	R/W	Lower 16 bits of a 32-bit BIST error counter
19	BIST Error Counter	R/W	Upper 16 bits of a 32-bit BIST error counter
20	Rx 8B/10B Error Counter	R/W	Lower 16 bits of a 32-bit Rx 8B/10B coding error counter
21	Rx 8B/10B Error Counter	R/W	Upper 16 bits of a 32-bit Rx 8B/10B coding error counter
22	Rx Disparity Error Counter	R/W	Lower 16 bits of a 32-bit Rx 8B/10B disparity error counter
23	Rx Disparity Error Counter	R/W	Upper 16 bits of a 32-bit Rx 8B/10B disparity error counter
24	Rx FIFO Error Counter	R/W	Lower 16 bits of a 32-bit Rx FIFO under/over error counter
25	Rx FIFO Error Counter	R/W	Upper 16 bits of a 32-bit Rx FIFO under/over error counter
26	Reserved	N/A	Reserved for future use
27	Reserved	N/A	Reserved for future use
28	Reserved	N/A	Reserved for future use
29	Reserved	N/A	Reserved for future use
30	Counter Control	R/W	Control for stopping and starting counters
31	Register Block Index	R/W	4-bit register block index

Register Blocks 1 through 4 contain counters used to tally various error conditions during normal operation as well as during BIST operation. Register blocks 1 through 4 are identical in makeup with register block 1 being associated with channel A, register block 2 associated with channel B, register block 3 associated with channel C, and register block 4 associated with channel D of the VSC7226.

Table 15. Device ID (Register Block 0, Register Address 16)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
At Reset	0	1	*	*	0	0	0	1	1	1	1	0	1	0	0	1
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

NOTE: *Bits 13:12 are 01 for VSC7226-01 and VSC7226-05; bit 10 for the VSC7226-02 and VSC7226-06.*

This is a read-only register that contains the lower 16 bits of a 32-bit device ID code that is formatted per the JTAG (IEEE 1149.1) standard. This register reads $51E9 for VSC7226-01 and VSC7226-05 versions or $61E9 for VSC7226-02 and VSC7226-06 versions.

Bit 0: 1

Bits 11:1 Manufacturer's ID (0x0F4)

Bits 15:12 Lower nibble of four-nibble device ID. 0x5 for VSC7226-01 and VSC7226-05, and 0x6 for VSC7226-02 and VSC7226-06.

Table 16. Device ID (Register Block 0, Register Address 17)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
At Reset	0	0	1	1	0	0	0	0	1	0	0	0	1	1	0	1
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

This is a read-only register that contains the upper 16 bits of a 32-bit device ID code which is formatted per the JTAG (IEEE 1149.1) standard. This register reads $308D.

Bits 11:0 Upper three nibbles of four nibble device ID (0x08D)
Bits 15:12 Version number of device

Table 17. Global Config (Register Block 0, Register Address 18)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
At Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

This is a read-only register that shows the logic levels that are applied to the various global configuration mode pins on the VSC7226. A high logic level on a global configuration mode pin will be shown as a 1 in the corresponding bit field and a low logic level will be shown as a 0 in the corresponding bit field.

Bit 0 RATE configuration mode pin
Bits 3:1 TMODE[2:0] configuration mode pins
Bits 6:4 RMODE[2:0] configuration mode pins
Bits 8:7 REFMUL[1:0] configuration mode pins
Bit 9 PTXEN configuration mode pin
Bit 10 RTXEN configuration mode pin
Bit 11 RRXSEL configuration mode pin
Bit 12 EDBYP configuration mode pin
Bit 13 PLOOP configuration mode pin
Bit 14 SLOOP configuration mode pin
Bit 15 BIST configuration mode pin

Table 18. Global Config (Register Block 0, Register Address 19)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
At Reset	—	—	—	—	—	—	—	—	—	—	—	—	—	X	X	X
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

This register is a read-only register that shows the logic levels that are applied to the various global configuration mode pins on the VSC7226. A high logic level on a global configuration mode pin will be shown as a 1 in the corresponding bit field and a low logic level will be shown as a 0 in the corresponding bit field.

Bit 0 TXEMP configuration mode pin
Bit 1 RBCREF configuration mode pin
Bit 2 REDSW configuration mode pin
Bits 15:2 Undefined (reserved for future use)

Table 19. Loopback and BIST Control (Register Block 0, Register Address 20)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
At Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7:0 of this read/write register allow enabling of both serial and parallel loopback modes on a per channel basis when the corresponding external configuration pin is set LOW. If the PLOOP and/or SLOOP global configuration mode pins are set HIGH, the ability to enable parallel and/or serial loopback on a per channel basis is not possible.

Bits 15:8 of this register enable the BIST pattern generator on the transmit links and pattern detector on the receive links on a per channel basis when the BIST global mode pin is set LOW. If the BIST global configuration mode pin is set HIGH, the ability to enable the BIST pattern generator and pattern detector on a per channel basis is not possible.

Bit 0 Set HIGH to enable parallel loopback on channel A
Bit 1 Set HIGH to enable parallel loopback on channel B
Bit 2 Set HIGH to enable parallel loopback on channel C
Bit 3 Set HIGH to enable parallel loopback on channel D
Bit 4 Set HIGH to enable serial loopback on channel A
Bit 5 Set HIGH to enable serial loopback on channel B
Bit 6 Set HIGH to enable serial loopback on channel C
Bit 7 Set HIGH to enable serial loopback on channel D
Bit 8 Set HIGH to enable the BIST pattern generator on the transmit link of channel A
Bit 9 Set HIGH to enable the BIST pattern generator on the transmit link of channel B
Bit 10 Set HIGH to enable the BIST pattern generator on the transmit link of channel C
Bit 11 Set HIGH to enable the BIST pattern generator on the transmit link of channel D
Bit 12 Set HIGH to enable the BIST pattern detector on the receive link of channel A
Bit 13 Set HIGH to enable the BIST pattern detector on the receive link of channel B
Bit 14 Set HIGH to enable the BIST pattern detector on the receive link of channel C
Bit 15 Set HIGH to enable the BIST pattern detector on the receive link of channel D

Table 20. Redundant I/O Control (Register Block 0, Register Address 21)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
At Reset	—	—	—	—	1	1	1	1	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This register is a read/write register which allows disabling of the primary and redundant transmit output buffers on a per channel basis. If the PTXEN and/or RTXEN global configuration mode pins are set LOW, the ability to control the primary and redundant transmit output buffers on a per channel basis is not possible. In addition, this register allows the selection of the primary/redundant receive input source on a per channel basis if the RRXSEL global configuration mode pin is set HIGH. The ability to select the primary/redundant receive input source on a per channel basis is not possible if the RRXSEL global configuration mode pin is set LOW.

Bit 0 Set LOW to disable the primary transmit output buffer on channel A
Bit 1 Set LOW to disable the primary transmit output buffer on channel B
Bit 2 Set LOW to disable the primary transmit output buffer on channel C
Bit 3 Set LOW to disable the primary transmit output buffer on channel D
Bit 4 Set LOW to disable the redundant transmit output buffer on channel A
Bit 5 Set LOW to disable the redundant transmit output buffer on channel B
Bit 6 Set LOW to disable the redundant transmit output buffer on channel C
Bit 7 Set LOW to disable the redundant transmit output buffer on channel D
Bit 8 Set LOW to enable the primary receive input source on channel A
Bit 9 Set LOW to enable the primary receive input source on channel B
Bit 10 Set LOW to enable the primary receive input source on channel C
Bit 11 Set LOW to enable the primary receive input source on channel D
Bits 15:12 Undefined (reserved for future use)

Table 21. Tx/Rx Rate Control and Rate Matching (Register Block 0, Register Address 22)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
At Reset	—	—	—	—	1	1	1	1	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 0:7 of this read/write register enables independent half-rate operation on the transmit and receive links on a per channel basis when the RATE configuration mode pin is HIGH. If the RATE global configuration mode pin is set LOW, the ability to set half-rate operation on a per channel basis is not possible. With RATE = 1, this register can set the operating speed from full-rate to half-rate, without any change for the REFMUL(1,0) and clock frequency of REFCLK.

Bits 11:8 of this register enables rate matching via the IDLE insertion/deletion logic on the receive links on a per channel basis when the ADEN configuration mode pin is HIGH. If the ADEN global configuration mode pin is set LOW, the ability to enable IDLE insertion/deletion on a per channel basis is not possible.

Bit 0 Set LOW to enable half-rate operation on transmit link of channel A
Bit 1 Set LOW to enable half-rate operation on transmit link of channel B
Bit 2 Set LOW to enable half-rate operation on transmit link of channel C
Bit 3 Set LOW to enable half-rate operation on transmit link of channel D

Bit 4	Set LOW to enable half-rate operation on receive link of channel A
Bit 5	Set LOW to enable half-rate operation on receive link of channel B
Bit 6	Set LOW to enable half-rate operation on receive link of channel C
Bit 7	Set LOW to enable half-rate operation on receive link of channel D
Bit 8	Set LOW to enable IDLE insertion/deletion on the receive link of channel A
Bit 9	Set LOW to enable IDLE insertion/deletion on the receive link of channel B
Bit 10	Set LOW to enable IDLE insertion/deletion on the receive link of channel C
Bit 11	Set LOW to enable IDLE insertion/deletion on the receive link of channel D
Bits 15:12	Undefined (reserved for future use)

Table 22. 8B/10B Control, Undefined Encoding Control, Comma Alignment (Register Block 0, Register Address 23)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
At Reset	—	—	—	—	—	—	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7:0 of this read/write register independently bypass the 8B/10B encoding/decoding logic in the transmitter/receiver on a per channel basis when EDBYP is LOW. If the EDBYP global configuration mode pin is set HIGH, the ability to disable or bypass 8B/10B encoding/decoding on a per channel basis is not possible.

Bit 8 can be used to force K30.7 at the serial output of the transmitter when an undefined 8-bit character is present at its input. This mode applies when the 8B/10B encoder is not bypassed and WSENn, C/Dn and KCHAR are set to 0, 1, 1. When HIGH, K30.7 is output. When LOW, 001111 0001 (RD-), or 110000 1110 (RD+) is output.

Bit 9 can be used to force K30.7 at the parallel output of the receiver when an undefined 10-bit character is present at its input. This mode applies when the 8B/10B decoder is not bypassed. When HIGH, K30.7 is output. When LOW, the output is unknown.

Bit 10 is used to enable the comma alignment to one of the clock edges of the RBC. Bits 14:11 are used to define which clock edge of the RBC is used for the Comma Alignment. Setting bits 14:11 LOW aligns the falling edge of RBCn to commas in the corresponding channel n parallel output when it is enabled. Setting bits 14:11 to HIGH aligns the rising edge of the RBC to commas in the corresponding channel n parallel output when it is enabled. If bit 10 is set LOW, bit 14:11 has no effect on comma alignment.

Bit 0	Set HIGH to bypass 8B/10B encoding of data on transmit link of channel A
Bit 1	Set HIGH to bypass 8B/10B encoding of data on transmit link of channel B
Bit 2	Set HIGH to bypass 8B/10B encoding of data on transmit link of channel C
Bit 3	Set HIGH to bypass 8B/10B encoding of data on transmit link of channel D
Bit 4	Set HIGH to bypass 8B/10B decoding of data on receive link of channel A
Bit 5	Set HIGH to bypass 8B/10B decoding of data on receive link of channel B
Bit 6	Set HIGH to bypass 8B/10B decoding of data on receive link of channel C
Bit 7	Set HIGH to bypass 8B/10B decoding of data on receive link of channel D
Bit 8	Set HIGH to force K30.7 as the serial transmitter output for out-of-band input
Bit 9	Set HIGH to force K30.7 as the parallel receiver output for out-of-band input
Bit 10	Set HIGH to enable comma alignment to the desired clock edge of the RBC

Bit 11	Set HIGH to force comma alignment to use rising edge of channel A; set LOW to use falling edge
Bit 12	Set HIGH to force comma alignment to use rising edge of channel B; set LOW to use falling edge
Bit 13	Set HIGH to force comma alignment to use rising edge of channel C; set LOW to use falling edge
Bit 14	Set HIGH to force comma alignment to use rising edge of channel D; set LOW to use falling edge
Bits 15	Undefined (reserved for future use)

Table 23. Comma Detection & Valid Transmission Control (Register Block 0, Register Address 24)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
At Reset	—	—	—	—	0	0	0	0	0	0	0	0	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 3:0 of this read/write register can be used to always enable comma detection on a per channel basis with ENDEC on. The default (at RESET) operating mode of the VSC7226 is such that commas are detected only when in the LOS state, which will prevent single bit errors producing false comma's from adjusting the framing boundary while in the SYNC_ ACQUIRED state. When bits 3:0 are set LOW, comma detection is always enabled.

Bits 11:4 of this register control the number of valid transmissions required to progress toward state 0 in the invalid transmission counter of Figure 6,"State Diagram of Invalid Transmission Counter" on page 17. Each channel may be controlled individually with 2 bits assigned to each channel. The bit settings and corresponding valid transmission requirements are as follows:

00	One valid transmission is required to move one step
01	Two valid transmissions are required to move one step
10	Three valid transmissions are required to move one step
11	Four valid transmissions are required to move one step

Bit 0	Set LOW to enable comma detection always for channel A
Bit 1	Set LOW to enable comma detection always for channel B
Bit 2	Set LOW to enable comma detection always for channel C
Bit 3	Set LOW to enable comma detection always for channel D
Bits 5:4	Control valid transmission requirement for channel D
Bits 7:6	Control valid transmission requirement for channel C
Bits 9:8	Control valid transmission requirement for channel B
Bits 11:10	Control valid transmission requirement for channel A
Bits 15:12	Undefined (reserved for future use)

Table 24. LOS State Machine and Code Block Size Control (Register Block 0, Register Address 25)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
At Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 3:0 of this read/write register are used to select one of two possible LOS State Machines shown in Figure 5,"State Diagrams of Loss of Synchronization State Machine" on page 17. One bit is used for control of each channel. When set LOW, the state machine of 5a is selected and when HIGH, that of 5b is selected.

Bits 15:4 are used to define the byte size of code blocks. Code blocks are used in the counting of valid/invalid transmissions (see "Receiver State Machine" on page 16.) When the code block size is set to n bytes, data will be examined in n-byte blocks for valid/invalid transmissions. One or more invalid characters within a code block will cause the invalid transmission counter to increment by one. Control is provided on a per channel basis with 3 bits assigned to each channel. The correspondence between these bit settings and the number of bytes making up a code block is:

000 1 byte per code block
001 2 bytes per code block
010 3 bytes per code block
011 4 bytes per code block
100 5 bytes per code block
101 6 bytes per code block
110 7 bytes per code block
111 8 bytes per code block

Bit 0 Set HIGH to select the LOS state machine of 5b for channel A
Bit 1 Set HIGH to select the LOS state machine of 5b for channel B
Bit 2 Set HIGH to select the LOS state machine of 5b for channel C
Bit 3 Set HIGH to select the LOS state machine of 5b for channel D
Bits 6:4 Use to control code block size for channel D
Bits 9:7 Use to control code block size for channel C
Bits 12:10 Use to control code block size for channel B
Bits 15:13 Use to control code block size for channel A

Table 25. Tx Pre-Emphasis Control (Register Block 0, Register Address 26)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
At Reset	—	-—	—	-—	—	-—	—	-—	—	-—	—	-—	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This register is a read/write register which enables signal pre-emphasis on a per-channel basis when the TXEMP configuration mode pin is set LOW. If the TXEMP global configuration mode pin is set HIGH, the ability to enable transmit signal pre-emphasis on a per channel basis is not possible.

Bit 0 Set HIGH to enable transmitter signal pre-emphasis on the transmit link of channel A
Bit 1 Set HIGH to enable transmitter signal pre-emphasis on the transmit link of channel B
Bit 2 Set HIGH to enable transmitter signal pre-emphasis on the transmit link of channel C
Bit 3 Set HIGH to enable transmitter signal pre-emphasis on the transmit link of channel D
Bits 15:4 Undefined (reserved for future use)

Table 26. Recovered Byte Clock Control and Signal Detect Output (Register Block 0, Register Address 27)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
At Reset	—	-—	—	—	X	X	X	X	X	X	X	X	0	0	0	0
Access	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bits 3:0 of this register are read/write and are used to select receiver output timing referenced to REFCLK on a per channel basis. The external pin labeled RBCREF provides global control of this timing mode. When RBCREF is LOW, these bits can be used to select REFCLK based output timing. When HIGH, per channel control is not possible.

Bits 11:4 of this register are read only bits and report the status of the external pins PSDET and RSDET for each channel. When PSDET or RSDET are HIGH (LOW), the corresponding bit is asserted HIGH (LOW).

Bit 0 Set HIGH to enable REFCLK based receiver output timing on channel A
Bit 1 Set HIGH to enable REFCLK based receiver output timing on channel B
Bit 2 Set HIGH to enable REFCLK based receiver output timing on channel C
Bit 3 Set HIGH to enable REFCLK based receiver output timing on channel D
Bit 4 Reports the status of RSDET for channel D
Bit 5 Reports the status of PSDET for channel D
Bit 6 Reports the status of RSDET for channel C
Bit 7 Reports the status of PSDET for channel C
Bit 8 Reports the status of RSDET for channel B
Bit 9 Reports the status of PSDET for channel B
Bit 10 Reports the status of RSDET for channel A
Bit 11 Reports the status of PSDET for channel A
Bits 15:4 Undefined (reserved for future use)

Table 27. Rx Output Squelch and PECL Output Power Control (Register Block 0, Register Address 28)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
At Reset	—	—	—	—	—	—	—	—	1	1	1	1	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This is a read/write register and is used to select receiver output squelching on a per channel basis and to exercise per channel control of the transmitter high-speed PECL output half-swing capability. Bits 3:0 are for the output squelch feature and bits 7:4 are for the half-swing feature.

When squelching is enabled, the selected channel's parallel outputs will be driven HIGH when the detected signal voltage is less than the signal detect threshold on PSDETn or RSDETn, whichever is in use for that channel. There is no external pin providing global control of this function. Control is only provided through the settings of these register bits.

When half-swing is enabled, the selected channel's serial transmitter output swing will be reduced by one-half. The external pin labeled REDSW implements this function on a global basis. When REDSW is HIGH, all four channels operate in the reduced output power mode. Bits 3:0 may be used to enable full output swing on a per channel basis. When REDSW is LOW, full swing operation is selected on all channels and individual channel control is not possible. The default condition is full output swing operation on all channels.

Bit 0 Set HIGH to enable receiver output squelching on channel A
Bit 1 Set HIGH to enable receiver output squelching on channel B
Bit 2 Set HIGH to enable receiver output squelching on channel C
Bit 3 Set HIGH to enable receiver output squelching on channel D
Bit 4 Set LOW to enable full swing output on channel A
Bit 5 Set LOW to enable full swing output on channel B
Bit 6 Set LOW to enable full swing output on channel C
Bit 7 Set LOW to enable full swing output on channel D
Bits 15:8 Undefined (reserved for future use)

Table 28. Add/Drop Character Definition (Register Block 0, Register Address 29)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
At Reset	—	—	—	—	—	—	—	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This is a read/write register which is used to assign an alternate 8-bit pattern as the add/drop character for rate matching. Normally, the K28.5 IDLE character is used for this purpose. Rate matching may be necessary when the received data's recovered clock does not match the clock used to time the parallel data out of the receiver, potentially resulting in FIFO overrun or underrun. The ADEN pin enables the receiver add/drop logic, causing the insertion/deletion of add/drop characters. Bit 8 of this register, when set HIGH, allows the use of an alternate K-character for this purpose. Bits 0 through 7 are used to define the K-character used. The alternate K-character must be chosen from the list given in Table 4 on page 6, with the exception that K28.7 should not be used.

Bit 0 Defines bit 0 of the alternate special K-character for add/drop
Bit 1 Defines bit 1 of the alternate special K-character for add/drop
Bit 2 Defines bit 2 of the alternate special K-character for add/drop
Bit 3 Defines bit 3 of the alternate special K-character for add/drop
Bit 4 Defines bit 4 of the alternate special K-character for add/drop
Bit 5 Defines bit 5 of the alternate special K-character for add/drop
Bit 6 Defines bit 6 of the alternate special K-character for add/drop
Bit 7 Defines bit 7 of the alternate special K-character for add/drop
Bit 8 Set HIGH to enable use of an alternate definition of the add/drop character
Bits 15:9 Undefined (reserved for future use)

Table 29. Word Synchronization Pattern Definition (Register Block 0, Register Address 30)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
At Reset	—	—	—	—	—	—	—	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This is a read/write register which is used to define an alternative 8-bit alignment character to be used for the Word Synchronization pattern. The Word Sync pattern is generated on each channel when its WSENn input is HIGH. The pattern normally consists of 16 IDLE characters (K28.5) as defined in the section, "Word Sync Generation" on page 7. Bits 0 through 7 define a single word sync character to be used rather than the 16-word sequence, and when bit 8 is set HIGH, the use of the alternate character is enabled. The alternate alignment character must be chosen from the list given in Table 4 on page 6, with the exception that K28.7 should not be used.

Bit 0 Defines bit 0 of the alternate special K-character for word alignment
Bit 1 Defines bit 1 of the alternate special K-character for word alignment
Bit 2 Defines bit 2 of the alternate special K-character for word alignment
Bit 3 Defines bit 3 of the alternate special K-character for word alignment
Bit 4 Defines bit 4 of the alternate special K-character for word alignment
Bit 5 Defines bit 5 of the alternate special K-character for word alignment
Bit 6 Defines bit 6 of the alternate special K-character for word alignment
Bit 7 Defines bit 7 of the alternate special K-character for word alignment
Bit 8 Set HIGH to enable the use of an alternate definition of the word alignment character
Bits 15:9 Undefined (reserved for future use)

Table 30. Register Block Index (Register Block 0-4, Register Address 31)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
At Reset	—	—	—	—	—	—	—	—	—	—	—	—	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This register is a read/write register which is used to select the desired register block for accessing the other registers as defined in Table 12 on page 25. Once written to a different value, the register block index will hold the new value until a power-on reset condition occurs. The register block index can always be accessed at register address 31 regardless of which register block is currently selected.

Bits 3:0 Set to select 1 of 16 blocks of MDIO/MDC serial interface registers

Bits 15:4 Undefined (reserved for future use)

Table 31. BIST Cycle Counter (Register Block 1-4, Register Address 16 and 17)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
At Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

These two 16-bit read/write registers (located at address 16 and 17 and in each of the register blocks 1 through 4, respectively) contain the lower and upper words of four 32-bit BIST cycle counters. When reading the contents of these registers, register address 16 must be read first, followed by register address 17, with no transactions taking place between the two read operations. There is one counter for each of the four transmit channels in the VSC7226. Register block 1 holds the counter for channel A, register block 2 holds the counter for channel B, register block 3 holds the counter for channel C and register block 4 holds the counter for channel D. These counters are incremented by one when the following conditions are true:

- BIST operation for the appropriate transmit channel is enabled
- The appropriate counter enable bits in register address 30 are set
- An entire 259 byte BIST pattern has been transmitted

These counters can be read at anytime without affecting the counter increment process. The counters can be cleared by writing any value to either the lower or upper byte of the BIST cycle counters. Upon power-on reset, the counters are cleared to 0.

Table 32. BIST Error Counter (Register Block 1-4, Register Address 18 and 19)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
At Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

These two 16-bit read/write registers (located at address 18 and 19 and in each of the register blocks 1 through 4, respectively) contain the lower and upper words of four 32-bit BIST error counters. When reading the contents of these registers, register address 18 must be read first, followed by register address 19, with no transactions taking place between the two read operations. There is one counter for each of the four receive channels in the VSC7226. Register block 1 holds the counter for channel A, register block 2 holds the counter for channel B, register block 3 holds the counter for channel C and register block 4 holds the counter for channel D. These counters are incremented by 1 when the following conditions are true:

- BIST operation for the appropriate receive channel is enabled
- The appropriate counter enable bits in register address 30 are set

The BIST pattern detector finds any invalid pattern in one BIST cycle that ends with D31.7, followed by three bytes of K28.5. (This is different from STERRn which will be flagged whenever a mismatched pattern is encountered.)

These counters can be read at anytime without affecting the counter increment process. The counters can be cleared by writing any value to either the lower or upper byte of the BIST error counters. Upon power-on reset, the counters are cleared to 0.

Table 33. Rx 8B/10B Error Counter (Register Block 1-4, Register Address 20 and 21)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
At Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

These two 16-bit read/write registers (located at address 20 and 21 and in each of the register blocks 1 through 4, respectively) contain the lower and upper words of four 32-bit error counters for counting 8B/10B coding violations on the receive channels. When reading the contents of these registers, register address 20 must be read first, followed by register address 21, with no transactions taking place between the two read operations. There is one counter for each of the four receive channels in the VSC7226. Register block 1 holds the counter for channel A, register block 2 holds the counter for channel B, register block 3 holds the counter for channel C and Register block 4 holds the counter for channel D. These counters are incremented by 1 when the following conditions are true:

- 8B/10B decoding is enabled for the appropriate receive channel
- The appropriate counter enable bits in register address 30 are set
- The 8B/10B decoder finds an invalid 8B/10B pattern on the appropriate receive channel

These counters can be read at anytime without affecting the counter increment process. The counters can be cleared by writing any value to either the lower or upper byte of the error counters. Upon power-on reset, the counters are cleared to 0.

Table 34. Rx Disparity Error Counter (Register Block 1-4, Register Address 22 and 23)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
At Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

These two 16-bit read/write registers (located at address 22 and 23 and in each of the register blocks 1 through 4, respectively) contain the lower and upper words of four 32-bit error counters for counting 8B/10B disparity violations on the receive channels. When reading the contents of these registers, register address 22 must be read first, followed by register address 23, with no transactions taking place between the two read operations. There is one counter for each of the four receive channels in the VSC7226. register block 1 holds the counter for channel A, register block 2 holds the counter for channel B, register block 3 holds the counter for channel C and register block 4 holds the counter for channel D. These counters are incremented by 1 when the following conditions are true:

- 8B/10B decoding is enabled for the appropriate receive channel
- The appropriate counter enable bits in register address 30 are set
- The 8B/10B decoder finds an incorrect disparity on the appropriate receive channel

These counters can be read at anytime without affecting the counter increment process. The counters can be cleared by writing any value to either the lower or upper byte of the error counters. Upon power-on reset, the counters are cleared to 0.

Table 35. Rx FIFO Error Counter (Register Block 1-4, Register Address 24 and 25)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
At Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

These two 16-bit read/write registers (located at address 24 and 25 and in each of the register blocks 1 through 4, respectively) contain the lower and upper words of four 32-bit error counters for counting FIFO overflow or underflow conditions on the receive channels. There is one counter for each of the four receive channels in the VSC7226. Register block 1 holds the counter for channel A, register block 2 holds the counter for channel B, register block 3 holds the counter for channel C and register block 4 holds the counter for channel D. These counters are incremented by 1 when the following conditions are true:

- The appropriate counter enable bits in register address 30 are set
- An overflow or underflow condition occurs on the appropriate receive channel

These counters can be read at anytime without affecting the counter increment process. The counters can be cleared by writing any value to either the lower or upper byte of the error counters. Upon power-on reset, the counters are cleared to 0.

Table 36. Counter Control (Register Block 1-4, Register Address 30)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
At Reset	—	—	—	—	—	—	—	—	—	—	—	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This register is a read/write register which is used to start and stop the 32-bit counters as defined above. To enable the incrementing of a counter, the appropriate bit in counter control register must be set HIGH. To disable the incrementing of a counter, the appropriate bit in counter control register must be set LOW. The setting or clearing of the counter control bits does not clear the corresponding counter. Counters can only be cleared by writing any value to the lower or upper 16-bit registers of the appropriate counter.

Bit 0 Set HIGH/LOW to enable/disable incrementing of the BIST cycle counter at register address 16 and 17

Bit 1 Set HIGH/LOW to enable/disable incrementing of the BIST error counter at register address 18 and 19

Bit 2 Set HIGH/LOW to enable/disable incrementing of the Rx 8B/10B error counter at register address 20 and 21

Bit 3 Set HIGH/LOW to enable/disable incrementing of the Rx disparity error counter at register address 22 and 23

Bit 4 Set HIGH/LOW to enable/disable incrementing of the Rx FIFO error counter at register address 24 and 25

Bits 15:5 Undefined (reserved for future use)

SPECIFICATIONS

DC Characteristics

Over Recommended Operating Conditions.

Table 37. DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Condition
LVTTL Inputs/Outputs						
V_{OH}	Output HIGH voltage	V_{DD}–0.2			V	I_{OH} = –1mA
V_{OL}	Output LOW voltage			0.5	V	I_{OL} = +1mA
V_{IH}	Input HIGH voltage	2.0		V_{DD}	V	
V_{IL}	Input LOW voltage	0		0.8	V	
I_{IH}	Input HIGH current			50	µA	V_{IN} = 2.0V
I_{IL}	Input LOW current			–50	µA	V_{IN} = 0.8V
SSTL_2 Inputs/Outputs						
VREFT	Voltage reference input	1.15	1.25	1.35	V	Nominally V_{DDD}/2
V_{IH}	Input HIGH voltage	VREFT+0.35		V_{DDD}+0.30	V	
V_{IL}	Input LOW voltage	–0.30		VREFT –0.35	V	
I_{IH}	Input HIGH current			100	µA	V_{IN} = V_{DDD} + 0.3V
I_{IL}	Input LOW current			–100	µA	V_{IN} = –0.3V
VREFR	Voltage reference output	1.15	1.25	1.35	V	Nominally V_{DDQ}/2
V_{OH}	Output HIGH voltage	VREFR+0.42		V_{DDQ}	V	Unterminated 50Ω transmission line I_{OH} = –7.6mA
V_{OL}	Output LOW voltage	0		VREFR–0.42	V	Unterminated 50Ω transmission line I_{OL} = +7.6mA
High-Speed Inputs/Outputs (TXEMP = 0)[1]						
ΔV_{OUT75}	Tx Output differential peak-to-peak voltage swing[2]	1100		2000	mVp-p	150Ω differential load (Tx+) – (Tx-), REDSW = 0
ΔV_{OUT50}	Tx Output differential peak-to-peak voltage swing[2]	900		1800 1400 for -05 and -06	mVp-p	100Ω differential load (Tx+) – (Tx–), REDSW = 0
ΔV_{OUT75}	Tx Output differential peak-to-peak voltage swing[2]	500		1000	mVp-p	150Ω differential load (Tx+) – Tx–), REDSW = 1
ΔV_{OUT50}	Tx Output differential peak-to-peak voltage swing[2]	450		900	mVp-p	100Ω differential load (Tx+) – (Tx–), REDSW = 1
ΔV_{IN}	Receiver differential peak-to-peak input voltage swing[2]	200		2200	mVp-p	Differential measurement (Rx+) – (Rx–)
Miscellaneous						
V_{DD}, V_{DDQ}, V_{DDA}, V_{DDPN}, V_{DDRN}, V_{DDD}	Power supply voltage	2.375		2.625	V	2.5V±5%.
P_D	Power dissipation			2389	mW	Outputs open, at V_{DD} max

Table 37. DC Characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Units	Condition
I_{DD}	Power supply current			910	mA	Outputs open, at V_{DD} max

1. Measurements taken at inner edge of data eye.

2. Refer to Vitesse Application Note AN-37 for information on differential measurement techniques.

AC Specifications

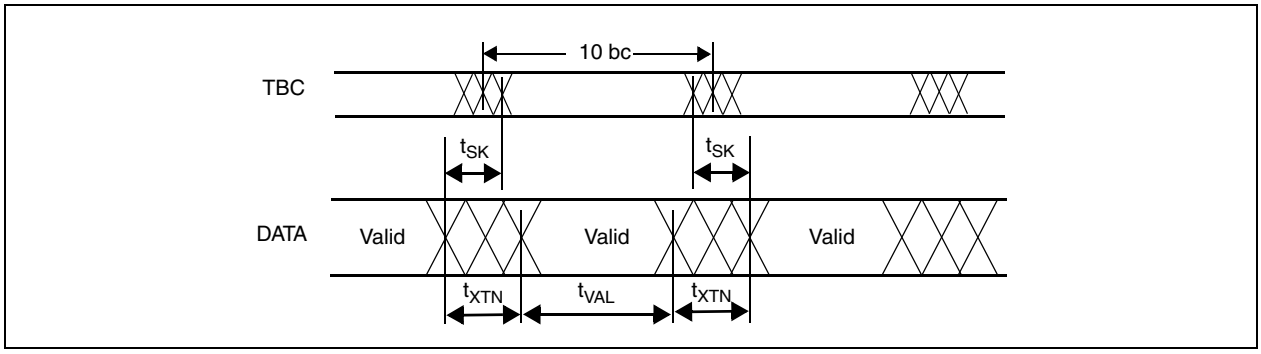


Figure 12. Transmitter Input Timing Waveforms, TMODE[2:0] = 0xx

Table 38. Transmitter Input AC Characteristics, TMODE[2:0] = 0xx

Symbol	Parameter	Min	Typ	Max	Units	Condition
t_{SK}	Skew, TBC transition range to data transition range			3	bc(1)	
	Duty cycle for TBC	35		65	%	
t_{XTN}	Data transition time			6(2)	bc	
t_{VAL}	Data valid time	4			bc	

1. *Bit clock or baud rate clock. For a serial rate of 2.5Gb/s, bc = 400ps.*
2. *Achieving t_{XTN} max (t_{VAL} min) requires a 50% duty cycle.*

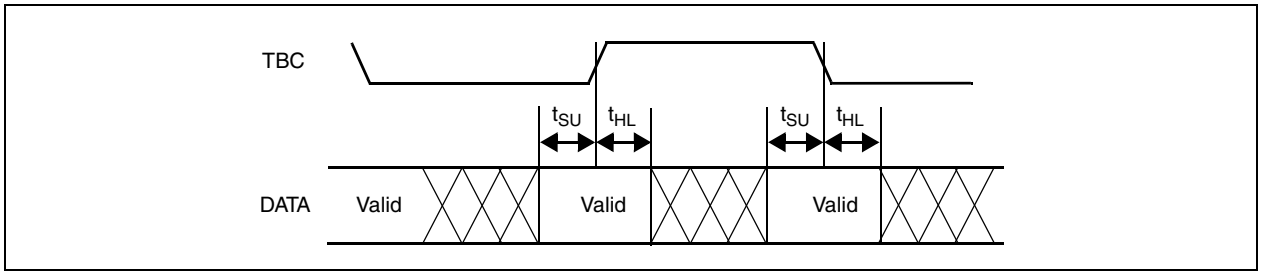


Figure 13. Transmitter Input Timing Waveforms, TMODE[2:0] = 1xx

Table 39. Transmitter Input AC Characteristics, TMODE[2:0] = 1xx

Symbol	Parameter	Min	Typ	Max	Units	Condition
t_{SU}	Data setup time	2.0			bc	
t_{HL}	Data hold time	2.0			bc	

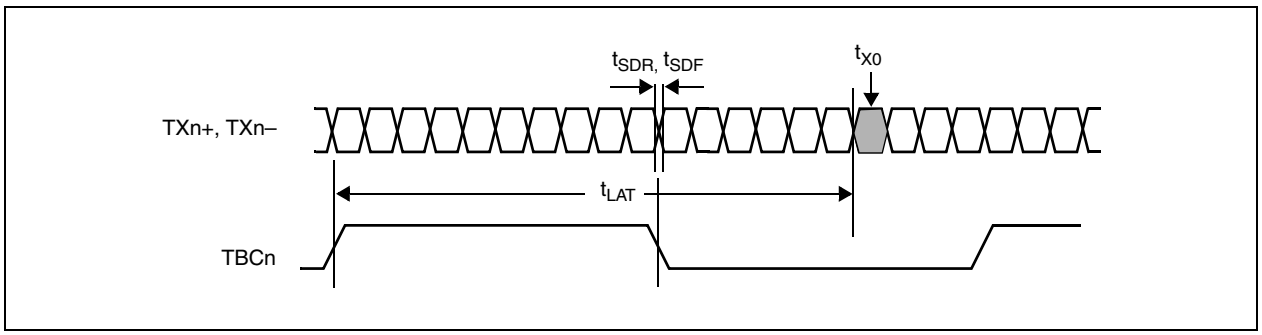


Figure 14. Transmitter Serial Timing Waveforms

Table 40. Transmitter Serial AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Condition
t_{SDR}, t_{SDF}	TXn+/- rise and fall time	70		200	ps	Measured between 20% to 80% of the valid data level at full swing.
		70		200	ps	Measured between 20% to 80% of the valid data level at half swing.
t_{LAT}	Latency, TBCn to TX0 (VSC7226-01 and VSC7226-05 only)	 12.5 11 16 14		 15 13 19 17	 ns ns ns ns	At 3.125Gb/s. EDBYP = 0, TMODE = 0xx. EDBYP = 0, TMODE = 1xx. At 2.4Gb/s. EDBYP = 0, TMODE = 0xx. EDBYP = 0, TMODE = 1xx.
t_J	Serial data output Total jitter (p-p) (VSC7226-01 and VSC7226-05 only)			192 117 112	ps ps ps	At 1.2Gb/s per GbE/FC. At 2.4Gb/s per FC. At 3.125Gb/s per XAUI. Methodology per FC-PH revision 4.3, tested on a sample basis with clock multiplier = 10x and 20x. **NOTE:** The PLL clock used to latch out the serial diata is based on the local REFCLK.
t_{DJ}	Serial data output Deterministic jitter (p-p)			80 57 55	ps ps ps	At 1.2Gb/s per GbE/FC. At 2.4Gb/s per FC. At 3.125Gb/s per XAUI. Methodology per FC-PH revision 4.3, tested on a sample basis with clock multiplier = 10x and 20x. **NOTE:** The PLL clock used to latch out the serial diata is based on the local REFCLK.

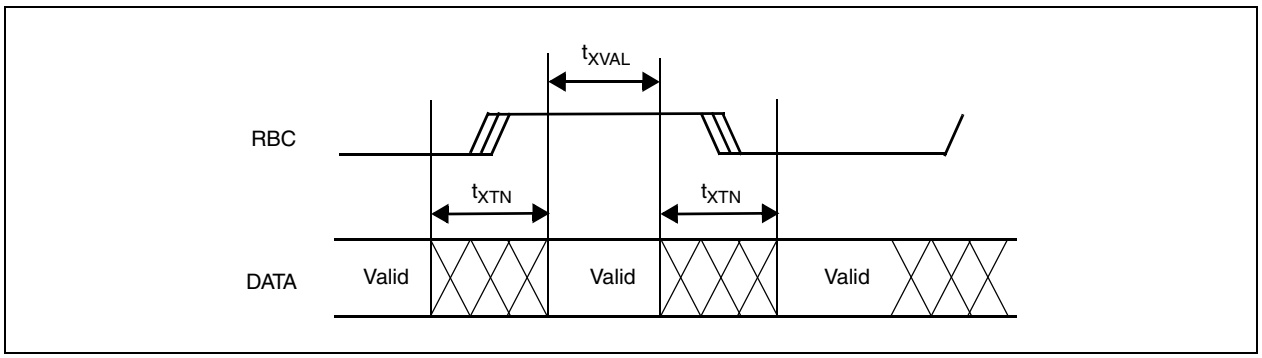


Figure 15. Receiver Output Timing Waveforms, RMODE[2:0] = 0xx

Table 41. Receiver Output AC Characteristics, RMODE[2:0] = 0xx

Symbol	Parameter	Min	Typ	Max	Units	Condition
t_{XVAL}	Data valid time	10bc–1.0ns			bc, ns	
t_{XTN}	Data in transition		1	2	bc	
	Duty Cycle	40		60	%	

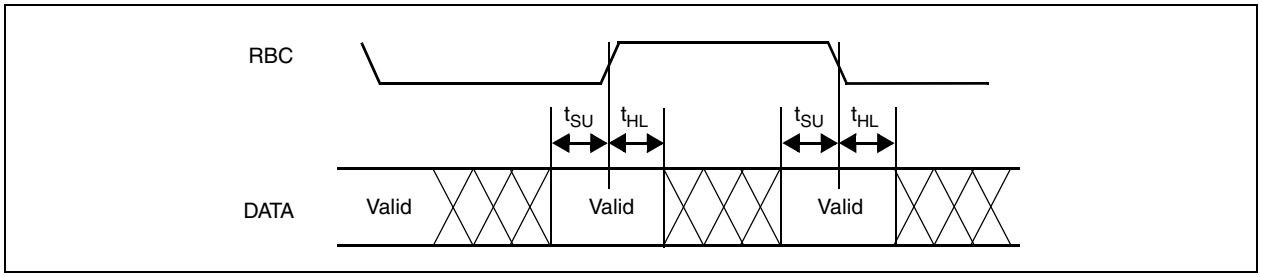


Figure 16. Receiver Output Timing Waveforms, RMODE[2:0] = 1xx

Table 42. Receiver Output AC Characteristics, RMODE[2:0] = 1xx

Symbol	Parameter	Min	Typ	Max	Units	Conditions
t_{SU}	Data setup time	2.5	4.0		bc	
t_{HL}	Data hold time	2.5	4.5		bc	

Table 43. General Receive AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Condition
t_4	Period of RBCn		20/(Rx Data Rate)			
Δt_4	Deviation of RBCn period from REFCLK period $t_{(RBC)} = t_{REFCLK} \pm \Delta t_4$	See Table 44 on page 47				
t_R, t_F	Output rise and fall time, SSTL_2 outputs	90	200	650	ps	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$ into 10pF load.
R_{LAT}	Latency from RX0 to RBC	44 35 35 28		56 44 60 47	ns ns ns ns	At 2.4Gb/s. At 3.125Gb/s. EDBYP = 1, re-center only. At 2.4Gb/s. At 3.125Gb/s. EDBYP = x, re-center + drift.
t_{LOCK}	Data acquisition lock time	81	124	290	Data transi-tions	Tested on a sample basis. Note: Probability of recovery for data acquisition is 95% per Section 5.3 of FC-PH revision 4.3.
T_{JTD}	Receive data total jitter tolerance (p-p)			0.7	UI	Methodology per FC-PH, revision 4.3, tested on a sample basis with input amplitude at 200mV differential.
D_{JTD}	Receive data deterministics jitter tolerance (p-p)			0.4	UI	Methodology per FC-PH, revision 4.3, tested on a sample basis with input amplitude at 200mV differential.

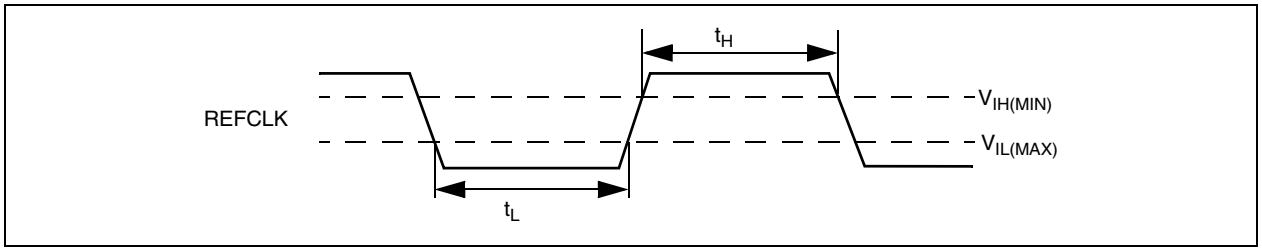


Figure 17. Reference Clock Timing Waveforms

Table 44. Reference Clock Requirements

Symbol	Parameter	Min	Typ	Max	Units	Condition
FR	Frequency Range: VSC7226-01 and VSC7226-05	240		312.5	MHz	REFMUL[1:0] = 00, RATE = 1.
		120		156.25	MHz	REFMUL[1:0] = 01, RATE = 1. REFMUL[1:0] = 00, RATE = 0.
		60		78.125	MHz	REFMUL[1:0] = 10, RATE = 1. REFMUL[1:0) = 01, RATE = 0.
		30		39.06	MHz	REFMUL[1:0] = 10, RATE = 0.
FR	Frequency Range: VSC7226-02 and VSC7226-06	190		252	MHz	REFMUL[1:0] = 00, RATE = 1.
		95		126	MHz	REFMUL[1:0) = 01, RATE = 1. REFMUL[1:0) = 00, RATE = 0.
		47.5		63	MHz	REFMUL[1:0] = 10, RATE = 1. REFMUL[1:0] = 01, RATE = 0.
		23.75		31.5	MHz	REFMUL[1:0] = 10, RATE = 0.
FO	Frequency Offset	–200		+200	ppm	|REFCLK (Tx) – REFCLK (Rx)| = max offset between Tx and Rx device REFCLKs on one serial link.
DC	REFCLK duty cycle	35		65	%	Measured at 1.4V.
t_H, t_L	REFCLK and TBC pulse width	2.4			ns	At 156.25MHz .
t_{RCR}, t_{RCF}	REFCLK rise and fall time			0.8	ns	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$. At 156.25MHz.
REFCLK Jitter	REFCLK jitter power $\int_{100Hz}^{7MHz} PhaseNoise$			100	ps	Peak-to-Peak for 10^{-12} Bit Error Ratio with zero length external path, tested on a sample basis.

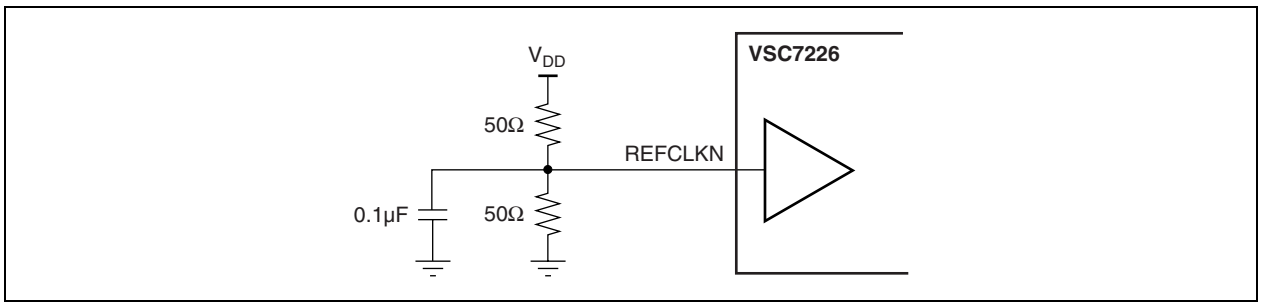


Figure 18. REFCLKN Termination When Single-Ended LVTTL Clock is Used at REFCLKP (Note that the depicted termination is recommended, not mandatory.)

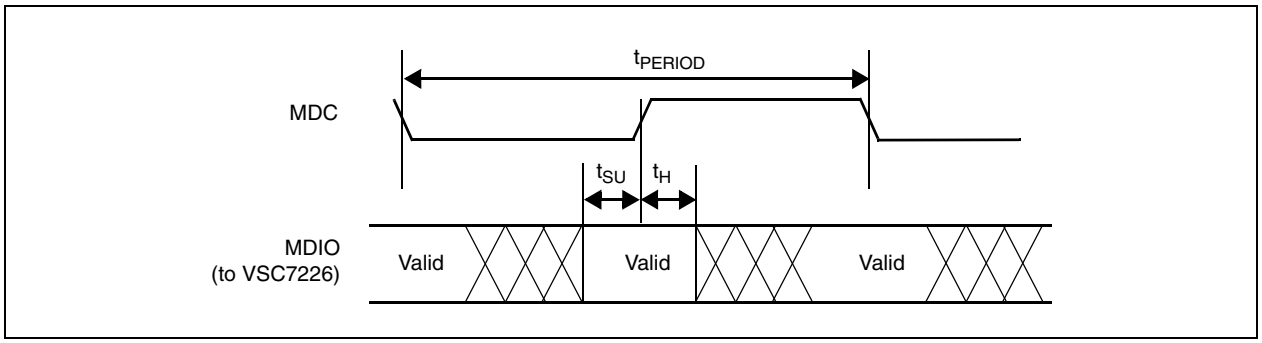


Figure 19. MDIO Input Timing Waveforms

Table 45. MDIO Input Timing AC Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units	Condition
t_{SU}	Data setup time	10			ns	
t_{HL}	Data hold time	10			ns	
t_{PERIOD}	MDC clock period	400			ns	

1. Values are guaranteed by design, but not tested.

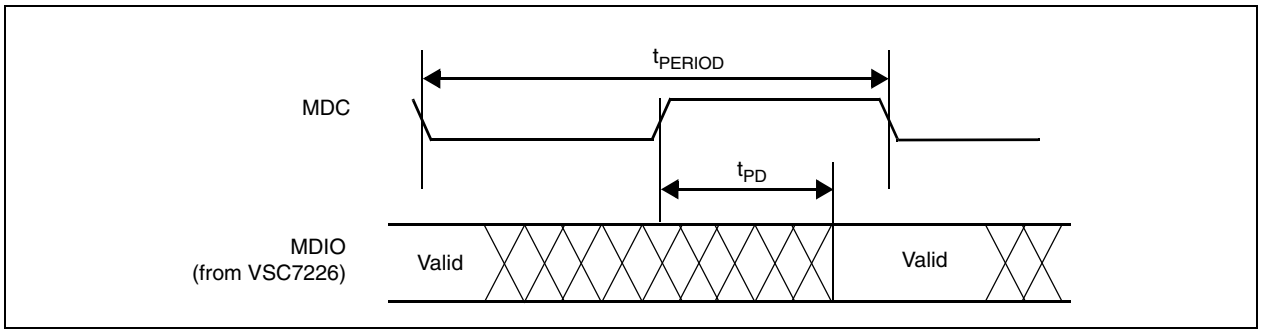


Figure 20. MDIO Output Timing Waveforms

Table 46. MDIO Output Timing AC Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units	Condition
t_{PD}	Data valid after MDC rising edge	0		300	ns	With MRS=1
t_{PD}	Data valid after MDC rising edge	200		300	ns	With MRS=0
t_{PERIOD}	MDC clock period	400			ns	

1. Values are guaranteed by design, but not tested.

Table 47. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Power supply voltage	2.375	2.5	2.625	V
T	Operating temperature range[1] VSC7226-01 and VSC7226-02	0		+100	°C
T	Operating temperature range[1] VSC7226-05 and VSC7226-06	–40		+100	°C

1. Lower limit of specification is ambient temperature, and upper limit is case temperature.

Table 48. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}	Power supply voltage (any V_{DDx} except V_{DDT})	–0.5	+4.0	V
	DC input voltage (PECL, TTL, SSTL)	–0.5	+3.47	V
	DC output voltage (TTL, SSTL)	–0.5	V_{DD} + 0.5	V
	Output current (PECL, TTL, SSTL)	–50	+50	mA
T_C	Case temperature under bias	–55	+125	°C
T_S	Storage temperature	–65	+150	°C
V_{ESD}	Electrostatic discharge (ESD) voltage (human body model)	–750	+750	V

Stresses listed under Absolute Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

PACKAGE INFORMATION

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	RTXD+	RTXD-	PRXD+	PRXD-	TBCD	VDDD	REFCLKP	TMODE2	C/DC	TBCC	VSSD	TCO	VDDD	TDI	TCK	VREFR	RSDETD	VSSQ	PSDETD	VDDQ	A
B	PTXD+	PTXD-	VSSD	TMODE1	WSEND	TD6	TD4	REFCLKN	WSENC	TC5	VDDD	TC1	TRSTN	VDDD	MRS	STERRD	IDLED	RBCD	VSSQ	ERRD	B
C	VDDD	REFMUL1	BIST	VSSD	TMODE0	TD7	VSSD	TD2	TD0	TC6	TC3	TC2	VSSD	MDIO	KCHD	RD7	RD6	RD5	RD4	RSDETC	C
D	PRXD+	PRXD-	VDDPD	VDDD	VDDRD	C/DD	TD5	TD3	TD1	TC7	TC4	TMS	MDC	TDO	VDDQ	VSSQ	RD3	VDDQ	VSSQ	PSDETC	D
E	RRXC+	RRXC-	REFMUL0	VSSD													RD2	RD1	STERRC	IDLEC	E
F	RTXC+	RTXC-	RBCREF	REDSW													RD0	VDDQ	VSSQ	VDDQ	F
G	VDDPC	VDDRC	RMODE2	RATE													VDDQ	ERRC	KCHC	RC7	G
H	PTXC+	PTXC-	RMODE1	VSSD													VSSQ	RC6	RBCC	RC5	H
J	PRXC+	PRXC-	RMODE0	VSSD													RC4	VSSQ	VDDQ	RC3	J
K	CAP0	VSSA	VSSD	VSSA													RC2	RC1	RCD	VDDQ	K
L	CAP1	VDDA	VDDD	VDDA													RSDETB	PSDETB	STERRB	VSSQ	L
M	PRXB+	PRXB-	TXEMP	VSSD													IDLEB	VSSQ	VDDQ	ERRB	M
N	PTXB+	PTXB-	MDIOA4	VSSD													VSSQ	KCHB	RBCB	RB7	N
P	VDDPB	VDDRB	MDIOA3	SLOOP													VDDQ	RB6	RB5	RB4	P
R	RTXB+	RTXB-	MDIOA2	TEST0													RSDETA	VDDQ	VSSQ	VDDQ	R
T	RRXB+	RRXB-	MDIOA1	VSSD													PSDETA	STERRA	RB3	RB2	T
U	PRXA+	PRXA-	VDDPA	VSSD	VSSD	TA4	C/DA	WSENA	TB4	TB7	EDBYP	RESETN	VSSD	VSSD	VDDQ	VSSQ	IDLEA	VDDQ	VSSQ	RB1	U
V	VDDD	MDIOA0	VREFT	VSSD	TA1	TA3	TA7	VDDD	TB3	TBCB	ADEN	RRXSEL	RTXEN	VSSREG	ERRA	KCHA	RA7	RA6	VSSQ	RB0	V
W	PTXA+	PTXA-	VDDRA	VDDD	TA0	TBCA	TA6	VSSD	TB2	TB6	WSENB	KCHAR	PTXEN	VDDREG		RA5	RA4	VDDQ	RBCA	RA3	W
Y	RTXA+	RTXA-	RRXA+	RRXA-	RREF	TA2	TA5	TB0	TB1	TB5	C/DB	PLOOP	VDD18	VDDD	VDDD	VDDD	RA2	VSSQ	RA1	RA0	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

TOP VIEW

Table 49. Pin Identifications for VSC7226 (all variants)

Pin	Name	I/O	Type	Pin Description
5W, 5V 6Y, 6V 6U, 7Y 7W, 7V	TA0, TA1 TA2, TA3 TA4, TA5 TA6, TA7	I	SSTL_2	Transmit Data for Channel A, Synchronous to TBCA.
8Y, 9Y 9W, 9V 9U, 10Y 10W, 10U	TB0, TB1 TB2, TB3 TB4, TB5 TB6, TB7	I	SSTL_2	Transmit Data for Channel B, Synchronous to TBCB.
12A, 12B 12C, 11C 11D, 10B 10C, 10D	TC0, TC1 TC2, TC3 TC4, TC5 TC6, TC7	I	SSTL_2	Transmit Data for Channel C, Synchronous to TBCC.
9C, 9D 8C, 8D 7B, 7D 6B, 6C	TD0, TD1 TD2, TD3 TD4, TD5 TD6, TD7	I	SSTL_2	Transmit Data for Channel D, Synchronous to TBCD.
7U 11Y 9A 6D	C/DA C/DB C/DC C/DD	I	SSTL_2	Control/Data for Channel n. If KCHAR = C/Dn = LOW, Tn[7:0] is used to generate transmit data. If KCHAR = C/Dn = HIGH, special Kxx.x characters are transmitted based upon the value of Tn[7:0]. If KCHAR = LOW and C/Dn = HIGH, IDLE characters are transmitted. When EDBYP = HIGH, this is equivalent to data bit Tn8.
8U 11W 9B 5B	WSENA WSENB WSENC WSEND	I	SSTL_2	Word Sync Enable for Channel n. Asserted HIGH for one cycle to initiate transmission of the word sync sequence as defined in 3 and related text. When EDBYP=HIGH, this is equivalent to data bit Tn9.
6W 10V 10A 5A	TBCA TBCB TBCC TBCD	I	SSTL_2	Transmit Byte Clock. Input data timing references for Tn[7:0], WSENn and C/Dn. TBCA may be used as the timing reference for all four data channels or TBCA may be used for channels A and B, and TBCC for channels C and D.
12W	KCHAR	I	LVTTL	Special Kxx.x Character Enable. When C/Dn is HIGH, KCHAR controls data sent to the transmitter. When LOW, IDLE characters are sent. When HIGH, Kxx.x special characters are sent as encoded on Tn[7:0]. This is intended to be a static input and cannot be changed on a cycle-by-cycle basis. When EDBYP = HIGH, this is equivalent to ENCDET.
5C 4B 8A	TMODE0 TMODE1 TMODE2	I	LVTTL	Transmit Input Data Timing Mode. Determines the timing reference for Tn[7:0], WSENn and C/Dn on all channels as defined in Table 2.
4G	RATE	I	LVTTL	Tx and Rx Rate Select. This is a global control which selects full-speed mode for transmit and receive on all four channels when HIGH and low-speed mode when LOW. **NOTE:** Per channel independent Tx and Rx control is also provided through MDIO registers.
3E 2C	REFMUL0 REFMUL1	I	LVTTL	Reference Clock Multiplier. Reference clock may be multiplied by 10, 20, or 40 as shown in Table 1 to obtain the serial baud rate clock. Parallel data is always clocked into the device at 1/10th the multiplied clock.

Table 49. Pin Identifications for VSC7226 (all variants) (continued)

Pin	Name	I/O	Type	Pin Description
1W, 2W 1N, 2N 1H, 2H 1B, 2B	PTXA+/- PTXB+/- PTXC+/- PTXD+/-	O	PECL	Primary Differential Serial Tx Outputs for Channel n. These pins output serialized transmit data on all four channels when PTXEN is HIGH. **NOTE:** MDIO registers may be used for individual channel control.
1Y, 2Y 1R, 2R 1F, 2F 1A, 2A	RTXA+/- RTXB+/- RTXC+/- RTXD+/-	O	PECL	Redundant Differential Serial Tx Outputs for Channel n. These pins generate serialized transmit data on all four channels when RTXEN is HIGH. **NOTE:** MDIO registers may be used for individual channel control.
13W	PTXEN	I	LVTTL	Primary Tx Output Enable. When HIGH, all four PTXn+/- outputs are active. When LOW, all PTXn+/- are powered down and the outputs are un-driven. **NOTE:** Per channel control is also provided through MDIO registers.
13V	RTXEN	I	LVTTL	Redundant Tx Output Enable. When HIGH, all four RTXn+/- outputs are active. When LOW, all RTXn+/- are powered down and the outputs are un-driven. **NOTE:** Per channel control is also provided through MDIO registers.
20Y, 19Y 17Y, 20W 17W, 16W 18V, 17V	RA0, RA1 RA2, RA3 RA4, RA5 RA6, RA7	O	SSTL_2	Receive Data for Channel A. Synchronous to RBCn or REFCLK as selected by RMODE[2:0], as are IDLEA, KCHA and ERRA.
20V, 20U 20T, 19T 20P, 19P 18P, 20N	RB0, RB1 RB2, RB3 RB4, RB5 RB6, RB7	O	SSTL_2	Receive Data for Channel B. Synchronous to RBCn or REFCLK as selected by RMODE[2:0], as are IDLEB, KCHB and ERRB.
19K, 18K 17K, 20J 17J, 20H 18H, 20G	RC0, RC1 RC2, RC3 RC4, RC5 RC6, RC7	O	SSTL_2	Receive Data for Channel C. Synchronous to RBCn or REFCLK as selected by RMODE[2:0], as are IDLEC, KCHC and ERRC.
17F, 18E 17E, 17D 19C, 18C 17C, 16C	RD0, RD1 RD2, RD3 RD4, RD5 RD6, RD7	O	SSTL_2	Receive Data for Channel D. Synchronous to RBCn or REFCLK as selected by RMODE[2:0], as are IDLED, KCHD and ERRD.
17U 17M 20E 17B	IDLEA IDLEB IDLEC IDLED	O	SSTL_2	IDLE Detect for Channel n. When HIGH, an IDLE character has been detected by the decoder and is on Rn[7:0]. When EDBYP = HIGH, this is equivalent to COMDETn.
16V 18N 19G 15C	KCHA KCHB KCHC KCHD	O	SSTL_2	Kxx.x Character Detect for Channel n. When HIGH, a special Kxx.x character has been detected by the decoder and is on Rn[7:0]. When EDBYP = HIGH, this is equivalent to data bit Rn8.
15V 20M 18G 20B	ERRA ERRB ERRC ERRD	O	SSTL_2	Error Detect for Channel n. When HIGH, an invalid 10-bit character or disparity error has been detected and the data on Rn[7:0] is invalid. When EDBYP = HIGH, this is equivalent to data bit Rn9.
19W 19N 19H 18B	RBCA RBCB RBCC RBCD	O	SSTL_2	Receiver Byte Clock Outputs for Channel n. These outputs are driven from either recovered byte clock(s) or REFCLK based clock, at $1/10^{th}$, $1/20^{th}$ or $1/40^{th}$ the baud rate, as selected by REFMUL[1:0].

Table 49. Pin Identifications for VSC7226 (all variants) (continued)

Pin	Name	I/O	Type	Pin Description
3J 3H 3G	RMODE0 RMODE1 RMODE2	I	LVTTL	Receive Output Data Timing Mode. Determines the timing reference for all receive channels' Rn[7:0], IDLEn, KCHn and ERRn output data, and also for the PSDETn, RSDETn and STERRn outputs, as defined in Table 6.
3F	RBCREF	I	LVTTL	Receiver Output Byte Clock Derived from REFCLK. When set HIGH, this pin causes all four receiver channels to use REFCLK-based output timing. When set LOW, the byte clock is based on the recovered bit clock. **NOTE:** Per channel control is also provided through MDIO registers.
4F	REDSW	I	LVTTL	Reduced PECL Output Swing. When HIGH, reduced Tx PECL output swing operation is in effect for all channels. When LOW, full output voltage swing is selected. **NOTE:** Per channel control is also provided through MDIO registers when REDSW is set HIGH.
1U, 2U 1M, 2M 1J, 2J 1D, 2D	PRXA+/- PRXB+/- PRXC+/- PRXD+/-	I	PECL	Primary Differential Serial RX Inputs for Channel n. These pins receive the serialized input data when SLOOP is LOW and RRXSEL is LOW. Otherwise, they are unused. They are internally biased at ~2/3 V_{DD} through a 7.1kΩ resistor to the bias voltage. AC-coupling is recommended.
3Y, 4Y 1T, 2T 1E, 2E 3A, 4A	RRXA+/- RRXB+/- RRXC+/- RRXD+/-	I	PECL	Redundant Differential Serial RX Inputs for Channel n. These pins receive the serialized input data when SLOOP is LOW and RRXSEL is HIGH. Otherwise, they are unused. They are internally biased at ~2/3V_{DD} through a 7.1kΩ resistor to the bias voltage. AC-coupling is recommended.
12Y	PLOOP	I	LVTTL	Parallel Loopback. When set HIGH, this input places all four channels in a parallel loopback configuration. The Rn[7:0] outputs are looped back to the Tn[7:0] inputs. **NOTE:** Per channel control is also provided through MDIO registers.
4P	SLOOP	I	LVTTL	Serial Loopback. When set HIGH, this input places all four channels in a serial loopback configuration. The transmitter's serial transmit data is internally connected to the receiver's CRU input. **NOTE:** Per channel control is also provided through MDIO registers.
12V	RRXSEL	I	LVTTL	Redundant Serial Rx Input Select. This input selects PRXn+/- as the Rx serial input source for all four channels when LOW and RRXn+/- as the serial input source when HIGH. **NOTE:** Per channel control is also provided through MDIO registers.
17T 18L 20D 19A	PSDETA PSDETB PSDETC PSDETD	O	SSTL_2	Primary Analog Signal Detect, Channel n. This output goes HIGH when the amplitude on PRXn is greater than approximately 270mV and LOW when the input is less than approximately 65mV. PSDETn is not defined when the input is between 270mV and 65mV. Output timing is same as Rn[7:0].
17R 17L 20C 17A	RSDETA RSDETB RSDETC RSDETD	O	SSTL_2	Redundant Analog Signal Detect, Channel n. This output goes HIGH when the amplitude on RRXn is greater than approximately 270mV and LOW when the input is less than approximately 65mV. RSDETn is not defined when the input is between 270mV and 65mV. Output timing is same as Rn[7:0].
7A 8B	REFCLKP REFCLKN	I	PECL	REFCLK Differential Positive and Negative PECL or Single-Ended TTL Inputs. Provides the reference clock at 1/10th, 1/20th or 1/40th of the baud rate to the PLL as selected by REFMUL[1:0]. IF TTL, connect to REFCLKP and terminate REFCLKN with a 0.1µF capacitor to ground and 50Ω pull-up and pull-down biasing resistors. If PECL, connect both REFCLKP and REFCLKN. See Figure 18 on page 48 for termination scheme when single-ended TTL clock is used.
1K 1L	CAP0 CAP1		Analog	Loop Filter Capacitor for Clock Generation PLL. Nominally 0.1µF, 20%, X7R, amplitude is less than 3V.

Table 49. Pin Identifications for VSC7226 (all variants) (continued)

Pin	Name	I/O	Type	Pin Description
11V	ADEN	I	LVTTL	Add/Drop Enable Mode. When LOW, enables rate matching (IDLE delete/duplicate) logic on all four channels. **NOTE:** Per channel control is also provided through MDIO registers when ADEN is HIGH.
3C	BIST	I	LVTTL	Built-In Self-Test Mode. When HIGH, all transmit channels continuously send a 256 byte incrementing data pattern, and all receive channels signal correct reception of the test pattern with a LOW on the STERRn outputs.
18T 19L 19E 16B	STERRA STERRB STERRC STERRD	O	SSTL_2	Self-Test Error Indicator, Channel n. Active when BIST is HIGH. When LOW, BIST data is being received correctly. When HIGH, BIST errors are detected.
11U	EDBYP	I	LVTTL	Encoder/Decoder Bypass Enable. When HIGH, the VSC7226 is configured for 10-bit operation, internal 8B/10B encoding is bypassed. When LOW, an 8-bit interface is used, internal 8B/10B encoding is enabled. **NOTE:** Per channel control is also provided through MDIO registers.
3M	TXEMP	I	LVTTL	Tx Emphasis. When HIGH, signal pre-emphasis is applied to all four channels **NOTE:** Per-channel control is provided by MDIO registers.
13D	MDC	I	LVTTL	MDIO Management Interface Clock. Used to clock MDIO data to/from the VSC7226. 2.5MHz maximum; no minimum.
14C	MDIO	I/O	LVTTL	MDIO Data I/O. Bidirectional signal used to access the control and status registers within the VSC7226. This pin has an internal pull-down resistor, therefore, it requires an external 1.5kΩ pull-up resistor as specified in IEEE-802.3, section 22.
2V 3T 3R 3P 3N	MDIOA0 MDIOA1 MDIOA2 MDIOA3 MDIOA4	I	LVTTL	MDIO Management Addresses. Used to specify a unique 5-bit address for the MDIO interface.
12U	RESETN	I	LVTTL	RESETN Input. When asserted LOW, the transmitter input skew buffers and receiver elastic buffers are re-centered, the receiver LOS state machines are forced to the LOS state, and the MDIO registers are reset to default values.
3V	VREFT	I	Analog	Voltage Reference Input for SSTL_2. Nominally $V_{DDD}/2$.(1)
16A	VREFR	O	Analog	Voltage Reference Output for SSTL_2. Nominally $V_{DDQ}/2$.(2)
5Y	RREF	I	Analog	Connect external resistor between 100Ω and 150Ω to this pin to set the approximate internal input resistance for high-speed inputs to between 100Ω and 150Ω at a 1:1 ratio.
15A	TCK	I	LVTTL	JTAG Test Access Port Test Clock Input
12D	TMS	I	LVTTL	JTAG Test Access Port Test Mode Select Input
14A	TDI	I	LVTTL	JTAG Test Access Port Test Data Input
14D	TDO	O	LVTTL	JTAG Test Access Port Test Data Output
13B	TRSTN	I	LVTTL	JTAG Test Access Port Test Logic Reset Input
4R	TEST0N	I	LVTTL	Reserved for Test Purposes.Set HIGH when in normal operation.
15W	RSVD	N/A	N/A	Reserved Input for Future Use. Must be set HIGH for future compatibility.
15B	MRS		LVTTL	MDIO Read Select. Must be set HIGH for MDIO read timing to be backward compatible with previous versions of the VSC7226 (B and older).To be MDIO read timing compatible to IEEE, MRS should be LOW. Refer to Figures 9 and 10.
2L,4L	VDDA		VDD	Analog Power Supply to PLL

Table 49. Pin Identifications for VSC7226 (all variants) (continued)

Pin	Name	I/O	Type	Pin Description
2K, 4K	VSSA		GND	Analog Ground to PLL
6A, 13A 11B, 14B 1C, 4D 3L, 1V 8V, 4W 15Y, 16Y	VDDD		VDD	Digital Power Supply. Bypass capacitors to VSSD on all pins are recommended.
11A, 3B 4C, 7C 13C, 4E 4H, 4J 3K, 4M 4N, 4T 4U, 5U 13U, 14U 4V, 8W	VSSD		GND	Digital Ground
20A, 15D 18D, 18F 20F, 17G 19J, 20K 19M, 17P 18R, 20R 15U, 18U 18W	VDDQ		VDD	SSTL_2 Output Power Supply. Bypass capacitors to VSSQ on all pins are recommended.
18A, 19B 16D, 19D 19F, 17H 18J, 20L 18M, 17N 19R, 16U 19U, 19V 18Y	VSSQ		GND	SSTL_2 Output Ground
3U 3W 1P 2P 1G 2G 3D 5D	VDDPA VDDRA VDDPB VDDRB VDDPC VDDRC VDDPD VDDRD		VDD	PECL Output Power Supply for PTXA PECL Output Power Supply for RTXA PECL Output Power Supply for PTXB PECL Output Power Supply for RTXB PECL Output Power Supply for PTXC PECL Output Power Supply for RTXC PECL Output Power Supply for PTXD PECL Output Power Supply for RTXD If use of an output is not necessary, leave the power supply pin open or ground it. Bypass capacitors to VSS on all pins are recommended. Filtering is also recommended.
14W	VDDREG		VDD	Provides access to internal voltage regulator. Connect to V_{DDA} during normal operation.
14V	VSSREG		GND	Ground for internal voltage regulator.

Table 49. Pin Identifications for VSC7226 (all variants) (continued)

Pin	Name	I/O	Type	Pin Description
13Y, 14Y	VDD18		Analog	External capacitance of 4.7µF or greater must be connected from either 13Y or 14Y to GND. These pins are tied together on-chip. Connected to internal 1.8V regulator.

1. *Use a resistive divider network to obtain a different reference voltage for all SSTL-2 inputs. The network must source/sink 100µA.*
2. *Not affected by the voltage applied to VDDT.*

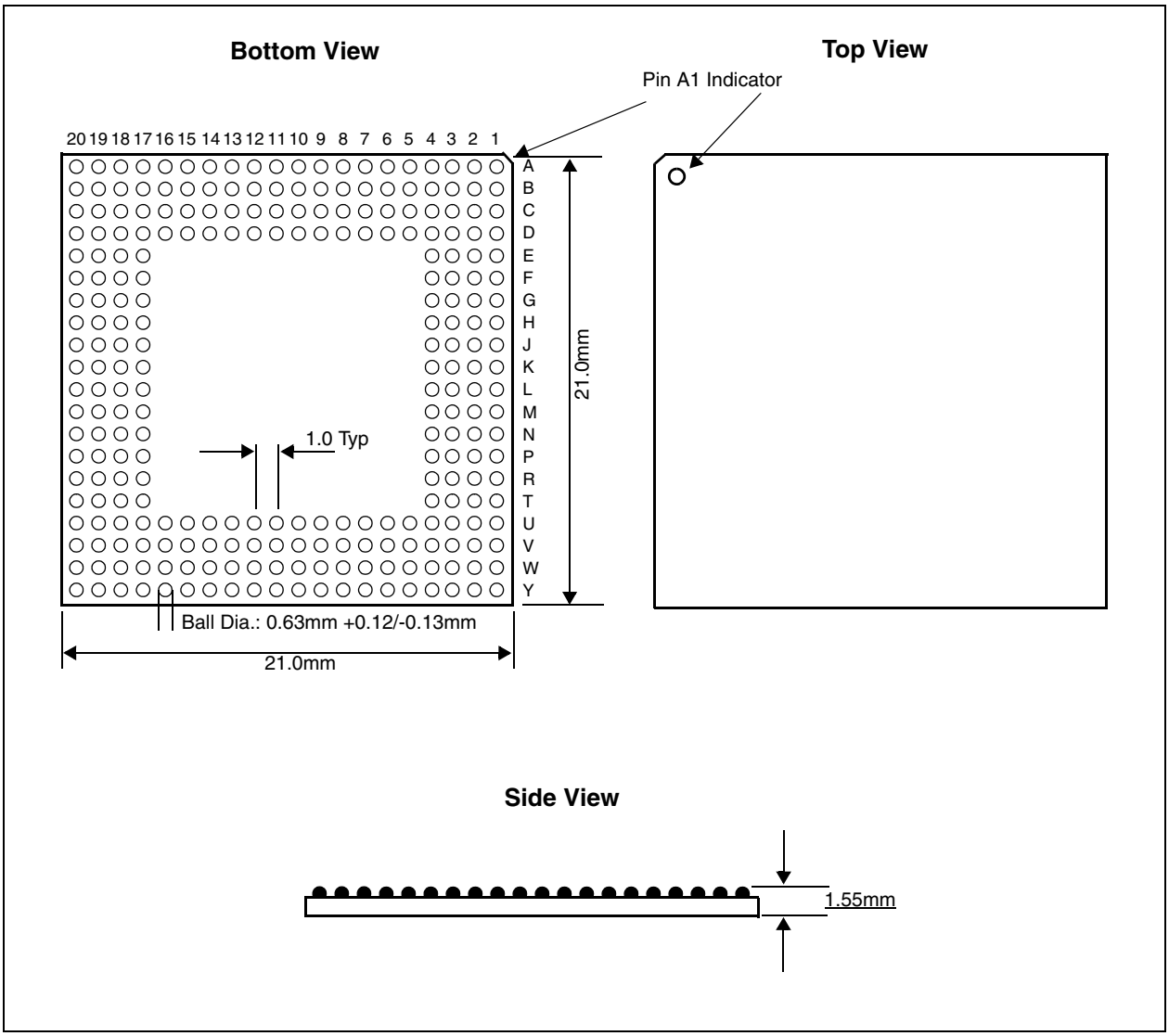


Figure 21. Package Drawing for VSC7226 (all variants)

Thermal Specifications

Thermal specifications for this device are based on the JEDEC standard EIA/JESD51-2 and have been modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information, see the JEDEC standard.

Table 50. Thermal Resistances

Part Number	θ_{JC}	θ_{JA} (°C/W) vs. Airflow (ft/min)		
		0	100	200
VSC7226UI-01, VSC7226XUI-01 VSC7226UI-02, VSC7226XUI-02 VSC7226UI-05, VSC7226XUI-05 VSC7226UI-06, VSC7226XUI-06	1.3	18.3	16.2	14.7

Moisture Sensitivity Level

Moisture sensitivity level ratings for Vitesse products comply with the joint IPC and JEDEC standard IPC/JEDEC J-STD-020.

VSC7226UI-01, VSC7226UI-02, VSC7226UI-05, and VSC7226UI-06 are rated moisture sensitivity level 3 or better.

VSC7226XUI-01, VSC7226XUI-02, VSC7226XUI-05, and VSC7226XUI-06 are rated moisture sensitivity level 4.

For more information, see the IPC and JEDEC standard.

REVISION HISTORY

This section describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

Revision 4.1 of this datasheet was published in May 25, 2006. The following is a summary of the changes implemented in the datasheet:

- The VSC7226 is now offered in lead(Pb)-free packages. For more ordering information, see "Ordering Information," page 59.
- In the table describing data output timing modes for RMODE2, the bit reference was corrected from RMODE[2:0] to RMODE2.

Revision 4.0 of this datasheet was published on August 14, 2003. The following is a summary of the changes implemented in the datasheet:

- The extended temperature range of the VSC7226-05 and the VSC7226-06 were introduced.
- The maximum operation speed of VSC7226-02 and VSC7226-06 at full rate has been changed from 2.4Gb/s to 2.52Gb/s.
- The block diagram of the device has been corrected to reflect the selection of word clock and RBC.
- PECL input termination has been improved, and the ratio of the external resistor at pin RREF to the internal termination impedance has been changed from 10:1 to 1:0; that is, for 100Ω termination, the resistor at RREF should be 100Ω instead of 1kΩ.
- In TBI mode, Comma detection and alignment of all four channels is now enabled or disabled by mode pins KCHAR/ENCDET together; and there is no MDIO control on this function.
- Using MDIO register 23, the customer can now select the comma to be always aligned with rising edge or falling edge of the RBC (recovered byte clock) on per channel basis. The default is to be backward-compatible, and this means that the comma could be aligned to either edge of the RBC.
- Two options on MDIO Read Operation have been made available, and pin 15B, named MRS (MDIO Read Select) is used to select the backward-compatible mode (set high as before) or the IEEE 802.3u compatible mode (set low). The difference between the two modes is the Turnaround (TA) to be Z0 or Z00.
- IDCODE has been updated to reflect revision C in MDIO register 17 as 308Dh.
- The Parametric Test load circuit has been deleted because a single test load circuit cannot reflect the different setups used for different parametric tests.
- The AC/DC parameters have been updated.
- The termination circuit for REFCLKN when LVTTL clock is used on REFCLKP is no longer mandatory.
- Pin names in Figure 20 have been corrected: F4=REDSW, 15B=MRS, U12=RESETN.
- The pin description of the TMDOEn pins have been corrected to cite Table 2 rather than Table 1.
- The threshold values quoted for pin PSDETn and RSDETn of the pin table have been corrected to match the numbers quoted on signal detection section.
- The phase lock time is a probabilistic number as indicated in the Fibre Channel specifications. Conditions have been added to the table to reflect this.

ORDERING INFORMATION

The VSC7226 device is available in two package types. VSC7226UI is a 256-pin tape ball grid array (TBGA) with a 21 mm × 21 mm body size. The device is also available in a lead(Pb)-free package, VSC7226XUI.

Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

The following table lists the ordering information for the VSC7226 device.

Table 51. Ordering Information

Part Number	Description
VSC7226UI-01	256-pin TBGA, 21 mm × 21 mm body size 2.4Gb/s to 3.125Gb/s and 1.2Gb/s to 1.5625Gb/s Operating temperature range: 0°C ambient to +100°C case
VSC7226XUI-01	Lead(Pb)-free, 256-pin TBGA, 21 mm × 21 mm body size 2.4Gb/s to 3.125Gb/s and 1.2Gb/s to 1.5625Gb/s Operating temperature range: 0°C ambient to +100°C case
VSC7226UI-02	256-pin TBGA, 21 mm × 21 mm body size 1.9Gb/s to 2.52Gb/s and 0.95Gb/s to 1.26Gb/s Operating temperature range: 0°C ambient to +100°C case
VSC7226XUI-02	Lead(Pb)-free, 256-pin TBGA, 21 mm × 21 mm body size 1.9Gb/s to 2.52Gb/s and 0.95Gb/s to 1.26Gb/s Operating temperature range: 0°C ambient to +100°C case
VSC7226UI-05	256-pin TBGA, 21 mm × 21 mm size 2.4Gb/s to 3.125Gb/s and 1.2Gb/s to 1.5625Gb/s Operating temperature range: –40ºC ambient to +100ºC case
VSC7226XUI-05	Lead(Pb)-free, 256-pin TBGA, 21 mm × 21 mm body size 2.4Gb/s to 3.125Gb/s and 1.2Gb/s to 1.5625Gb/s Operating temperature range: –40ºC ambient to +100ºC case
VSC7226UI-06	256-pin TBGA, 21 mm × 21 mm body size 1.9Gb/s to 2.52Gb/s and 0.95Gb/s to 1.26Gb/s Operating temperature range: –40°C ambient to +100ºC case
VSC7226XUI-06	Lead(Pb)-free, 256-pin TBGA, 21 mm × 21 mm body size 1.9Gb/s to 2.52Gb/s and 0.95Gb/s to 1.26Gb/s Operating temperature range: –40°C ambient to +100ºC case

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