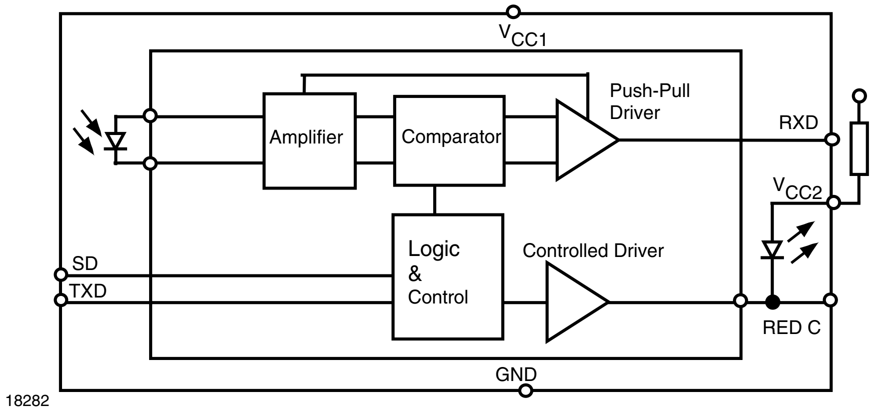
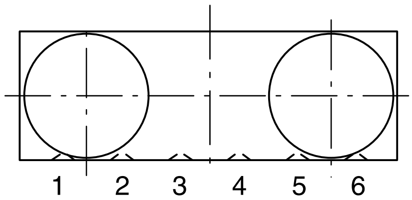
Functional Block Diagram



Pinout

TFBS4710
weight 100 mg



Definitions:

In the Vishay transceiver data sheets the following nomenclature is used for defining the IrDA operating modes:

SIR: 2.4 kbit/s to 115.2 kbit/s, equivalent to the basic serial infrared standard with the physical layer version IrPhy 1.0

MIR: 576 kbit/s to 1152 kbit/s

FIR: 4 Mbit/s

VFIR: 16 Mbit/s

MIR and FIR were implemented with IrPhy 1.1, followed by IrPhy 1.2, adding the SIR Low Power Standard. IrPhy 1.3 extended the Low Power Option to MIR and FIR and VFIR was added with IrPhy 1.4. A new version of the standard in any case obsoletes the former version.

With introducing the updated versions the old versions are obsolete. Therefore the only valid IrDA standard is the actual version IrPhy 1.4 (in Oct. 2002).

Pin Description

Pin Number	Function	Description	I/O	Active
1	IRED Anode	IRED Anode is connected to a power supply. The LED current can be decreased by adding a resistor in series between the power supply and IRED Anode. A separate unregulated power supply can be used at this pin.		
2	TXD	This Input is used to turn on IRED transmitter when SD is low. An on-chip protection circuit disables the LED driver if the TXD pin is asserted for longer than 80 µs	I	HIGH
3	RXD	Received Data Output, normally stays high but goes low for a fixed duration during received pulses. It is capable of driving a standard CMOS or TTL load.	O	LOW
4	SD	Shutdown. Setting this pin active for more than 1.5 ms switches the device into shutdown mode	I	HIGH
5	V_{CC}	Regulated Supply Voltage		
6	GND	Ground		

Absolute Maximum Ratings

Reference Point Ground, Pin 6 unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Supply voltage range, all states		V_{CC}	- 0.3		+ 6.0	V
Input current	For all Pins except IRED Anode Pin	I_{CC}			10.0	mA
Output Sink Current, RXD					25.0	mA
Average output current, pin 1	20 % duty cycle	I_{IRED} (DC)			60	mA
Repetitive pulsed output current	< 90 µs, t_{on} < 20 %	I_{IRED} (RP)			300	mA
IRED anode voltage, pin 1		V_{IREDA}	- 0.5		+ 6.0	V
Voltage at all inputs and outputs	V_{in} > V_{CC} is allowed	V_{IN}	- 0.5		+ 6.0	V
Power dissipation	See derating curve				200	mW
Junction temperature					125	°C
Ambient temperature range (operating)		T_{amb}	- 30		+ 85	°C
Storage temperature range		T_{stg}	- 40		+ 100	°C
Soldering temperature	See Recommended Solder Profile				260	°C

Electrical Characteristics

Transceiver

T_{amb} = 25 °C, V_{CC} = V_{IREDA} = 2.4 V to 5.5 V unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Supply voltage range, all states		V_{CC}	2.4		5.5	V
Idle supply current at V_{CC1} (receive mode, no signal)	SD = Low, E_e = 1 klx*), T_{amb} = - 25 °C to + 85 °C, V_{CC1} = V_{CC2} = 2.7 V to 5.5 V	I_{CC1}		90	130	µA
	SD = Low, E_e = 1 klx*), T_{amb} = 25 °C, V_{CC1} = V_{CC2} = 2.7 V to 5.5 V	I_{CC1}		75		µA
Receive current	V_{CC} = 2.7 V	I_{CC}		280		µA
Shutdown current	SD = High, T = 25 °C, E_e = 0 klx	I_{SD}			2	µA
	SD = High, T = 85 °C	I_{SD}			3	µA
Operating temperature range		T_A	- 25		+ 85	°C
Output voltage low, RXD	I_{OL} = 1 mA	V_{OL}	- 0.5		0.15 x V_{CC}	V
Output voltage high, RXD	I_{OH} = - 500 µA	V_{OH}	0.8 x V_{CC}		V_{CC} + 0.5	V
	I_{OH} = - 250 µA	V_{OH}	0.9 x V_{CC}		V_{CC} + 0.5	V
RXD to V_{CC} impedance		R_{RXD}	400	500	600	kΩ
Input voltage low: TXD, SD		V_{IL}	- 0.5		0.5	V
Input voltage high: TXD, SD	CMOS level (0.5 x V_{CC} typ, threshold level)	V_{IH}	V_{CC} - 0.5		6.0	V
Input leakage current (TXD, SD)	V_{in} = 0.9 x V_{CC}	I_{ICH}	- 2		+ 2	µA
Controlled pull down current	SD, TXD = "0" or "1", 0 < V_{in} < 0.15 V_{CC}	I_{IRTx}			+ 150	µA
	SD, TXD = "0" or "1" V_{in} > 0.7 V_{CC}	I_{IRTx}	- 1	0	1	µA
Input capacitance		C_{IN}			5	pF

Optoelectronic Characteristics

Receiver

T_{amb} = 25 °C, V_{CC} = 2.4 V to 5.5 V unless otherwise noted

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
Minimum detection threshold irradiance, SIR mode	9.6 kbit/s to 115.2 kbit/s λ = 850 nm - 900 nm, α = 0°, 15°	E_e	10 (1.0)	25 (2.5)	40 (4)	mW/m² (µW/cm²)
Maximum detection threshold irradiance	λ = 850 nm - 900 nm	E_e		5 (500)		kW/m² (mW/cm²)
Maximum no detection threshold irradiance		E_e			4 (0.4)	mW/m² (µW/cm²)
Rise time of output signal	10 % to 90 %, C_L = 15 pF	$t_{r(RXD)}$	10		100	ns
Fall time of output signal	90 % to 10 %, C_L = 15 pF	$t_{f(RXD)}$	10		100	ns
RXD pulse width	Input pulse width > 1.2 µs	t_{PW}	1.65	2.0	3.0	µs
Leading edge jitter	Input Irradiance = 100 mW/m², ≤ 115.2 kbit/s				250	ns
Standby /Shutdown delay	After shutdown active				150	µs
Receiver startup time	Power-on delay					
Latency		t_L			150	µs

Transmitter

T_{amb} = 25 °C, V_{CC} = 2.4 V to 5.5 V unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ.	Max	Unit
IRED operating current		I_D	250	300	350	mA
IRED forward voltage	I_r = 300 mA	V_f	1.4	1.8	1.9	V
IRED leakage current	TXD = 0 V, 0 < V_{CC} < 5.5 V	I_{IRED}	- 1		1	µA
Output radiant intensity	α = 0°, 15°, TXD = High, SD = Low	I_e	40	70	350	mW/sr
	V_{CC} = 5.0 V, α = 0°, 15°, TXD = High or SD = High (Receiver is inactive as long as SD = High)	I_e			0.04	mW/sr
Output radiant intensity, angle of half intensity		α		± 24		°
Peak-emission wavelength		λ_p	880		900	nm
Spectral bandwidth		Δλ		45		nm
Optical rise time		t_{ropt}	10		100	ns
Optical fall time		t_{fopt}	10		100	ns
Optical output pulse duration	Input pulse width 1.63 µs, 115.2 kbit/s	t_{opt}	1.46	1.63	1.8	µs
	Input pulse width t_{TXD} < 20 µs	t_{opt}	t_{TXD}		t + 0.15	µs
	Input pulse width t_{TXD} ≥ 20 µs	t_{opt}			50	µs
Optical overshoot					25	%

Recommended Solder Profiles

Solder Profile for Sn/Pb soldering

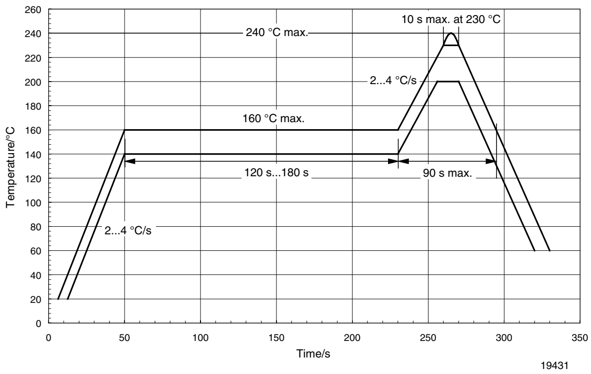


Figure 1. Recommended Solder Profile for Sn/Pb soldering

Lead (Pb)-Free, Recommended Solder Profile

The TFBS4710 is a lead (Pb)-free transceiver and qualified for lead (Pb)-free processing. For lead (Pb)-free solder paste like Sn(3.0-4.0)Ag(0.5-0.9)Cu, there are two standard reflow profiles: Ramp-Soak-Spike (RSS) and Ramp-To-Spike (RTS). The Ramp-Soak-Spike profile was developed primarily for reflow ovens heated by infrared radiation. With widespread use of forced convection reflow ovens the Ramp-To-Spike profile is used increasingly. Shown below in figure 2 is VISHAY's recommended profiles for use with the TFBS4710 transceivers. For more details please refer to Application note: SMD Assembly Instruction.

Wave Soldering

For TFDUxxxx and TFBSxxxx transceiver devices wave soldering is not recommended.

Manual Soldering

Manual soldering is the standard method for lab use. However, for a production process it cannot be recommended because the risk of damage is highly dependent on the experience of the operator. Nevertheless, we added a chapter to the above mentioned application note, describing manual soldering and desoldering.

Storage

The storage and drying processes for all VISHAY transceivers (TFDUxxxx and TFBSxxx) are equivalent to MSL4.

The data for the drying procedure is given on labels on the packing and also in the application note "Taping, Labeling, Storage and Packing" (http://www.vishay.com/docs/82601/82601.pdf).

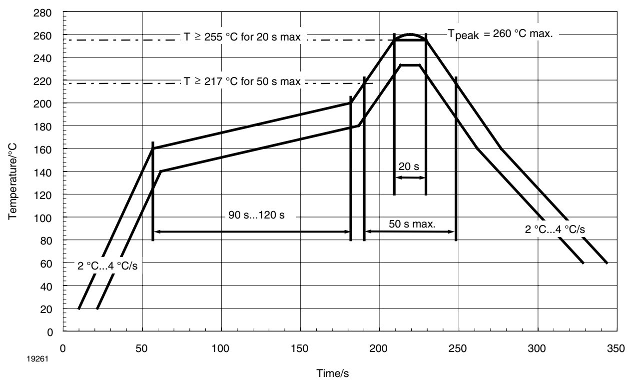


Figure 2. Solder Profile, RSS Recommendation

Recommended Circuit Diagram

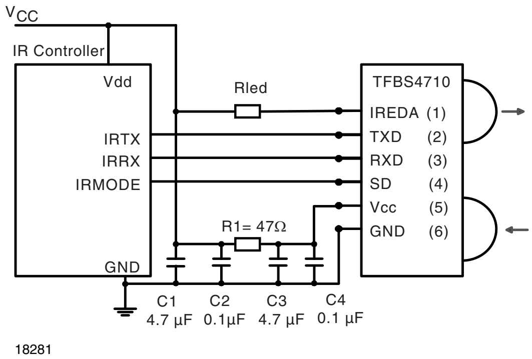


Figure 3. Recommended Application Circuit

The TFBS4710 integrates a sensitive receiver and a built-in power driver. This combination needs a careful circuit layout. The use of thin, long, resistive and inductive wiring should be avoided. The inputs (TXD, SD) and the output (RXD) should be directly (DC) coupled to the I/O circuit.

The combination of resistor R1 and capacitors C1, C2, C3 and C4 filter out any power supply noise to provide a smooth supply voltage.

The placement of these components is critical. It is strongly recommended to position C3 and C4 as close as possible to the transceiver power supply pins. A Tantalum capacitor should be used for C1 and C3 while a ceramic capacitor should be used for C2 and C4.

A current limiting resistor is not needed for normal operation. It is strongly recommended to use the Rled values mentioned in Table 1 below for high temperature operation. For Low Power Mode, IRED Anode voltage of less than 5 V is recommended.

Under extreme EMI conditions as placing a RF - transmitter antenna on top of the transceiver, it is recommended to protect all inputs by a low-pass filter, as a minimum a 12 pF capacitor, especially at the RXD port.

Basic RF design rules for circuit design should be followed. Especially longer signal lines should not be used without proper termination. For reference see "The Art of Electronics" by Paul Horowitz, Winfield Hill, 1989, Cambridge University Press, ISBN: 0521370957.

Table 1.
High Operating Temperature > 70 °C

	Rled (Ω)	Rled (Ω)
V_{LED} (V)	Standard Power Mode (Intensity > 40 mW/sr, 0° - 15°)	Low Power Mode (Intensity > 3.6 mW/sr, 0° - 15°)
2.7	3	50
3.3	6	> 50
5.0	18	> 60

I/O and Software

In the description, already different I/Os are mentioned. Different combinations are tested and the function verified with the special drivers available from the I/O suppliers. In special cases refer to the I/O manual, the Vishay application notes, or contact directly Vishay Sales, Marketing or Application.

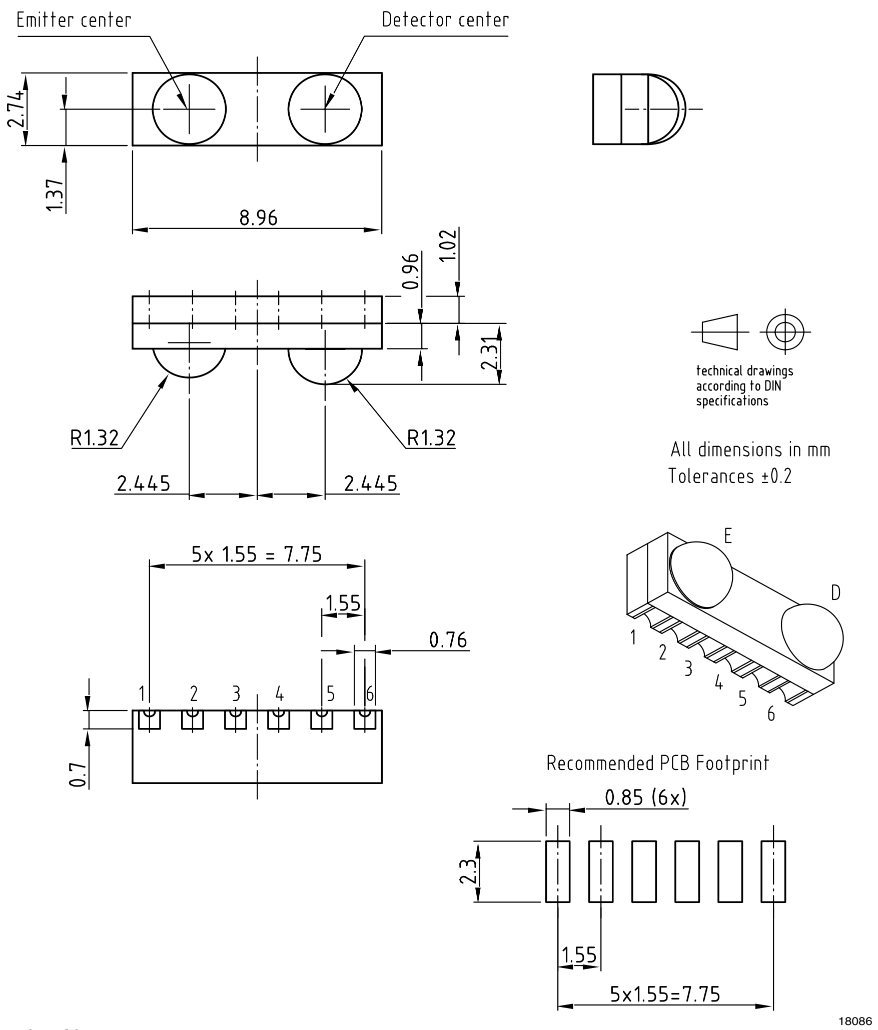
Table 2.
Recommended Application Circuit Components

Component	Recommended Value	Vishay Part Number
C1, C3	4.7 µF, 16 V	293D 475X9 016B
C2, C4	0.1 µF, Ceramic	VJ 1206 Y 104 J XXMT
R1	47 Ω, 0.125 W	CRCW-1206-47R0-F-RT1
Rled	See Table 1	

Table 3.
Truth table

Inputs			Outputs		Remark
SD	TXD	Optical input Irradiance mW/m^2	RXD	Transmitter	Operation
high > 1 ms	x	x	weakly pulled (500 Ω) to V_{CC1}	0	Shutdown
low	high	x	high inactive	I_e	Transmitting
	high > µs	x	high inactive	0	Protection is active
	low	< 4	high inactive	0	Ignoring low signals below the IrDA defined threshold for noise immunity
	low	> Min. Detection Threshold Irradiance < Max. Detection Threshold Irradiance	low (active)	0	Response to an IrDA compliant optical input signal
	low	> Max. Detection Threshold Irradiance	undefined	0	Overload conditions can cause unexpected outputs

Package Dimensions



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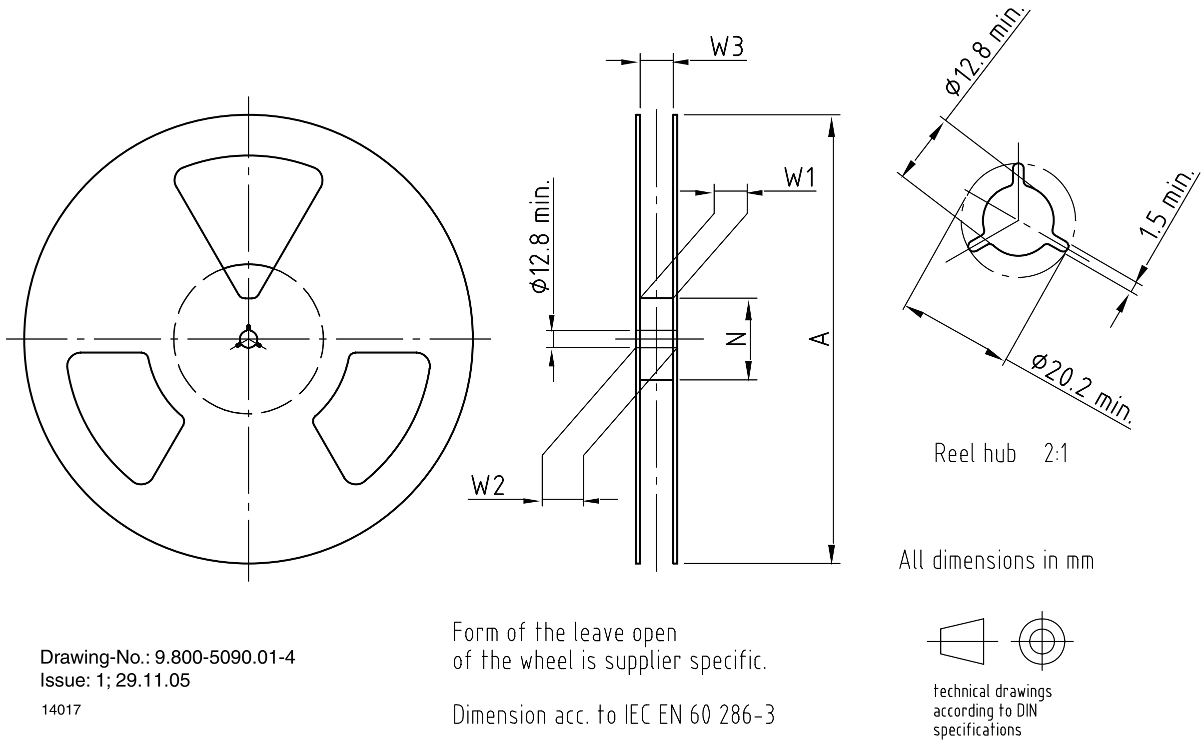
Issue: 1; 24.06.03

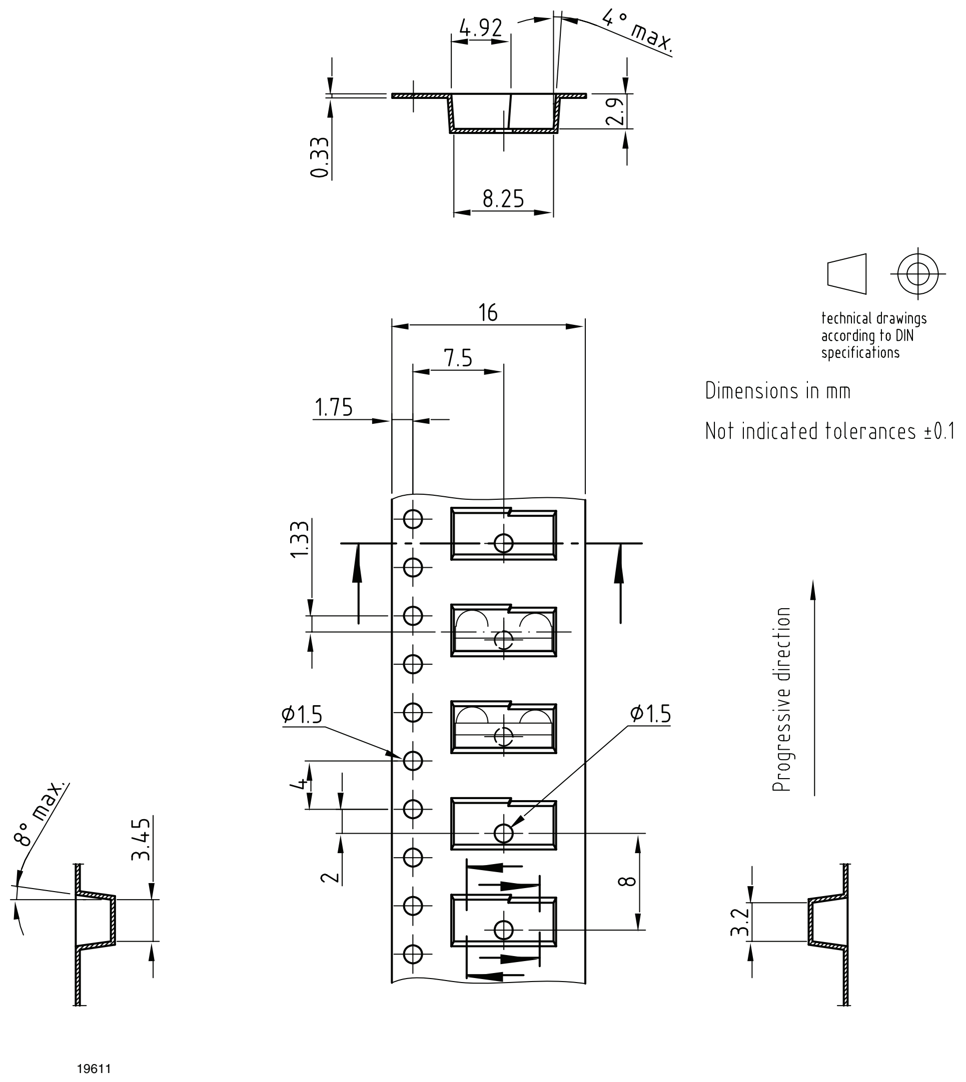
Figure 4. Package drawing TFBS4710

Reel Dimensions



Tape Width	A max.	N	W_1 min.	W_2 max.	W_3 min.	W_3 max.
mm	mm	mm	mm	mm	mm	mm
16	330	50	16.4	22.4	15.9	19.4

Tape Dimensions



Drawing-No.: 9.700-5299.01-4
Issue: 1; 18.08.05

Figure 5. Tape drawing for TFBS4710 for side view mounting

Ozone Depleting Substances Policy Statement

It is the policy of Vishay Semiconductor GmbH to

1. Meet all present and future national and international statutory requirements.
2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Vishay Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively
2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA
3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Vishay Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

We reserve the right to make changes to improve technical design and may do so without further notice.

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