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Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Previous Revision: 2.9	
Revision 3.0, 2010-12-28	
all	Converted into structured FrameMaker (EDD 3.4)
4-3	More detailed explanation of AGC
5-6, 5-8	More detailed information of LNA high gain mode and LNA low gain mode

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1 Product Info

General Description

The IC is a very low power consumption single chip ASK Single Conversion Receiver for receive frequencies bands 868-870 MHz and 433-435 MHz. The IC offers a high level of integration and needs only a few external components. The device contains a low noise amplifier (LNA), a double balanced mixer, a fully integrated VCO, a PLL synthesizer, a crystal oscillator, a limiter with RSSI generator, a data filter, a data comparator (slicer) and a peak detector. Additionally there is a power down feature to save battery life.

Features

- Low supply current (I_s = 4.8 mA typ. at 868 MHz, I_s = 4.6 mA typ. at 434 MHz)
- Supply voltage range 5 V ±10 %
- Power down mode with very low supply current (50 nA typ)
- Fully integrated VCO and PLL Synthesizer
- RF input sensitivity < – 107 dBm
- Selectable frequency ranges around 868-870 MHz and 433-435 MHz
- Selectable reference frequency
- Limiter with RSSI generation, operating at 10.7 MHz
- 2nd order low pass data filter with external capacitors
- Data slicer with self-adjusting threshold

Application

- Keyless Entry Systems
- Remote Control Systems
- Alarm Systems
- Low Bitrate Communication Systems

Package

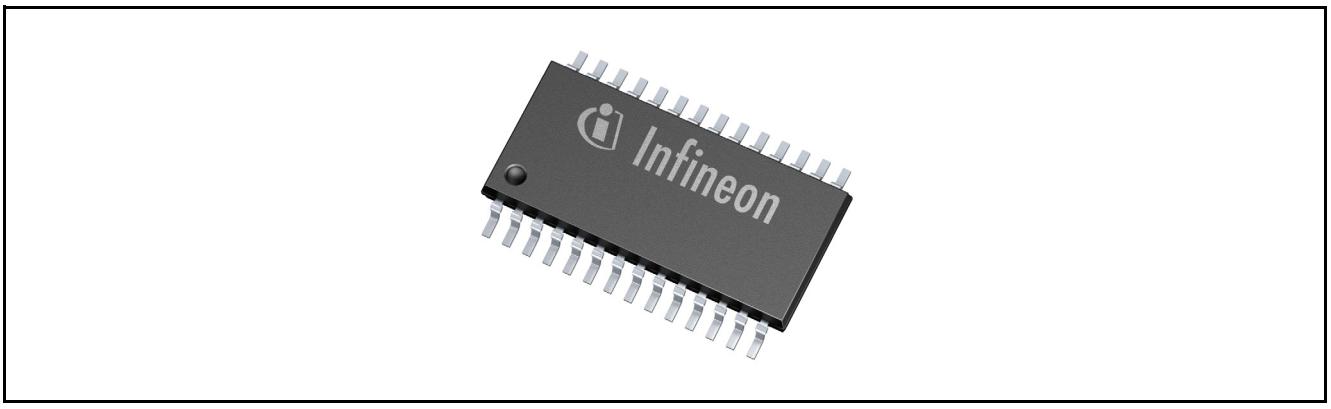

Figure 1 PG-TSSOP-28

Ordering Information

Type	Ordering Code	Package[1)]
TDA5200	SP000016381	PG-TSSOP-28

1) Available on tape and reel

2 Product Description

2.1 Overview

The IC is a very low power consumption single chip ASK Superheterodyne Receiver (SHR) for the frequency bands 868-870 MHz and 433-435 MHz. The IC offers a high level of integration and needs only a few external components. The device contains a low noise amplifier (LNA), a double balanced mixer, a fully integrated VCO, a PLL synthesizer, a crystal oscillator, a limiter with RSSI generator, a data filter, a data comparator (slicer) and a peak detector. Additionally there is a power down feature to save battery life.

2.2 Application

- Keyless Entry Systems
- Remote Control Systems
- Alarm Systems
- Low Bitrate Communication Systems

2.3 Features

- Low supply current (I_s = 4.8 mA typ. at 868 MHz, I_s = 4.6 mA typ. at 434 MHz)
- Supply voltage range 5 V ±10 %
- Power down mode with very low supply current (100 nA typ.)
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- RF input sensitivity < – 107 dBm
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- Selectable reference frequency
- Limiter with RSSI generation, operating at 10.7 MHz
- 2nd order low pass data filter with external capacitors
- Data slicer with self-adjusting threshold

2.4 Package Outlines

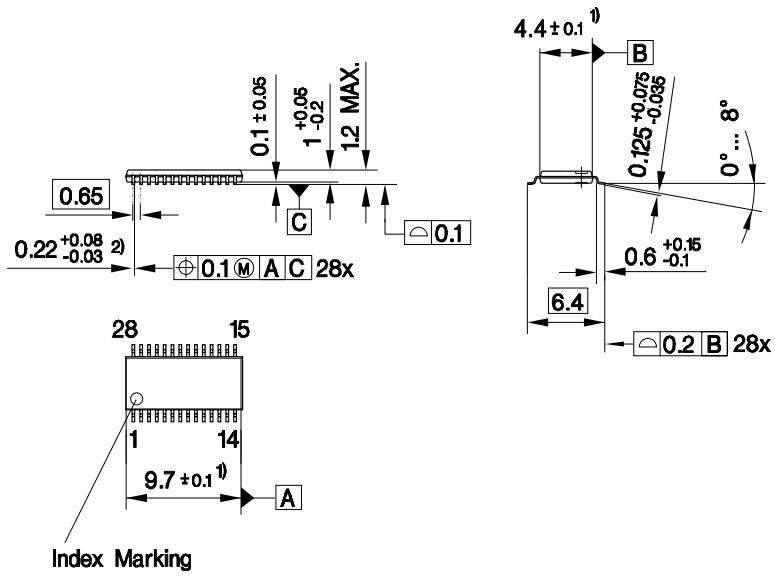


Figure 2 PG-TSSOP-28 Package Outlines

3 Functional Description

3.1 Pin Configuration

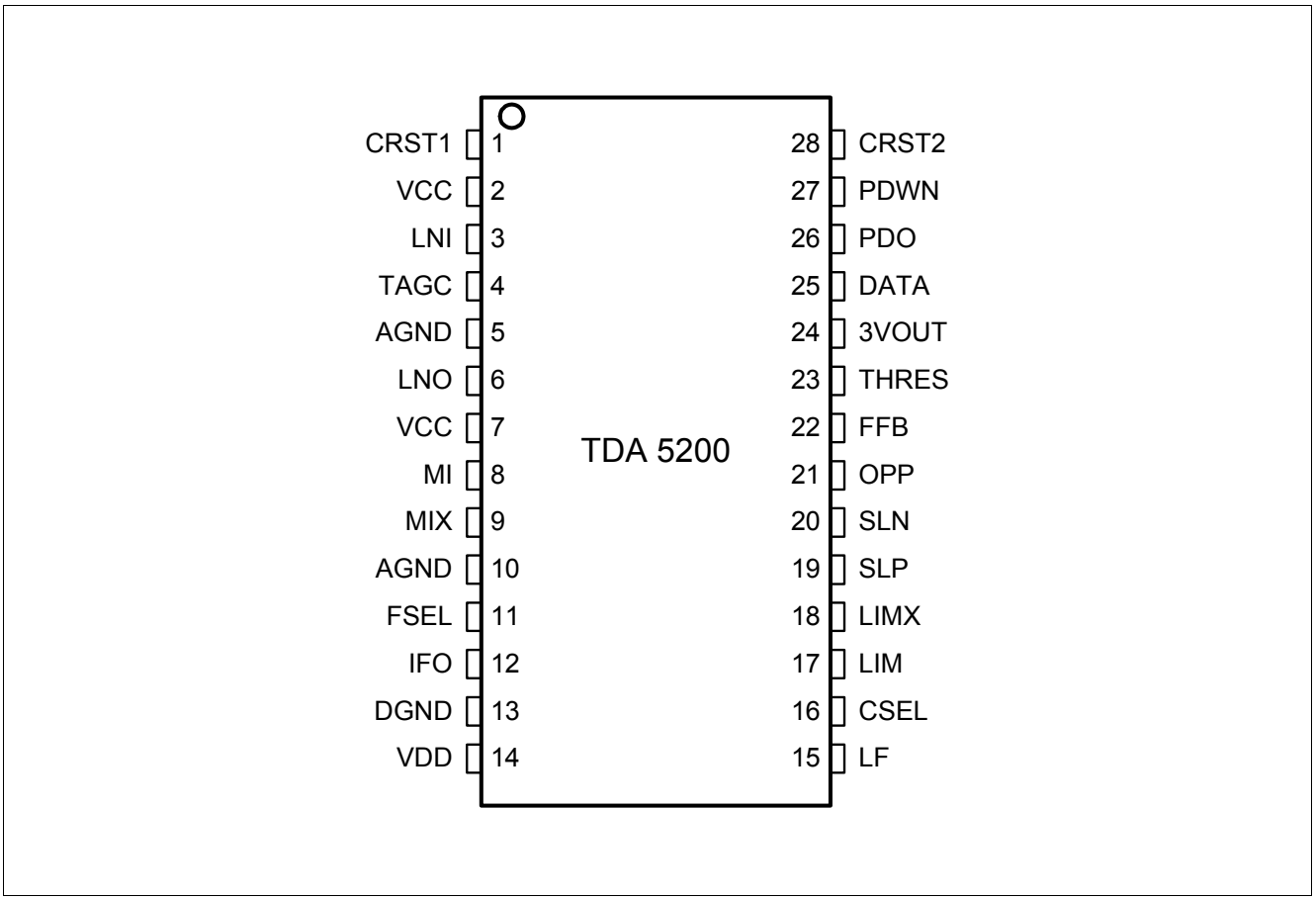


Figure 3 IC Pin Configuration

3.2 Pin Definition and Function

Table 1 Pin Definition and Function

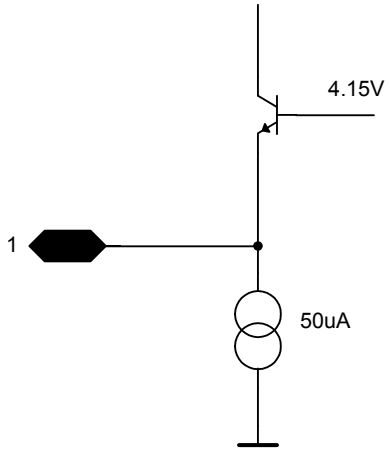
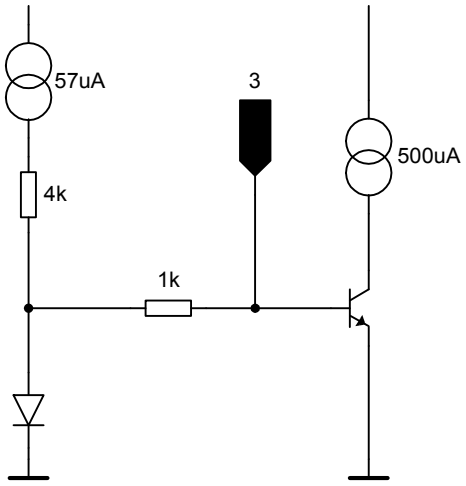
Pin No.	Name	Pin Type	Buffer Type	Function
1	CRST1	In/Out		**External Crystal Connector 1**
2	VCC	In		**5 V Supply**
3	LNI	In		**LNA Input**

Table 1 Pin Definition and Function (cont'd)

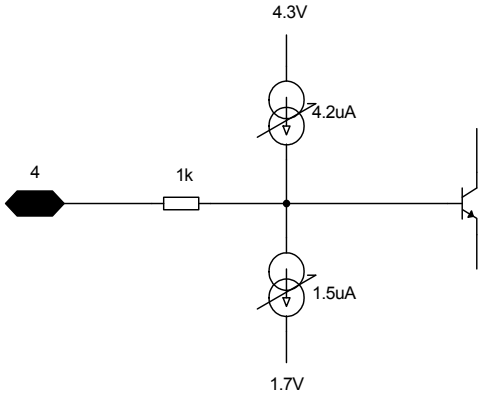
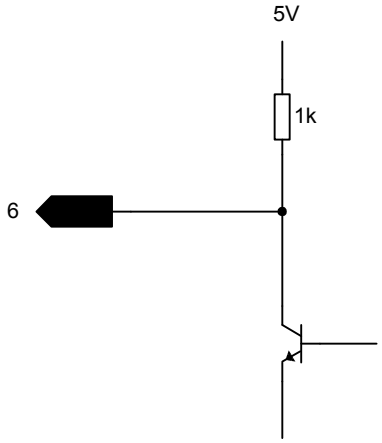
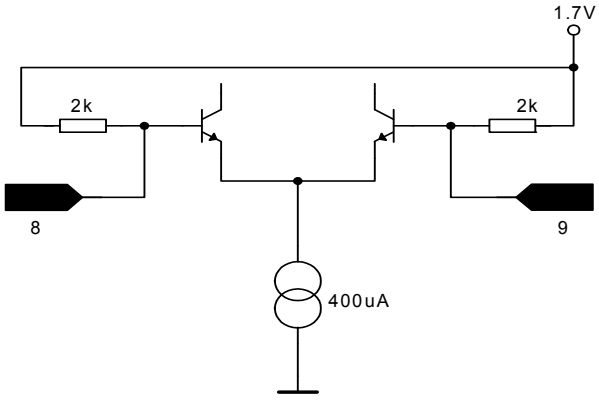
Pin No.	Name	Pin Type	Buffer Type	Function
4	TAGC	In/Out		**AGC Time Constant Control**
5	AGND	In		**Analogue Ground Return**
6	LNO	Out		**LNA Output**
7	VCC	In		**5 V Supply**
8	MI	In		**Mixer Input**

Table 1 Pin Definition and Function (cont'd)

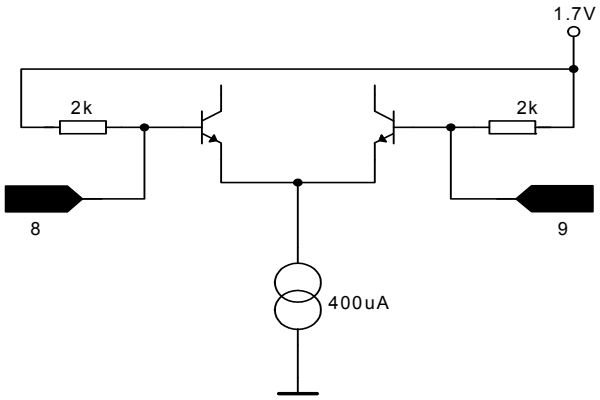
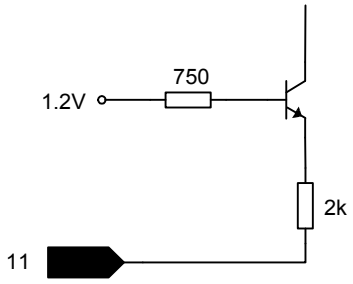
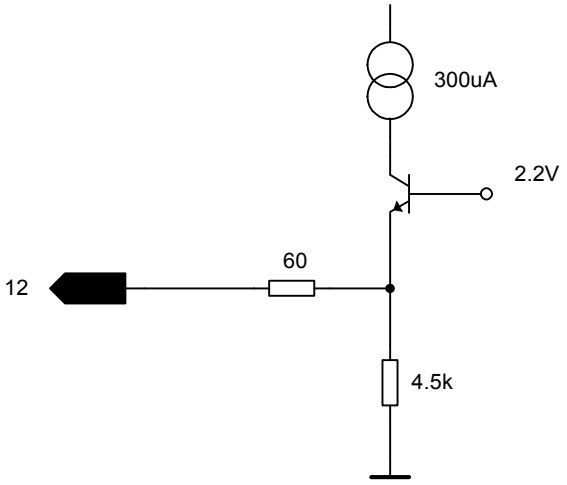
Pin No.	Name	Pin Type	Buffer Type	Function
9	MIX	In		**Complementary Mixer Input**
10	AGND	In		**Analogue Ground Return**
11	FSEL	In		**Operating Frequency Selector** 869/434 MHz
12	IFO	Out		**IF Mixer Output** 10.7 MHz
13	DGND	In		**Digital Ground Return**
14	VDD	In		**5 V Supply** PLL Counter Circuitry

Table 1 Pin Definition and Function (cont'd)

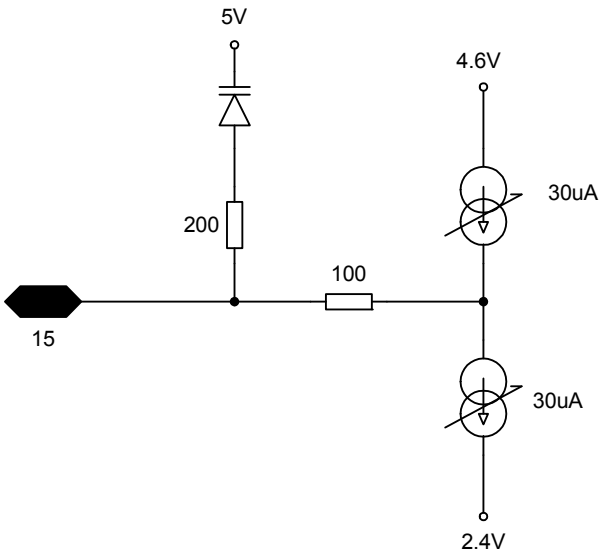
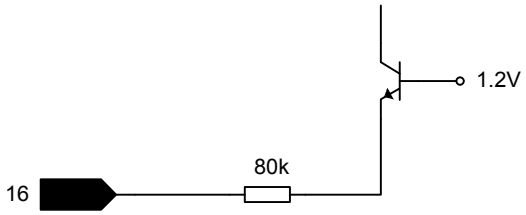
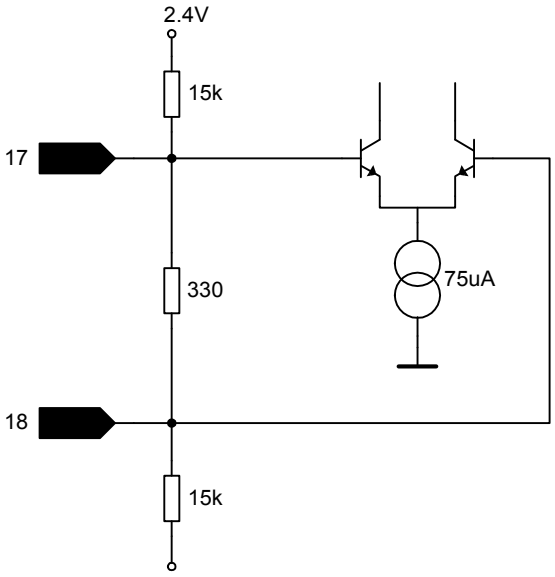
Pin No.	Name	Pin Type	Buffer Type	Function
15	LF	In/Out		**PLL Filter Access Point**
16	CSEL	In		**Quartz Selector** 6.xx MHz or 13.xx MHz
17	LIM	In		**Limiter Input**

Table 1 Pin Definition and Function (cont'd)

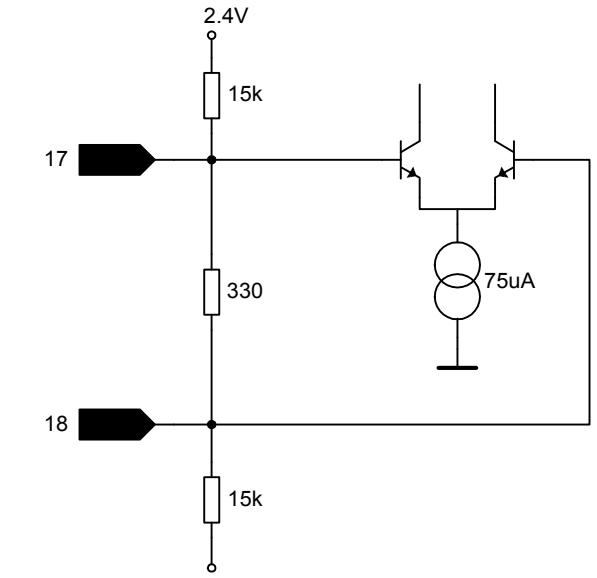
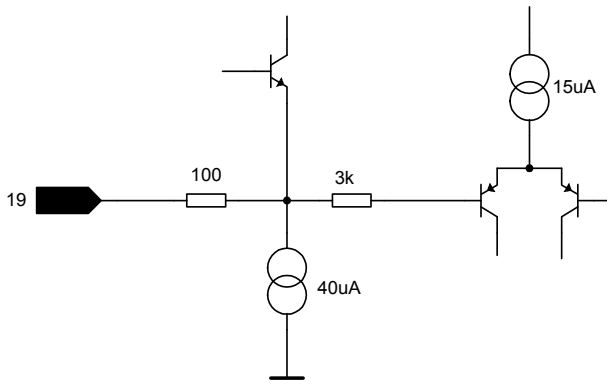
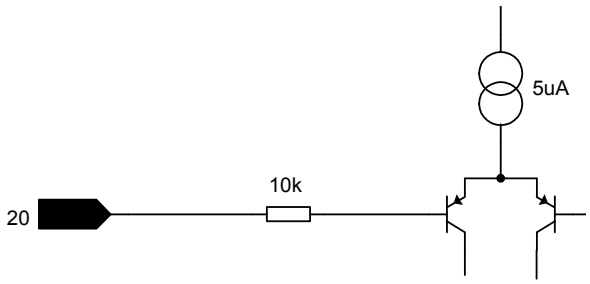
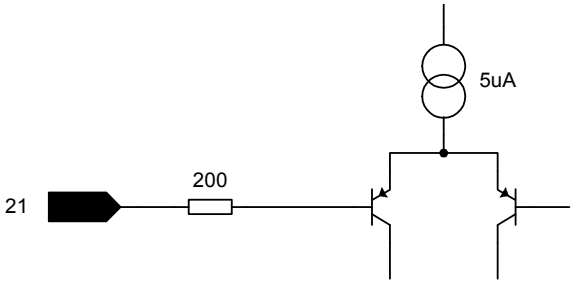
Pin No.	Name	Pin Type	Buffer Type	Function
18	LIMX	In		**Complementary Limiter Input**
19	SLP	In		**Data Slicer Positive Input**
20	SLN	In		**Data Slicer Negative Input**
21	OPP	In		**OpAmp Noninverting Input**

Table 1 Pin Definition and Function (cont'd)

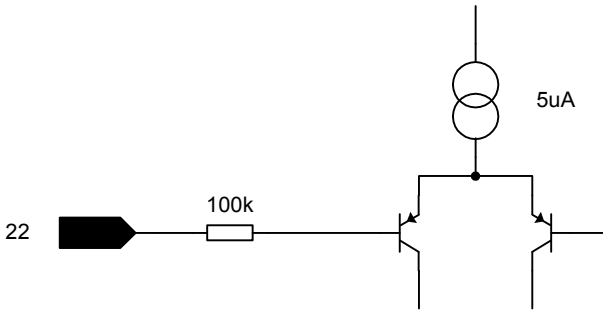
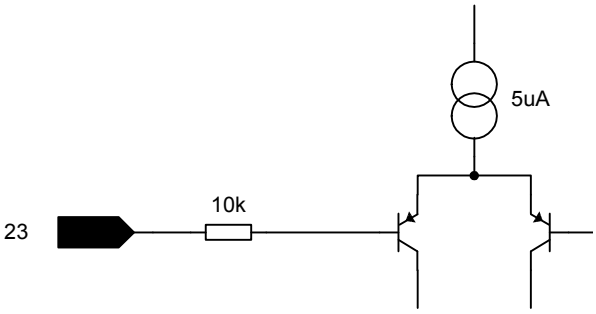
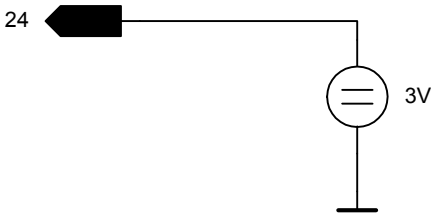
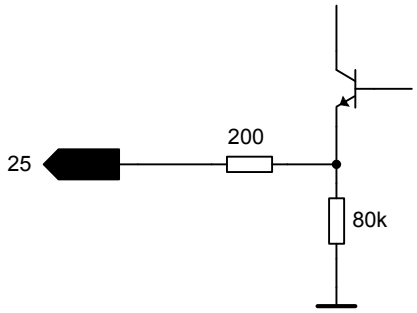
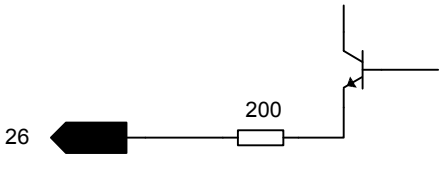
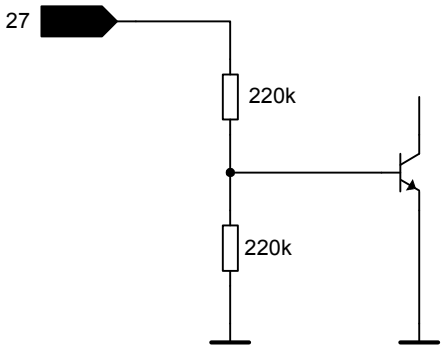
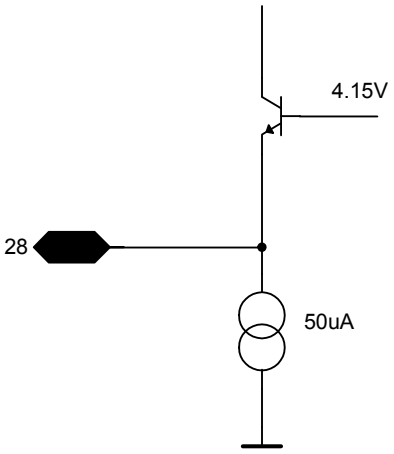
Pin No.	Name	Pin Type	Buffer Type	Function
22	FFB	In		**Data Filter Feedback Pin**
23	THRES	In		**AGC Threshold Input**
24	3VOUT	Out		**3 V Reference Output**
25	DATA	Out		**Data Output**
26	PDO	Out		**Peak Detector Output**

Table 1 Pin Definition and Function (cont'd)

Pin No.	Name	Pin Type	Buffer Type	Function
27	PDWN	In		**Power Down Input**
28	CRST2	In/Out		**External Crystal Connector 2**

3.3 Functional Block Diagram

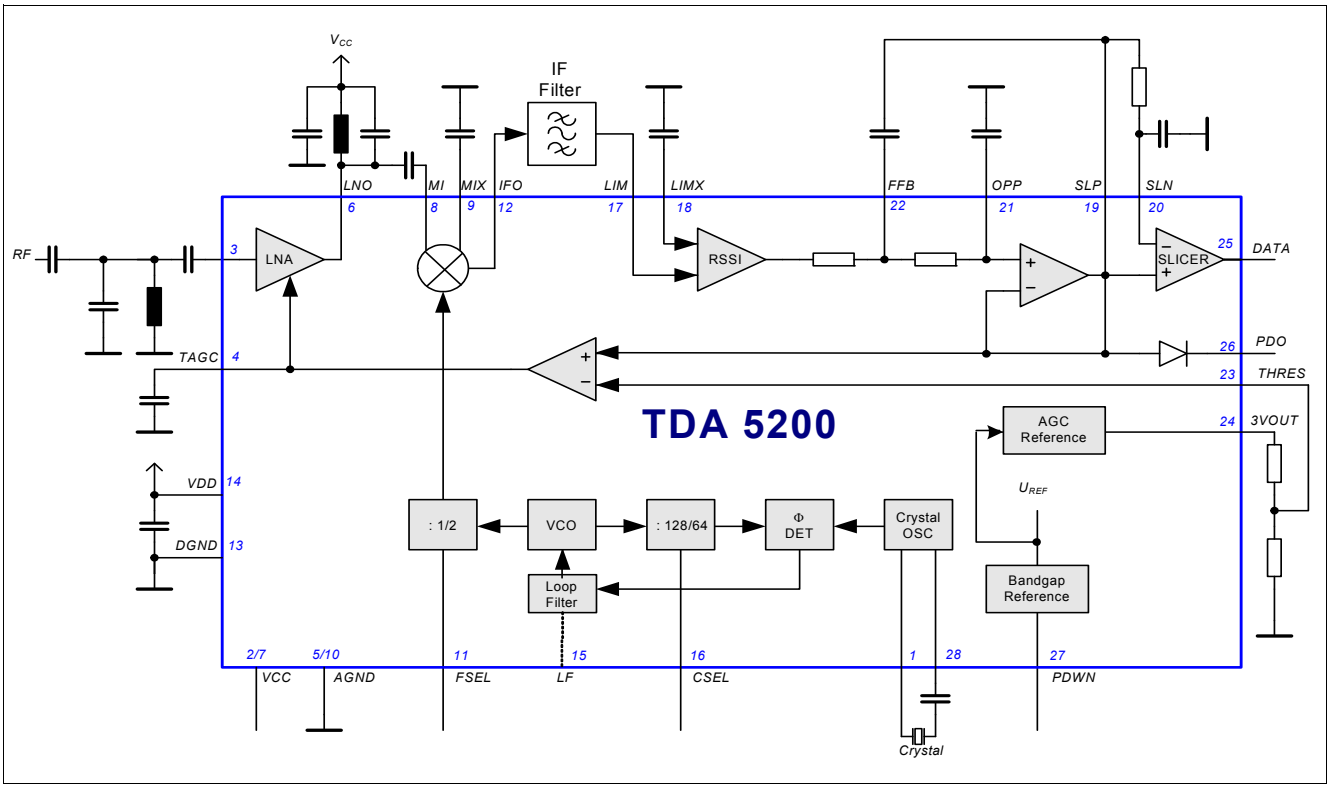


Figure 4 Main Block Diagram

3.4 Functional Blocks

3.4.1 Low Noise Amplifier (LNA)

The LNA is an on-chip cascode amplifier with a voltage gain of 15 dB to 20 dB. The gain figure is determined by the external matching networks situated ahead of LNA and between the LNA output **LNO** (Pin 6) and the Mixer Inputs **MI** and **MIX** (Pin 8 and Pin 9). The noise figure of the LNA is approximately 3.2 dB, the current consumption is 500 µA. The gain can be reduced by approximately 18 dB. The switching point of this AGC action can be determined externally by applying a threshold voltage at the **THRES** pin (Pin 23). This voltage is compared internally with the received signal (RSSI) level generated by the limiter circuitry. In case that the RSSI level is higher than the threshold voltage the LNA gain is reduced and vice versa. The threshold voltage can be generated by attaching a voltage divider between the **3VOUT** pin (Pin 24) which provides a temperature stable 3 V output generated from the internal bandgap voltage and the **THRES** pin as described in **Chapter 4.1**. The time constant of the AGC action can be determined by connecting a capacitor to the **TAGC** pin (Pin 4) and should be chosen along with the appropriate threshold voltage according to the intended operating case and interference scenario to be expected during operation. The optimum choice of AGC time constant and the threshold voltage is described in **Chapter 4.1**.

3.4.2 Mixer

The Double Balanced Mixer down-converts the input frequency (RF) in the range of 433-435 MHz / 868-870 MHz to the intermediate frequency (IF) at 10.7 MHz with a voltage gain of approximately 21 dB. A low pass filter with a corner frequency of 20 MHz is built on chip in order to suppress RF signals to appear at the IF output (IFO pin). The IF output is internally consisting of an emitter follower that has a source impedance of approximately 330 Ω to facilitate interfacing the pin directly to a standard 10.7 MHz ceramic filter without additional matching circuitry.

3.4.3 PLL Synthesizer

The Phase Locked Loop synthesizer consists of a VCO, an asynchronous divider chain, a phase detector with charge pump and a loop filter and is fully implemented on-chip. The VCO is including spiral inductors and varactor diodes. It's nominal centre frequency is 840 MHz. No additional components are necessary.
Local oscillator high side injection has to be used for receive frequencies below approximately 420 MHz or 840 MHz, low side injection for receive frequencies above approximately 420 MHz or 840 MHz - see also **Chapter 4.4**. Therefore low-side injection of the local oscillator has to be used for operation both in the 868 MHz and the 434 MHz ISM bands.
The oscillator signal is fed both to the synthesizer divider chain and to the down-converting mixer. In case of operation in the 433-435 MHz range, the signal is divided by two before it is fed to the mixer. This is controlled by the selection pin FSEL (Pin 11) as described in the following table. The overall division ratio of the divider chain can be selected to be either 128 or 64, depending on the frequency of the reference oscillator quartz (see below). The loop filter is also realized fully on-chip.

Table 2 FSEL Pin Operating States

FSEL	RF Frequency
Open	433-435 MHz
Shorted to ground	868-870 MHz

3.4.4 Crystal Oscillator

The on-chip crystal oscillator circuitry allows for utilization of quartzes both in the 6 MHz and 13 MHz range as the overall division ratio of the PLL can be switched between 64 and 128 via the **CSEL** (Pin 16) pin according to the following table.

Table 3 CSEL Pin Operating States

CSEL	Crystal Frequency
Open	6.xx MHz
Shorted to ground	13.xx MHz

The calculation of the value of the necessary quartz load capacitance is shown in **Chapter 4.3**, the quartz frequency calculation is explained in **Chapter 4.4**.

3.4.5 Limiter

The Limiter is an AC coupled multistage amplifier with a cumulative gain of approximately 80 dB that has a bandpass-characteristic centered around 10.7 MHz. It has an input impedance of 330 Ω to allow for easy interfacing to a 10.7 MHz ceramic IF filter. The limiter circuit acts as a Receive Signal Strength Indicator (RSSI) generator which produces a DC voltage that is directly proportional to the input signal level as can be seen in **Figure 6**. This signal is used to demodulate the ASK receive signal in the subsequent baseband circuitry and to turn down the LNA gain by approximately 17 dB in case the input signal strength is too strong as described in **Chapter 3.4.1** and **Chapter 4.1**.

3.4.6 Data Filter

The data filter comprises an OP-Amp with a bandwidth of 100 kHz used as a voltage follower and two 100 kΩ on-chip resistors. Along with two external capacitors a 2nd order Sallen-Key low pass filter is formed. The selection of the capacitor values is described in **Chapter 4.2**.

3.4.7 Data Slicer

The data slicer is a fast comparator with a bandwidth of 100 kHz. This allows for a maximum receive data rate of approximately 120 kBaud. The maximum achievable data rate also depends on the IF Filter bandwidth and the local oscillator tolerance values. Both inputs are accessible. The output delivers a digital data signal (CMOS-like levels) for the detector. The self-adjusting threshold on pin 20 is generated by RC-term or peak detector depending on the baseband coding scheme. The data slicer threshold generation alternatives are described in more detail in **Chapter 4.5**.

3.4.8 Peak Detector

The peak detector generates a DC voltage which is proportional to the peak value of the receive data signal. An external RC network is necessary. The output can be used as an indicator for the signal strength and also as a reference for the data slicer. The maximum output current is 500 µA.

3.4.9 Bandgap Reference Circuitry

A Bandgap Reference Circuit provides a temperature stable reference voltage for the device. A power down mode is available to switch off all sub-circuits which is controlled by the PWDN pin (Pin 27) as shown in the following table. The supply current drawn in this case is typically 50 nA.

Table 4 PDWN Pin Operating States

PDWN	Operating State
Open or tied to ground	Power Down Mode
Tied to V_{CC}	Receiver On

4 Applications

4.1 Choice of LNA Threshold Voltage and Time Constant

In the following figure the internal circuitry of the LNA automatic gain control is shown.

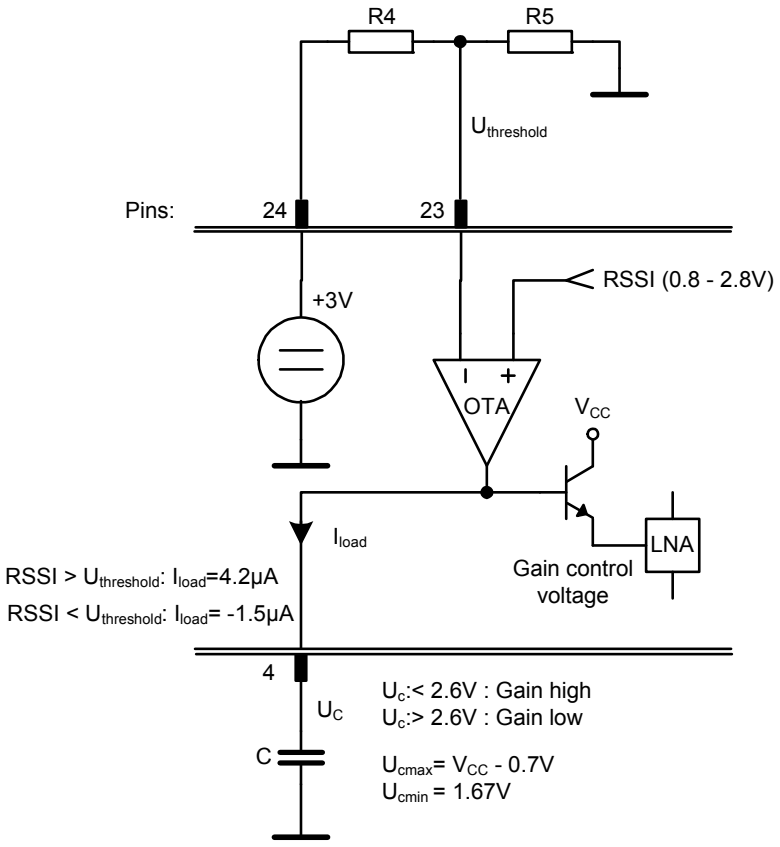


Figure 5 LNA Automatic Gain Control Circuitry

The LNA automatic gain control circuitry consists of an operational transimpedance amplifier that is used to compare the received signal strength signal (RSSI) generated by the Limiter with an externally provided threshold voltage U_{thres}. As shown in the following figure the threshold voltage can have any value between approximately typically 0.8 V and 2.8 V to provide a switching point within the receive signal dynamic range.

This voltage U_{thres} is applied to the **THRES** pin (Pin 23). The threshold voltage can be generated by attaching a voltage divider between the **3VOUT** pin (Pin 24) which provides a temperature stable 3 V output generated from the internal bandgap voltage and the **THRES** pin. If the RSSI level generated by the Limiter is higher than U_{thres}, the OTA generates a positive current I_{load}. This yields a voltage rise on the **TAGC** pin (Pin 4). Otherwise, the OTA generates a negative current. These currents do not have the same values in order to achieve a fast-attack and slow-release action of the AGC and are used to charge an external capacitor which finally generates the LNA gain control voltage.

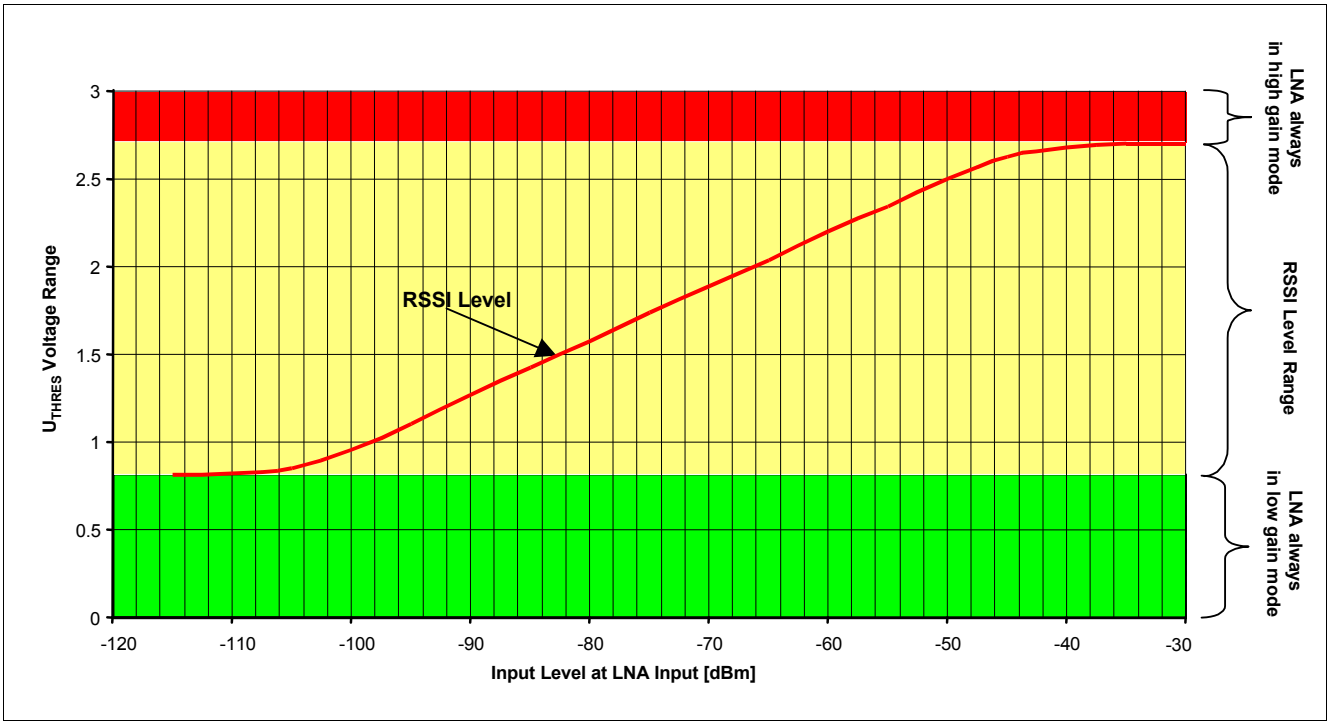


Figure 6 Typical Curve of RSSI Level and Permissive AGC Threshold Levels

The switching point should be chosen according to the intended operating scenario. The determination of the optimum point is described in the accompanying Application Note, a threshold voltage level of 1.8 V is apparently a viable choice. It should be noted that the output of the 3VOUT pin is capable of driving up to 50 µA, but that the THRES pin input current is only in the region of 40 nA. As the current drawn out of the 3VOUT pin is directly related to the receiver power consumption, the power divider resistors should have high impedance values. R4 can be chosen as 120 kΩ, R5 as 180 kΩ to yield an overall 3VOUT output current of 10 µA.

Notes

1. *To keep the LNA in high gain mode for the complete RF-input level range a voltage equal or higher than 3.3 V has to be applied at pin 23. Alternatively, pin 23 has to be connected to pin 24 and pin 4 has to be connected to GND. In addition this would save an external capacitor.*
2. *To keep the LNA in low gain mode for the complete RF-input level range a voltage lower than 0.7 V has to be applied to the THRES pin (e.g. THRES connected to GND). In the above-mentioned mode pin 4 has to be connected by a capacitor to GND.*
3. *As stated above, the gain control voltage of the LNA is generated at the capacitor connected to the TAGC pin by the charging and discharging currents of the OTA. Consequently this capacitor is responsible for the AGC time constant. As the charging and discharging currents are not equal two different time constants will result. The time constant corresponding to the charging process of the capacitor shall be chosen according to the data rate. According to measurements performed at Infineon the capacitor value should be greater than 47 nF.*

4.2 Data Filter Design

Utilizing the on-board voltage follower and the two 100 kΩ on-chip resistors a 2nd order Sallen-Key low pass data filter can be constructed by adding 2 external capacitors between pin 19 (SLP) and pin 22 (FFB) and to pin 21 (OPP) as depicted in the following figure and described in the following formulas[1].

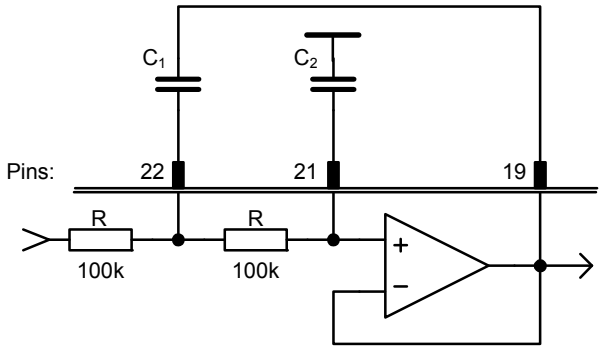


Figure 7 Data Filter Design

$$C1 = \frac{2Q\sqrt{b}}{R2\Pi f_{3dB}} \quad (1)$$

$$C2 = \frac{\sqrt{b}}{4QR\Pi f_{3dB}} \quad (2)$$

with

$$Q = \frac{\sqrt{b}}{a} \quad (3)$$

the quality factor of the poles where

in case of a **Bessel** filter a = 1.3617, b = 0.618

and thus Q = 0.577

and in case of a **Butterworth** filter a = 1.141, b = 1

and thus Q = 0.71

Example

Butterworth filter with f_{3dB} = 5 kHz and R = 100 kΩ

C_1 = 450 pF, C_2 = 225 pF

1) Taken from Tietze/Schenk: Halbleiterschaltungstechnik, Springer Berlin, 1999

4.3 Quartz Load Capacitance Calculation

The value of the capacitor necessary to achieve that the quartz oscillator is operating at the intended frequency is determined by the reactive part of the negative resistance of the oscillator circuit as shown in **Chapter 5.1.3** and by the quartz specifications given by the quartz manufacturer.

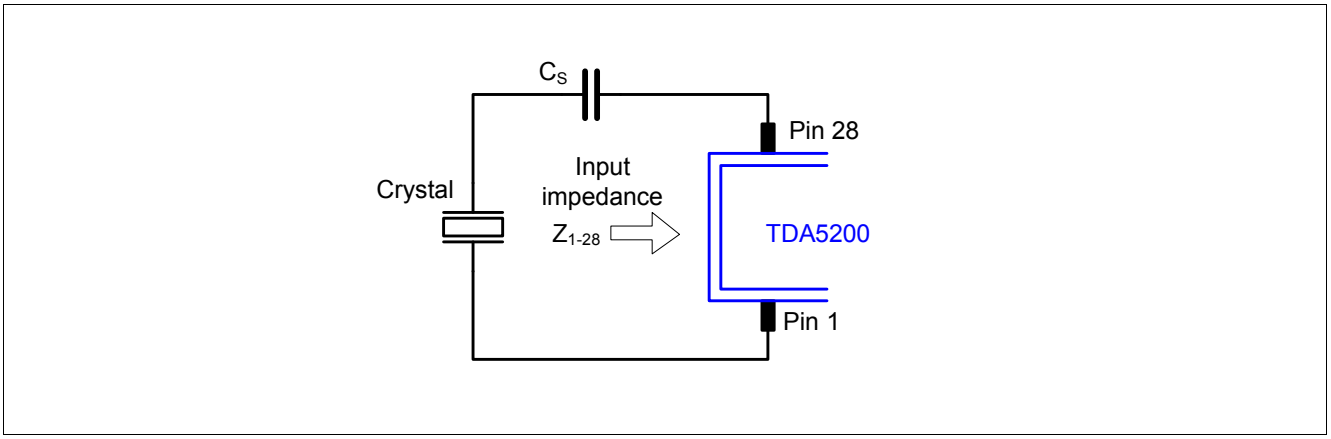


Figure 8 Determination of Series Capacitance Value for the Quartz Oscillator

Crystal specified with load capacitance

$$C_S = \frac{1}{\frac{1}{C_L} + 2\pi f X_L} \quad (4)$$

with C_L the load capacitance (refer to the quartz crystal specification).

Examples

6.7 MHz	C_L = 12 pF	X_L = 750 Ω	C_S = 8.7 pF
13.401 MHz	C_L = 12 pF	X_L = 1250 Ω	C_S = 5.3 pF

These values may be obtained in high accuracy by putting two capacitors in series to the quartz, such as 20 pF and 15 pF in the 6.7 MHz case and 15 pF and 8.2 pF in the 13.401 MHz case.

But please note that the calculated value of C_S includes the parasitic capacitors also.

4.4 Quartz Frequency Calculation

As described in **Chapter 3.4.3**, the operating range of the on-chip VCO is 820 MHz to 860 MHz with a nominal center frequency of approximately 840 MHz. This signal is divided by 2 before applied to the mixer in case of operation at 434 MHz. This local oscillator signal can be used to down-convert the RF signals both with high- or low-side injection at the mixer. The resulting receive frequency ranges then extend between 810 MHz and 870 MHz or between 400 MHz and 440 MHz. Low-side injection of the local oscillator has to be used for receive frequencies between 840 MHz and 870 MHz as well as high-side injection for receive frequencies below 840 MHz. Corresponding to that in the 400 MHz region low-side injection is applicable for receive frequencies above 420 MHz, high-side injection below this frequency. Therefore for operation both in the 868 MHz and the 434 MHz ISM bands low-side injection of the local oscillator has to be used. Then the local oscillator frequency is calculated by subtracting the IF frequency (10.7 MHz) from the RF frequency (434 MHz or 868 MHz). The overall division ratios in the PLL are 64 or 128 in case of operation at 868 MHz or 32 and 64 in case of operation at 434 MHz, depending on the crystal frequency used as shown below.

Therefore, the quartz frequency is calculated by using the following formula:

$$f_{QU} = \frac{f_{RF} \pm 10.7}{r} \tag{5}$$

with

f_{RF} Receive frequency
f_{LO} Local oscillator (PLL) frequency (f_{RF} ± 10.7)
f_{QU} Quartz oscillator frequency
r Ratio of local oscillator (PLL) frequency and quartz frequency as shown in the subsequent table

Table 5 PLL Division Ratio Dependence on States of CSEL

FSEL	CSEL	Ratio r = (f_{LO}/f_{QU})
Open	Open	64
Open	GND	32
GND	Open	128
GND	GND	64

Subtraction of 10.7 occurs in case the receive frequency is higher than the intended local oscillator frequency, addition in case the receive frequency lies below the local oscillator frequency.

Example

$$f_{QU} = (868.4MHz - 10.7MHz)/64 = 13.40156MHz \tag{6}$$

$$f_{QU} = (868.4MHz - 10.7MHz)/128 = 6.7008MHz \tag{7}$$

$$f_{QU} = (434.2MHz - 10.7MHz)/32 = 13.23437MHz \tag{8}$$

4.5 Data Slicer Threshold Generation

The threshold of the data slicer can be generated in two ways, depending on the signal coding scheme used. In case of a signal coding scheme without DC content such as Manchester coding the threshold can be generated using an external RC-Integrator as shown in **Figure 9**. The time constant T_A of the RC-Integrator has to be significantly larger than the longest period of no signal change T_L within the data sequence. In order to keep distortion low, the minimum value for R is 20 kΩ.

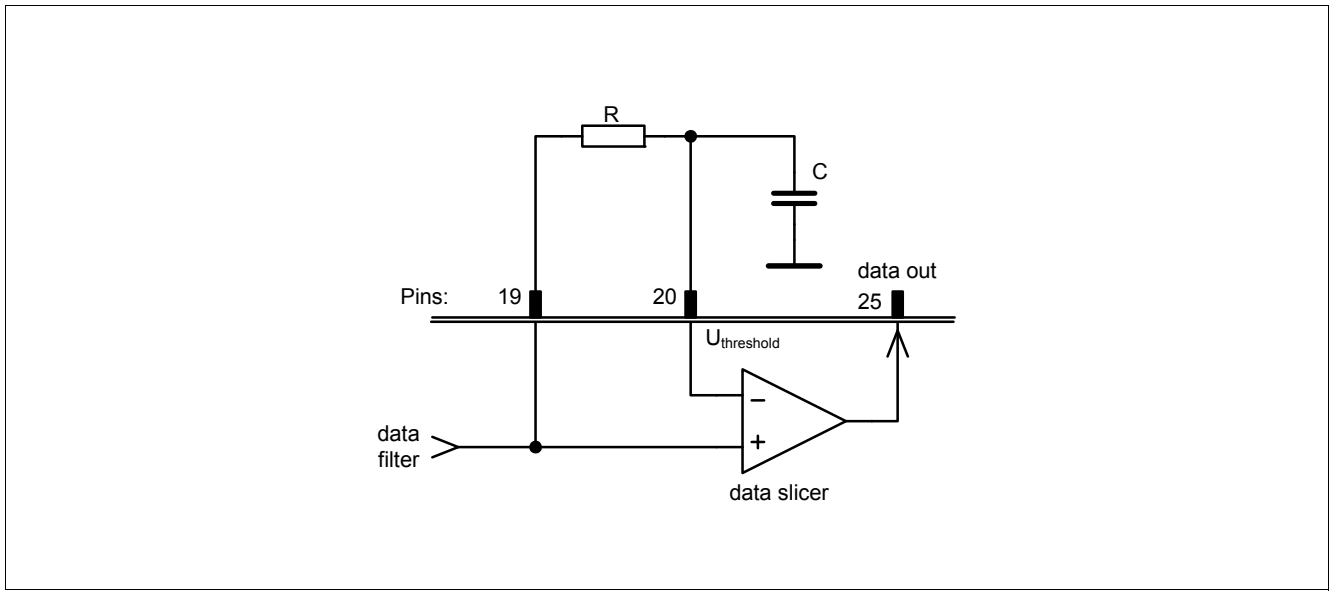


Figure 9 Data Slicer Threshold Generation with External R-C Integrator

Another possibility for threshold generation is to use the peak detector in connection with two resistors and one capacitor as shown in the following figure. The component values are depending on the coding scheme and the protocol used.

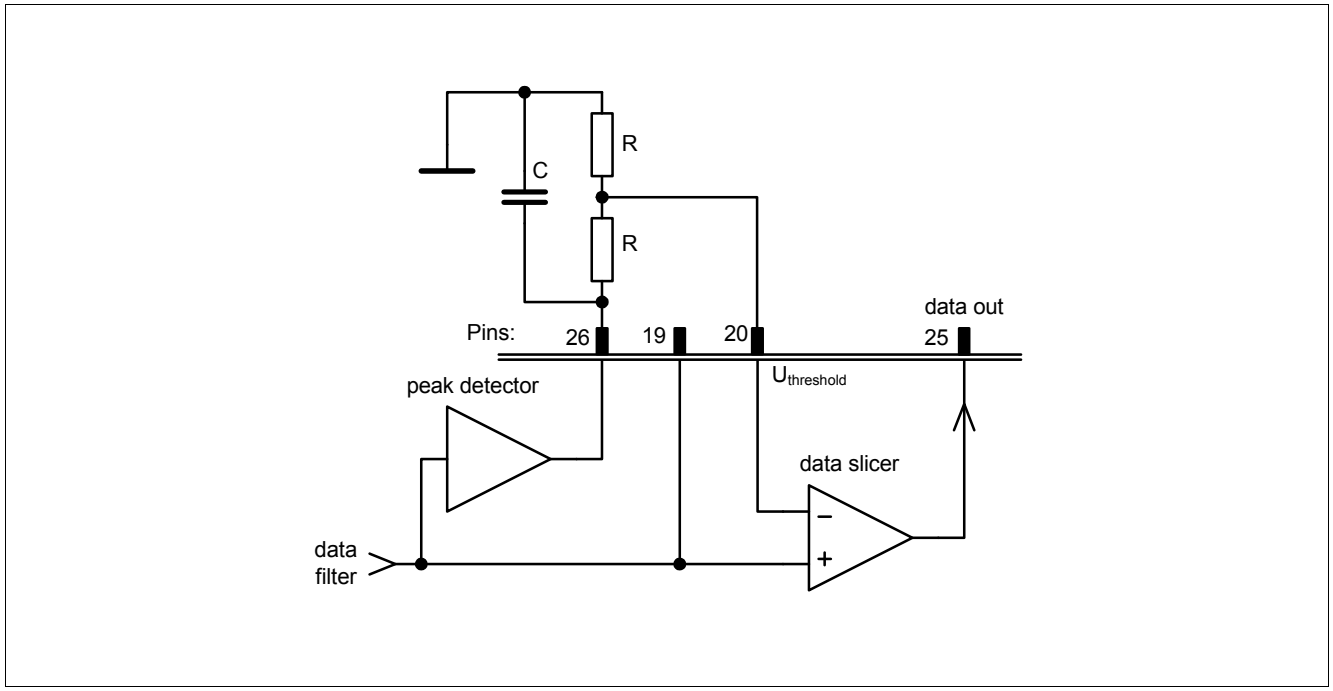


Figure 10 Data Slicer Threshold Generation Utilizing the Peak Detector

5 Electrical Characteristics

5.1 Electrical Data

5.1.1 Absolute Maximum Ratings

Attention: The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC will result.

Table 6 Absolute Maximum Ratings, Ambient Temperature T_{AMB} = - 40 °C ... + 85 °C

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage	V_{CC}	-0.3		5.5	V		1.1
Junction Temperature	T_j	-40		+125	°C		1.2
Storage Temperature	T_s	-40		+150	°C		1.3
Thermal Resistance	R_{thJA}			114	K/W		1.4
ESD HBM integrity, all pins	V_{ESD}			±1,5	kV	AEC Q100-002 / JESD22-A114B	1.5
ESD SDM integrity, all pins	V_{ESD}			±750	V	AINSI / ESD SP5.3.2-2008	1.6

5.1.2 Operating Range

Within the operating range the IC operates as explained in the circuit description. The AC/DC characteristic limits are not guaranteed.

Supply voltage: V_{CC} = 4.5 V ... 5.5 V

Table 7 Operating Range, Ambient Temperature T_{AMB} = - 40 °C ... + 85 °C

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Supply Current	$I_{S\ 868}$			5.6	mA	f_{RF} = 868 MHz		2.1
	$I_{S\ 434}$			5.4	mA	f_{RF} = 434 MHz		2.2
Receiver Input Level	RF_{in}	-107		-13	dBm	@ source impedance 50 Ω, BER 2E-3, average power level, Manchester encoded data rate 4 kBit, 280 kHz IF Bandwidth	■	2.3
LNI Input Frequency	f_{RF}	433		435	MHz			2.4
	f_{RF}	868		870	MHz			2.5
MI/X Input Frequency	f_{MI}	433		435	MHz			2.6
	f_{MI}	868		870	MHz			2.7
3 dB IF Frequency Range	$f_{IF\ -3\ dB}$	5		23	MHz			2.8
Power Down Mode On	$PWDN_{ON}$	0		0.8	V			2.9
Power Down Mode Off	$PWDN_{OFF}$	2		V_{CC}	V			2.10
Gain Control Voltage, LNA high gain state	V_{THRES}	2.8		V_{CC}-1	V			2.11
Gain Control Voltage, LNA low gain state	V_{THRES}	0		0.7	V			2.12

Attention: Test ■ means that the parameter is not subject to production test.
It was verified by design/characterization.

5.1.3 AC/DC Characteristics

AC/DC characteristics involve the spread of values guaranteed within the specified voltage and ambient temperature range. Typical characteristics are the median of the production. The device performance parameters marked with ■ are not subject to production test. They were verified by design/characterization.

Table 8 AC/DC Characteristics with T_{AMB} = 25 °C, V_{CC} = 4.5 ... 5.5 V

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Supply Current								
Supply current standby mode	$I_{S\ PDWN}$		50	70	nA	Pin 27 (PDWN) open or tied to 0 V		3.1
Supply current, device operating at 868 MHz	$I_{S\ 868}$		4.8	5.2	mA	Pin 11 (FSEL) tied to GND		3.2
Supply current, device operating at 434 MHz	$I_{S\ 434}$		4.6	5	mA	Pin 11 (FSEL) open		3.3
LNA - Signal Input LNI (PIN 3), V_{THRES} > 3.3 V, High Gain Mode								
Average Power Level at BER = 2E-3 (Sensitivity)	RF_{in}		-110		dBm	Manchester encoded data rate 4 kBit, 280 kHz IF Bandwidth	■	3.4
Input impedance f_{RF} = 434 MHz	$S_{11\ LNA}$		0.873 / -34.7 deg				■	3.5
Input impedance f_{RF} = 868 MHz	$S_{11\ LNA}$		0.738 / -73.5 deg				■	3.6
Input level @ 1 dB compression	$P1dB_{LNA}$		-10		dBm		■	3.7
Input 3rd order intercept point f_{RF} = 434 MHz	$IIP3_{LNA}$		-10		dBm	Matched input	■	3.8
Input 3rd order intercept point f_{RF} = 868 MHz	$IIP3_{LNA}$		-14		dBm	Matched input	■	3.9
LO signal feedthrough at antenna port	LO_{LNI}			-73	dBm		■	3.10
LNA - Signal Output LNO (PIN 6), V_{THRES} > 3.3 V, High Gain Mode								
Gain f_{RF} = 434 MHz	$S_{21\ LNA}$		1.509 / 138.2 deg				■	3.11
Gain f_{RF} = 868 MHz	$S_{21\ LNA}$		1.419 / 101.7 deg				■	3.12
Output impedance, f_{RF} = 434 MHz	$S_{22\ LNA}$		0.886 / -12.9 deg				■	3.13
Output impedance, f_{RF} = 868 MHz	$S_{22\ LNA}$		0.866 / -24.2 deg				■	3.14
LNA - Signal Input LNI, V_{THRES} = GND, Low Gain Mode								
Input impedance f_{RF} = 434 MHz	$S_{11\ LNA}$		0.873 / -34.7 deg				■	3.15

Table 8 AC/DC Characteristics with T_{AMB} = 25 °C, V_{CC} = 4.5 ... 5.5 V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Input impedance f_{RF} = 868 MHz	$S_{11\ LNA}$		0.738 / -73.5 deg				■	3.16
Input level @ 1 dB C. P. f_{RF} = 434 MHz	$P1dB_{LNA}$		-18		dBm	Matched input	■	3.17
Input level @ 1 dB C. P. f_{RF} = 868 MHz	$P1dB_{LNA}$		-6		dBm	Matched input	■	3.18
Input 3rd order intercept point f_{RF} = 434 MHz	$IIP3_{LNA}$		-10		dBm	Matched input	■	3.19
Input 3rd order intercept point f_{RF} = 868 MHz	$IIP3_{LNA}$		-5		dBm	Matched input	■	3.20
LNA - Signal Output LNO, V_{THRES} = GND, Low Gain Mode								
Gain f_{RF} = 434 MHz	$S_{21\ LNA}$		0.183 / 140.6 deg				■	3.21
Gain f_{RF} = 868 MHz	$S_{21\ LNA}$		0.179 / 109.1 deg				■	3.22
Output impedance f_{RF} = 434 MHz	$S_{22\ LNA}$		0.897 / -13.6 deg				■	3.23
Output impedance f_{RF} = 868 MHz	$S_{22\ LNA}$		0.868 / -26.3 deg				■	3.24
LNA - Antenna to IFO, V_{THRES} > 3.3 V, High Gain Mode								
Voltage Gain Antenna to Mixer-Out (IFO) f_{RF} = 434 MHz	$G_{AntMixerOut}$		42		dB			3.25
Voltage Gain Antenna to Mixer-Out (IFO) f_{RF} = 868 MHz	$G_{AntMixerOut}$		40		dB			3.26
LNA - Antenna to IFO, V_{THRES} = GND, Low Gain Mode								
Voltage Gain Antenna to Mixer-Out (IFO) f_{RF} = 434 MHz	$G_{AntMixerOut}$		22		dB			3.27
Voltage Gain Antenna to Mixer-Out (IFO) f_{RF} = 868 MHz	$G_{AntMixerOut}$		19		dB			3.28
AGC - Signal 3VOUT (PIN 24)								
Output voltage	V_{3VOUT}		3		V	At 5 µA		3.29
Current out	I_{3VOUT}			50	µA			3.30
AGC - Signal THRES (PIN 23)								
Input Voltage range	V_{THRES}	0		V_{CC}-1	V	See **chapter 4.1**		3.31
LNA low gain mode	V_{THRES}	0			V			3.32

Table 8 AC/DC Characteristics with T_{AMB} = 25 °C, V_{CC} = 4.5 ... 5.5 V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
LNA high gain mode	V_{THRES}	3.3[1)]		V_{CC}-1[1)]	V	Voltage must not be higher than V_{CC}-1 V		3.33
Current in	I_{THRES_in}		5		nA		■	3.34
AGC - Signal TAGC (PIN 4)								
Current out, LNA low gain state	I_{TAGC_out}		4.2		µA	RSSI > V_{THRES}		3.35
Current in, LNA high gain state	I_{TAGC_in}		1.5		µA	RSSI < V_{THRES}		3.36
MIXER - Signal Input MI/MIX (PINS 8/9)								
Input impedance f_{RF} = 434 MHz	$S_{11\ MIX}$		0.942 / -14.4 deg				■	3.37
Input impedance f_{RF} = 868 MHz	$S_{11\ MIX}$		0.918 / -28.1 deg				■	3.38
Input 3rd order intercept point f_{RF} = 434 MHz	$IIP3_{MIX}$		-28		dBm		■	3.39
Input 3rd order intercept point f_{RF} = 868 MHz	$IIP3_{MIX}$		-26		dBm		■	3.40
MIXER - Signal Output IFO (PIN 12)								
Output impedance	Z_{IFO}		330		Ω			3.41
Conversion Voltage Gain f_{RF} = 434 MHz	G_{MIX}		+19		dB			3.42
Conversion Voltage Gain f_{RF} = 868 MHz	G_{MIX}		+18		dB			3.43
LIMITER - Signal Input LIM/LIMX (PINS 17/18)								
Input Impedance	Z_{LIM}	264	330	396	Ω		■	3.44
RSSI dynamic range	DR_{RSSI}	60		80	dB			3.45
RSSI linearity	LIN_{RSSI}		±1		dB		■	3.46
Operating frequency (3 dB points)	f_{LIM}	5	10.7	23	MHz		■	3.47
DATA FILTER								
Useable bandwidth	$BW_{BB\ FILT}$			100	kHz		■	3.48
RSSI Level at Data Filter Output SLP	$RSSI_{low}$		1.1		V	LNA in high gain RF_{IN} = -103 dBm 868 MHz		3.49
RSSI Level at Data Filter Output SLP	$RSSI_{high}$		2.65		V	LNA in high gain RF_{IN} = -30 dBm 868 MHz		3.50
SLICER - Signal Output DATA (PIN 25)								
Useable bandwidth	$BW_{BB\ SLIC}$			100	kHz		■	3.51

Table 8 AC/DC Characteristics with T_{AMB} = 25 °C, V_{CC} = 4.5 ... 5.5 V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Capacitive loading of output	$C_{max\ SLIC}$			20	pF			3.52
LOW output voltage	V_{SLIC_L}		0		V			3.53
HIGH output voltage	V_{SLIC_H}	V_{CC}-1.3	V_{CC}-1	V_{CC}-0.7	V	Output current = 200 µA		3.54
Output current	I_{SLIC_out}			200	µA			3.55
PEAK DETECTOR - Signal Output PDO (PIN 26)								
LOW output voltage	V_{SLIC_L}		0		V			3.56
HIGH output voltage	V_{SLIC_H}			V_{CC}-1	V			3.57
Load current	I_{load}	-500			µA	Static load current must not exceed -500 µA		3.58
Leakage current	$I_{leakage}$		700		nA			3.59
CRYSTAL OSCILLATOR - Signals CRST1, CRST2, (PINS 1/28)								
Operating frequency	f_{CRSTL}	6		14	MHz	Fundamental mode, series resonance		3.60
Input Impedance @ ~6 MHz	$Z_{1\text{-}28}$		-900 + j750		Ω		■	3.61
Input Impedance @ ~13 MHz	$Z_{1\text{-}28}$		-450 + j1250		Ω		■	3.62
Serial Capacity @ ~6 MHz	C_{S6} = C1		8.7		pF			3.63
Serial Capacity @ ~13 MHz	C_{S13} = C1		5.3		pF			3.64
PLL - Signal LF (PIN 15)								
Tuning voltage relative to V_{CC}	V_{TUNE}	0.4	1.6	2.4	V			3.65
POWER DOWN MODE - Signal PDWN (PIN 27)								
Power Mode On	V_{ON}	2.8		V_{CC}	V			3.66
Power Mode Off	V_{PWDN}	0		0.8	V			3.67
Input bias current PDWN	I_{PDWN}		19		µA			3.68
Start-up Time until valid IF signal is detected	T_{SU}		<1		ms	Depends on the used crystal		3.69
PLL DIVIDER - Signal CSEL (PIN 16)								
f_{CRSTL} range 6.xx MHz	V_{CSEL}	1.4		4[2)]	V	Or open		3.70
f_{CRSTL} range 13.xx MHz	V_{CSEL}	0		0.2	V			3.71
Input bias current CSEL	I_{CSEL}		5		µA	CSEL tied to GND		3.72

1) See **Chapter 4.1** Choice of LNA Threshold Voltage and Time Constant.

2) Maximum voltage in Power-On state is 4 V, but in PDWN-state the maximum voltage is 2.8 V.

5.2 Test Board

5.2.1 Test Circuit

The device performance parameters marked with ■ in **Chapter 5.1.3** are not subject to production test. They were verified by design/characterization.

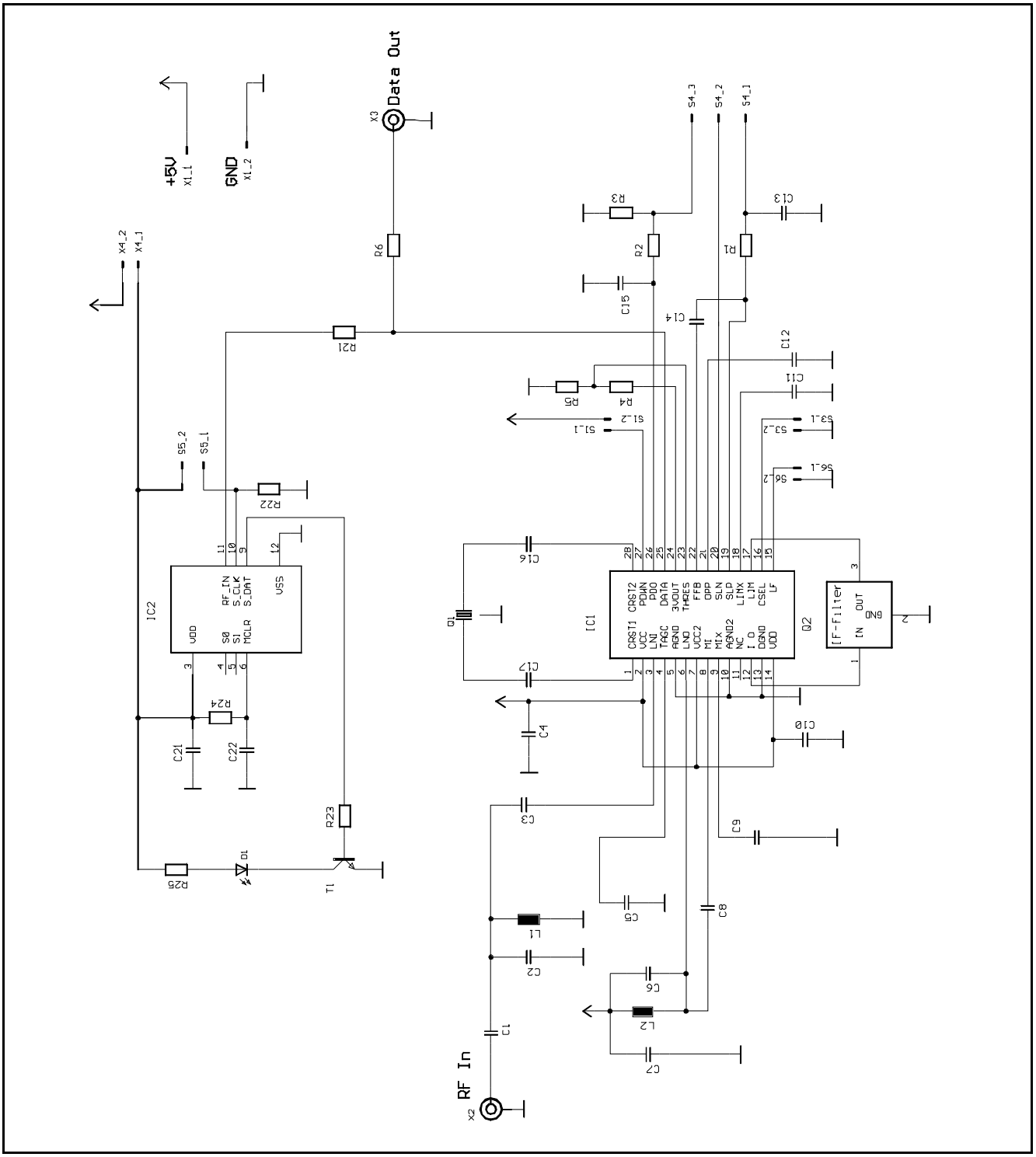


Figure 11 Schematic of the Evaluation Board

5.2.2 Test Board Layouts

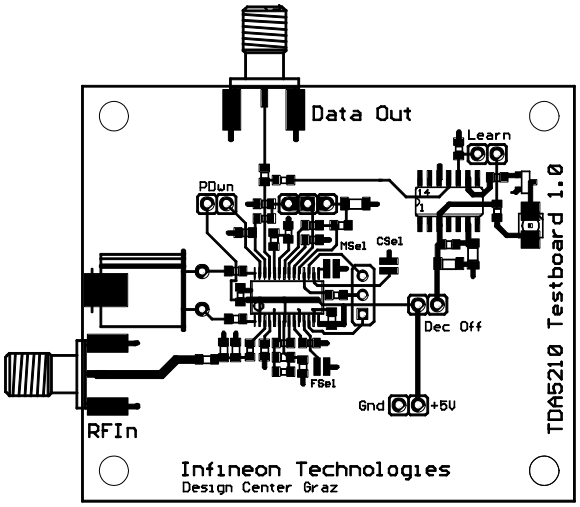


Figure 12 Top Side of the Evaluation Board

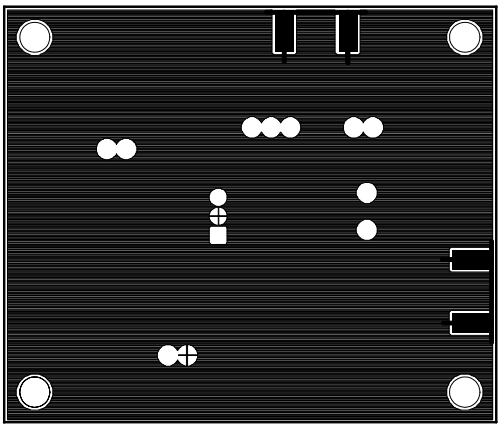


Figure 13 Bottom Side of the Evaluation Board

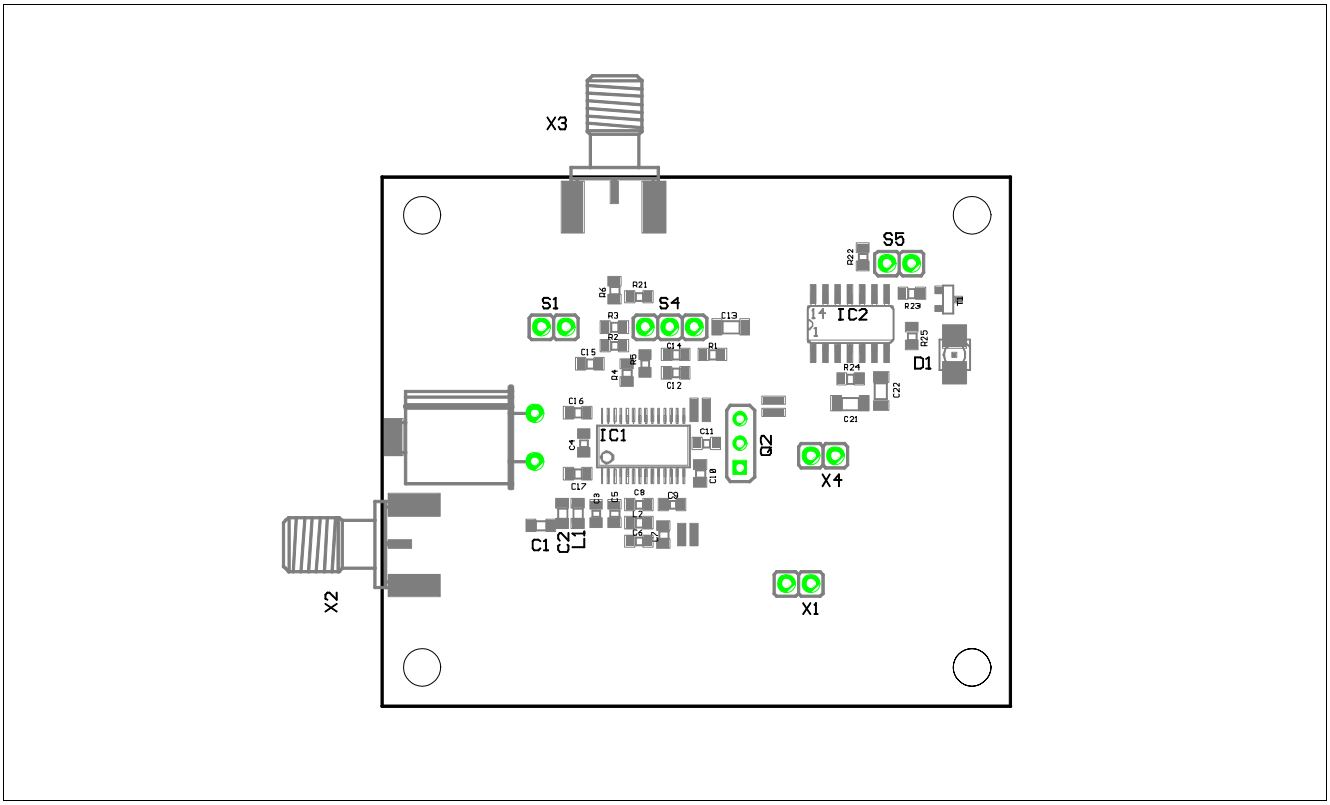


Figure 14 Component Placement on the Evaluation Board

5.2.3 Bill of Materials

The following components are necessary for evaluation of the TDA5200 without use of a Microchip HCS515 decoder.

Table 9 Bill of Materials

Ref	Value	Specification
R1	100 kΩ	0805, ± 5 %
R2	100 kΩ	0805, ± 5 %
R3	820 kΩ	0805, ± 5 %
R4	120 kΩ	0805, ± 5 %
R5	180 kΩ	0805, ± 5 %
R6	10 kΩ	0805, ± 5 %
L1	434 MHz: 15 nH 868 MHz: 3.3 nH	Toko, PTL2012-F15N0G Toko, PTL2012-F3N3C
L2	434 MHz: 8.2 pF 868 MHz: 3.9 nH	0805, COG, ± 0.1 pF Toko, PTL2012-F3N9C
C1	1 pF	0805, COG, ± 0.1 pF
C2	434 MHz: 4.7 pF 868 MHz: 3.9 pF	0805, COG, ± 0.1 pF 0805, COG, ± 0.1 pF
C3	434 MHz: 6.8 pF 868 MHz: 5.6 pF	0805, COG, ± 0.1 pF 0805, COG, ± 0.1 pF
C4	100 pF	0805, COG, ± 5 %
C5	47 nF	1206, X7R, ± 10 %
C6	434 MHz: 10 nH 868 MHz: 3.9 pF	Toko, PTL2012-F10N0G 0805, COG, ± 0.1 pF
C7	100 pF	0805, COG, ± 5 %
C8	434 MHz: 33 pF 868 MHz: 22 pF	0805, COG, ± 5 % 0805, COG, ± 5 %
C9	100 pF	0805, COG, ± 5 %
C10	10 nF	0805, X7R, ± 10 %
C11	10 nF	0805, X7R, ± 10 %
C12	220 pF	0805, COG, ± 5 %
C13	47 nF	0805, X7R, ± 10 %
C14	470 pF	0805, COG, ± 5 %
C15	47 nF	0805, X7R, ± 5 %
C16	15 pF	0805, COG, ± 1 %
C17	8.2 pF	0805, COG, ± 1 %
Q2	(fRF – 10.7 MHz)/32 or (fRF – 10.7 MHz)/64	HC49/U, fundamental mode, CL = 12 pF, e.g. 434.2 MHz: Jauch Q 13,23437-S11-1323-12-10/20 e.g. 868.4 MHz: Jauch Q 13,40155-S11-1323-12-10/20
F1	SFE10.7MA5-A or SKM107M1-A20-10	Murata Toko
X2, X3	142-0701-801	Johnson

Table 9 Bill of Materials

Ref	Value	Specification
X1, X4, S1, S5		2-pole pin connector
S4		3-pole pin connector, or not equipped
IC1	TDA 5200	Infineon

Please note that in case of operation at 434 MHz a capacitor has to be soldered in place of L2 and an inductor in place of C6.

The following components are necessary in addition to the above mentioned ones for evaluation of the TDA 5200 in conjunction with a Microchip HCS515 decoder.

Table 10 Bill of Materials Addendum

Ref	Value	Specification
R21	22 kΩ	0805, ± 5 %
R22	100 kΩ	0805, ± 5 %
R23	22 kΩ	0805, ± 5 %
R24	820 kΩ	0805, ± 5 %
R25	560 kΩ	0805, ± 5 %
C21	100 nF	1206, X7R, ± 10 %
C22	100 nF	1206, X7R, ± 10 %
IC2	HCS515	Microchip
T1	BC 847B	Infineon
D1	LS T670-JL	Infineon

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