Special Features

– High power factor
– Typical 50 µA start-up supply current
– Low quiescent current (15 mA)
– Undervoltage lockout with internal stand-by operation
– Internally synchronized fixed operating frequency ranging from 15 kHz to 200 kHz
– External synchronization possible
– Shutdown of both outputs externally triggerable
– Peak current limitation
– Overvoltage protection
– Average current sensing by noise filtering

1.2 General Remarks

The TDA 16888 comprises the complete control for power factor controlled switched mode power supplies. With its PFC and PWM section being internally synchronized, it applies for off-line converters with input voltages ranging from 90 V to 270 V.

While the preferred topologies of the PFC preconverter are boost or flyback, the PWM section can be designed as forward or flyback converter. In order to achieve minimal line current gaps the maximum duty cycle of the PFC is about 94%. The maximum duty cycle of the PWM, however, is limited to 50% to prevent transformer saturation.

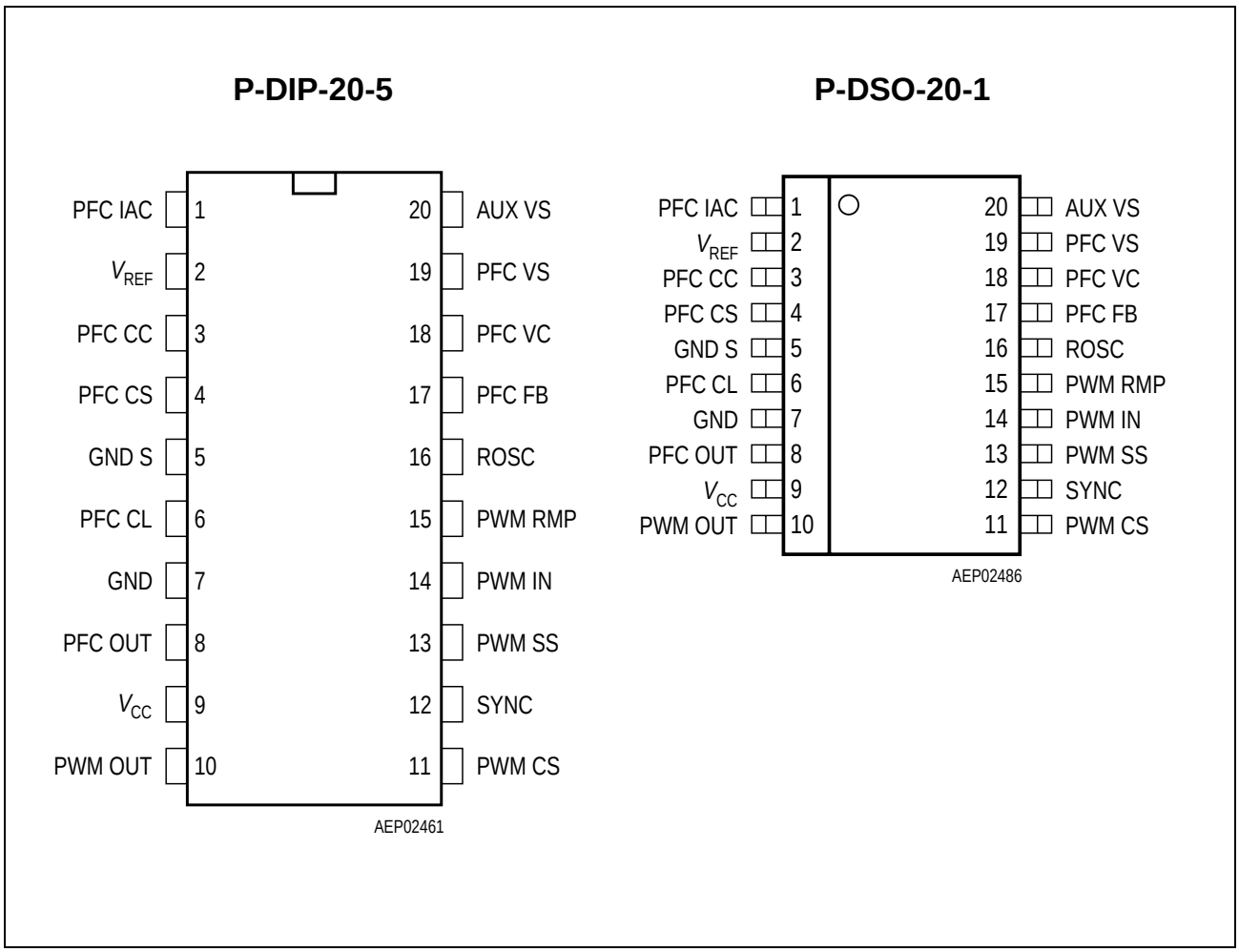


Figure 1 **Pin Configuration** (top view)

1.3 Pin Definitions and Functions

Pin No.	Symbol	Function
1	PFC IAC	AC line voltage sensing input
2	V_{REF}	7.5 V reference
3	PFC CC	PFC current loop compensation
4	PFC CS	PFC current sense
5	GND S	Ground sensing input
6	PFC CL	Sensing input for PFC current limitation
7	GND	Ground
8	PFC OUT	PFC driver output
9	V_{CC}	Supply voltage
10	PWM OUT	PWM driver output
11	PWM CS	PWM current sense
12	SYNC	Oscillator synchronization input
13	PWM SS	PWM soft-start
14	PWM IN	PWM output voltage sensing input
15	PWM RMP	PWM voltage ramp
16	ROSC	Oscillator frequency set-up
17	PFC FB	PFC voltage loop feedback
18	PFC VC	PFC voltage loop compensation
19	PFC VS	PFC output voltage sensing input
20	AUX VS	Auxiliary power supply voltage sense

1.4 Block Diagram

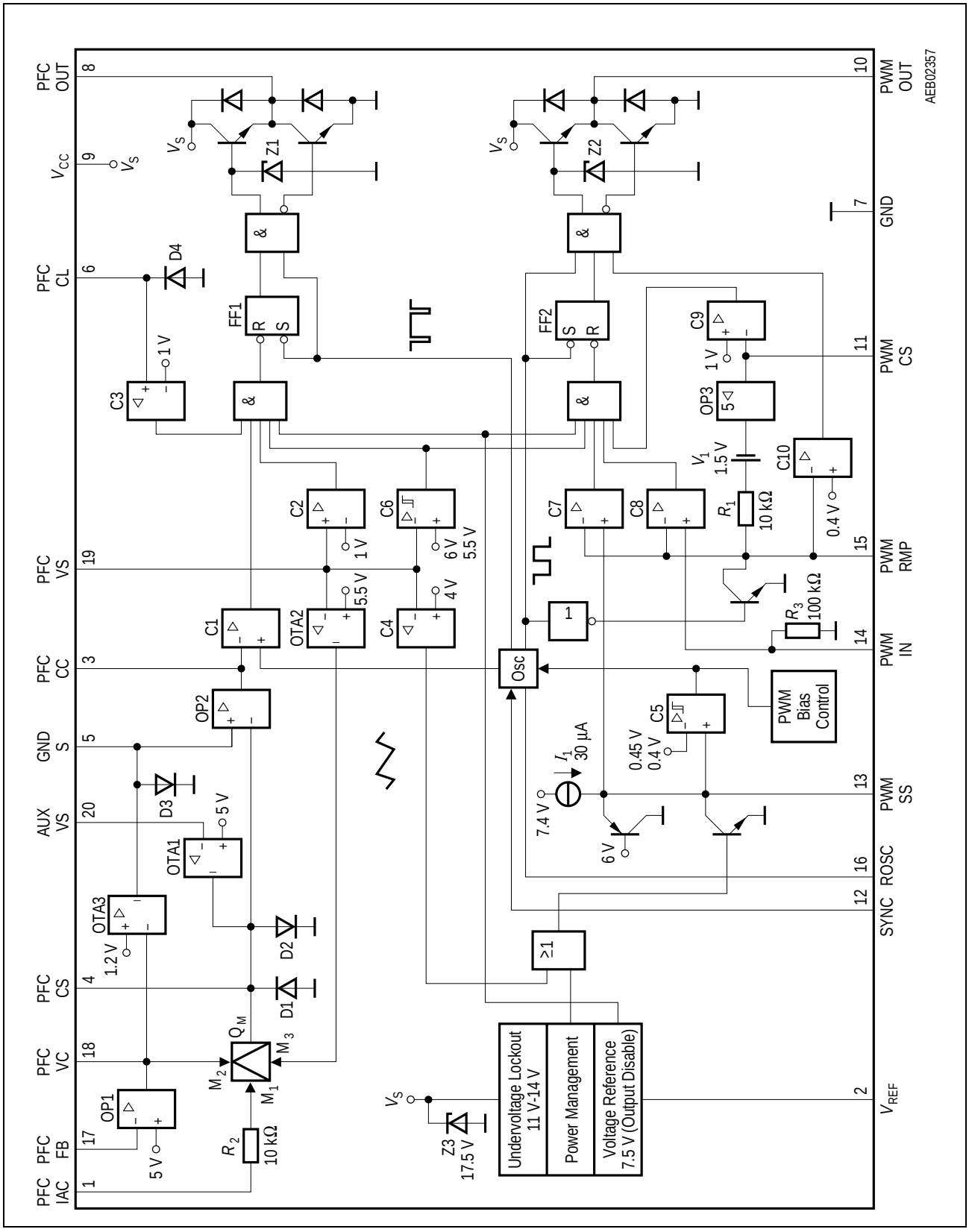


Figure 2

2 Functional Description

Power Supply

The TDA 16888 is protected against overvoltages typically above 17.5 V by an internal Zener diode Z3 at pin 9 (V_{CC}) and against electrostatic discharging at any pin by special ESD circuitry.

By means of its power management the TDA 16888 will switch from internal stand-by, which is characterized by negligible current consumption, to operation mode as soon as a supply voltage threshold of 14 V at pin 9 (V_{CC}) is exceeded. To avoid uncontrolled ringing at switch-over an undervoltage lockout is implemented, which will cause the power management to switch from operation mode to internal stand-by as soon as the supply voltage falls below a threshold of 11 V. Therefore, even if the supply voltage will fall below 14 V, operation mode will be maintained as long as the supply voltage is well above 11 V.

As soon as the supply voltage has stabilized, which is determined by the TDA 16888's power management and its soft-start feature at pin 13 (PWM SS), the PWM section will be enabled by means of its internal bias control.

Protection Circuitry

Both PFC and PWM section are equipped with a fast overvoltage protection (C6) sensing at pin 19 (PFC VS), which when being activated will immediately shut down both gate drives. In addition to improve the PFC section's load regulation it uses a fast but soft overvoltage protection (OTA2) prior to the one described above, which when being activated will cause a well controlled throttling of the multiplier output Q_M.

In case an undervoltage of the PFC output voltage is detected at pin 19 (PFC VS) by comparator C4 the gate drive of the PWM section will be shut down in order to reduce the load current and to increase the PFC output voltage. This undervoltage shutdown has to be prior to the undervoltage lockout of the internal power management and therefore has to be bound to a threshold voltage at pin 9 (V_{CC}) well above 11 V.

In order to prevent the external circuitry from destruction the PFC output PFC OUT (pin 8) will immediately be switched off by comparator C2, if the voltage at pin 19 (PFC VS) drops to ground caused by a broken wire. In a similar way measures are taken to handle a broken wire at any other pin in order to ensure a safe operation of the IC and its adjoining circuitry.

If necessary both outputs, PFC OUT (pin 8) and PWM OUT (pin 10), can be shutdown on external request. This is accomplished by shorting the external reference voltage at pin 2 (V_{REF}) to ground. To protect the external reference, it is equipped with a foldback characteristic, which will cut down the output current when V_{REF} (pin 2) is shorted (see **Figure 4**).

Both PFC and PWM section are equipped with a peak current limitation, which is realized by the comparators C3 and C9 sensing at pin 6 (PFC CL) and pin 11 (PWM CS) respectively. When being activated this current limitation will immediately shut down the respective gate drive PFC OUT (pin 8) or PWM OUT (pin 10).

Finally each pin is protected against electrostatic discharge.

Oscillator/Synchronization

The PFC and PWM clock signals as well as the PFC voltage ramp are synchronized by the internal oscillator (see **Figure 18**). The oscillator's frequency is set by an external resistor connected to pin 16 (ROSC) and ground (see **Figure 5**). The corresponding capacitor, however, is integrated to guarantee a low current consumption and a high resistance against electromagnetic interferences. In order to ensure superior precision of the clock frequency, the clock signal CLK OSC is derived from a triangular instead of a saw-tooth signal. Furthermore to provide a clock reference CLK OUT with exactly 50% duty cycle, the frequency of the oscillator's clock signal CLK OSC is halved by a D-latch before being fed into the PFC and PWM section respectively (see **Figure 18**).

The ramp signal of the PFC section $V_{\text{PFC RMP}}$ is composed of a slowly falling and a steeply rising edge. This ramp has been reversed in contrast to the common practice, in order to simultaneously allow for current measurement at pin 5 (GND S) and for external compensation of OP2 by means of pin 5 (GND S) and pin 3 (PFC CC).

The oscillator can be synchronized with an external clock signal supplied at pin 12 (SYNC). However, since the oscillator's frequency is halved before being fed into the PFC and PWM section, a synchronization frequency being twice the operating frequency is recommended. As long as the synchronization signal is H the oscillator's triangular signal V_{OSC} is interrupted and its clock signal CLK OSC is H (see **Figure 19** and **Figure 20**). However, as soon as the external clock changes from H to L the oscillator is released. Correspondingly, by means of an external clock signal supplied at pin 12 (SYNC) the oscillator frequency f_{OSC} set by an external resistor at pin 16 (ROSC) can be varied on principle only within the range from 0.66 f_{OSC} to 2 f_{OSC}. If the oscillator has to be synchronized over a wider frequency range, a synchronization by means of the sink current at pin 16 (ROSC) has to be preferred to a synchronization by means of pin 12 (SYNC). Anyhow, please note, that pin 12 (SYNC) is not meant to permanently shutdown both PFC and PWM section. It can be used to halt the oscillator freezing the prevailing state of both drivers but does not allow to automatically shut them down. A shutdown can be achieved by shorting pin 2 (V_{REF}) to ground, instead.

Finally, In order to reduce the overall current consumption under low load conditions, the oscillator frequency itself is halved as long as the voltage at pin 13 (PWM SS) is less than 0.4 V (disabled PWM section).

PFC Section

At normal operation the PFC section operates with dual loop control. An inner loop, which includes OP2, C1, FF1 and the PFC's driver, controls the shape of the line current by average current control enabling either continuous or discontinuous operation. By the outer loop, which is supported by OP1, the multiplier, OP2, C1, FF1 and the PFC's driver, the PFC output voltage is controlled. Furthermore there is a third control loop composed of OTA1, OP2, C1, FF1 and the PFC's driver, which allows the PFC section to be operated as an auxiliary power supply even when the PWM section is disabled. With disabled PWM section, however, the PFC section is operated with half of its nominal operating frequency in order to reduce the overall current consumption.

Based on a pulse-width-modulation, which is leading edge triggered with respect to the internal clock reference CLK OUT and which is trailing edge modulated according to the PFC ramp signal $V_{\text{PFC RMP}}$ and the output voltage of OP2 $V_{\text{PFC CC}}$ (see **Figure 18**), the PFC section is designed for a maximum duty cycle of ca. 94% to achieve minimal line current gaps.

PWM Section

The PWM section is equipped with improved current mode control containing effective slope compensation as well as enhanced spike suppression in contrast to the commonly used leading edge current blanking. This is achieved by the chain of operational amplifier OP3, voltage source V_1 and the 1st order low pass filter composed of R_1 and an external capacitor, which is connected to pin 15 (PWM RMP). For crosstalk suppression between PFC and PWM section a signal-to-noise ratio comparable to voltage mode controlled PWM's is set by operational amplifier OP3 performing a fivefold amplification of the PWM load current, which is sensed by an external shunt resistor. In order to simultaneously perform effective slope compensation and to suppress leading spikes, which are due to parasitic capacitances being discharged whenever the power transistor is switched on, the resulting signal is subsequently increased by the constant voltage of V_1 and finally fed into the 1st order low pass filter. The peak ramp voltage, that in this way can be reached, amounts to ca. 6.5 V. By combination of voltage source V_1 and the following low pass filter a basic ramp (step response) with a leading notch is created, which will fully compensate a leading spike (see **Figure 12**) provided, the external capacitor at pin 15 (PWM RMP) and the external current sensing shunt resistor are scaled properly.

The pulse-width-modulation of the PWM section is trailing edge modulated according to the PWM ramp signal $V_{\text{PWM RMP}}$ at pin 15 (PWM RMP) and the input voltage $V_{\text{PWM IN}}$ at pin 14 (PWM IN) (see **Figure 18**). In contrast to the PFC section, however, the pulse-width-modulation of the PWM section is trailing edge triggered with respect to the internal clock reference CLK OUT in order to avoid undesirable electromagnetic interference of both sections. Moreover the maximum duty cycle of the PWM is limited to 50% to prevent transformer saturation.

By means of the above mentioned improved current mode control a stable pulse-width-modulation from maximum load down to no load is achieved. Finally, in case of no load conditions the PWM section may as well be disabled by shorting pin 13 (PWM SS) to ground.

3 Functional Block Description

Gate Drive

Both PFC and PWM section use fast totem pole gate drives at pin 8 (PFC OUT) and pin 10 (PWM OUT) respectively, which are designed to avoid cross conduction currents and which are equipped with Zener diodes (Z1, Z2) in order to improve the control of the attached power transistors as well as to protect them against undesirable gate overvoltages. At voltages below the undervoltage lockout threshold these gate drives are active low. In order to keep the switching losses of the involved power diodes low and to minimize electromagnetic emissions, both gate drives are optimized for soft switching operation. This is achieved by a novel slope control of the rising edge at each driver's output (see **Figure 13**).

Oscillator

The TDA 16888's clock signals as well as the PFC voltage ramp are provided by the internal oscillator. The oscillator's frequency is set by an external resistor connected to pin 16 (ROSC) and ground (see **Figure 5**). The corresponding capacitor, however, is integrated to guarantee a low current consumption and a high resistance against electromagnetic interferences. In order to ensure superior precision of the clock frequency, the clock signal CLK OSC is derived from the minima and maxima of a triangular instead of a saw-tooth signal (see **Figure 18**). Furthermore, to provide a clock reference CLK OUT with exactly 50% duty cycle, the frequency of the oscillator's clock signal CLK OSC is halved by a D-latch before being fed into the PFC and PWM section respectively.

The ramp signal of the PFC section $V_{\text{PFC RMP}}$ is composed of a slowly falling and a steeply rising edge, the latter of which is triggered by the rising edge of the clock reference CLK OUT. This ramp has been reversed in contrast to the common practice, in order to simultaneously allow for current measurement at pin 5 (GND S) and for external compensation of OP2 by means of pin 5 (GND S) and pin 3 (PFC CC). The slope of the falling edge, which in conjunction with the output of OP2 controls the pulse-width-modulation of the PFC output signal $V_{\text{PFC OUT}}$, is derived from the current set by the external resistor at pin 16 (ROSC). In this way a constant amplitude of the ramp signal (ca. 4.5 V) is ensured. In contrast, the slope of the rising edge, which marks the minimum blanking interval and therefore limits the maximum duty cycle $t_{\text{on,max}}$ of the PFC output signal, is determined by an internal current source.

In contrast to the PFC section the ramp signal of the PWM section is trailing edge triggered with respect to the internal clock reference CLK OUT to avoid undesirable electromagnetic interference of both sections. Moreover, the maximum duty cycle of the PWM is limited by the rising edge of the clock reference CLK OUT to 50% to prevent transformer saturation.

The oscillator can be synchronized with an external clock signal supplied at pin 12 (SYNC). As long as this clock signal is H the oscillator's triangular signal V_{OSC} is interrupted and its clock signal CLK OSC is H (see **Figure 19** and **Figure 20**). However, as soon as the external clock changes from H to L the oscillator is released. Correspondingly, by means of an external clock signal supplied at pin 12 (SYNC) the oscillator frequency f_{OSC} set by an external resistor at pin 16 (ROSC) can be varied on principle only within the range from 0.66 f_{OSC} to 2 f_{OSC}. Please note, that the slope of the falling edge of the PFC ramp is not influenced by the synchronization frequency. Instead the lower voltage peak is modulated. Consequently, on the one hand at high synchronization frequencies $f_{SYNC} > f_{OSC}$ the amplitude of the ramp signal and correspondingly its signal-to-noise ratio is decreased (see **Figure 19**). On the other hand at low synchronization frequencies $f_{SYNC} < f_{OSC}$ the lower voltage peak is clamped to the minimum ramp voltage (typ. 1.1 V), that at least can be achieved (see **Figure 20**), which may cause undefined PFC duty cycles as the voltage $V_{PFC\ CC}$ at pin 3 (PFC CC) drops below this threshold. However, if the oscillator has to be synchronized over a wide frequency range, a synchronization by means of the sink current at pin 16 (ROSC) has to be preferred to a synchronization by means of pin 12 (SYNC).

In order to reduce the overall current consumption under low load conditions, the oscillator frequency itself is halved as long as the voltage at pin 13 (PWM SS) is less than 0.4 V (disabled PWM section).

Multiplier

The multiplier serves to provide the controlled current I_{QM} by combination of the shape of the sinusoidal input current I_{M1} derived from the voltage at pin 1 (PFC IAC) by means of the 10 kΩ resistor R_2, the magnitude of the PFC output voltage V_{M2} given at pin 18 (PFC VC) and the possibility for soft overvoltage protection V_{M3} (see **Chapter Protection Circuitry**). By means of this current the required power factor as well as the magnitude of the PFC output voltage is ensured. To achieve an excellent performance over a wide range of output power and input voltage, the input voltage V_{M2} is amplified by an exponential function before being fed into the multiplier (see **Figure 8**).

Voltage Amplifier OP1

Being part of the outer loop the error amplifier OP1 controls the magnitude of the PFC output voltage by comparison of the PFC output voltage measured at pin 17 (PFC FB) with an internal reference voltage. The latter is fixed to 5 V in order to achieve immunity from external noise. To allow for individual feedback the output of OP1 is connected to pin 18 (PFC VC).

Current Amplifier OP2

Being part of the inner loop the error amplifier OP2 controls the shape of the line current by comparison of the controlled current I_{QM} with the measured average line current. This is achieved by setting the pulse width of the PFC gate drive in conjunction with the comparator C1. In order to limit the voltage range supplied at pin 4 (PFC CS) and at pin 5 (GND S), clamping diodes D1, D2 and D3 are connected with these pins and ground. To allow for individual feedback the output of OP2 is connected to pin 3 (PFC CC).

Ramp Amplifier OP3

For crosstalk suppression between PFC and PWM section a signal-to-noise ratio comparable to voltage mode controlled PWMs is set by operational amplifier OP3 performing a fivefold amplification of the PWM load current, which is sensed by an external shunt resistor. In order to suppress leading spikes, which are due to parasitic capacitances being discharged whenever the power transistor is switched on, the resulting signal is subsequently increased by the constant voltage of V_1 and finally fed into a 1st order low pass filter. By combination of voltage source V_1 and the following low pass filter a step response with a leading notch is created, which will fully compensate a leading spike (see **Figure 12**) provided, the external capacitor at pin 15 (PWM RMP) and the external current sensing shunt resistor are scaled properly.

Operational Transconductance Amplifier OTA1

The TDA 16888's auxiliary power supply mode is controlled by the fast operational transconductance amplifier OTA1. When under low load or no load conditions a voltage below 5 V is sensed at pin 20 (AUX VS), it will start to superimpose its output on the output Q_M of the multiplier and in this way will replace the error amplifier OP1 and the multiplier. At normal operation, however, when the voltage at pin 20 (AUX VS) is well above 5 V, this operational transconductance amplifier is disabled.

Operational Transconductance Amplifier OTA2

By means of the operational transconductance amplifier OTA2 sensing at pin 19 (PFC VS) a fast but soft overvoltage protection of the PFC output voltage is achieved, which when being activated ($V_{PFC\ VS}$ > 5.5 V) will cause a well controlled throttling of the multiplier output Q_M (see **Figure 9**).

Operational Transconductance Amplifier OTA3

In order to achieve offset compensation of error amplifier OP2 under low load conditions, that will not suffice to start OTA1, the operational transconductance amplifier OTA3 is introduced. It will start operation as soon as these conditions are reached, i.e. the voltage at pin 18 (PFC VC) falls below 1.2 V.

Comparator C1

The comparator C1 serves to adjust the duty cycle of the PFC gate drive. This is achieved by comparison of the output voltage of OP2 given at pin 3 (PFC CC) and the voltage ramp of the oscillator.

Comparator C2

The comparator C2 serves to prevent the external circuitry from destruction by immediately switching the PFC output PFC OUT (pin 8) off, if the voltage at pin 19 (PFC VS) drops below 1 V due to a broken wire.

Comparator C3

By means of this extremely fast comparator sensing at pin 6 (PFC CL) peak current limitation is realized. When being activated ($V_{\text{PFC CL}}$ < 1 V) it will immediately shut down the gate drive of the PFC section (pin 8, PFC OUT). In order to protect C3 against undervoltages at pin 6 (PFC CL) due to large inrush currents, this pin is equipped with an additional clamping diode D4.

Comparator C4

This comparator along with the TDA 16888's power management serves to reset the PWM section's soft start at pin 13 (PWM SS). C4 becomes active as soon as an undervoltage ($V_{\text{PFC VS}}$ < 4 V) of the PFC output voltage is sensed at pin 19 (PFC VS).

Comparator C5

Based on the status of the PWM section's soft start at pin 13 (PWM SS), the comparator C5 controls the bias of the entire PWM section. In this way the PWM section is switched off giving a very low quiescent current, until its soft start is released.

Comparator C6

Overvoltage protection of the PWM section's input voltage sensed at pin 19 (PFC VS) is realized by comparator C6, which when being activated will immediately shut down both gate drives PFC OUT (pin 8) and PWM OUT (pin 10).

Comparator C7

This comparator sensing at pin 13 (PWM SS) and at pin 15 (PWM RMP) controls the pulse width modulation of the PWM section during the soft start. This is done right after the PWM section is biased by comparator C5.

Comparator C8

The control of the pulse width modulation of the PWM section is taken over by comparator C8 as soon as the soft start is finished. This is achieved by comparison of the PWM output voltage at pin 14 (PWM IN) and the PWM voltage ramp at pin 15 (PWM RMP).

Comparator C9

By means of this extremely fast comparator sensing at pin 11 (PWM CS) peak current limitation is realized. When being activated ($V_{\text{PWM CS}}$ > 1 V) it will immediately shut down the gate drive of the PWM section (PWM OUT).

Comparator C10

By means of the threshold of 0.4 V the comparator C10 allows the PWM duty cycle to be continuously controlled from 0 to 50%. As long as the ramp voltage at pin 15 (PWM RMP) is below this threshold the gate drive of the PWM section (pin 10, PWM OUT) is turned off.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

T_A = – 25 to 85 °C

Parameter#	Symbol	Limit Values		Unit	Remarks
		min.	max.		
V_{CC} supply voltage	V_S	– 0.3	V_{Z3}	V	V_{Z3} = Zener voltage of Z3
Zener current of Z3	I_{Z3}	–	50	mA	–
V_{REF} voltage	V_{VREF}	– 0.3	8	V	$V_{VREF} < V_S$
ROSC voltage	V_{ROSC}	– 0.3	8	V	$V_{ROSC} < V_S$
SYNC voltage	V_{SYNC}	– 0.3	8	V	–
PFC FB voltage	$V_{PFC\ FB}$	– 0.3	8	V	–
PFC IAC voltage	$V_{PFC\ IAC}$	– 0.3	15	V	–
AUX VS voltage	$V_{AUX\ VS}$	– 0.3	8	V	–
PFC VS voltage	$V_{PFC\ VS}$	– 0.3	8	V	$\lvert I_{PFC\ VS}\rvert < 1$ mA
PFC CL voltage	$V_{PFC\ CL}$	– 1	3	V	$\lvert I_{PFC\ CL}\rvert < 1$ mA
PWM SS voltage	$V_{PWM\ SS}$	– 0.3	8	V	$V_{PWM\ SS} < V_{VREF}$
PWM IN voltage	$V_{PWM\ IN}$	– 0.3	8	V	–
PWM RMP voltage	$V_{PWM\ RMP}$	– 0.3	8	V	$V_{PWM\ RMP} < V_{VREF}$
PWM CS voltage	$V_{PWM\ CS}$	– 0.3	3	V	–
PFC VC voltage	$V_{PFC\ VC}$	– 0.3	8	V	–
PFC VC current	$I_{PFC\ VC}$	– 20	20	mA	–
PFC CS current	$I_{PFC\ CS}$	– 5	5	mA	–
GND S current	$I_{GND\ S}$	– 5	5	mA	–
PFC CC voltage	$V_{PFC\ CC}$	– 0.3	8	V	–
PFC CC current	$I_{PFC\ CC}$	– 20	20	mA	–
PFC/PWM OUT DC current	I_{OUT}	– 100	100	mA	–
PFC/PWM OUT peak clamping current	I_{OUT}	–	200	mA	V_{OUT} = High
PFC/PWM OUT peak clamping current	I_{OUT}	– 500	–	mA	V_{OUT} = Low
Junction temperature	T_J	– 40	150	°C	–

4.1 Absolute Maximum Ratings (cont'd)

T_A = – 25 to 85 °C

Parameter#	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Storage temperature	T_S	– 65	150	°C	–
Thermal resistance	R_{thJA}	–	60	K/W	P-DIP-20-5
Thermal resistance	R_{thJA}	–	70	K/W	P-DSO-20-1

*Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. To avoid destruction make sure, that for any pin except for pins PFC OUT and PWM OUT the currents caused by transient processes stay well below 100 mA. For the same reason make sure, that any capacitor that will be connected to pin 9 (V_{CC}) is discharged before assembling the application circuit. In order to characterize the gate driver's output performance **Figure 14**, **Figure 15**, **Figure 16** and **Figure 17** are provided, instead of referring just to a single parameter like the maximum gate charge or the maximum output energy.*

4.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
V_{CC} supply voltage	V_S	0	V_{Z3}	V	V_{Z3} = Zener voltage of Z3
Zener current	I_{Z3}	0	50	mA	Limited by $T_{J,max}$
PFC/PWM OUT current	I_{OUT}	– 1	1.5	A	–
PFC IAC input current	$I_{PFC\ IAC}$	0	1	mA	–
PFC/PWM frequency	f_{OUT}	15	200	kHz	–
Junction temperature	T_J	– 25	125	°C	–

*Note: Within the operating range the IC operates as described in the functional description. In order to characterize the gate driver's output performance **Figure 14**, **Figure 15**, **Figure 16** and **Figure 17** are provided, instead of referring just to a single parameter like the maximum gate charge or the maximum output energy.*

4.3 Characteristics

Supply Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Zener voltage[1]	V_{Z3}	16.0	17.5	19.0	V	I_{Z3} = 30 mA
Zener current	I_{Z3}	–	–	500	µA	$V_S \leq$ 15.5 V[2]
Quiescent supply current	I_S	–	–	12	mA	$V_{PWM\ SS}$ = 0 V R_{ROSC} = 51 kΩ C_L = 0 V PFC enabled PWM disabled
		–	–	15	mA	$V_{PWM\ SS}$ = 6 V R_{ROSC} = 51 kΩ C_L = 0 F PFC enabled PWM enabled
Supply current	I_S	–	–	40	mA	$V_{PWM\ SS}$ = 6 V R_{ROSC} = 51 kΩ C_L = 4.7 nF PFC enabled PWM enabled

1) See **Figure 3**

2) Design characteristics (not meant for production testing)

Note: The electrical characteristics involve the spread of values guaranteed within the specified supply voltage and ambient temperature range T_A from – 25 °C to 85 °C Typical values represent the median values, which are related to production processes. If not otherwise stated, a supply voltage of V_S = 15 V is assumed.

Undervoltage Lockout

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Power up, rising voltage threshold[1)]	$V_{S,UP}$	13.0	14.0	14.5	V	–
Power down, falling voltage threshold[1)]	$V_{S,DWN}$	10.5	11.0	11.5	V	–
Power up, threshold current	$I_{S,UP}$	–	23	100	µA	$V_S = V_{S,UP} - 0.1$ V $V_{PFC\ CL} < 0.3$ V[2)] Stand-by mode

1) See **Figure 3**

2) To ensure the voltage fallback of pin PFC CL is disabled.

Internal Voltage Reference

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Trimmed reference voltage	V_{REF}	4.9	5.0	5.1	V	Measured at pin PFC VC
Line regulation	ΔV_{REF}	–	–	40	mV	$\Delta V_S = 3$ V

External Voltage Reference

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Buffered output voltage	V_{VREF}	7.2	7.5	7.8	V	– 3 mA ≤ I_{VREF} ≤ 0
Line regulation	ΔV_{VREF}	–	–	50	mV	ΔV_S = 3 V
Load regulation	ΔV_{VREF}	0	40	100	mV	ΔI_{VREF} = 2 mA
Maximum output current[1)]	I_{VREF}	– 10	– 6	– 4	mA	V_{VREF} = 6.5 V
Short circuit current[1)]	I_{VREF}	–	– 2	–	mA	V_{VREF} = 0 V
Shutdown hysteresis, rising voltage threshold	V_{VREF}	–	6.6	–	V	–
Shutdown hysteresis, falling voltage threshold	V_{VREF}	–	6.2	–	V	–
Shutdown delay	$t_{d,VREF}$	–	500	–	ns	V_{VREF} = 5 V[2)3)] $V_{PFC\ OUT}$ = 3 V[2)3)] $V_{PWM\ OUT}$ = 3 V[2)3)]

1) See **Figure 4**
2) Design characteristics (not meant for production testing)
3) Transient reference value

Oscillator

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
PFC/PWM frequency[1)]	f_{OUT50}	43	50	57	kHz	R_{ROSC} = 110 kΩ
PFC/PWM frequency[1)]	f_{OUT100}	87	100	113	kHz	R_{ROSC} = 51 kΩ
PFC/PWM frequency, line regulation	Δf_{OUT}	–	–	1	%	ΔV_S = 3 V R_{ROSC} = 51 kΩ
Maximum ramp voltage	$V_{PFC\ RMP}$	5.0	5.4	5.6	V	–
Minimum ramp voltage	$V_{PFC\ RMP}$	0.8	1.1	1.4	V	–
SYNC, low level voltage	V_{SYNC}	–	–	0.4	V	–
SYNC, high level voltage	V_{SYNC}	3.5	–	V_{VREF}	V	–
SYNC, input current	I_{SYNC}	–	–	20	µA	V_{SYNC} < 0.4 V
		–	–	150	µA	V_{SYNC} = 3.5 V

1) See **Figure 5**

PFC Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Max duty cycle[1]	$D_{on,PFC}$	91	94	98	%	$V_{PFC\ OUT}$ = 2 V[3] R_{ROSC} = 51 kΩ C_L = 4.7 nF
Multiplier throttling (OTA2), threshold voltage[2]	$V_{PFC\ VS}$	5.2	5.5	5.8	V	0.9 $I_{PFC\ CS}$ $I_{PFC\ IAC}$ = 100 µA $V_{PFC\ VC}$ = 6 V OTA1 disabled
Overvoltage protection (C6), rising voltage threshold	$V_{PFC\ VS}$	5.8	6	6.2	V	–
Overvoltage protection (C6), falling voltage threshold	$V_{PFC\ VS}$	5.3	5.5	5.7	V	–
Overvoltage protection (C6), turn-off delay	$t_{d,OV}$	–	2	–	µs	$V_{PFC\ VS}$ = 6.5 V[3][4] $V_{PFC\ OUT}$ = 3 V[3][4]
Broken wire detection (C2), threshold voltage	$V_{PFC\ VS}$	0.93	1	1.07	V	–
Voltage sense, input current	$I_{PFC\ VS}$	0.2	0.45	0.7	µA	$V_{PFC\ VS}$ = 1 V
Current limitation (C3), threshold voltage	$V_{PFC\ CL}$	0.93	1	1.07	V	–
Current limitation (C3), input current	$I_{PFC\ CL}$	1	–	10	µA	$V_{PFC\ CL}$ = 1 V
Current limitation (C3, D4), clamping voltage	$V_{PFC\ CL}$	– 0.9	–	– 0.1	V	$I_{PFC\ CL}$ = – 500 µA
Current limitation (C3), turn-off delay	$t_{d,CL}$	30	–	150	ns	$V_{PFC\ CL}$ = 0.75 V[3] $V_{PFC\ OUT}$ = 3 V[3] C_L = 4.7 nF

1) See **Figure 6**
2) See **Figure 9**
3) Transient reference value
4) Design characteristics (not meant for production testing)

Multiplier

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input current	$I_{PFC\ IAC}$	0	–	1	mA	–
Input voltage	$V_{PFC\ VC}$	0	–	6.7	V	–
Exponential function, threshold voltage	$V_{PFC\ VC}$	–	1.1	–	V	1)2)
Maximum output current	$I_{PFC\ CS}$	– 320	– 420	– 550	µA	OTA1 disabled
Output current3)	$I_{PFC\ CS}$	–	– 100	– 500	nA	$I_{PFC\ IAC}$ = 0 A $V_{PFC\ VC}$ = 2 V OTA1 disabled
		–	– 1.2	–	µA	$I_{PFC\ IAC}$ = 25 µA $V_{PFC\ VC}$ = 2 V OTA1 disabled
		–	– 10	–	µA	$I_{PFC\ IAC}$ = 25 µA $V_{PFC\ VC}$ = 4 V OTA1 disabled
		–	– 40	–	µA	$I_{PFC\ IAC}$ = 100 µA $V_{PFC\ VC}$ = 4 V OTA1 disabled
		–	– 150	–	µA	$I_{PFC\ IAC}$ = 400 µA $V_{PFC\ VC}$ = 4 V OTA1 disabled
		–	– 170	–	µA	$I_{PFC\ IAC}$ = 100 µA $V_{PFC\ VC}$ = 6 V OTA1 disabled

1) Design characteristics (not meant for production testing)

2) For input voltages below this threshold the multiplier output current remains constant. For input voltages above this threshold the output rises exponentially (see **Figure 8**).

3) See **Figure 7**

Operational Transconductance Amplifier (OTA1)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Auxiliary power supply, threshold voltage[1)]	$V_{AUX\ VS}$	4.8	5.0	5.2	V	$I_{PFC\ CS}$ = – 1 µA Multiplier disabled
Input current	$I_{AUX\ VS}$	–	–	15	µA	$V_{AUX\ VS}$ > 5.2 V
		– 20	–	–	µA	$V_{AUX\ VS}$ < 4.8 V
Output current	$I_{PFC\ CS}$	–	0	–	µA	$V_{AUX\ VS}$ > 5.2 V[1)]
		–	– 30	–	µA	$V_{AUX\ VS}$ < 4.8 V

1) For input voltages below this threshold the output current is linearly increasing until at ca. 4.8 V the maximum output current is reached.

Operational Transconductance Amplifier (OTA3)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Offset compensation, threshold voltage	$V_{PFC\ VC}$	1.1	1.2	–	V	–
Input current	$I_{PFC\ VC}$	– 1	–	–	µA	1)
Output current	$I_{GND\ S}$	–	0	–	µA	$V_{PFC\ VC}$ > 1.2 V
		–	– 10	–	µA	$V_{PFC\ VC}$ < 1.1 V

1) Design characteristics (not meant for production testing)

Voltage Amplifier (OP1)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Offset voltage	V_{Off}	– 4	–	4	mV	1)
Input current	$I_{PFC\ FB}$	– 1	–	1	µA	$V_{PFC\ FB}$ = 4 V
Open loop gain	$A_{PFC\ VC}$	–	85	–	dB	2)
Input voltage range	$V_{PFC\ FB}$	0	–	6	V	–
Voltage sense, threshold voltage	$V_{PFC\ FB}$	4.9	5	5.1	V	–
Output, maximum voltage	$V_{PFC\ VC}$	6.3	–	V_{VREF}	V	$I_{PFC\ VC}$ = – 500 µA
Output, minimum voltage	$V_{PFC\ VC}$	0.5	–	1.1	V	$I_{PFC\ VC}$ = 500 µA
Output, short circuit source current	$I_{PFC\ VC}$	–	– 10	–	mA	$V_{PFC\ VC}$ = 0 V $V_{PFC\ FB}$ = 4.9 V
Output, short circuit sink current	$I_{PFC\ VC}$	–	10	–	mA	$V_{PFC\ VC}$ = 6.4 V $V_{PFC\ FB}$ = 5.1 V

1) Guaranteed by wafer test
2) Design characteristics (not meant for production testing)

Current Amplifier (OP2)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Offset voltage	V_{Off}	– 5	– 1	3	mV	–
Input current	$I_{PFC\ CS}$ $I_{GND\ S}$	– 500	–	500	nA	–
Open loop gain	$A_{PFC\ CC}$	–	110	–	dB	–
Gain bandwidth product	f_T	–	2.5	–	MHz	1)
Phase margin	φ	–	60	–	°	1)
Common mode voltage range	V_{CMVR}	– 0.2	–	0.5	V	1)
Clamped input voltage, upper threshold (D2, D3)	$V_{PFC\ CS}$ $V_{GND\ S}$	0.4	–	1.0	V	$I_{PFC\ CS}$ = 500 µA $I_{GND\ S}$ = 500 µA Multiplier, OTA1 and OTA3 disabled
Clamped input voltage, lower threshold (D1)	$V_{PFC\ CS}$	– 0.9	–	– 0.1	V	$I_{PFC\ CS}$ = – 500 µA Multiplier and OTA1 disabled
Output, maximum voltage	$V_{PFC\ CC}$	6.3	–	V_{VREF}	V	$I_{PFC\ CC}$ = – 500 µA
Output, minimum voltage	$V_{PFC\ CC}$	0.5	–	1.1	V	$I_{PFC\ CC}$ = 500 µA
Output, short circuit source current	$I_{PFC\ CC}$	–	– 10	–	mA	$V_{PFC\ CC}$ = 0 V $V_{PFC\ CS}$ = 0 V $V_{GND\ S}$ = 0.5 V
Output, short circuit sink current	$I_{PFC\ CC}$	–	10	–	mA	$V_{PFC\ CC}$ = 6.5 V $V_{PFC\ CS}$ = 0.5 V $V_{GND\ S}$ = 0 V

1) Design characteristics (not meant for production testing)

PWM Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Undervoltage protection (C4), threshold voltage	$V_{PFC\ VS}$	3.8	4.0	4.2	V	–
Bias control (C5), rising voltage threshold	$V_{BC,Th}$	–	0.45	–	V	–
Bias control (C5), falling voltage threshold	$V_{BC,Th}$	–	0.4	–	V	–
Softstart (I_1), charging current	I_{I1}	20	30	40	µA	–
Softstart, maximum voltage	$V_{PWM\ SS}$	–	6.7	–	V	–
Input voltage	$V_{PWM\ IN}$	0.4	–	7.4	V	–
PWM IN – GND resistance	R_3	75	100	150	kΩ	–
Ramp (OP3), voltage gain	A_{OP3}	–	5	–	V/V	–
Ramp (C10), pulse start threshold voltage	V_{RMP}	0.36	0.4	0.5	V	–
Ramp, maximum voltage	V_{RMP}	–	6.5	–	V	–
Ramp (V_1), voltage offset	V_{V1}	–	1.5	–	V	–
Ramp (R_1), output impedance	Z_{RMP}	–	10	–	kΩ	–
Maximum duty cycle	$D_{on,PWM}$	41	–	50	%	$V_{PWM\ OUT}$ = 2 V[1)] R_{ROSC} = 51 kΩ C_L = 4.7 nF
Current sense (C9), voltage threshold	$V_{CS,Th}$	0.9	1.0	1.1	V	–
Current sense (C9), overload turn-off delay	$t_{d,CS}$	30	–	250	ns	$V_{PWM\ CS}$ = 1.25 V[1)] $V_{PWM\ OUT}$ = 3 V[1)] C_L = 4.7 nF

1) Transient reference value

Gate Drive (PWM and PFC Section)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output, minimum voltage	V_{OUT}	–	–	1.2	V	V_S = 5 V I_{OUT} = 5 mA
		–	–	1.5	V	V_S = 5 V I_{OUT} = 20 mA
		–	0.8	–	V	I_{OUT} = 0 A
		–	1.6	2.0	V	I_{OUT} = 50 mA
		– 0.2	0.2	–	V	I_{OUT} = – 50 mA
Output, maximum voltage	V_{OUT}	10	11	12	V	V_S = 16 V t_H = 10 µs C_L = 4.7 nF
		10.0	10.5	–	V	V_S = 12 V t_H = 10 µs C_L = 4.7 nF
		8.8	–	–	V	$V_S = V_{S,DWN}$ + 0.2 V t_H = 10 µs C_L = 4.7 nF
Rise time[1)]	t_r	–	150	–	ns	V_{OUT} = 2 V … 8 V[2)] C_L = 4.7 nF
		–	100	–	ns	V_{OUT} = 3 V … 6 V[2)] C_L = 4.7 nF
Fall time	t_f	–	30	–	ns	V_{OUT} = 9 V … 3 V[2)] C_L = 4.7 nF
		–	40	–	ns	V_{OUT} = 9 V … 2 V[2)] C_L = 4.7 nF
Output current, rising edge[3)]	I_{OUT}	– 1	–	–	A	C_L = 4.7 nF[4)]
Output current, falling edge[3)]	I_{OUT}	–	–	1.5	A	C_L = 4.7 nF[4)]

1) See **Figure 13**
2) Transient reference value
3) The gate driver's output performance is characterized in **Figure 14**, **Figure 15**, **Figure 16** and **Figure 17**.
4) Design characteristics (not meant for production testing)

Note: If not otherwise stated the figures shown in this section represent typical performance characteristics.

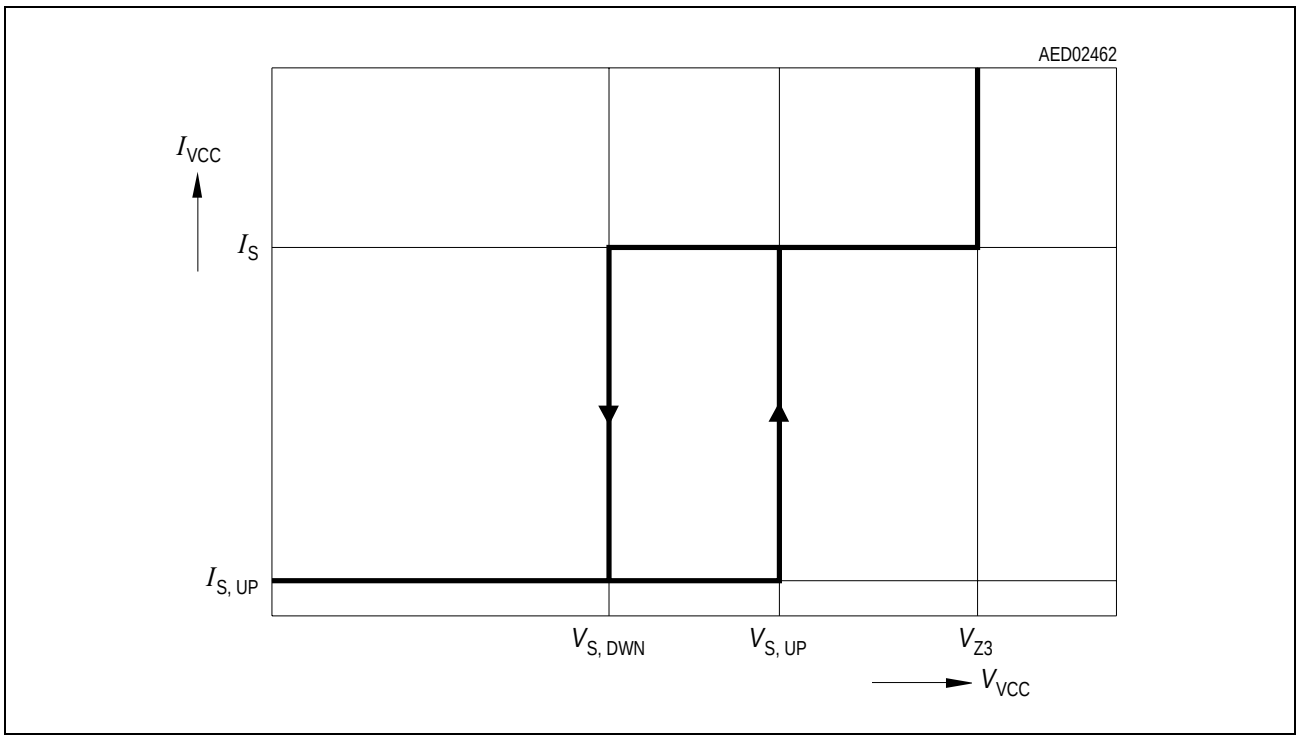


Figure 3 Undervoltage Lockout Hysteresis and Zener Diode Overvoltage Protection

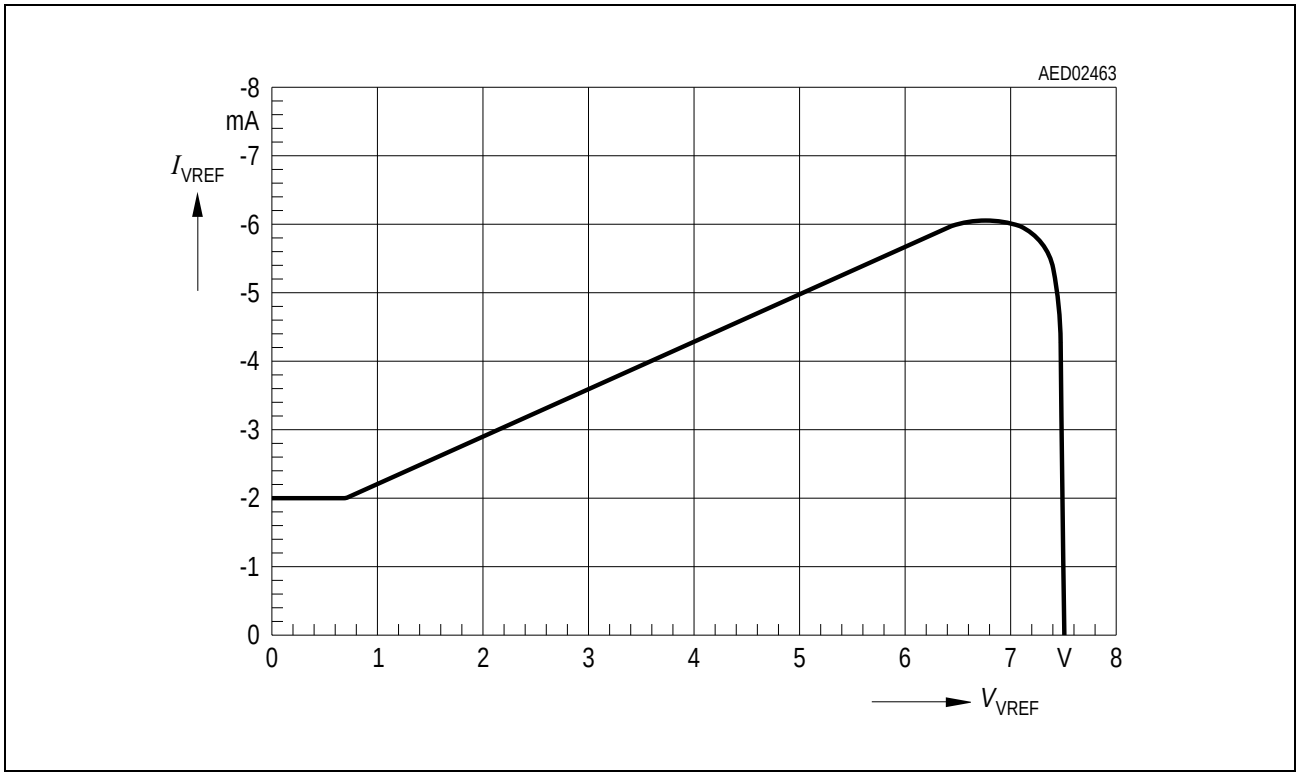


Figure 4 Foldback Characteristic of Pin 2 (V_{REF})

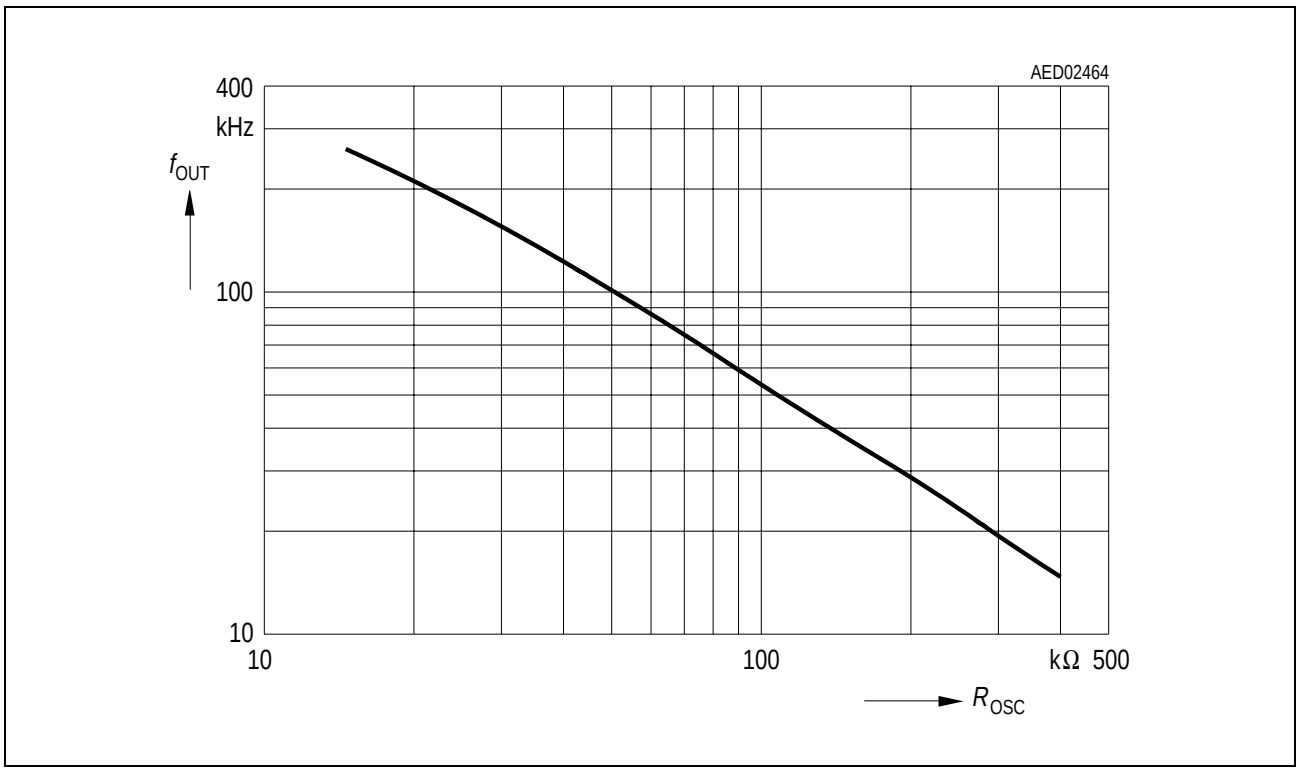


Figure 5 PFC/PWM Frequency

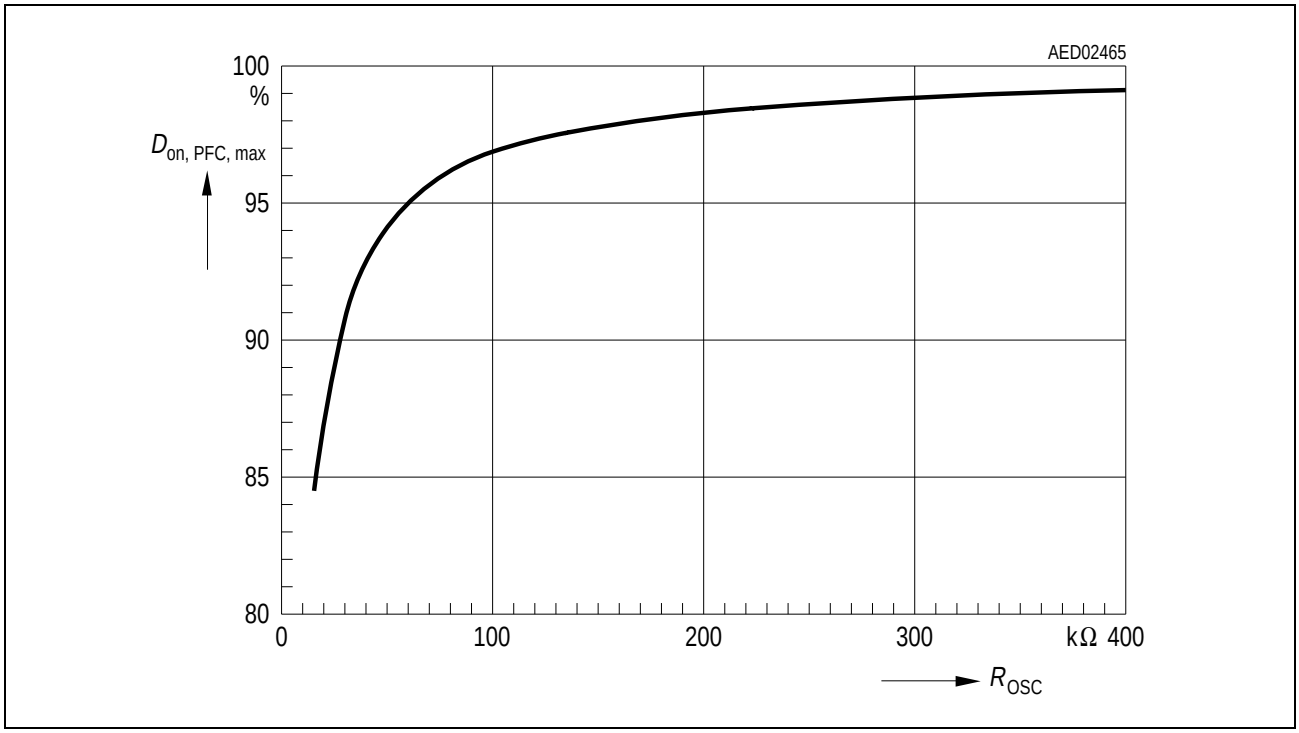


Figure 6 Maximum PFC Duty Cycle

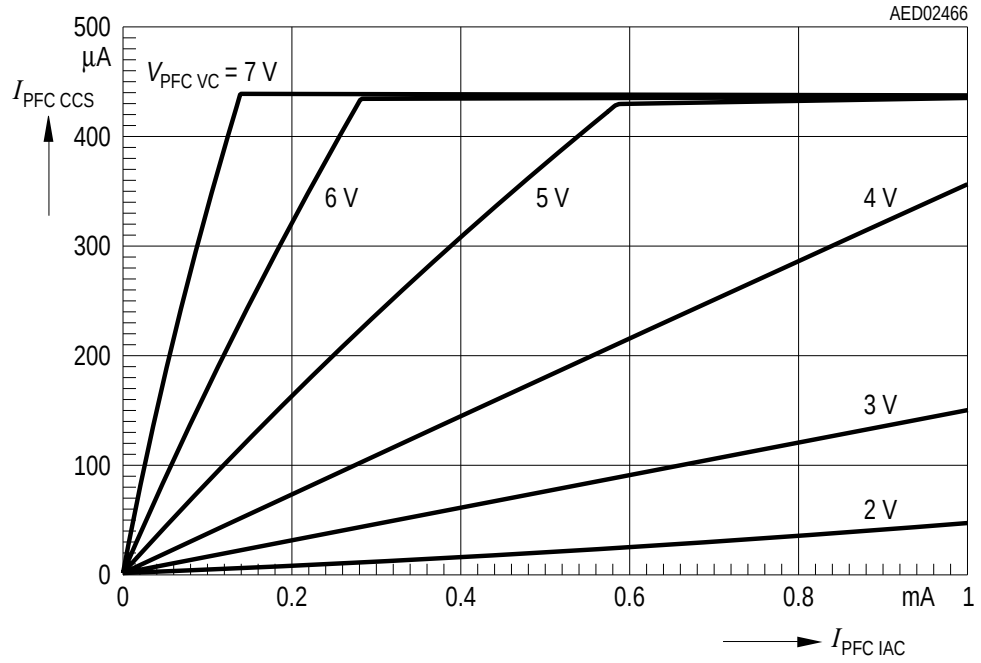


Figure 7 Multiplier Linearity

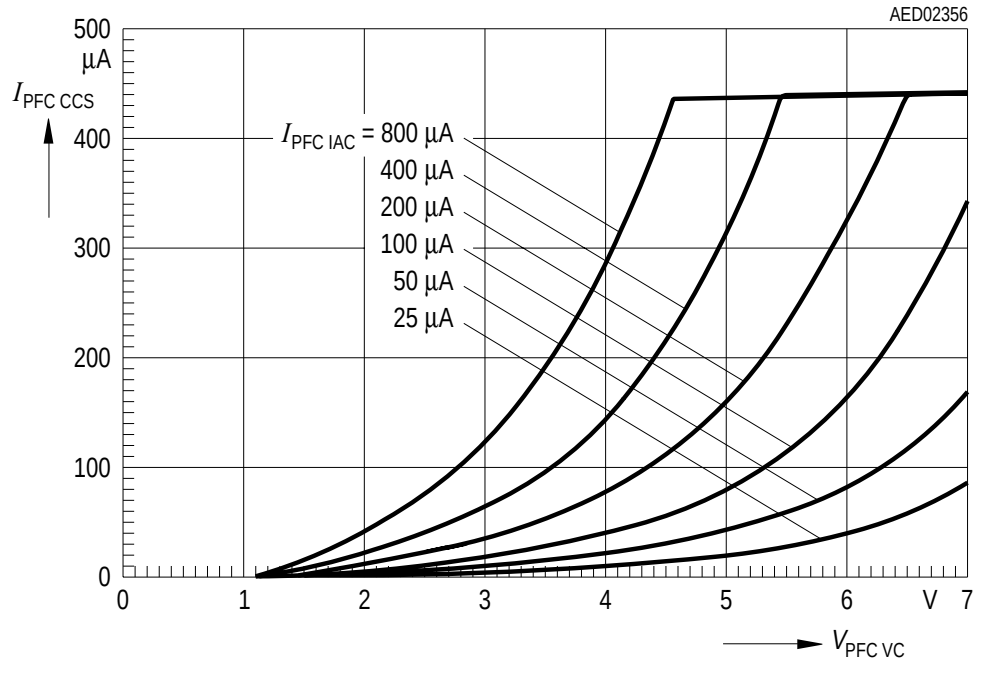


Figure 8 Multiplier Dynamic

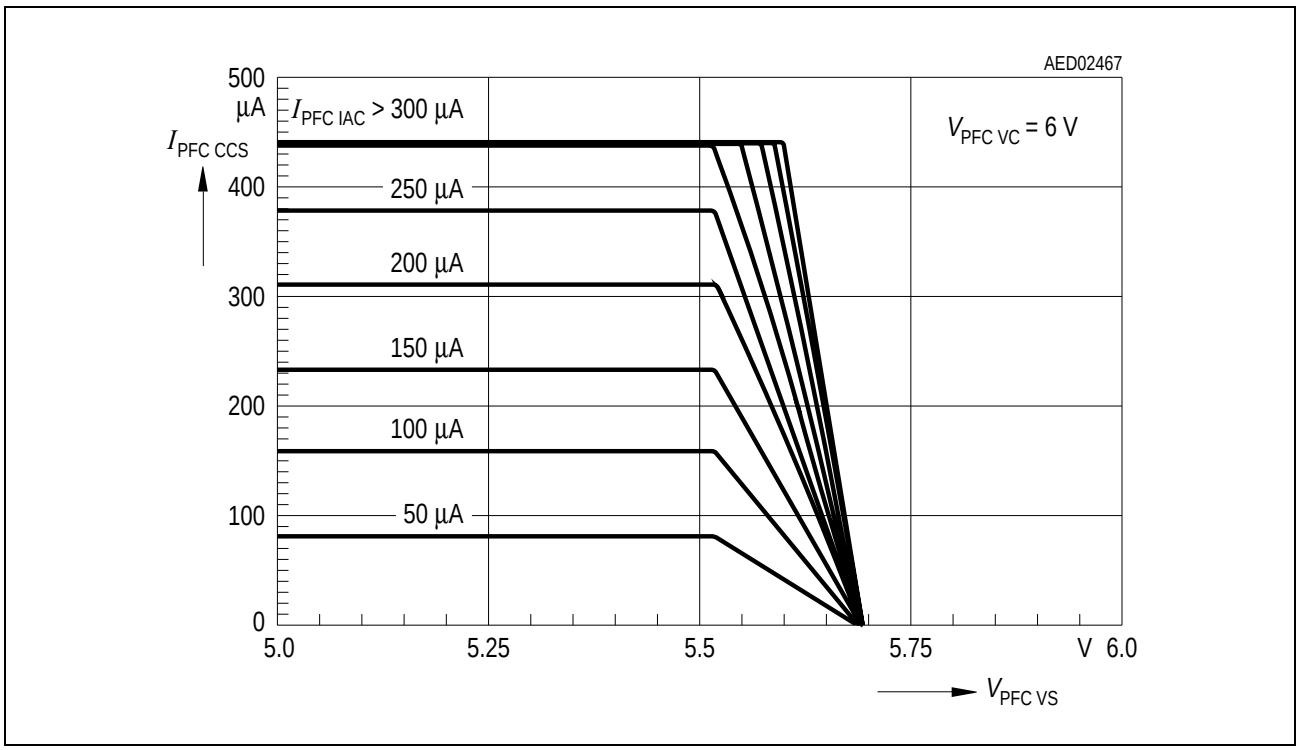


Figure 9 Multiplier Throttling by OTA2

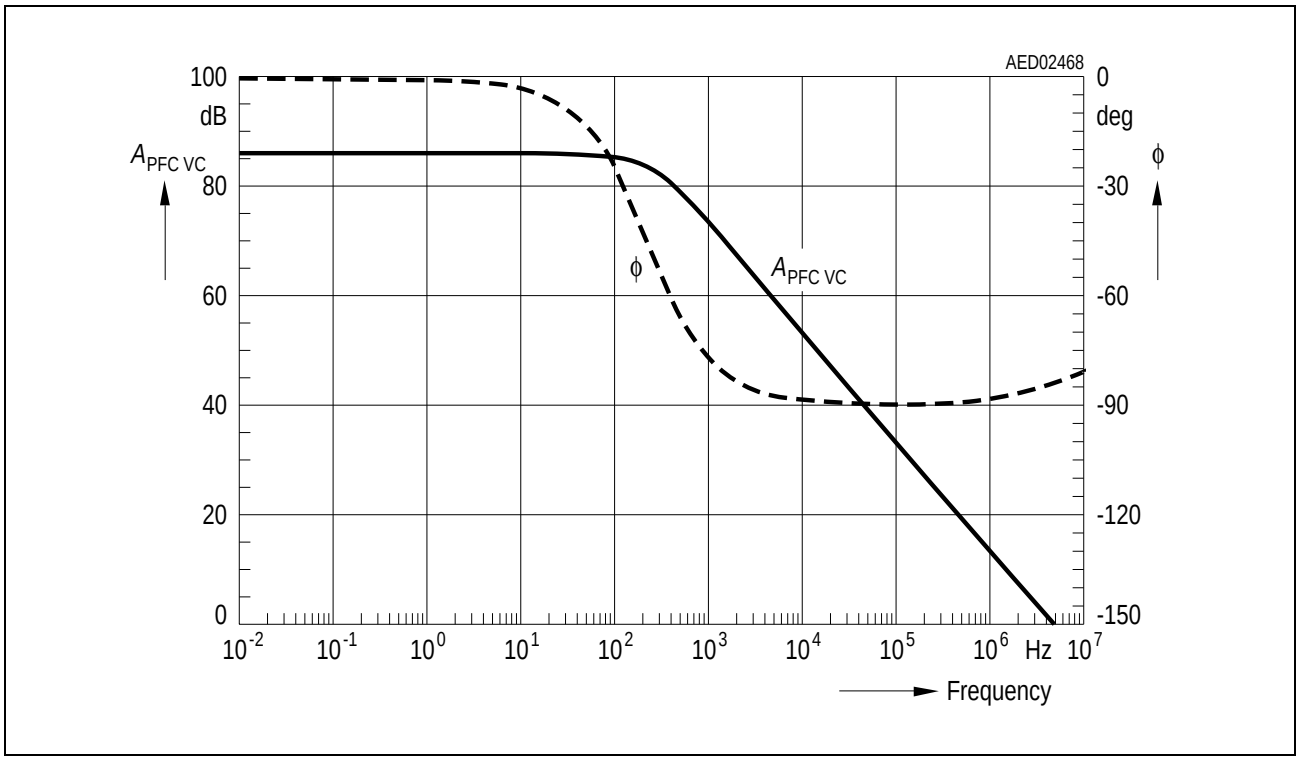


Figure 10 Open Loop Gain and Phase Characteristic of Voltage Amplifier OP1

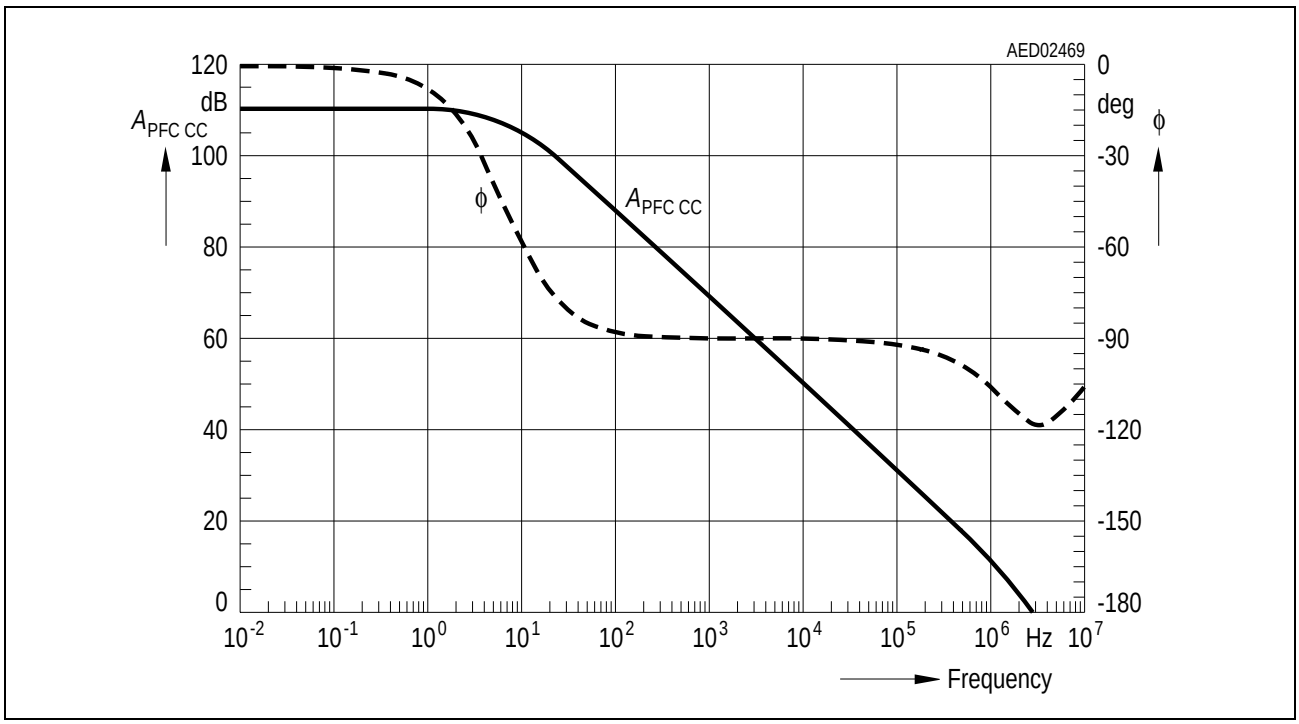


Figure 11 Open Loop Gain and Phase Characteristic of Current Amplifier OP2

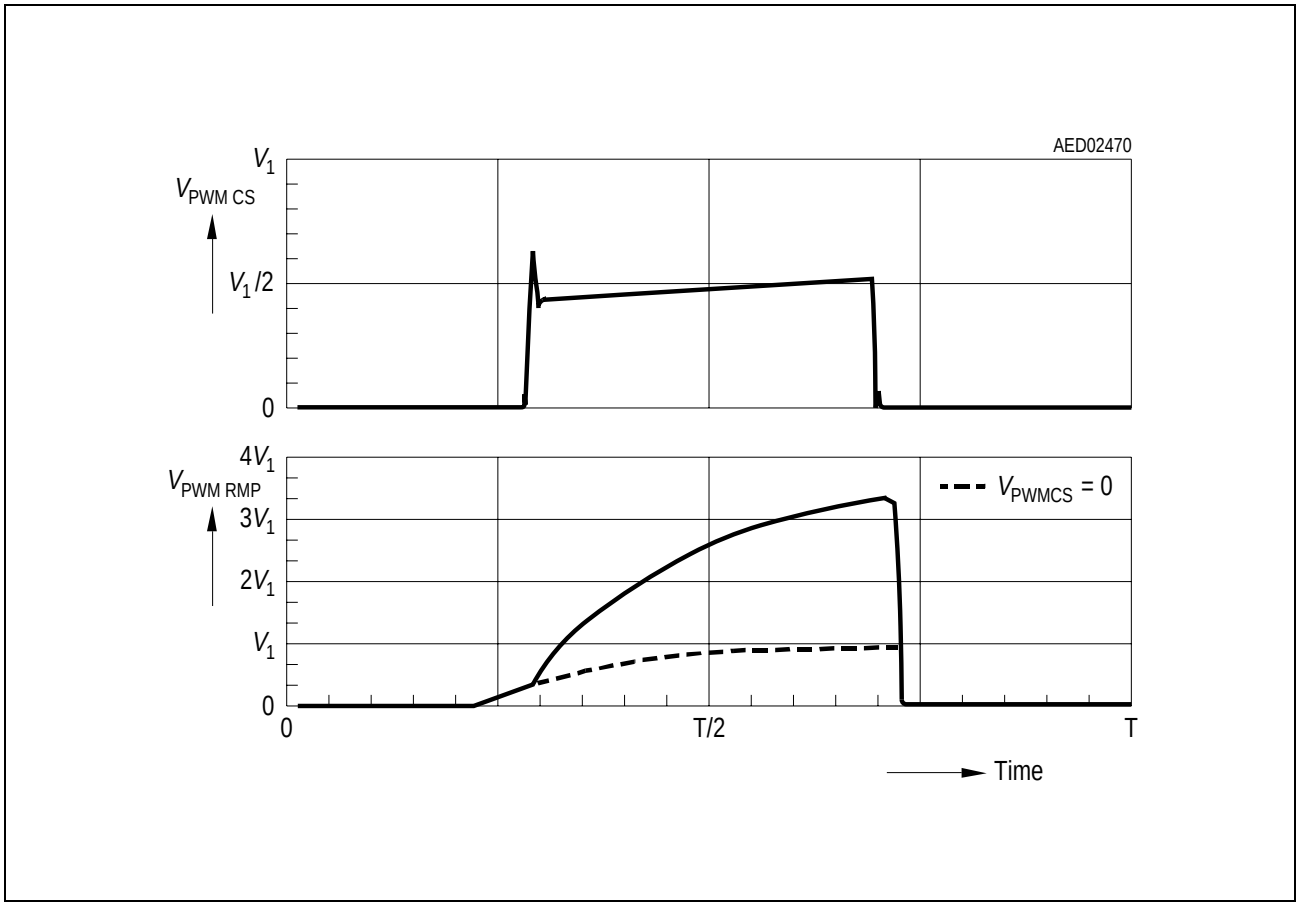


Figure 12 PWM Ramp Composition Scheme

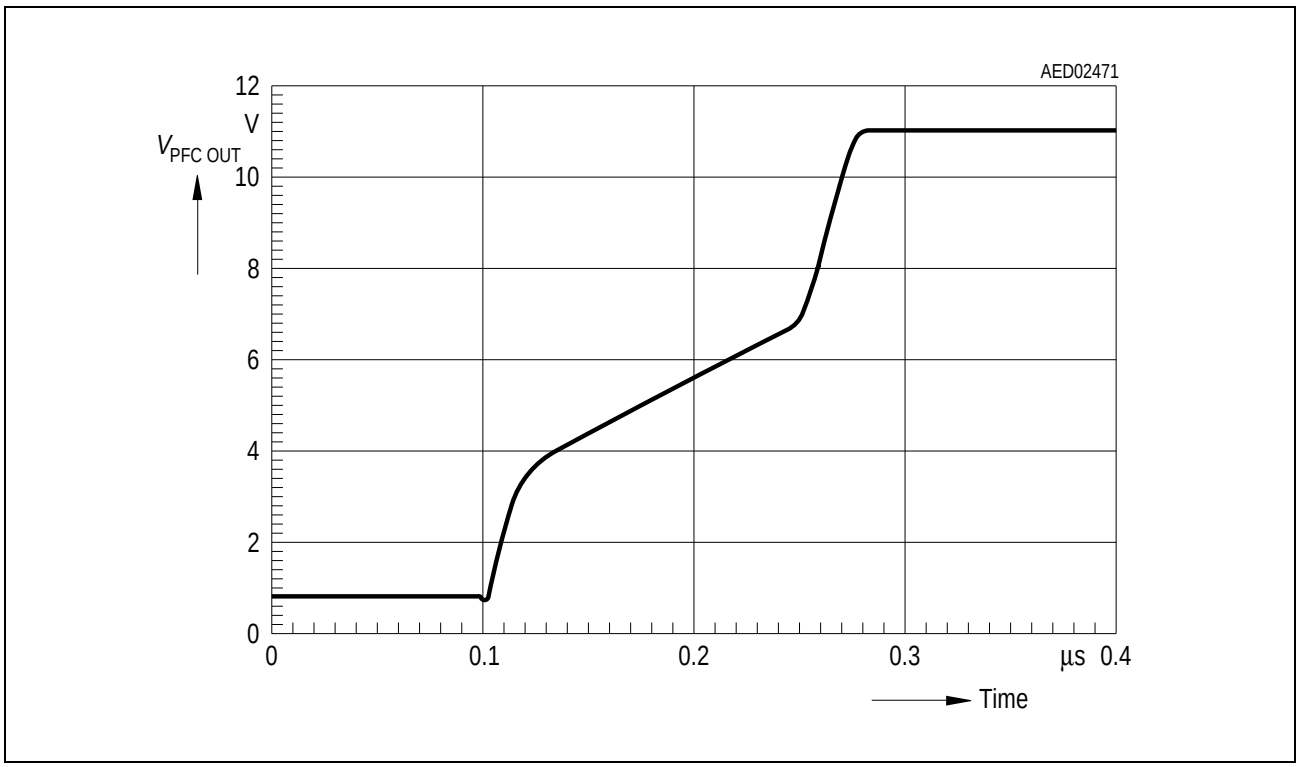


Figure 13 Rising Edge of Driver Output

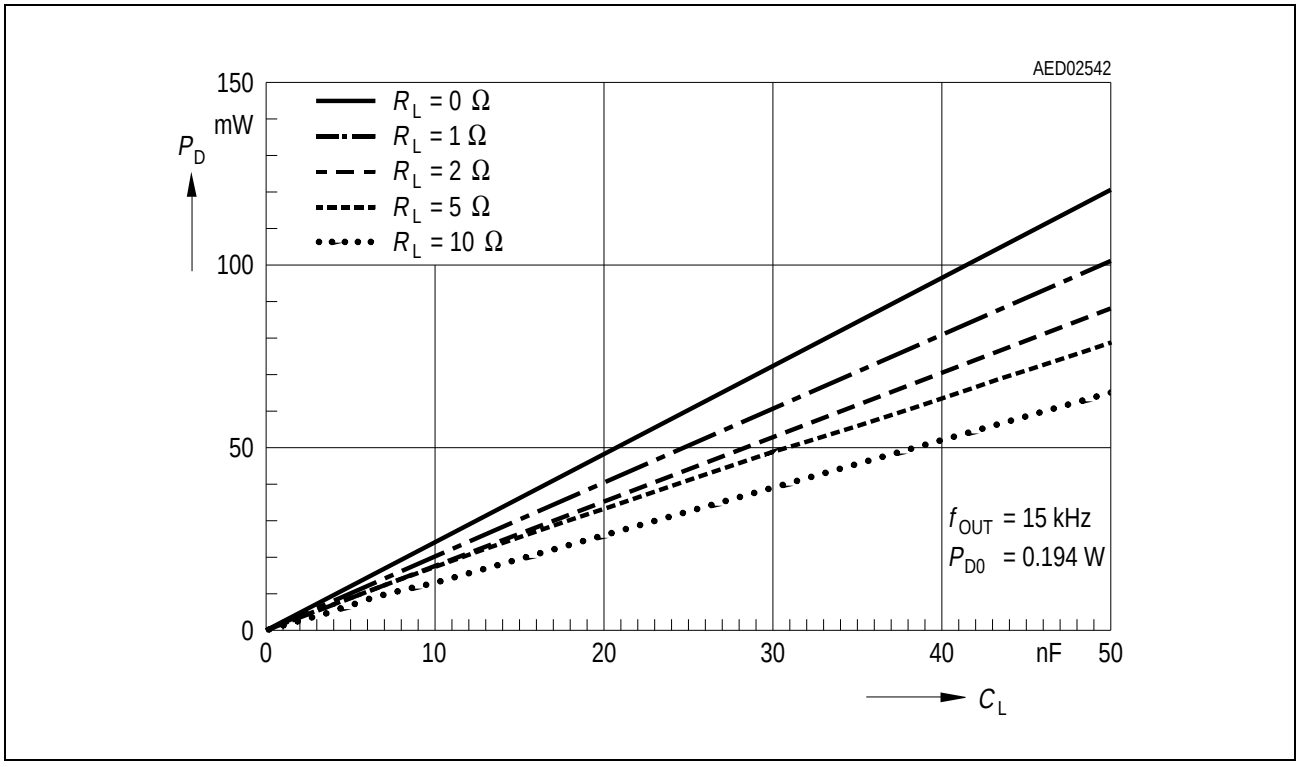


Figure 14 Power Dissipation of Single Gate Driver at f_{OUT} = 15 kHz

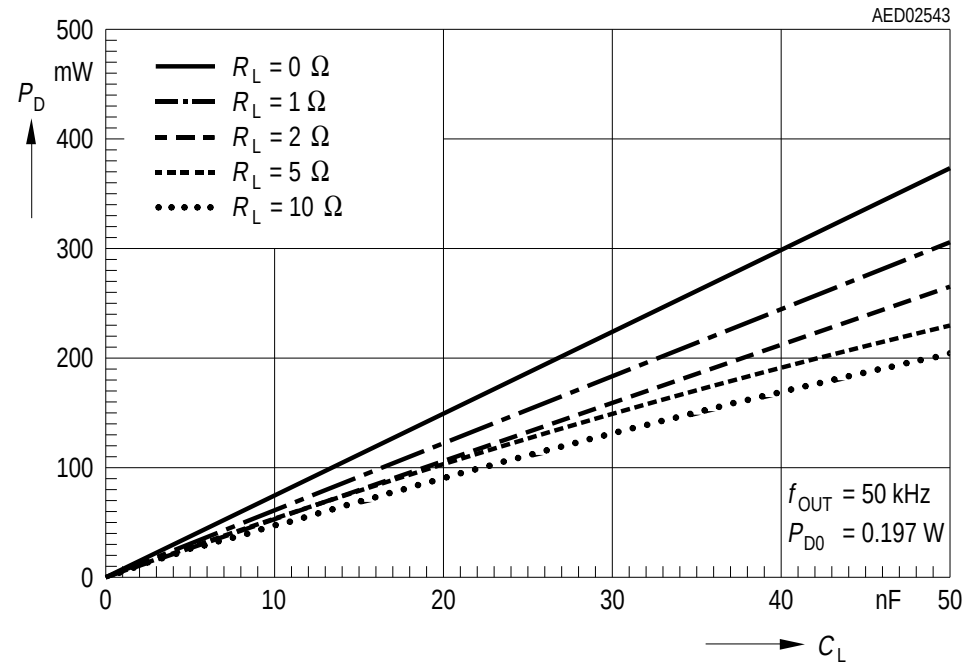


Figure 15 Power Dissipation of Single Gate Driver at f_{OUT} = 50 kHz

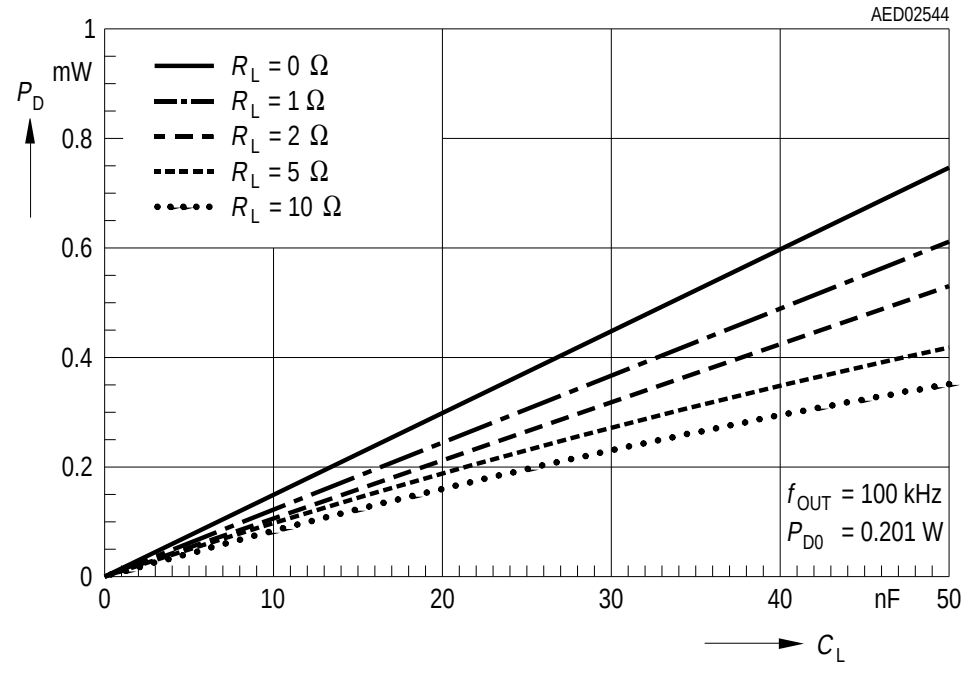


Figure 16 Power Dissipation of Single Gate Driver at f_{OUT} = 100 kHz

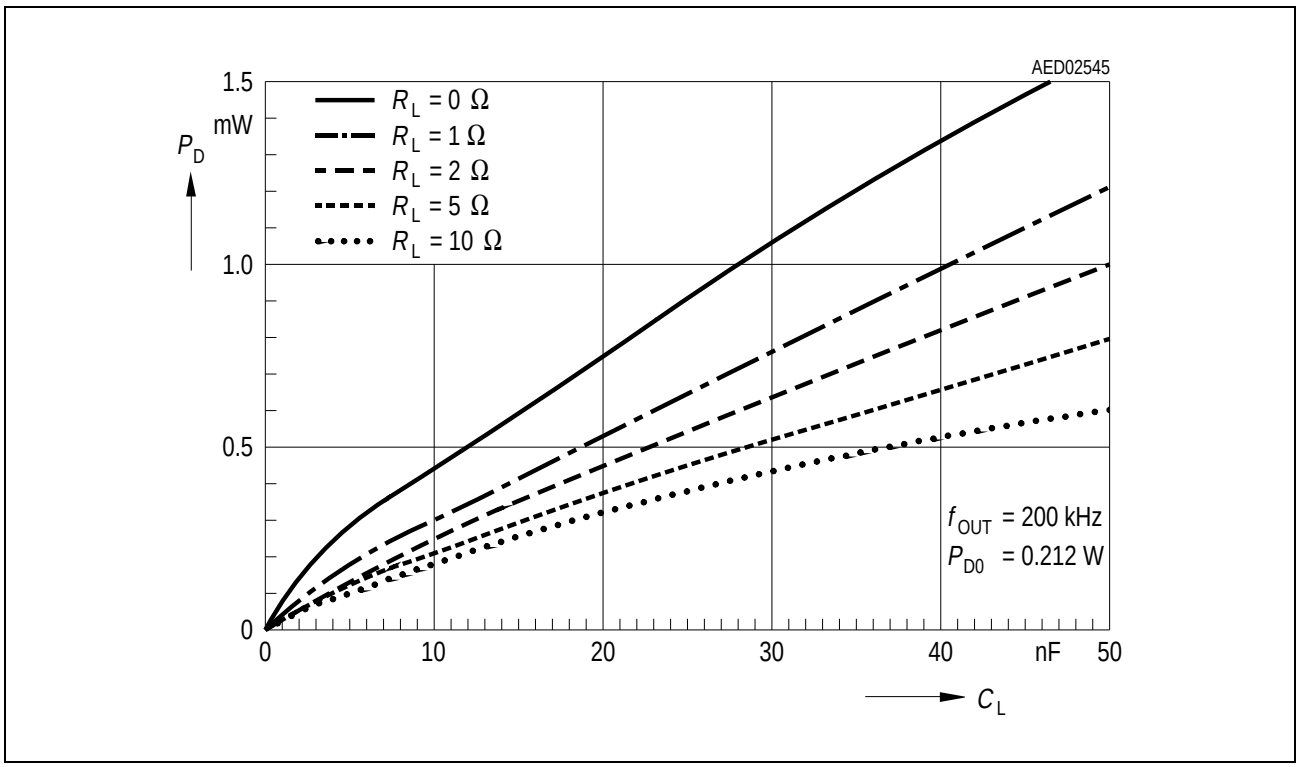


Figure 17 Power Dissipation of Single Gate Driver at f_{OUT} = 200 kHz

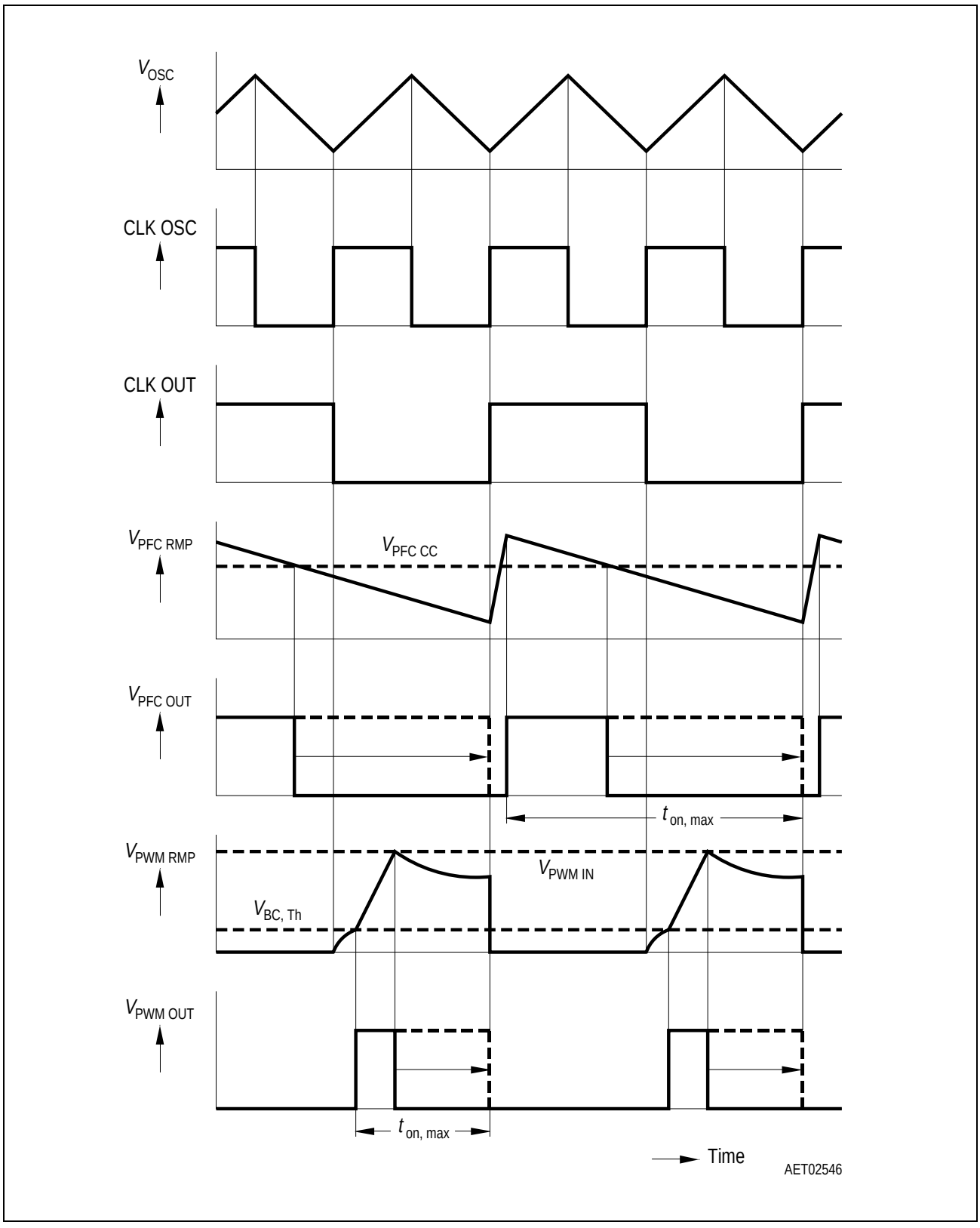


Figure 18 Timing Diagram without Synchronization

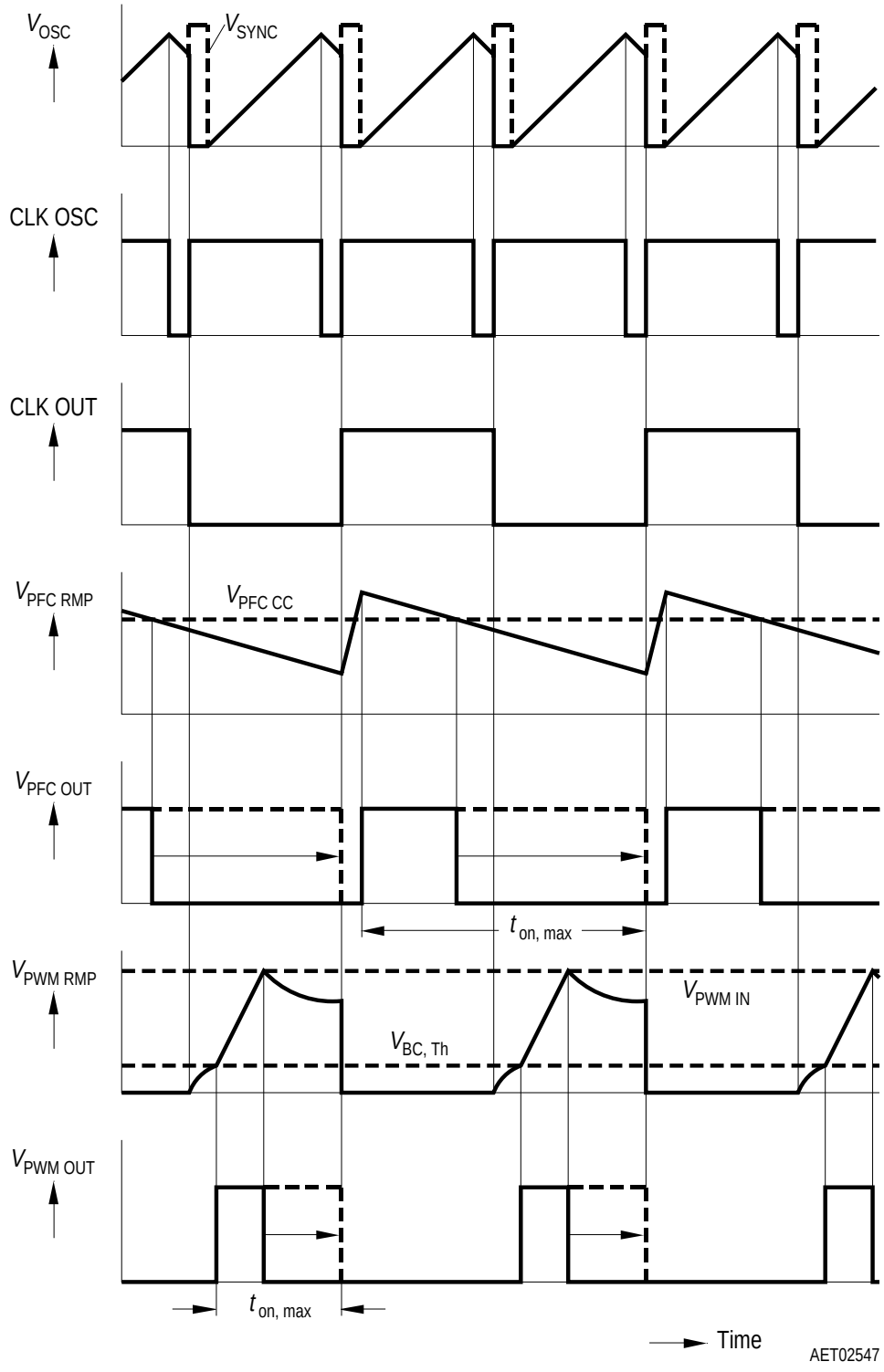


Figure 19 Timing Diagram with Synchronization ($f_{SYNC} > f_{OSC}$)

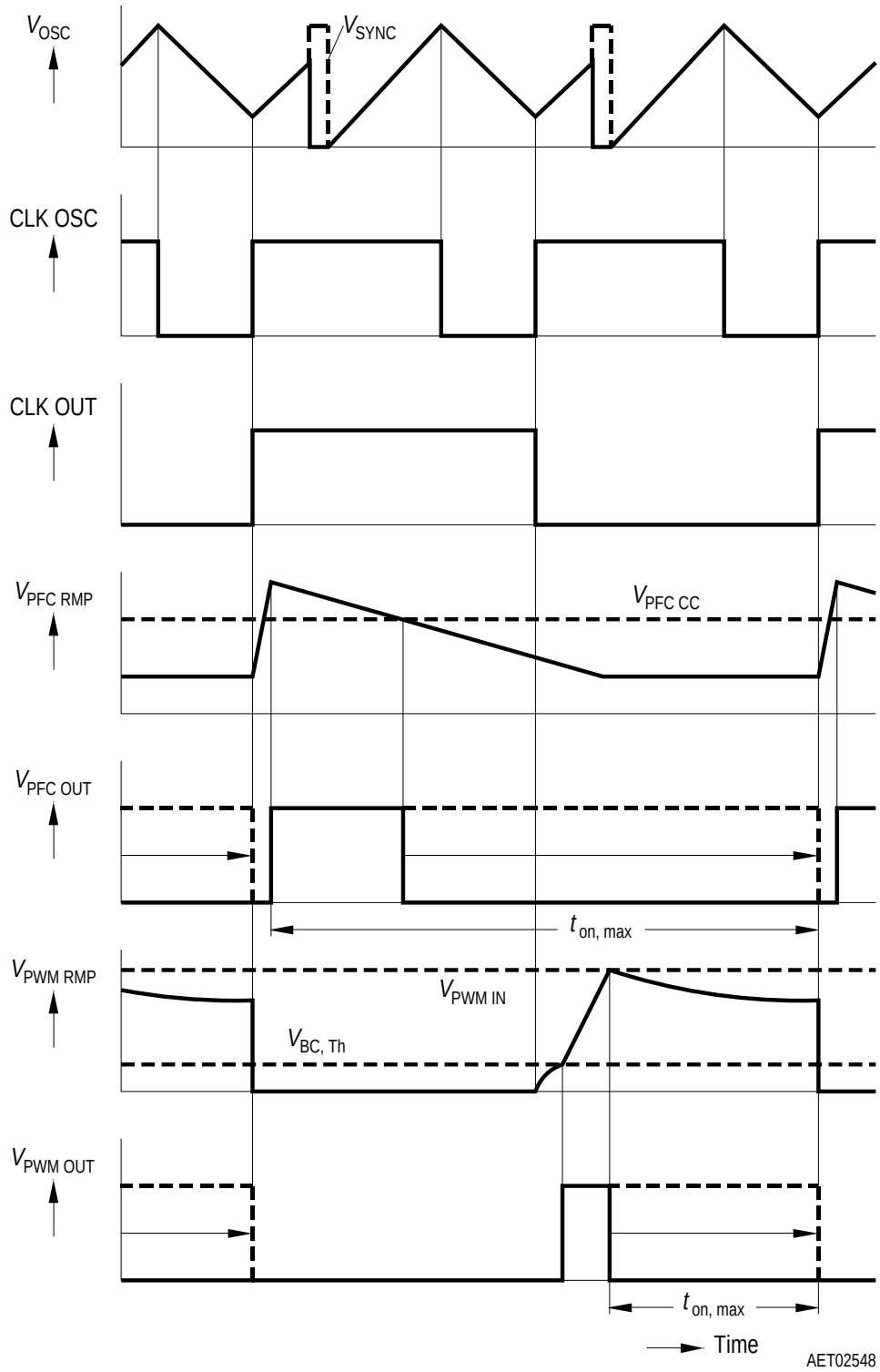
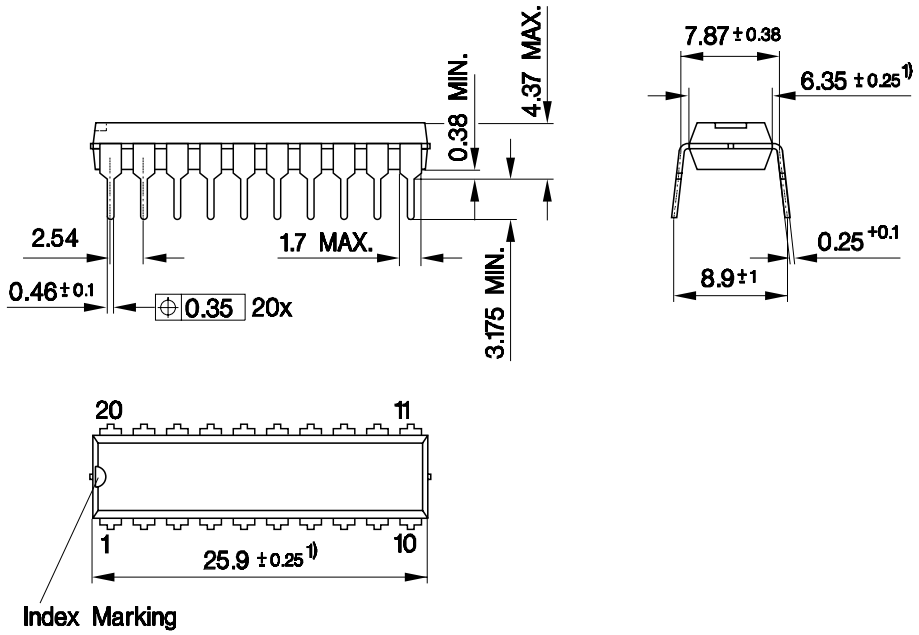


Figure 20 Timing Diagram with Synchronization ($f_{SYNC} < f_{OSC}$)

5 Package Outlines

P-DIP-20-5
(Plastic Dual In-line Package)



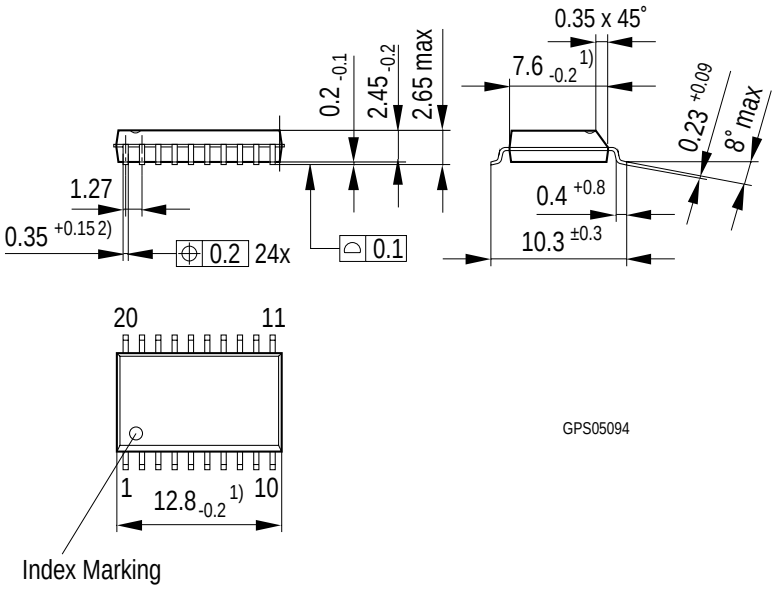
1) Does not include plastic or metal protrusion of 0.25 max. per side

GPD05587

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

Dimensions in mm

P-DSO-20-1
(Plastic Dual Small Outline)



1) Does not include plastic or metal protrusions of 0.15 max per side
2) Does not include dambar protrusion of 0.05 max per side

GPS 05094

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm