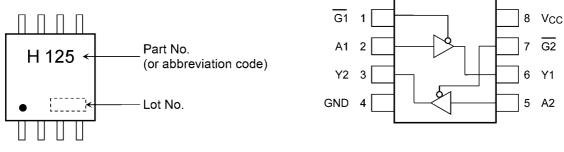
#### 4. Marking and Pin Assignment



Marking



#### 5. IEC Logic Symbol



#### 6. Truth Table

G	А	Y
Н	Х	Z
L	L	L
L	Н	Н

X: Don't care

Z: High impedance

### 7. Absolute Maximum Ratings (Note) (Unless otherwise specified, T<sub>a</sub> = 25 °C)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V <sub>CC</sub>		-0.5 to 7.0	V
Input voltage	V <sub>IN</sub>		-0.5 to 7.0	
DC output voltage	V <sub>OUT</sub>		-0.5 to V <sub>CC</sub> + 0.5	
Input diode current	I <sub>IK</sub>		-20	mA
Output diode current	I <sub>OK</sub>	(Note 1)	±20	1
DC output current	I <sub>OUT</sub>		±25	
V <sub>CC</sub> /ground current	I <sub>CC</sub>		±50	
Power dissipation	PD		300	mW
Storage temperature	T <sub>stg</sub>		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1:  $V_{OUT}$  < GND,  $V_{OUT}$  >  $V_{CC}$ 

#### 8. Operating Ranges (Note)

Characteristics	Symbol	Note	Test Condition	Rating	Unit
Supply voltage	V <sub>CC</sub>		—	2.0 to 5.5	V
Input voltage	V <sub>IN</sub>		—	0 to 5.5	
Output voltage	V <sub>OUT</sub>		—	0 to V <sub>CC</sub>	
Operating temperature	T <sub>opr</sub>	(Note 1)	—	-40 to 125	°C
		(Note 2)	_	-40 to 85	
Input rise and fall time	dt/dv		$V_{CC}$ = 3.3 ± 0.3 V	0 to 100	ns/V
			$V_{CC}$ = 5.0 ± 0.5 V	0 to 20	

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either  $V_{CC}$  or GND.

Note 1: For devices with the ordering part number ending in J(CT.

Note 2: For devices except those with the ordering part number ending in J(CT.

#### 9. Electrical Characteristics

#### 9.1. DC Characteristics (Unless otherwise specified, Ta = 25 °C)

Characteristics	Symbol	Test Condition		V <sub>CC</sub> (V)	Min	Тур.	Max	Unit
High-level input voltage	V <sub>IH</sub>	—		2.0	1.5	_	—	V
				3.0 to 5.5	$V_{CC} \times 0.7$	_	_	
Low-level input voltage	VIL	—		2.0	—	_	0.5	V
				3.0 to 5.5	—	_	$V_{CC} \times 0.3$	
High-level output voltage	V <sub>OH</sub>	$V_{IN} = V_{IH} \text{ or } V_{IL}$	I <sub>OH</sub> = -50 μA	2.0	1.9	2.0	—	V
				3.0	2.9	3.0	—	
				4.5	4.4	4.5	—	
			I <sub>OH</sub> = -4 mA	3.0	2.58	_	—	
			I <sub>OH</sub> = -8 mA	4.5	3.94	_	—	
Low-level output voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IL</sub>	I <sub>OL</sub> = 50 μA	2.0	—	0.0	0.1	V
				3.0	—	0.0	0.1	
				4.5	—	0.0	0.1	
			I <sub>OL</sub> = 4 mA	3.0	—	_	0.36	
			I <sub>OL</sub> = 8 mA	4.5	—		0.36	
3-state output OFF-state leakage current	I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND		5.5	—	_	±0.25	μA
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = 5.5 V or GND		0 to 5.5	—		±0.1	μA
Quiescent supply current	I <sub>CC</sub>	$V_{IN} = V_{CC}$ or GND		5.5		_	2.0	μA

#### 9.2. DC Characteristics (Unless otherwise specified, T<sub>a</sub> = -40 to 85 °C)

Characteristics	Symbol	Test Conditi	on	V <sub>CC</sub> (V)	Min	Max	Unit
High-level input voltage	V <sub>IH</sub>	_		2.0	1.5	—	V
				3.0 to 5.5	$V_{CC} \times 0.7$	_	
Low-level input voltage	VIL	_		2.0	_	0.5	V
				3.0 to 5.5	_	$V_{CC} \times 0.3$	
High-level output voltage	V <sub>OH</sub>	$V_{IN} = V_{IH} \text{ or } V_{IL}$	I <sub>OH</sub> = -50 μA	2.0	1.9	—	V
				3.0	2.9	—	
				4.5	4.4	—	
			I <sub>OH</sub> = -4 mA	3.0	2.48	—	
			I <sub>OH</sub> = -8 mA	4.5	3.80	—	
Low-level output voltage	V <sub>OL</sub>	$V_{IN} = V_{IL}$	I <sub>OL</sub> = 50 μA	2.0	—	0.1	V
				3.0	—	0.1	
				4.5	_	0.1	
			I <sub>OL</sub> = 4 mA	3.0	—	0.44	
			I <sub>OL</sub> = 8 mA	4.5	_	0.44	
3-state output OFF-state leakage current	I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND		5.5	_	±2.5	μA
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = 5.5 V or GND		0 to 5.5	_	±1.0	μA
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND		5.5	_	20.0	μA

#### 9.3. DC Characteristics (Note) (Unless otherwise specified, $T_a = -40$ to 125 °C)

Characteristics	Symbol	Test Cond	ition	V <sub>CC</sub> (V)	Min	Max	Unit
High-level input voltage	V <sub>IH</sub>	—		2.0	1.5	—	V
				3.0 to 5.5	$V_{CC} \times 0.7$	—	
Low-level input voltage	VIL	—		2.0	—	0.5	V
				3.0 to 5.5	—	$V_{CC} \times 0.3$	
High-level output voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 μA	2.0	1.9	—	V
				3.0	2.9	—	
				4.5	4.4	—	
			I <sub>OH</sub> = -4 mA	3.0	2.40	—	
			I <sub>OH</sub> = -8 mA	4.5	3.70	—	
Low-level output voltage	V <sub>OL</sub>	$V_{IN} = V_{IL}$	I <sub>OL</sub> = 50 μA	2.0	—	0.1	V
				3.0	_	0.1	
				4.5	—	0.1	
			I <sub>OL</sub> = 4 mA	3.0	—	0.55	
			I <sub>OL</sub> = 8 mA	4.5	—	0.55	
3-state output OFF-state leakage current	I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND		5.5	—	±10.0	μA
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = 5.5 V or GND		0 to 5.5	_	±2.0	μA
Quiescent supply current	I <sub>CC</sub>	$V_{IN} = V_{CC}$ or GND		5.5		40.0	μA

Note: For devices with the ordering part number ending in J(CT.

#### 9.4. AC Characteristics (Unless otherwise specified, $T_a = 25$ °C, Input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Note	Test Condition	V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	Min	Тур.	Max	Unit
Propagation delay time	t <sub>PLH</sub> ,t <sub>PHL</sub>		_	$\textbf{3.3}\pm\textbf{0.3}$	15	—	5.6	8.0	ns
					50	_	8.1	11.5	
				$5.0\pm0.5$	15	_	3.8	5.5	
					50		5.3	7.5	
3-state output enable time	t <sub>PZL</sub> ,t <sub>PZH</sub>		R <sub>L</sub> = 1 kΩ	$\textbf{3.3}\pm\textbf{0.3}$	15	_	5.4	8.0	ns
					50	_	7.9	11.5	
				$5.0\pm0.5$	15		3.6	5.1	
					50	_	5.1	7.1	
3-state output disable time	t <sub>PLZ</sub> ,t <sub>PHZ</sub>		R <sub>L</sub> = 1 kΩ	$3.3\pm0.3$	50		9.5	13.2	ns
				$5.0\pm0.5$	50		6.1	8.8	
Output skew	t <sub>osLH</sub> ,t <sub>osHL</sub>	(Note 1)	—	$3.3\pm0.3$	50	_	_	1.5	ns
				$5.0\pm0.5$	50			1.0	
Input capacitance	C <sub>IN</sub>		_				4	10	pF
Output capacitance	C <sub>OUT</sub>		_			_	6	_	pF
Power dissipation capacitance	C <sub>PD</sub>	(Note 2)	—			—	14	—	pF

Note 1: Parameter guaranteed by design. ( $t_{osLH} = |t_{PLH}m-t_{PLH}n|$ ,  $t_{osHL} = |t_{PHL}m-t_{PHL}n|$ )

Note 2: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

 $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per 1 bit)}$ 

## 9.5. AC Characteristics (Unless otherwise specified, $T_a = -40$ to 85 °C, Input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Note	Test Condition	V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	Min	Max	Unit
Propagation delay time	t <sub>PLH</sub> ,t <sub>PHL</sub>		—	$3.3\pm 0.3$	15	1.0	9.5	ns
					50	1.0	13.0	
				$5.0\pm0.5$	15	1.0	6.5	
					50	1.0	8.5	
3-state output enable time	t <sub>PZL</sub> ,t <sub>PZH</sub>		$R_L$ = 1 k $\Omega$	$\textbf{3.3}\pm\textbf{0.3}$	15	1.0	9.5	ns
					50	1.0	13.0	
				$5.0\pm0.5$	15	1.0	6.0	
					50	1.0	8.0	
3-state output disable time	t <sub>PLZ</sub> ,t <sub>PHZ</sub>		R <sub>L</sub> = 1 kΩ	$\textbf{3.3}\pm\textbf{0.3}$	50	1.0	15.0	ns
				$5.0\pm0.5$	50	1.0	10.0	
Output skew	t <sub>osLH</sub> ,t <sub>osHL</sub>	(Note 1)	—	$\textbf{3.3}\pm\textbf{0.3}$	50	_	1.5	ns
				$5.0\pm0.5$	50	_	1.0	
Input capacitance	C <sub>IN</sub>		_			_	10	pF

Note 1: Parameter guaranteed by design. ( $t_{osLH} = |t_{PLH}m-t_{PLH}n|$ ,  $t_{osHL} = |t_{PHL}m-t_{PHL}n|$ )

#### 9.6. AC Characteristics (Note) (Unless otherwise specified, $T_a = -40$ to 125 °C, Input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Note	Test Condition	V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	Min	Max	Unit
Propagation delay time	t <sub>PLH</sub> ,t <sub>PHL</sub>		_	$\textbf{3.3}\pm\textbf{0.3}$	15	1.0	11.0	ns
					50	1.0	14.5	
				$5.0\pm0.5$	15	1.0	7.5	
					50	1.0	9.5	
3-state output enable time	t <sub>PZL</sub> ,t <sub>PZH</sub>		$R_L = 1 k\Omega$	$\textbf{3.3}\pm\textbf{0.3}$	15	1.0	11.0	ns
					50	1.0	14.5	
				$5.0\pm0.5$	15	1.0	7.0	
					50	1.0	9.0	
3-state output disable time	t <sub>PLZ</sub> ,t <sub>PHZ</sub>		R <sub>L</sub> = 1 kΩ	$\textbf{3.3}\pm\textbf{0.3}$	50	1.0	16.5	ns
				$5.0\pm0.5$	50	1.0	11.0	
Output skew	t <sub>osLH</sub> ,t <sub>osHL</sub>	(Note 1)	_	$3.3\pm0.3$	50	_	1.5	ns
				$5.0\pm0.5$	50	_	1.0	
Input capacitance	C <sub>IN</sub>		_			_	10	pF

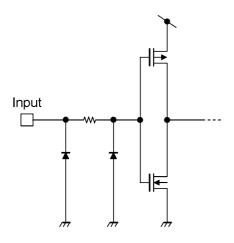
Note: For devices with the ordering part number ending in J(CT.

Note 1: Parameter guaranteed by design.  $(t_{osLH} = |t_{PLH}m-t_{PLH}n|, t_{osHL} = |t_{PHL}m-t_{PHL}n|)$ 

#### 9.7. Noise Characteristics (Unless otherwise specified, $T_a = 25$ °C, Input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Тур.	Limit	Unit
Quiet output maximum dynamic V <sub>OL</sub>	V <sub>OLP</sub>	C <sub>L</sub> = 50 pF	5.0	0.3	0.8	V
Quiet output minimum dynamic V <sub>OL</sub>	V <sub>OLV</sub>	C <sub>L</sub> = 50 pF	5.0	-0.3	-0.8	V
Minimum high-level dynamic input voltage	V <sub>IHD</sub>	C <sub>L</sub> = 50 pF	5.0	_	3.5	V
Maximum low-level dynamic input voltage	V <sub>ILD</sub>	C <sub>L</sub> = 50 pF	5.0	_	1.5	V

#### 10. Input Equivalent Circuit

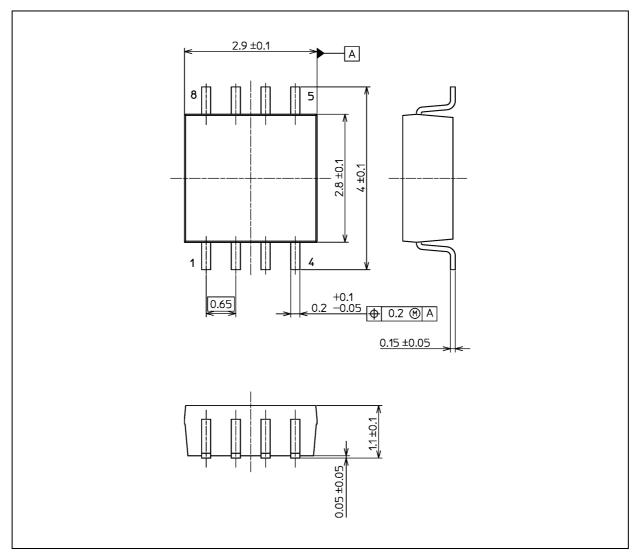




## TC7WH125FU

#### **Package Dimensions**

Unit: mm



Weight: 21 mg (typ.)

	Package Name(s)	
JEDEC: SOT-505		
Nickname: SM8		

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