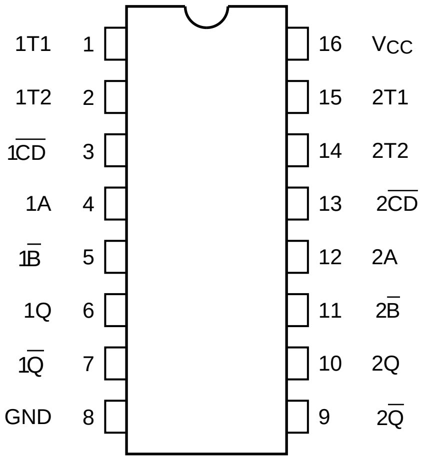
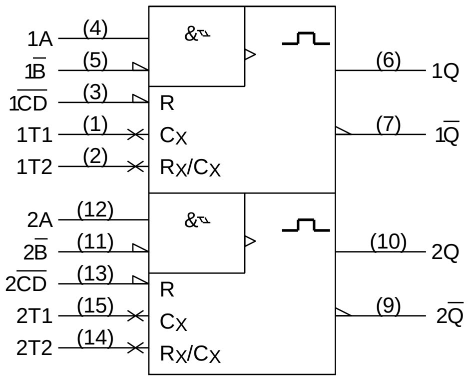
Pin Assignment



(top view)

IEC Logic Symbol

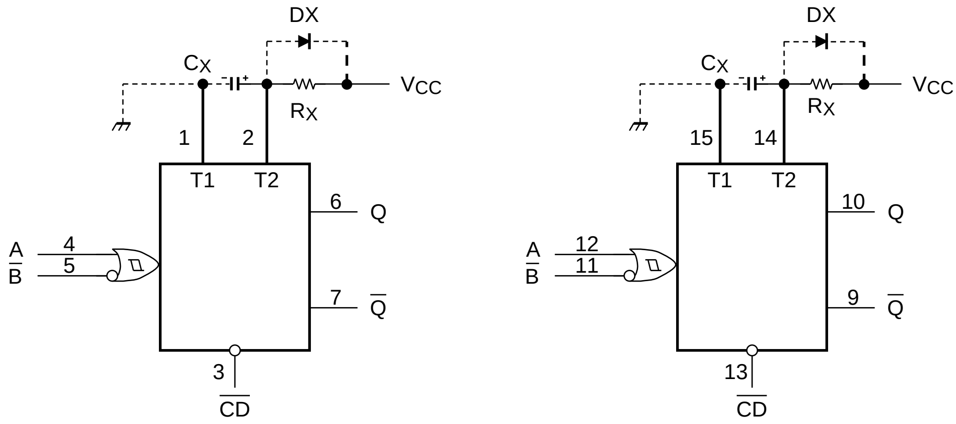


Truth Table

Inputs			Outputs		Note
A	$\overline{B}$	$\overline{CD}$	Q	$\overline{Q}$	
↑	H	H	⊓	⊔	Output Enable
X	L	H	L	H	Inhibit
H	X	H	L	H	Inhibit
L	↓	H	⊓	⊔	Output Enable
X	X	L	L	H	Reset

X: Don't care

Block Diagram (Note)



Note: C_X, R_X, D_X are external capacitor, resistor, and diode, respectively.

Note: External clamping diode, D_X

The external capacitor is charged to V_{CC} level in the wait state, i.e. when no trigger is applied. Supply voltage is turned off and C_X is discharged mainly through the internal (parasitic) diode. If C_X is sufficiently large and V_{CC} drops rapidly, there will be some possibility of damaging the IC by rush current or latch-up. If the capacitance of the supply voltage filter is large enough and V_{CC} drops slowly, the rush current is automatically limited and damage to the IC is avoided.

The maximum value of forward current through the parasitic diode is ±20 mA.

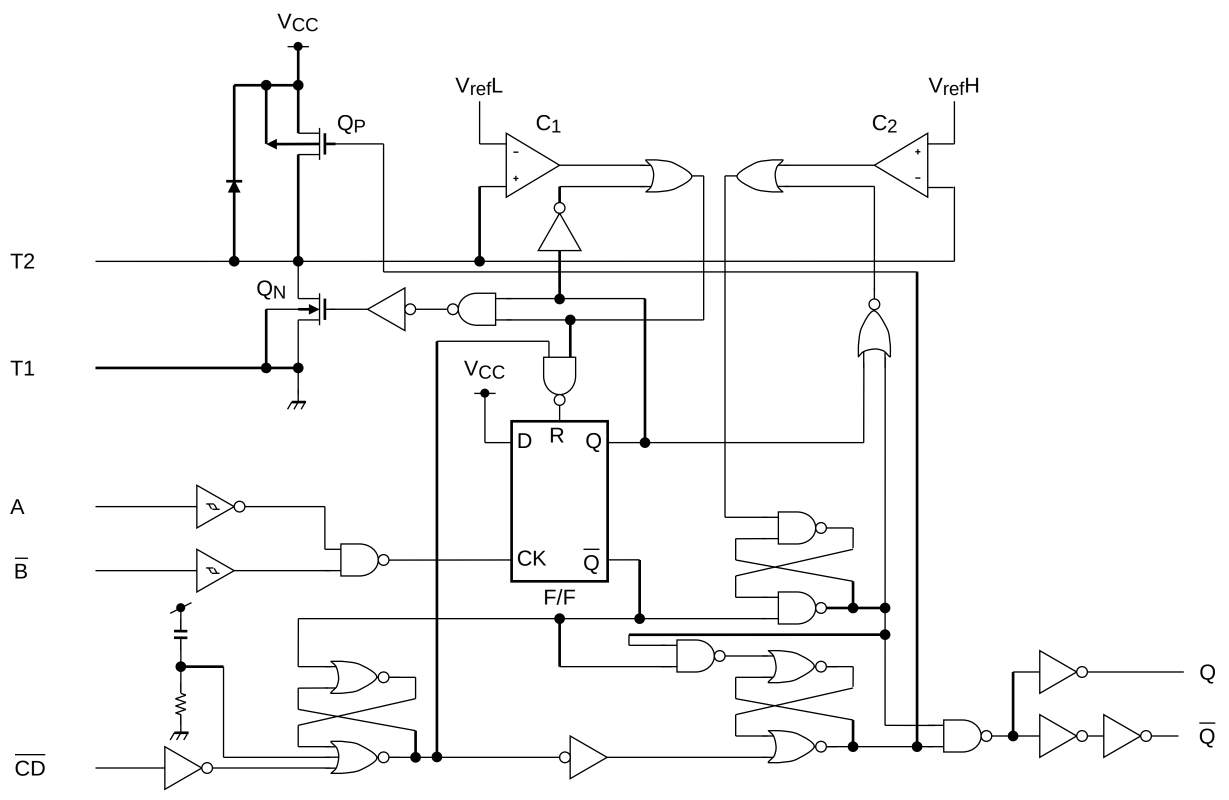
In the case of a large C_X, the limitation of fall time of the supply voltage is determined as follows:

$t_f \geq (V_{CC} - 0.7)\ C_X/20\ mA$

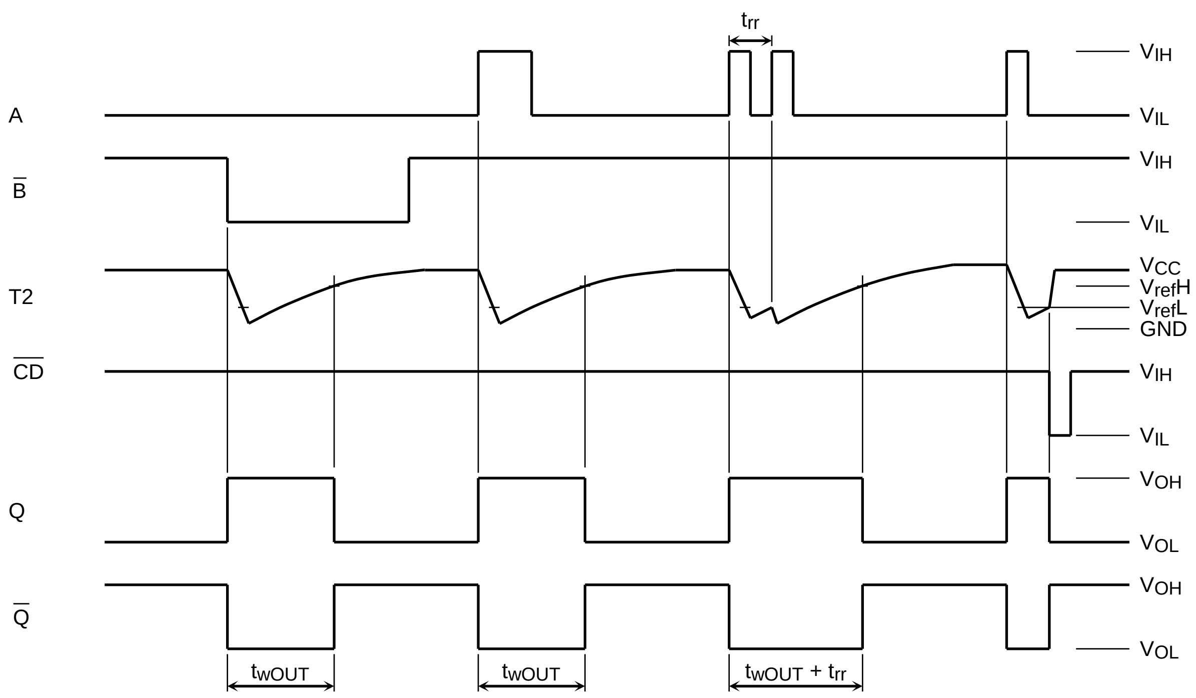
(t_f is the time from the voltage supply turning off to the level of supply voltage reaching 0.4 V_{CC}.)

In the care of a system that does not satisfy the above condition, an external clamping diode is needed to protect the IC from rush current.

System Diagram



Timing Chart



Functional Description

(1) Stand-by state

The external capacitor is fully charge to V_{CC} in the stand-by state. That means, before triggering, Q_P and Q_N transistors which are connected to the T2 node are in the off state. Two comparators that relate to the timing of the output pulse, and two reference voltage supplies stop their operation. The total supply current is only leakage current.

(2) Trigger operation

Trigger operation is effective in either of the following two cases. One is the condition where the A input is low, and the $\overline{B}$ input has a falling signal. The other, where the $\overline{B}$ input is high, and the A input has a rising signal.

After trigger becomes effective, comparators C_1 and C_2 start operating, and Q_N is turned on. The external capacitor discharges through Q_N. The voltage level at the T2 node drops. If the T2 voltage level falls to the internal reference voltage $V_{ref}L$, the output of C_1 becomes low. The flip-flop is then reset and Q_N turns off. At that moment C_1 stops but C_2 continues operating.

After Q_N turns off, the voltage at T2 start rising at a rate determined by the time constant of external capacitor C_X and resistor R_X.

After the triggering, output Q becomes high, following some delay time of the internal F/F and gates. It stays high even if the voltage of T2 changes from falling to rising. When T2 reaches the internal reference voltage $V_{ref}H$, the output of C_2 becomes low, the output Q goes low and C_2 stops its operation. That means, after triggering, when the voltage level of T2 reaches $V_{ref}H$, the IC returns to its MONOSTABLE state.

In the case of large value of C_X and R_X, and ignoring the discharge time of the capacitor and internal delays of the IC, the width of the output pulse, (t_{wOUT}), is as follows:

$$t_{wOUT} = 0.70 \cdot C_X \cdot R_X$$

(3) Retrigger operation

When another new trigger is applied to input A or $\overline{B}$ while in the MONOSTABLE state, it is effective only if the IC is charging C_X. The voltage level of T2 then falls to $V_{ref}L$ level again.

Therefore the Q output stays high if the next trigger comes in before the time period set by C_X and R_X.

If the 2nd trigger is very close to previous trigger, such as application during the discharge cycle, the 2nd trigger will not be effective.

The minimum time for effective 2nd trigger, t_{rr} (min), depends on V_{CC} and C_X.

(4) Reset operation

In normal operation, $\overline{CD}$ input is held high. If $\overline{CD}$ is low, a trigger has no effect because the Q output is held low and the trigger control F/F is reset. Also Q_P turns on and C_X is charged rapidly to V_{CC}.

This means if $\overline{CD}$ input is set low, the IC goes into a wait state.

Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7	V
DC input voltage	V_{IN}	-0.5 to V_{CC} + 0.5	V
DC output voltage	V_{OUT}	-0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±25	mA
DC V_{CC}/ground current	I_{CC}	±50	mA
Power dissipation	P_D	500 (DIP) (Note 1)/180 (SOP/TSSOP)	mW
Storage temperature	T_{stg}	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: 500 mW in the range of Ta = -40°C to 65°C. From Ta = 65°C to 85°C a derating factor of -10 mW/°C should be applied up to 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2 to 6	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time ($\overline{CD}$ only)	t_r, t_f	0 to 1000 (V_{CC} = 2.0 V) 0 to 500 (V_{CC} = 4.5 V) 0 to 400 (V_{CC} = 6.5 V)	ns
External capacitor	C_X	No limitation (Note 1)	F
External resistor	R_X	≥ 5 k (V_{CC} = 2.0 V) (Note 1) ≥ 1 k (V_{CC} ≥ 3.0 V) (Note 1)	Ω

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Note 1: The maximum allowable values of C_X and R_X are a function of leakage of capacitor C_X, the leakage of TC74HC4538A, and leakage due to board layout and surface resistance.
Susceptibility to externally induced noise signals may occur for R_X > 1 MΩ.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = −40 to 85°C Min	Ta = −40 to 85°C Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	1.50	—	V
				4.5	3.15	—	—	3.15	—	
				6.0	4.20	—	—	4.20	—	
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	—	0.50	V
				4.5	—	—	1.35	—	1.35	
				6.0	—	—	1.80	—	1.80	
High-level output voltage (Q, $\overline{Q}$)	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20 μA	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
				6.0	5.9	6.0	—	5.9	—	
			I_{OH} = -4 mA	4.5	4.18	4.31	—	4.13	—	
			I_{OH} = -5.2 mA	6.0	5.68	5.80	—	5.63	—	
Low-level output voltage (Q, $\overline{Q}$)	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
				6.0	—	0.0	0.1	—	0.1	
			I_{OL} = 4 mA	4.5	—	0.17	0.26	—	0.33	
			I_{OL} = 5.2 mA	6.0	—	0.18	0.26	—	0.33	
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	—	±0.1	—	±1.0	μA
T2 terminal input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	—	±0.5	—	±5.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	—	—	4.0	—	40.0	μA
Active-state supply current (Note 1)	$I_{CC'}$	V_{IN} = V_{CC} or GND, R_X/C_X = 0.5 V_{CC}		2.0	—	40	120	—	160	μA
				4.5	—	200	300	—	400	
				6.0	—	300	600	—	800	

Note 1: Per circuit

Timing Requirements (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = -40 to 85°C	Unit
			V_{CC} (V)	Typ.	Max	Max	
Minimum pulse width (A, $\overline{B}$)	$t_{W (L)}$ $t_{W (H)}$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum clear width ($\overline{CD}$)	$t_{W (L)}$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum clear removal time	t_{rem}	—	2.0	—	15	15	ns
			4.5	—	5	5	
			6.0	—	5	5	
Minimum retrigger time	t_{rr}	R_X = 1 kΩ, C_X = 100 pF	2.0	380	—	—	ns
			4.5	92	—	—	
			6.0	72	—	—	
		R_X = 1 kΩ, C_X = 0.01 μF	2.0	6.0	—	—	μs
			4.5	1.4	—	—	
			6.0	1.2	—	—	

AC Characteristics (C_L = 15 pF, V_{CC} = 5 V, Ta = 25°C, input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	t_{TLH} t_{THL}	—	—	6	12	ns
Propagation delay time (A, $\overline{B}$ -Q, $\overline{Q}$)	t_{pLH} t_{pHL}	—	—	25	44	ns
Propagation delay time ($\overline{CD}$ -Q, $\overline{Q}$)	t_{pLH} t_{pHL}	—	—	21	34	ns

AC Characteristics (C_L = 50 pF, input: t_r = t_f = 6 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit
			V_{CC} (V)	Min	Typ.	Max	Min	Max	
Output transition time	t_{TLH} t_{THL}	—	2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation delay time (A, $\overline{B}$-Q, $\overline{Q}$)	t_{pLH} t_{pHL}	—	2.0	—	120	250	—	315	ns
			4.5	—	30	50	—	63	
			6.0	—	25	43	—	54	
Propagation delay time ($\overline{CD}$-Q, $\overline{Q}$)	t_{pLH} t_{pHL}	—	2.0	—	100	195	—	245	ns
			4.5	—	25	39	—	49	
			6.0	—	20	33	—	42	
Output pulse width	t_{wOUT}	C_X = 0 F	2.0	—	540	1200	—	1500	ns
		R_X = 5 kΩ (V_{CC} = 2 V)	4.5	—	180	250	—	320	
		R_X = 1 kΩ (V_{CC} = 4.5 V, 6 V)	6.0	—	150	200	—	260	
		C_X = 0.01 μF R_X = 10 kΩ	2.0	70	83	96	70	96	μs
			4.5	69	77	85	69	85	
			6.0	69	77	85	69	85	
		C_X = 0.1 μF R_X = 10 kΩ	2.0	0.67	0.75	0.83	0.67	0.83	ms
			4.5	0.67	0.73	0.77	0.67	0.77	
			6.0	0.67	0.73	0.77	0.67	0.77	
Output pulse width error between circuits (in same package)	Δt_{wOUT}	—	—	—	±1	—	—	—	%
Input capacitance	C_{IN}	—		—	5	10	—	10	pF
Power dissipation capacitance	C_{PD}	(Note 1)		—	70	—	—	—	pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

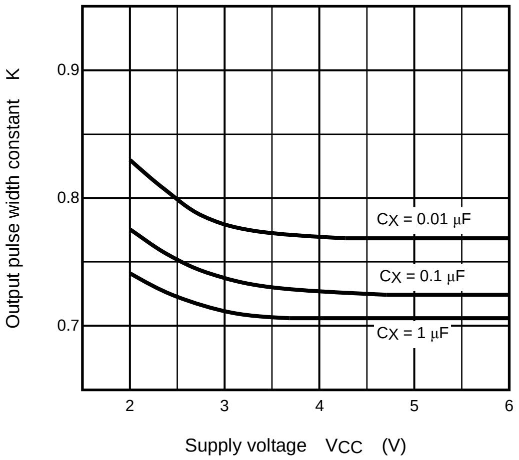
Average operating current can be obtained by the equation:

$I_{CC\,(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}' \cdot Duty/100 + I_{CC}/2$ (per circuit)

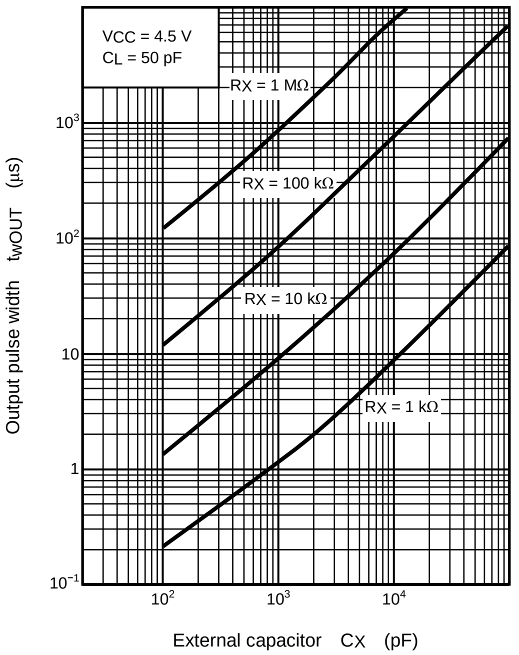
(I_{CC}': active supply current)

(Duty: %)

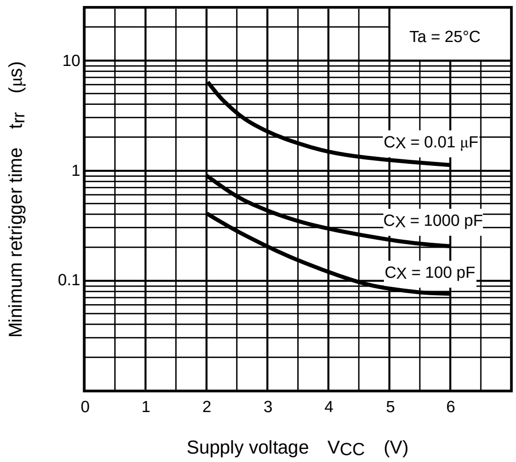
Output Pulse Width Constant K – Supply Voltage (typ.)
(external resistor (R_X) = 10 kΩ: $t_{wOUT} = K \cdot C_X \cdot R_X$)



t_{wOUT} – C_X Characteristics (typ.)

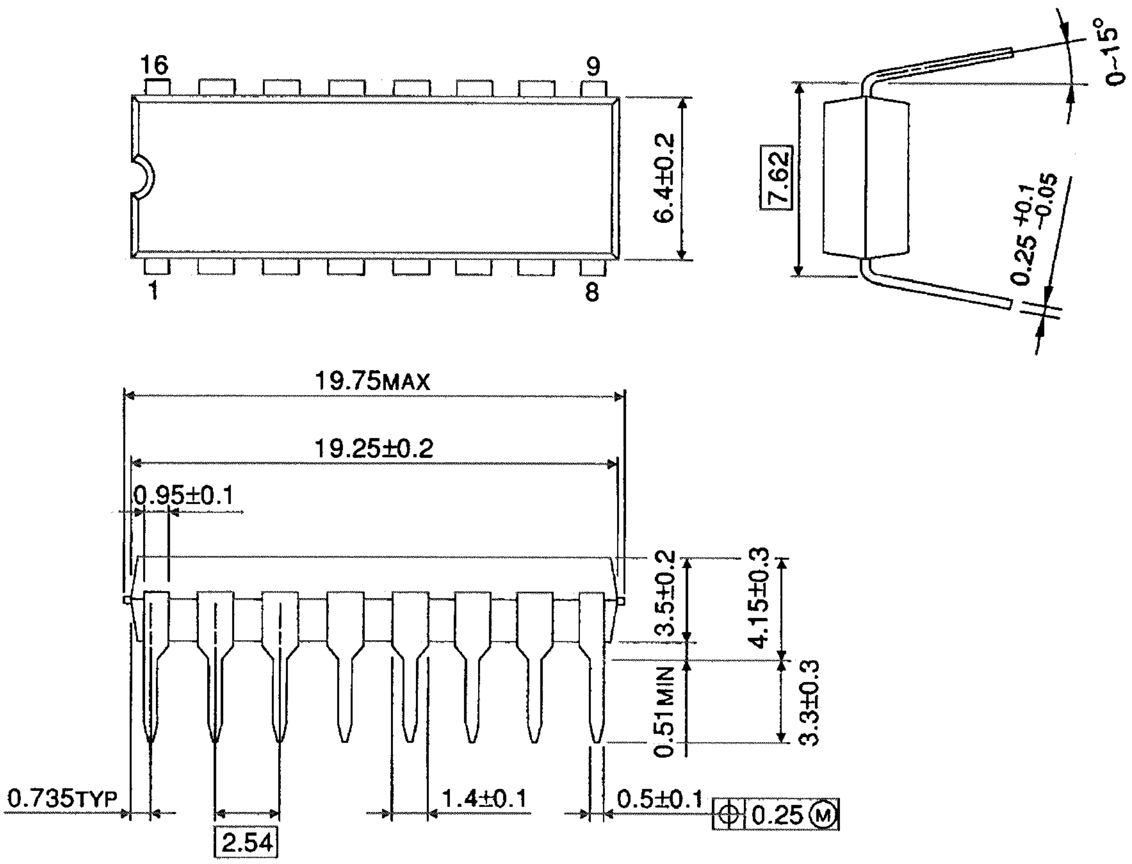


t_{rr} – V_{CC} Characteristics (typ.)



Package Dimensions

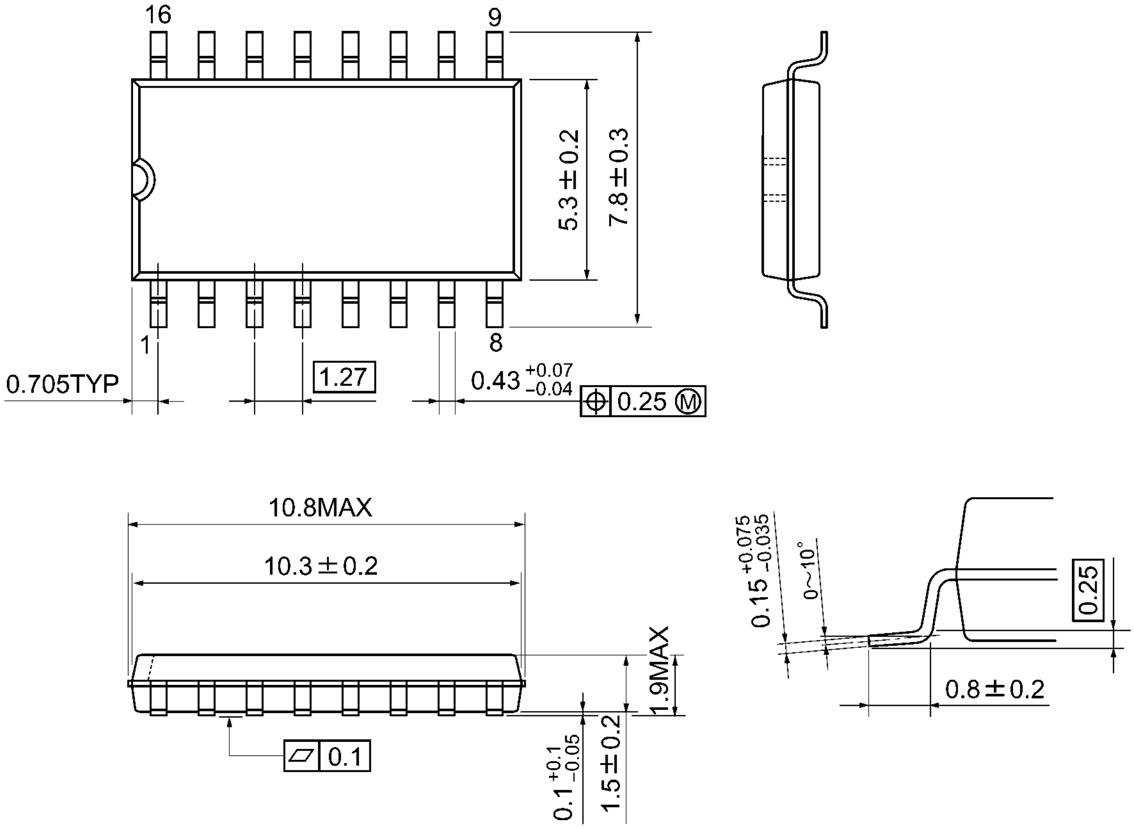
DIP16-P-300-2.54A Unit : mm



Weight: 1.00 g (typ.)

Package Dimensions

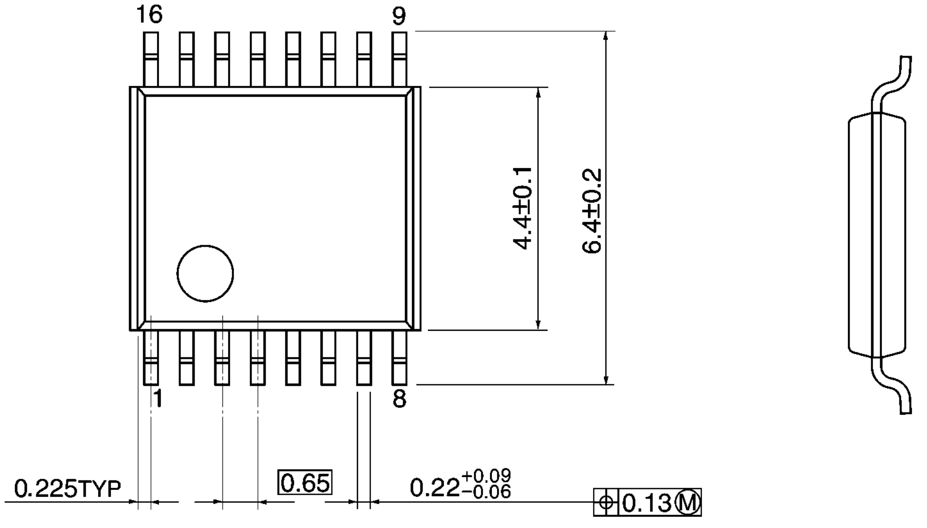
SOP16-P-300-1.27A Unit: mm

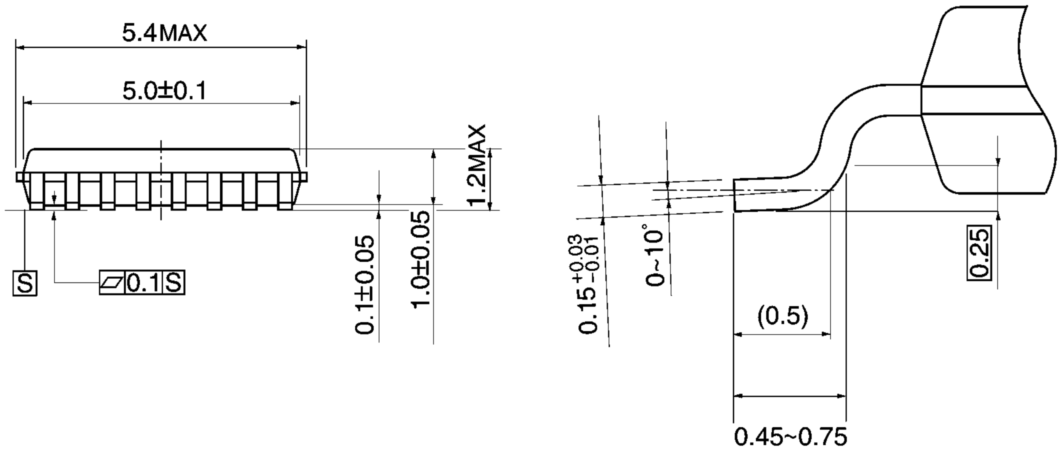


Weight: 0.18 g (typ.)

Package Dimensions

TSSOP16-P-0044-0.65A Unit: mm





Weight: 0.06 g (typ.)

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