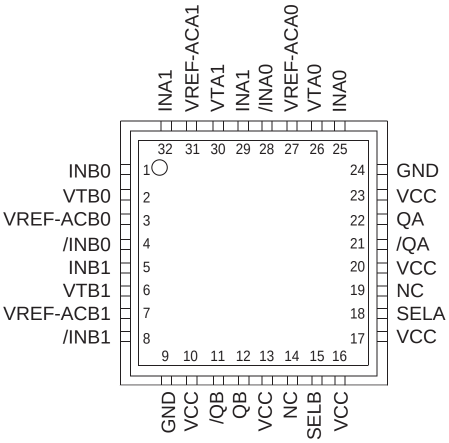
PACKAGE/ORDERING INFORMATION



32-Pin MLF® (MLF-32)

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY58027UMI	MLF-32	Industrial	SY58027U	Sn-Pb
SY58027UMITR[2]	MLF-32	Industrial	SY58027U	Sn-Pb
SY58027UMG[3]	MLF-32	Industrial	SY58027U with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY58027UMGTR[2, 3]	MLF-32	Industrial	SY58027U with Pb-Free bar-line indicator	Pb-Free NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electricals only.
2. Tape and Reel.
3. Pb-Free package recommended for new designs.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
25, 28, 29, 32, 1, 4, 5, 8	INA0, /INA0, INA1, /INA1, INB0, /INB0, INB1, /INB1	Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept AC- or DC-coupled differential signals as small as 100mV. Each pin of a pair internally terminates to a VT pin through 50ý. Note that these inputs will default to an indeterminate state if left open. Unused differential input pairs can be terminated by connecting one input to V_{CC} and the complementary input to GND through a 1ký resistor. The VT pin is to be left open in this configuration. Please refer to the “Input Interface Applications” section for more details.
26, 30, 2, 6	VTA0 , VTA1, VTB0, VTB1	Input Termination Center-Tap: Each side of the differential input pair, terminates to a VT pin. Each VT pin provides a center-tap to a termination network for maximum interface flexibility. See “Input Interface Applications” section for more details.
18, 15	SELA, SELB	Bank A, Bank B Input Channel Select (TTL/CMOS): These TTL/CMOS-compatible inputs select the inputs to the multiplexers. These inputs are internally connected to a 25ký pull-up resistor and will default to a logic HIGH state if left open. Input switching threshold is V_{CC}/2.
27, 31, 3, 7	VREF-ACA0, VREF-ACA1, VREF-ACB0, VREF-ACB1	Reference Output Voltage: These outputs bias to V_{CC} –1.2V. Connect to VT pin when AC-coupling the data inputs. Bypass with 0.01µF low ESR capacitor to V_{CC}. Maximum current source or sink is 0.5mA. See “Input Interface Applications” section.
10, 13, 16, 17, 20, 23	VCC	Positive Power Supply: Bypass with 0.1µF™ℑ0.01µF low ESR capacitors.
22, 21, 12, 11	QA, /QA, QB, /QB	Differential 100k LVPECL Outputs: MUX A and MUX B selected LVPECL outputs. See “Output Interface Applications” section for termination. Refer to the “Truth Table” for logic operation.
9, 24	GND, Exposed pad	Ground: Ground pins and exposed pad must be connected to the same ground plane.
14, 19	NC	Not connected.

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Absolute Maximum Ratings(1)

Power Supply Voltage (V_{CC})	–0.5V to +4.0V
Input Voltage (V_{IN})	–0.5V to V_{CC}
LVPECL Output Current (I_{OUT})	
Continuous	50mA
Surge	100mA
Termination Current(3)	
Source or sink current on V_T	±100mA
Input Current	
Source or sink current on IN, /IN	±50mA
Current (V_{REF-AC})	
Source or sink current on V_{REF-AC}(3)	±1.5mA
Lead Temperature (soldering, 20 sec.)	260°C
Storage Temperature Range (T_S)	–65°C to +150°C

Operating Ratings(2)

Power Supply Voltage (V_{CC})	+2.375V to +2.625V
	+3.0V to +3.6V
Ambient Temperature Range (T_A)	–40°C to +85°C
Package Thermal Resistance	
MLF® (θ_{JA})	
Still-Air	35°C/W
500lpfm	28°C/W
MLF® (ψ_{JB})(4)	
Junction-to-board	20°C/W

DC ELECTRICAL CHARACTERISTICS(5)

T_A= –40°C to +85°C; Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply	V_{CC} = 2.5V V_{CC} = 3.3V	2.375 3.0	2.5 3.3	2.625 3.6	V V
I_{CC}	Power Supply Current	No load, max. V_{CC}.		100	140	mA
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		80	100	120	ý
R_{IN}	Input Resistance (IN-to-V_T, /IN-to-V_T)		40	50	60	ý
V_{IH}	Input High Voltage (IN, /IN)	Note 6	V_{CC}–1.6		V_{CC}	V
V_{IL}	Input Low Voltage (IN, /IN)		0		V_{IH} –0.1	V
V_{IN}	Input Voltage Swing (IN, /IN)	See Figure 1a.	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing |IN – /IN|	See Figure 1b.	0.2			V
$V_{T\ IN}$	In to V_T (IN, /IN)				1.28	V
V_{REF-AC}	Output Reference Voltage		V_{CC}–1.3	V_{CC}–1.2	V_{CC}–1.1	V

Notes:

1. Permanent device damage may occur if ratings in the "Absolute Maximum Ratings" section are exceeded. This is a stress rating only and functional operation is not implied for conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability, use for input of the same package only.
4. Junction-to-board resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential (GND) on the PCB. Ψ_{JB} uses 4-layer θ_{JA} in still air unless otherwise stated.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. V_{IH} (min) not lower than 1.2V.

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LVPECL OUTPUTS DC ELECTRICAL CHARACTERISTICS(6)

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = –40°C to +85°C; R_L = 50ý to V_{CC}–2V, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage Q, /Q		V_{CC}–1.145	—	V_{CC}–0.895	V
V_{OL}	Output LOW Voltage Q, /Q		V_{CC}–1.545	—	V_{CC}–1.295	V
V_{OUT}	Output Voltage Swing Q, /Q	See Figure 1a.	150	400		mV
$V_{DIFF\text{-}OUT}$	Differential Output Voltage Swing |Q-/Q|	See Figure 1b.	300	800		mV

LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS(6)

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A= –40°C to 85°C unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		–175		75	µA
I_{IL}	Input LOW Current	V_{IL} = 0V	–300			µA

Note:

6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

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AC ELECTRICAL CHARACTERISTICS(7)

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A= –40°C to +85°C; R_L = 50ý to V_{CC}–2V, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	NRZ Data	10.7			Gbps
		V_{OUT} ž 200mV Clock		7		GHz
t_{pd}	Propagation Delay IN-to-Q	V_{IN} ž 300mV	140	215	290	ps
	SEL-to-Q		100	220	400	ps
t_{SKEW}	Input-to-Input Skew (Within-bank)	**Note 8**		6	15	ps
	Bank-to-Bank Skew	**Note 9**		8	20	ps
	Part-to-Part Skew	**Note 10**			100	ps
t_{JITTER}	Data Random Jitter (RJ)	**Note 11**			1	ps_{RMS}
	Deterministic Jitter (DJ)	**Note 12**			10	ps_{PP}
	Clock Cycle-to-Cycle Jitter (RJ)	**Note 13**			1	ps_{RMS}
	Total Jitter (TJ)	**Note 14**			10	ps_{PP}
	Crosstalk-Induced Jitter Channel-to-Channel	**Note 15,** Within-bank.			0.7	ps_{RMS}
t_r, t_f	Output Rise/Fall Time 20% to 80%	At full swing.	20	55	80	ps

Notes:

7. High-speed AC parameters are guaranteed by design and characterization. V_{IN} swing ž 100mV unless otherwise noted.
8. Input-to-input skew is the difference in time between two inputs to the output within a bank.
9. Bank-to-bank skew is the difference in time from input to the output between bank.
10. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
11. Random jitter is measured with a K28.7 comma detect character pattern, measured at 5Gbps and 2.5Gbps/3.2Gbps.
12. Deterministic jitter is measured at 2.5Gbps/3.2Gbps, with both K28.5 and 2^{23}–1 PRBS pattern.
13. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, T_n–$T_{n–1}$ where T is the time between rising edges of the output signal.
14. Total jitter definition: with an ideal clock input of frequency - f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
15. Crosstalk is measured at the output while applying two similar frequencies that are asynchronous with respect to each other at the inputs.

TRUTH TABLES

INA0	/INA0	INA1	/INA1	SELA	QA	/QA
0	1	X	X	0	0	1
1	0	X	X	0	1	0
X	X	0	1	1	0	1
X	X	1	0	1	1	0

INB0	/INB0	INB1	/INB1	SELB	QB	/QB
0	1	X	X	0	0	1
1	0	X	X	0	1	0
X	X	0	1	1	0	1
X	X	1	0	1	1	0

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SINGLE-ENDED AND DIFFERENTIAL SWINGS

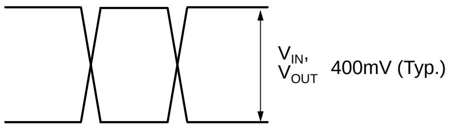


Figure 1a. Single-Ended Voltage Swing

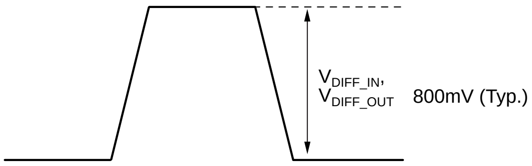
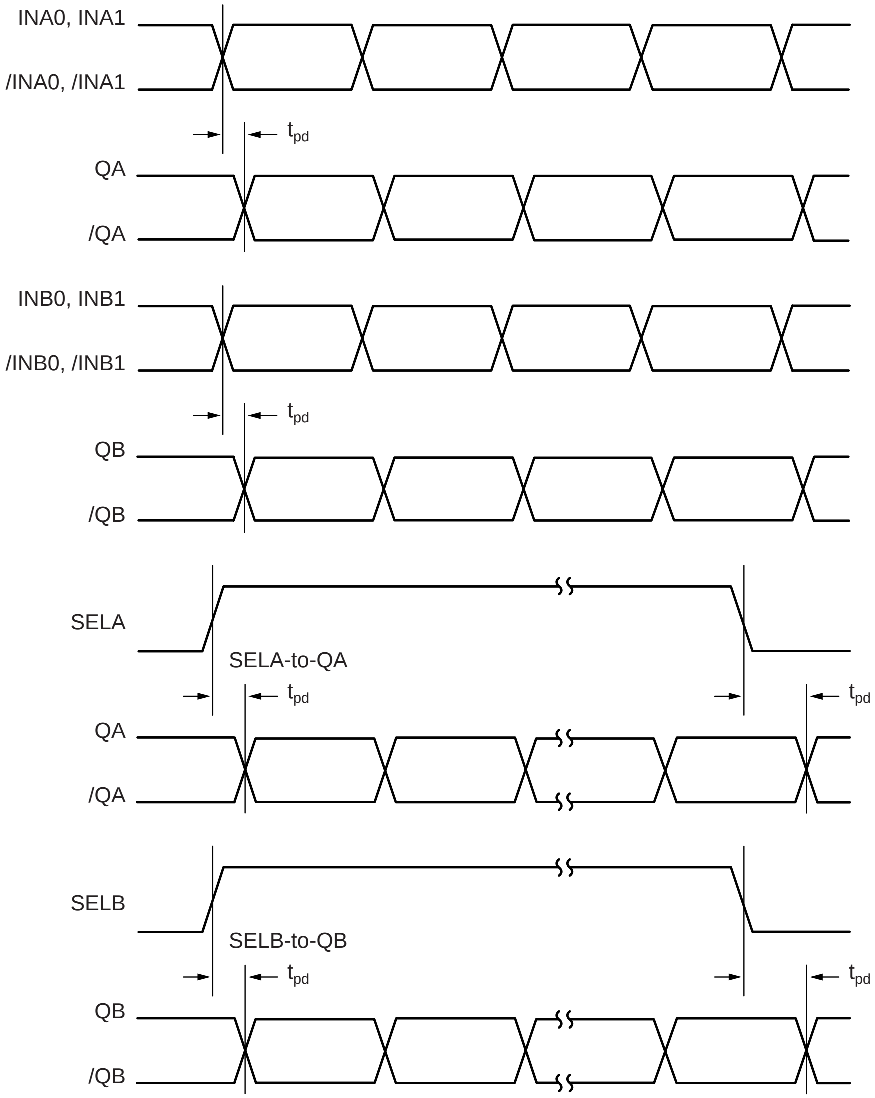


Figure 1b. Differential Voltage Swing

TIMING DIAGRAM



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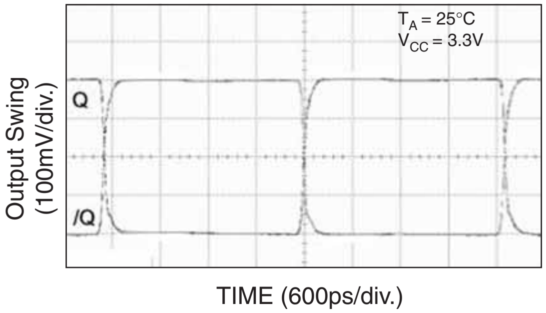
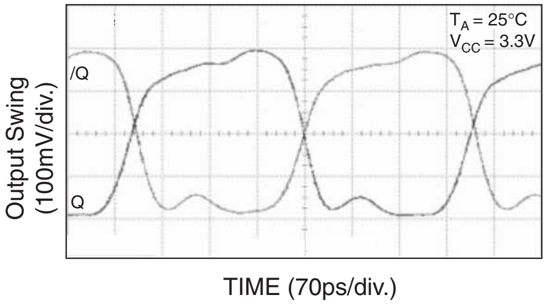
TYPICAL OPERATING CHARACTERISTICS

V_{CC} = 3.3V, T_A = 25°C, R_L = 50ý to V_{CC} – 2V, DC coupled, unless otherwise stated.

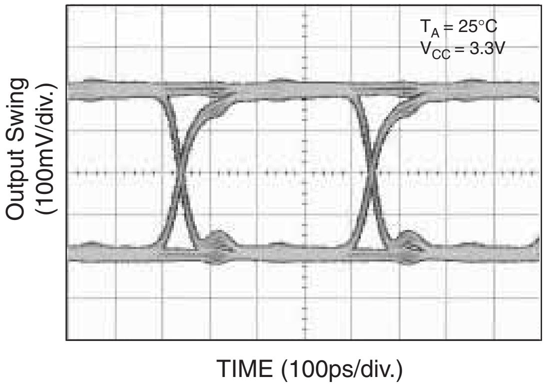
200MHz Output



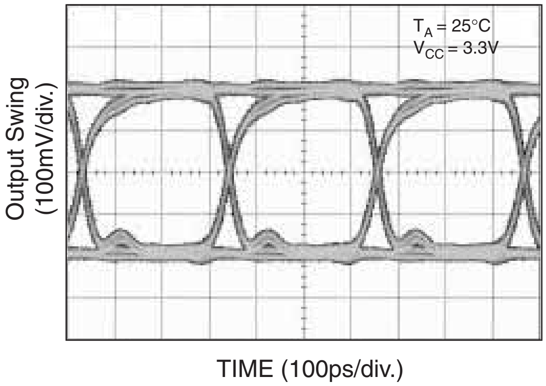
2GHz Output



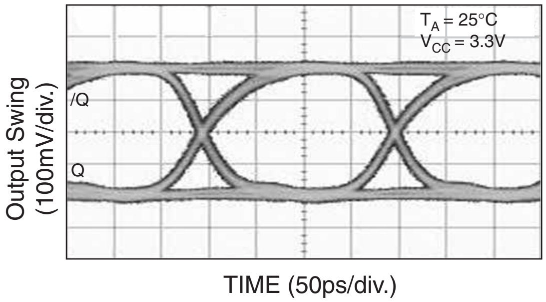
2.5Gbps Output



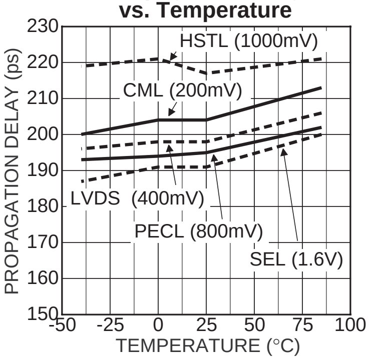
3.2Gbps Output



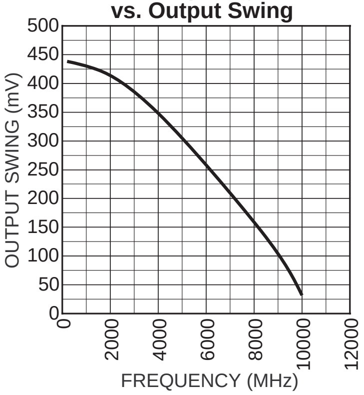
5Gbps Output



Propagation Delay vs. Temperature



Frequency vs. Output Swing



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INPUT AND OUTPUT STAGE INTERNAL TERMINATION

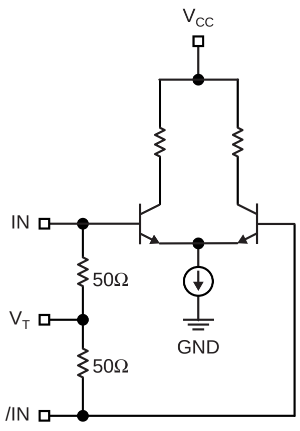


Figure 2a. Simplified Differential Input Stage

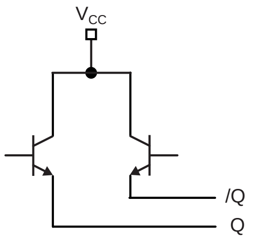
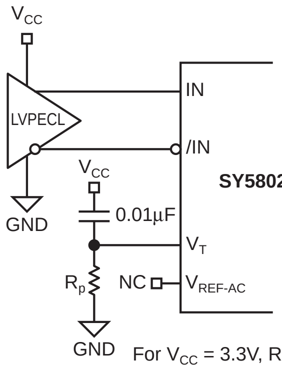


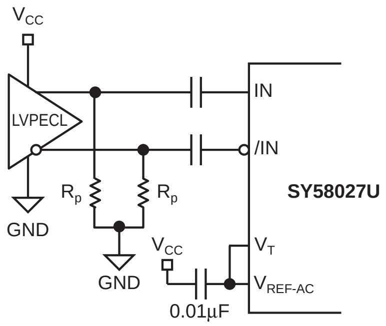
Figure 2b. Simplified LVPECL Output Stage

INPUT INTERFACE APPLICATIONS



For V_{CC} = 3.3V, R_p = 50Ω.
For V_{CC} = 2.5V, R_p = 19Ω.

Figure 3a. DC-Coupled PECL Interface



For V_{CC}=3.3V, R_p = 100Ω.
For V_{CC}=2.5V, R_p = 50Ω.

Figure 3b. AC-Coupled PECL Interface

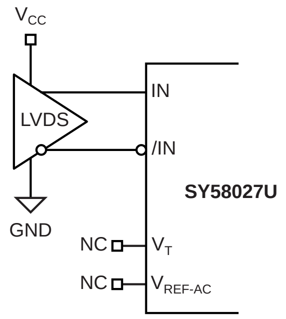
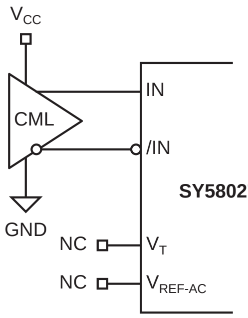


Figure 3c. LVDS Interface



Option: May connect V_T to V_{CC}.

Figure 3d. DC-Coupled CML Interface

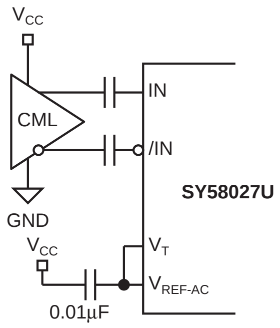


Figure 3e. AC-Coupled CML Interface

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OUTPUT INTERFACE APPLICATIONS

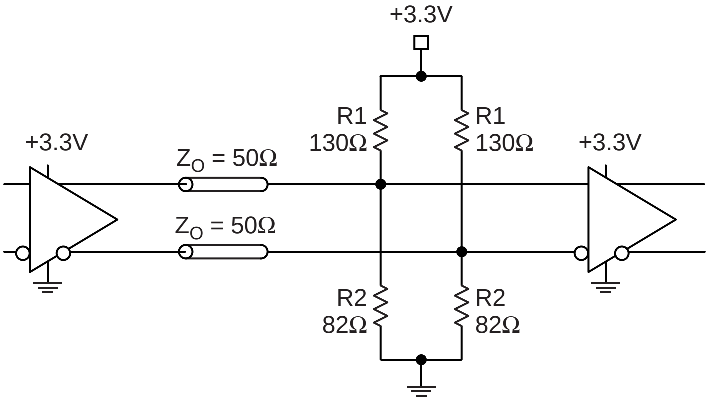

Figure 4a. Parallel Thevenin-Equivalent Termination

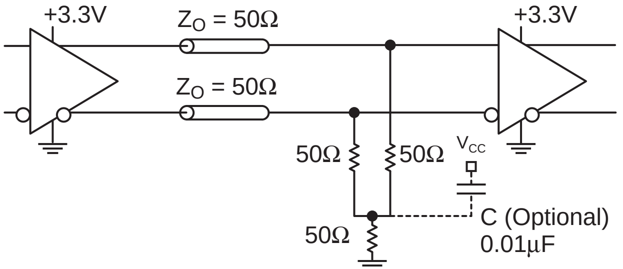

Figure 4b. Parallel Termination (3-Resistor)

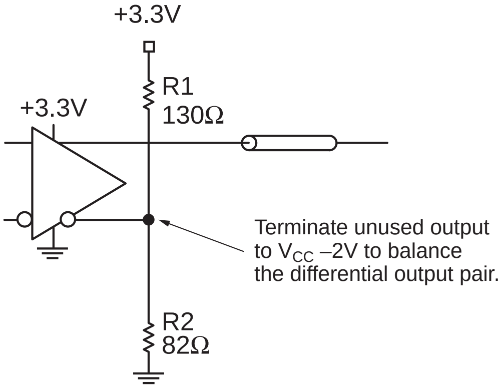

Figure 4c. Terminating Unused Output

RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
SY58016L	3.3V 10Gbps Differential CML Line Driver/Receiver with Internal Termination	http://www.micrel.com/product-info/products/sy58016l.shtml
SY58017U	10.7Gbps Differential CML 2:1 MUX with Internal Termination	http://www.micrel.com/product-info/products/sy58017u.shtml
SY58018U	5Gbps LVPECL 2:1 MUX with Internal Termination	http://www.micrel.com/product-info/products/sy58018u.shtml
SY58019U	10.7Gbps 400mV LVPECL 2:1 MUX with Internal Termination	http://www.micrel.com/product-info/products/sy58019u.shtml
SY58025U	10.7Gbps Dual 2:1 CML MUX with Internal Termination	http://www.micrel.com/product-info/products/sy58025u.shtml
SY58026U	5Gbps Dual 2:1 LVPECL MUX with Internal Termination	http://www.micrel.com/product-info/products/sy58026u.shtml
SY58051U	10.7Gbps AnyGate® with Internal Input and Output Termination	http://www.micrel.com/product-info/products/sy58051u.shtml
SY58052U	10Gbps Clock/Data Retimer with 50ý Input Termination	http://www.micrel.com/product-info/products/sy58052u.shtml
	MLF™ Application Note	www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

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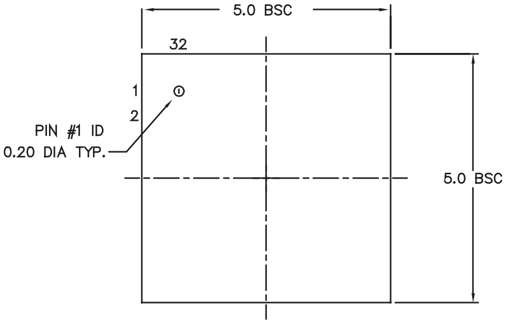
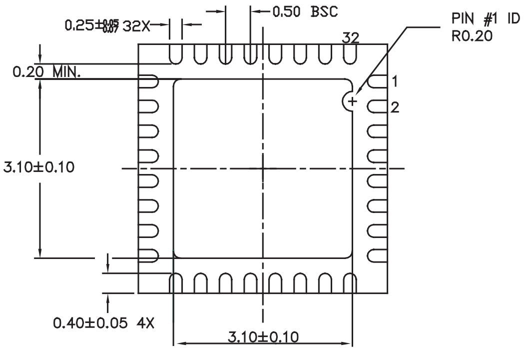
32-PIN *Micro*LeadFrame® (MLF-32)

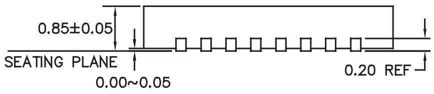


TOP VIEW

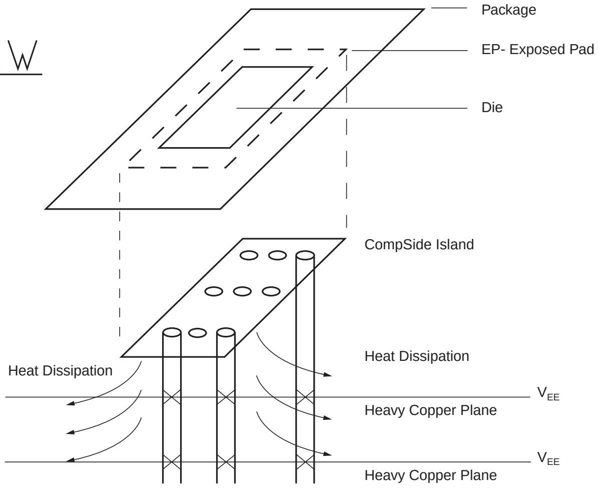


BOTTOM VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



SIDE VIEW



**PCB Thermal Consideration for 32-Pin MLF® Package
(Always solder, or equivalent, the exposed pad to the PCB)**

Package Notes:

1. Package meets Level 2 Moisture Sensitivity Classification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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