

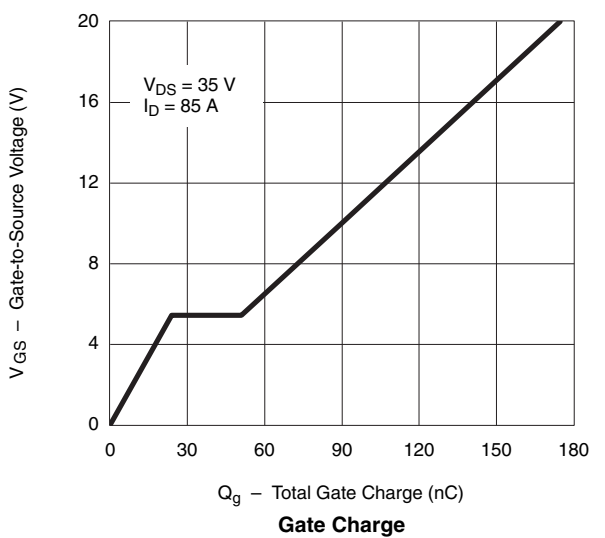
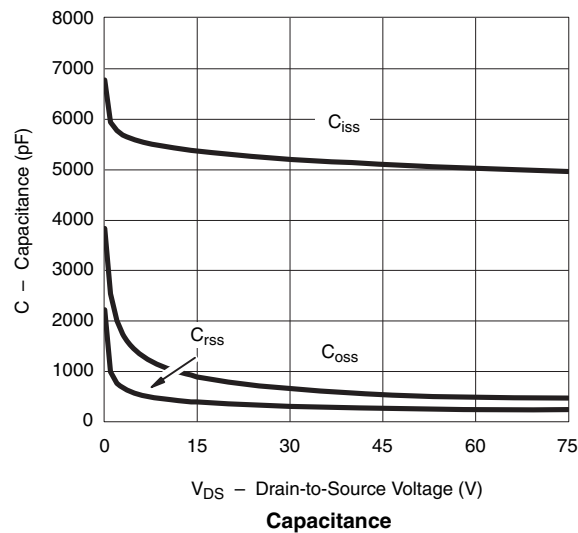
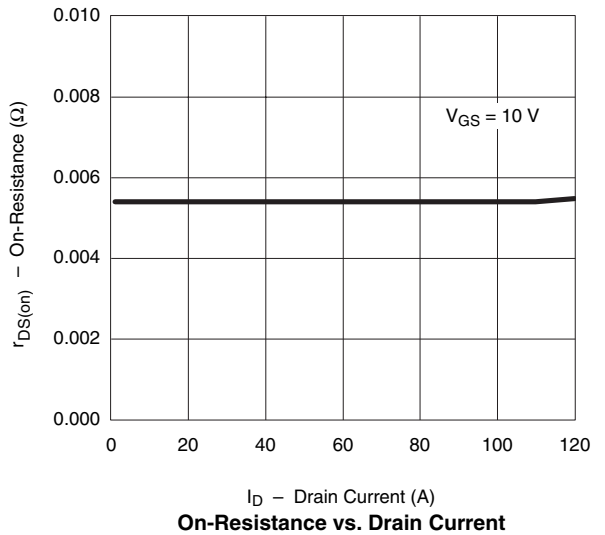
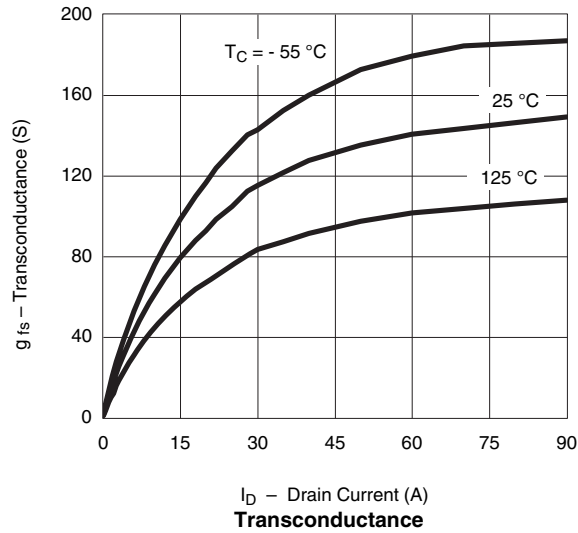
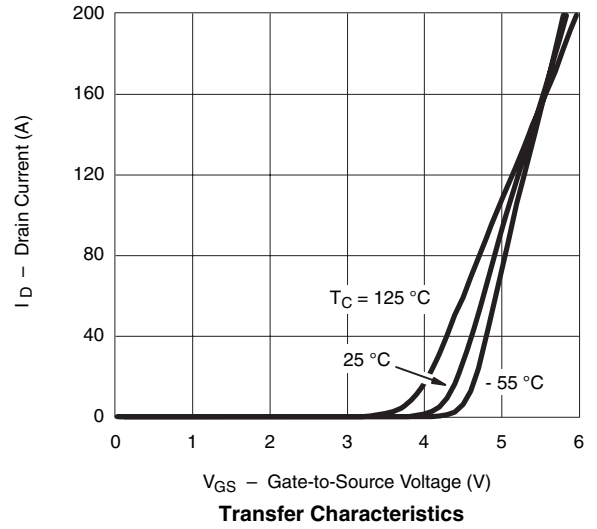
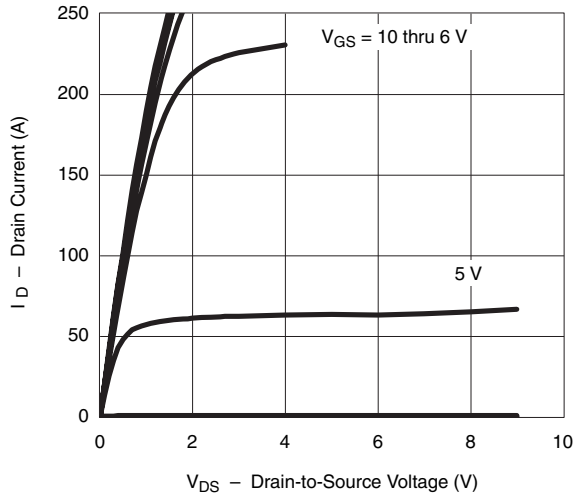
SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{DS} = 0 V, I _D = 250 μA	75			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2.5		4.0	
Gate Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 75 V, V _{GS} = 0 V			1	μA
		V _{DS} = 75 V, V _{GS} = 0 V, T _J = 125 °C			50	
		V _{DS} = 75 V, V _{GS} = 0 V, T _J = 175 °C			250	
On-State Drain Current ^a	I _{D(on)}	V _{DS} = ≥ 5 V, V _{GS} = 10 V	120			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 30 A		0.0055	0.010	Ω
		V _{GS} = 10 V, I _D = 30 A, T _J = 125 °C			0.0185	
		V _{GS} = 10 V, I _D = 30 A, T _J = 175 °C			0.0245	
Forward Transconductance	g _{fs}	V _{DS} = 15 V, I _D = 30 A	30			S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz		5250		pF
Output Capacitance	C _{oss}			700		
Reverse Transfer Capacitance	C _{rss}			310		
Total Gate Charge ^c	Q _g	V _{DS} = 35 V, V _{GS} = 10 V, I _D = 110 A		90	165	nC
Gate-Source Charge ^c	Q _{gs}			24		
Gate-Drain Charge ^c	Q _{gd}			27		
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 35 V, R _L = 0.4 Ω I _D ≡ 110 A, V _{GEN} = 10 V, R _g = 2.5 Ω		20	30	ns
Rise Time ^c	t _r			100	150	
Turn-Off DelayTime ^c	t _{d(off)}			45	70	
Fall Time ^c	t _f			75	115	
Source-Drain Diode Ratings and Characteristics (T _C = 25 °C) ^b						
Continous Current	I _S				110	A
Pulsed Current	I _{SM}				350	
Forward Voltage ^a	V _{SD}	I _F = 110 A, V _{GS} = 0 V		1.0	1.5	V
Reverse Recovery Time	t _{rr}	I _F = 85 A, di/dt = 100 A/μs		75	120	ns
Peak Reverse Recovery Current	I _{RM(REC)}			3.5	7	A
Reverse Recovery Charge	Q _{rr}				0.13	0.30

Notes:

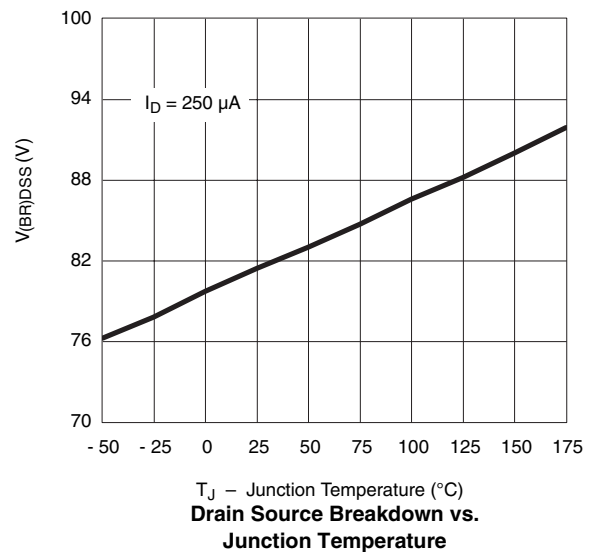
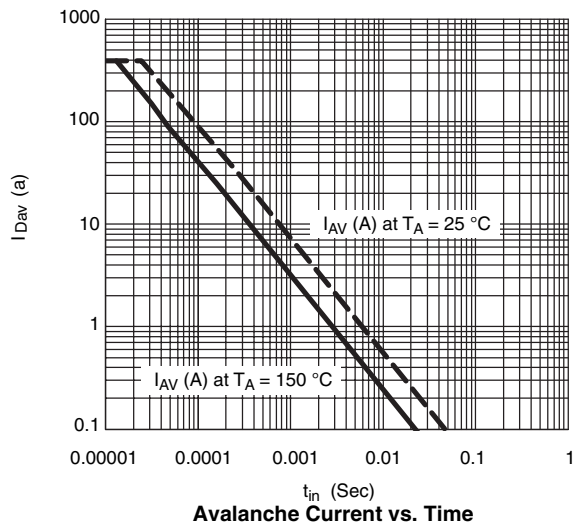
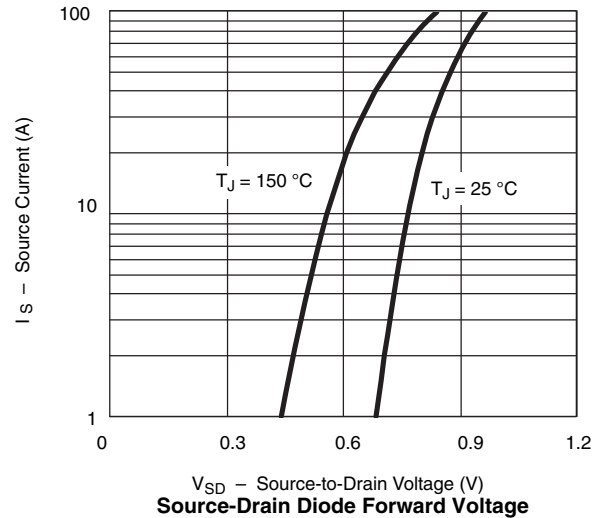
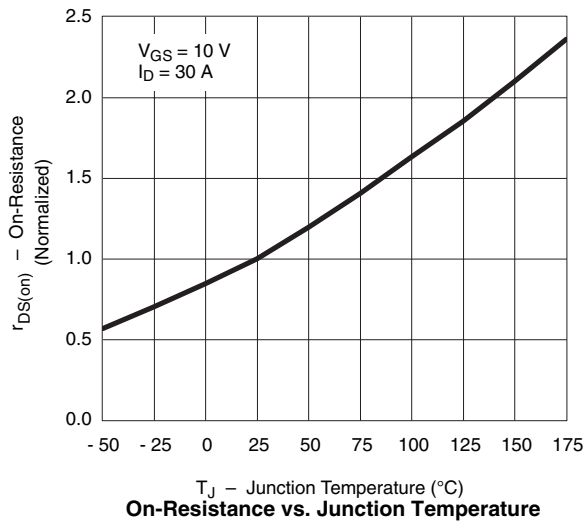
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

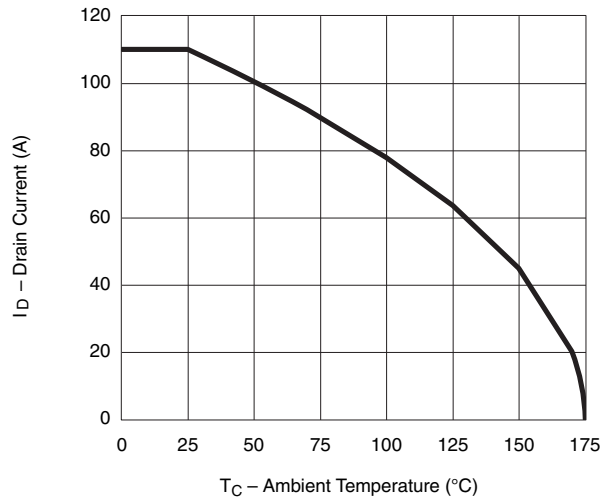
TYPICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise noted



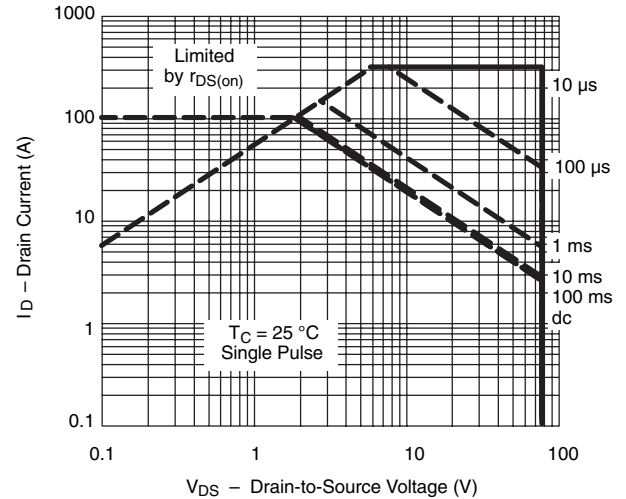
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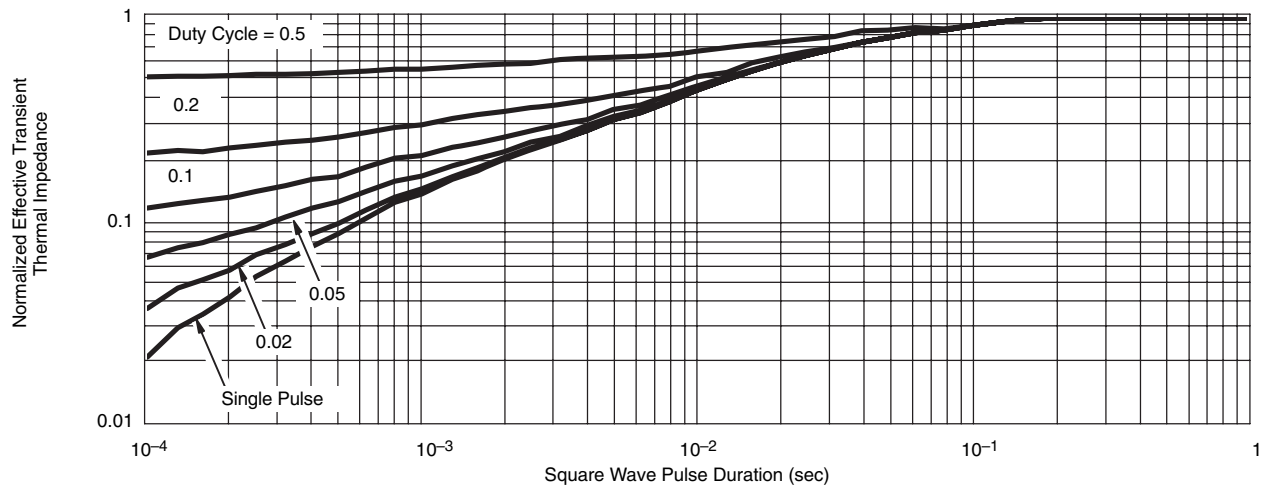
TYPICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise noted



Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?71838>.



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