Pass through mode allows the STMIPID02 to be used as a standalone MIPI D-PHY physical layer device.

With this device a host with a standard 8-bit, 10-bit or 12-bit parallel input interface can be connected to camera modules with either a MIPI CSI-2 or a SMIA CCP2 low-voltage, fully differential bit-serial, low EMI interface.

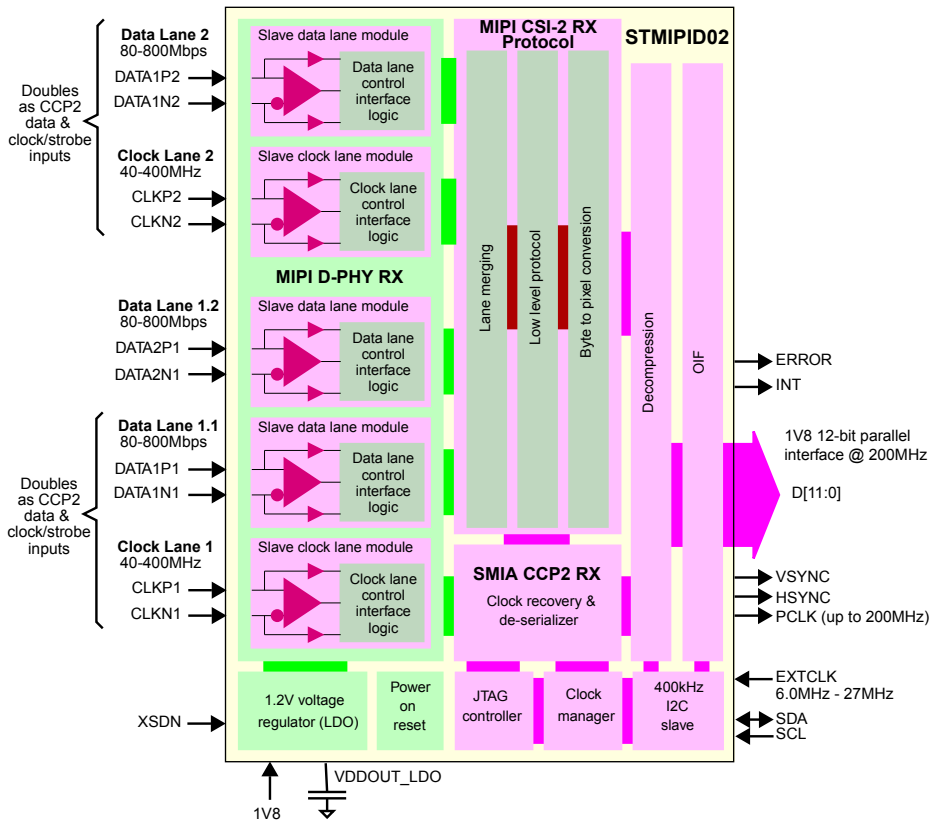
There is an interrupt output for every MIPI CSI-2 short packet.

Power management is simplified by the presence of an integrated 1.2 V regulator to supply the MIPI D-PHY receiver and core logic.

The STMIPID02 is fully configurable via an I2C compatible slave control I/F.

1 Block diagram

Figure 1. **Block diagram**



2 Application diagrams

Figure 2. **MIPI CSI-2 application diagram**

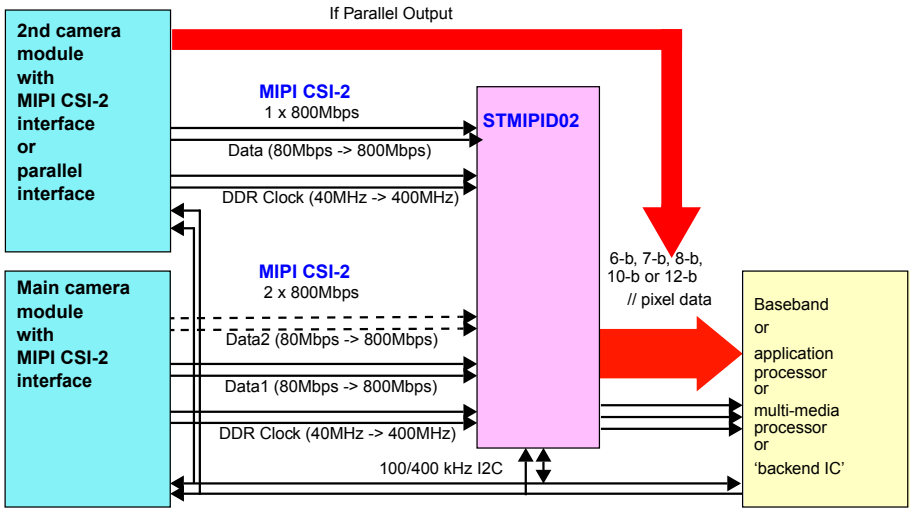
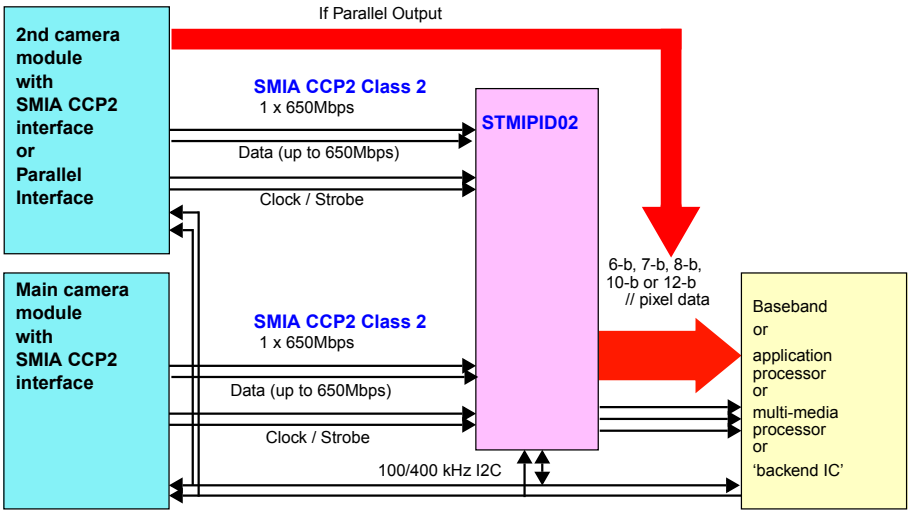


Figure 3. **SMIA CCP2 application diagram**



3 Output interface

The output interface is used to transfer image data from the STMIPID02 to the host.

Features

- CCIR601 compliant
- 12-bit data with pixel clock, HSYNC and VSYNC (external synchronization signals)
- Up to 200 MHz pixel clock, giving a data rate of 1.6 Gbit/s
- Programmable polarity of synchronization signals
- Tristate output control for multiple camera systems

By default, VSYNC envelopes all lines of valid image data. HSYNC is active on all lines including vertical frame blanking period.

HSYNC and VSYNC output polarities are programmable. The description and the figures below assume the default polarity.

The host uses the rising edge of the PCLK to sample both the data and the synchronization lanes.

Since the output data bus is 12 bits wide, for an output stream of less than 12 bits per pixel, the data can be placed on lower or upper bits of the bus. This is controlled by the Mode_Reg1[7] (address 0x14).

Table 1. Image format vs. number of bits on output interface

Image format received	Data type to be programmed in STMIPID02	Number of bits on parallel output of STMIPID02
RAW6	RAW6	6 bits
RAW7	RAW7	7 bits
RAW8	RAW8	8bits
RAW10	RAW10	10 bits
RAW12	RAW12	12 bits
RAW10 (as 10-6 compressed)	RAW6 (with decompression 6-10 enabled)	10 bits
RAW10 (as 10-7)	RAW7 (with decompression 7-10 enabled)	10 bits
RAW10 (as 10-8)	RAW8 (with decompression 8-10 enabled)	10 bits
RAW12 (as 12-10)	RAW10 (with decompression 10-12 enabled)	12 bits
RAW12 (as 12-8)	RAW8 (with decompression 8-12 enabled)	12 bits
RAW12 (as 12-7)	RAW8 (with decompression 7-12 enabled)	12 bits
RAW12 (as 12-6)	RAW8 (with decompression 6-12 enabled)	12 bits
RGB565	RAW8	8 bits
RGB888	RAW8	8 bits
RGB444	RAW8	8 bits
YUV420 8 bits	RAW8	8 bits
YUV422 8 bits	RAW8	8 bits
YUV420 10 bits	RAW10	10 bits

Figure 4. **12-bit parallel data interface signals - frame level**

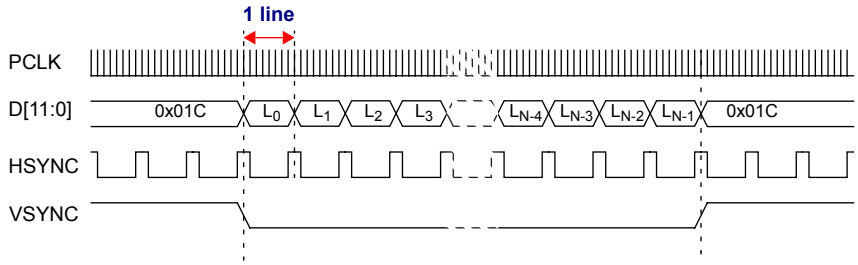
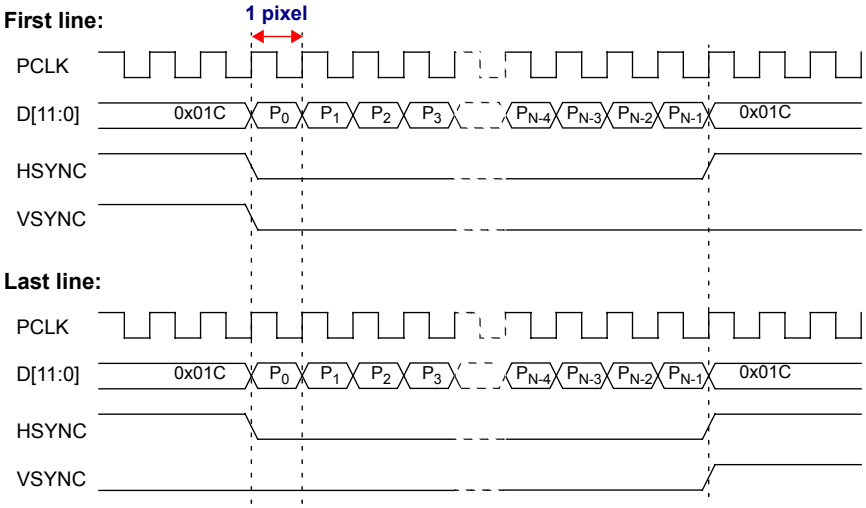


Figure 5. **12-bit parallel data interface signals - line level**



4 Control interface

The STMIPID02 is controlled through the 400 kHz I2C compatible slave command interface. The 8-bit device address is 0x28 for write operations and 0x29 for read operations. The register index is a 16-bit format and the register value is an 8-bit format. The external clock must be active for I2C slave operations.

Example

To write 0x15 in the register 0x02, the following sequence has to be applied:

S 0x28 **A** 0x00 **A** 0x02 **A** 0x15 **A**

To read the content of register 0x02:

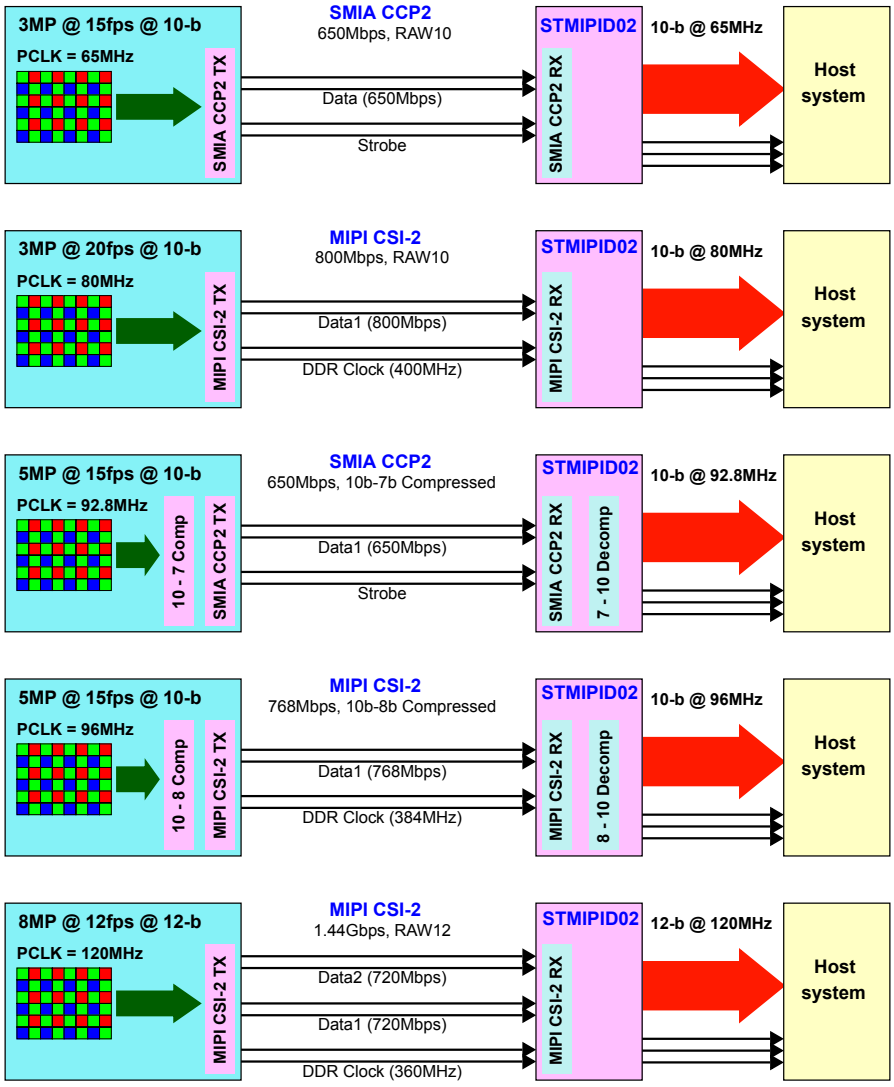
S 0x28 **A** 0x00 **A** 0x02 **A P S** 0x29 **A** xx **N P**

Where **S** = START; **P** = STOP; **A** = ACK; **N** = NACK

Detailed control inteface timings are described in Section 11.5.2 I2C slave timing (SCL, SDA).

5 Application examples

Figure 6. **Application examples**



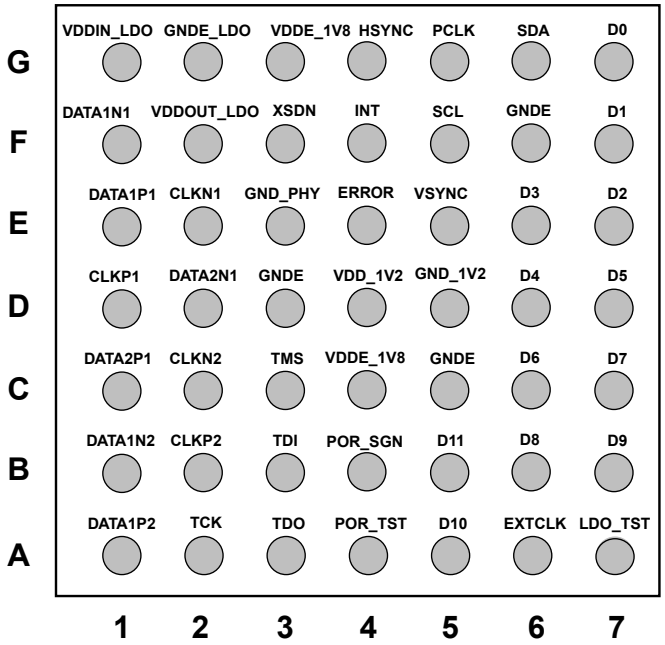
6 Key technical specifications

Table 2. Technical specifications

Technology	ST 65 nm CMOS
Pixel format(s)	SMIA: RAW6, RAW7, RAW8, RAW10, and RAW12 SMIA: 8-10, 7-10, 6-10, 8-12, 7-12, 6-12 DPCM/PCM decompression MIPI CSI-2: RAW6, RAW7, RAW8, RAW10, and RAW12 YUV, RGB, JPEG
Input video interface(s)	MIPI CSI-2 interface (2x800 Mbps + 1x800 Mbps) SMIA CCP2 Interface (1x208 Mbps Class 0 + 1x650 Mbps - Class 2)
Output video interface(s)	1V8, 200 MHz, 12-bit parallel interface + VSYNC, HSYNC, and PCLK
Control interface	100/400 kHz I2C
Clock input	6.0 MHz to 27 MHz
Supply voltage	Digital IO: 1.7 V - 1.9 V
Power consumption	TBC
Package type	VFBGA 3x 3x1 mm, 49 ball, F7x7 pitch, 0.4 mm ball 0.25 mm
Package size	3.0 mm x 3.0 mm x 1.0 mm (wlh)
Device address	0x28

7 Ball assignment and description

Figure 7. **Ball assignment: bottom view (49 balls)**



Note: The CSI-2 clock lanes must be in the middle of the two data lanes.

Note: The PCLK, HSYNC, VSYNC must be routed in the middle of the output data bus for skew management reasons.

Table 3. **Ball description**

Ball name	Type	Description
Power supplies		
VDDE_1V8	Power	1V8 digital IO supply
VDDIN_LDO	Power	1V8 voltage regulator supply
VDD_1V2	Power	1V2 MIPI D-PHY and digital core supply
GNDE	Ground	Digital IO ground
GNDE_LDO	Ground	Voltage regulator ground
GND_PHY	Ground	D-PHY ground
GND_1V2	Ground	Digital core ground
System interface		
EXTCLK	Input	System clock input (for I2C slave), 6.0 MHz - 27.0 MHz
ERROR	Output	Error interrupt, indicates that an error (either D-PHY or protocol) has occurred
INT	Output	MIPI CSI-2 short packet received interrupt, indicates that a short packet has been received

Ball name	Type	Description
XSDN	Input	Chip shutdown
Control interface		
SCL	Input	Host I2C clock
SDA	BiDir	Host I2C data
Dual lane input data interface		
CLKP1, CLKN1	Input	MIPI CSI-2 receiver 1 DDR clock input, MIPI D-PHY physical layer, doubles as CCP2 strobe/clock input in SMIA CCP2 Class 2 mode
DATA1P1, DATA1N1	Input	MIPI CSI-2 receiver 1 data lane 1, MIPI D-PHY physical layer, doubles as CCP2 data input in SMIA CCP2 Class 2 mode
DATA2P1, DATA2N1	Input	MIPI CSI-2 receiver 1 data lane 2, MIPI D-PHY physical layer
Single lane input data interface		
CLKP2, CLKN2	Input	MIPI CSI-2 receiver 2 DDR clock input, MIPI D-PHY physical layer, doubles as CCP2 strobe/clock input in SMIA CCP2 Class 2 mode
DATA1P2, DATA1N2	Input	MIPI CSI-2 receiver 2 data lane, MIPI D-PHY physical layer, doubles as CCP2 data input in SMIA CCP2 Class 2 mode
Output data interface		
D[11:0]	Output	Parallel video 12-bit data output
PCLK	Output	Pixel clock: PCLK rising edge is used to sample D[11:0], HSYNC and VSYNC. PCLK polarity is programmable
HSYNC	Output	Horizontal synchronization: HSYNC is high during active video and low during the horizontal blanking periods. HSYNC polarity is programmable
VSYNC	Output	Vertical synchronization: VSYNC is high during active video and low during the vertical blanking periods. VSYNC polarity is programmable
Power on reset (POR)		
POR_SGN	BiDir	Power on reset signal
POR_TST	Input	Power on reset test signal, should be set to ground for internal POR
Voltage regulator		
VDDOUT_LDO	Power	LDO 1.2 V output
Test interface (ST internal use)		
LDO_TST	Input	LDO regulator test mode
TDI	Input	Test data input
TMS	Input	Test mode
TCK	Input	Test clock
TDO	Output	Test data out

8 Functional description

8.1 Power up sequence

Please find below the timing of the power up sequence.

Figure 8. Power up sequence

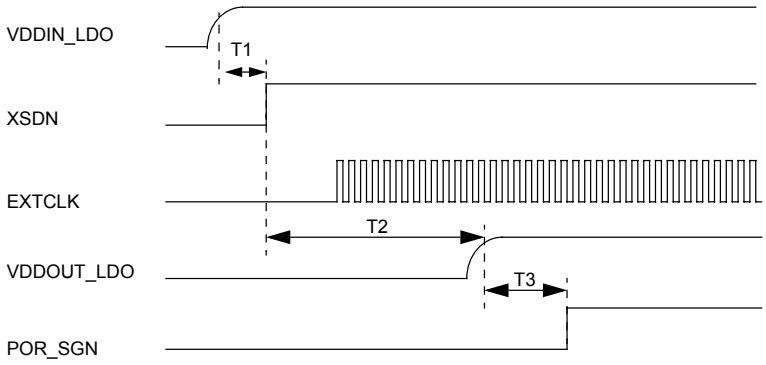


Table 4. Power up sequence timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	Time between power up and LDO enable	VDDIN_LDO stable		+inf	s
T2	Time between XSDN and CORE power up (LDO out rise to 1.2 V)			5	ms
T3	Time between CORE power up to 1.2 V and reset generation		20		µs

8.2 User modes

8.2.1 Standard modes

The output parallel interface outputs12 bits of data, HSYNC, VSYNC, and PCLK. It is recommended to enable the compensation macro (controlled by Mode_Reg3[5], at address 0x36) for both Standard and Bypass modes.

CSI2/CSI2

- Main camera: CSI2 up to 1.6 Gbps (with limitation detailed in Section 8.3 CSI2 limitations)
- Second camera: CSI2 up to 800 Mbps

CSI2/CCP2

- Main camera: CSI2 up to 1.6 Gbps (with limitation detailed in Section 8.3 CSI2 limitations)
- Second camera: CCP2 up to 650 Mbps

CSI2/ITU-R601

- Main camera: CSI2 up to 1.6 Gbps (with limitation detailed in Section 8.3 CSI2 limitations)
- Second camera: YUV directly connected to baseband parallel interface

8.2.2 Bypass modes

Bypass mode is used for any activities or applications where only PHY is needed, example, 8-bit data.

CSI2/CSI2

- Main camera: CSI2 up to 1.6 Gbps (with limitation detailed in Section 8.3 CSI2 limitations)
- Second camera: CSI2 up to 800 Mbps

CSI2/ ITU-R601

- Main camera: CSI2 up to 1.6 Gbps (with limitation detailed in Section 8.3 CSI2 limitations)
- Second camera: YUV directly connected to baseband parallel interface

8.3 CSI2 limitations

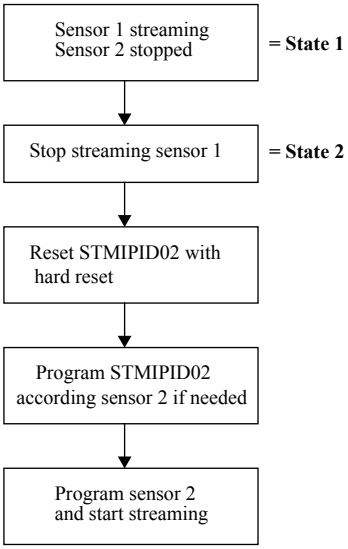
The bandwidth is limited to 800 Mbps in RAW6/RAW7 dual lane inputs. This is irrespective of the compression used or not

8.4 Sensor switching mechanism

The flow chart below explains the sensor switching mechanism. If one sensor is streaming and the other is not we are in **state1**. If both sensors are not streaming, we are in **state2**.

It is forbidden that both sensors stream simultaneously while switching. To switch sensors, it is obligatory to be in **state1** or **state2** .

Figure 9. Sensor switching mechanism



8.5 Error signal

Below is an accumulated status of all errors found in the chip.

1. Status of all errors from all D-PHY's
2. Checksum and ECC failures of CSI reception
3. ccp_shift_sync, ccp_false_sync and ccp_crc_error of CCP reception

The individual status of an error can be checked on the respective I2C register bit. The status can be cleared by programming Mode_reg2[6] register.

8.6 INT signal

This is a status showing reception of a short packet in the CSI stream. The user needs to clear the status by programming Clock_control_reg1[5] to observe the next short packet. If the user does not clear this bit then he may miss the transition on the INT ball when the next short packet is observed. The application of short packet interrupts is not envisioned yet.

9 Register description

9.1 Clock lane 1 registers

Register Name	Access	Local Address	Description
clk_lane_reg1	R/W	0x02	General and CSI controls of clock lane1 (CLKP1,CLKN1)

Bit No	Bit Name	Default Value	Description
7	ui_x4_clk_lane[5]	0	CSI control (unused in CCP mode) : Unit interval time multiplied by four This signal indicates the bit period in units of 0.25 ns. If the unit interval is 3 ns, twelve (0x0C) should be programmed. This value is used to generate delays. Therefore, if the period is not a multiple of 0.25 ns, the value should be rounded down. For example, a 600 Mbps single lane linkuses a unit interval of 1.667 ns. Multiplying by four results in 6.667. In this case, a value of 6 (not 7) should be programmed.
6	ui_x4_clk_lane[4]		
5	ui_x4_clk_lane[3]		
4	ui_x4_clk_lane[2]		
3	ui_x4_clk_lane[1]		
2	ui_x4_clk_lane[0]		
1	swap_pins_clk_lane	0	Swap P and N pins 0= Swap disabled 1= Swap enabled (CLKP1 and CLKN1 are swapped)
0	Enable	0	Enable clock lane module (CLKP1 and CLKN1) 0= Disable clock lane 1 1= Enable clock lane 1

Register Name	Access	Local Address	Description
clk_lane_reg3	R/W	0x04	CCP/CSI controls of the clock lane 1

Bit No	Bit Name	Default Value	Description
[7:5]	Reserved	000	Reserved
4	hs_rx_term_e_subLVDS_clk_lane	0	High Speed termination enable for CCP mode (unsused in CSI mode) 0= Disable HS termination 1= Enable HS termination, mandatory for CCP mode
3	hs_rx_e_subLVDS_clk_lane	0	High Speed Receiver enable for CCP mode (unsused in CSI mode) 0= Disable HS receiver 1= Enable HS receiver, mandatory for CCP mode
2	hs_rx_wakeup_subLVDS_clk_lane	0	High Speed Receiver wake-up enable for CCP mode (unsused in CSI mode) 0= HS-receiver in low power mode 1= Enable HS receiver, mandatory for CCP mode
1	cntrl_mipi_subLVDS_clk_lane	0	Select CSI or CCP mode 0= SMIA CCP 1= MIPI CSI
0	Reserved	0	Reserved

Register Name	Access	Local Address	Description
clk_lane_wr_reg1	RO	0x01	Clock lane 1 status in CSI mode

Bit No	Bit Name	Default Value	Description
[7:2]	Reserved	000000	Reserved
1	ulp_active_not_clk_lane	0	CSI Ultra low-power state active 0= The clock lane is not in ULP state or prepare to leave ULP state 1= The clock lane has reached the ULP state.
0	stop_state_clk_lane	0	CSI Lane in stop state This signal indicates that the lane module is in STOP state.

9.2 Data lane 1.1 controls

Register Name	Access	Local Address	Description
data_lane0_reg1	R/W	0x05	General controls of data lane1.1 (DATA1P1 and DATA1N1)

Bit No	Bit Name	Default Value	Description
[7:2]	Reserved	000000	Reserved
1	Swap_pins_data_lane	0	Swap P and N pins 0= Swap enabled (DATA1P1 and DATA1N1 are swapped) **1= Swap disabled**
0	Enable_data_lane	0	Enable data lane 1.1 (DATA1P1 and DATA1N1) 0= Disable data lane 1.1 1= Enable data lane 1.1

Register Name	Access	Local Address	Description
data_lane0_reg2	R/W	0x06	CCP/CSI controls of the data lane 1.1

Bit No	Bit Name	Default Value	Description
[7:4]	Reserved	0000	Reserved
3	hs_rx_term_e_subLVDS	0	High Speed termination enable for CCP mode (unsused in CSI mode) 0= Disable HS termination 1= Enable HS termination, mandatory for CCP mode
2	hs_rx_e_subLVDS	0	High Speed Receiver enable for CCP mode (unsused in CSI mode) 0= Disable HS receiver 1= Enable HS receiver, mandatory for CCP mode
1	hs_rx_wakeup_subLVDS_data_lane	0	High Speed Receiver wake-up enable for CCP mode (unsused in CSI mode) 0= HS-receiver in low power mode 1= Enable HS receiver, mandatory for CCP mode
0	cntrl_mipi_subLVDS_data_lane	0	Select CSI or CCP mode 0= SMIA CCP 1= MIPI CSI

Register Name	Access	Local Address	Description
data_lane0_reg3	RO	0x07	CSI controls of data lane 1.1

Bit No	Bit Name	Default Value	Description
[7:2]	Reserved	000000	Reserved
1	ulp_active_not_data_lane	0	CSI Ultra low-power state active 0= The clock lane is not in ULP state or prepare to leave ULP state 1= The clock lane has reached the ULP state.
0	stop_state_data_lane	0	CSI Lane in stop state This signal indicates that the lane module is in STOP state.

Register Name	Access	Local Address	Description
data_lane0_reg4	RO	0x0C	CSI protocol Error status registers

Bit No	Bit Name	Default Value	Description
[7:6]	Reserved	0	Reserved.
5	err_control	0	Unexpected control sequence error This signal is asserted when an incorrect line state sequence is detected.
4	err_sync_esc	0	Escape synchronization error If the number of bits received during a low-power data transmission is not a multiple of eight when the transmission ends, this signal is asserted and remains high until the next change in line state.
3	err_esc	0	Error during escape command If an unrecognized escape entry command is received, this signal is asserted and remains high until the next change in line state.
2	err_eot_sync_hs	0	Error during high-speed end of transmission (EoT)
1	err_sot_sync_hs	0	Synchronization error during high-speed start of transmission (SoT)
0	err_sot_hs	0	Error during high-speed start of transmission (SoT)

9.3 Data lane 1.2 controls

Register Name	Access	Local Address	Description
data_lane1_reg1	R/W	0x09	General controls of data lane1.2

Bit No	Bit Name	Default Value	Description
[7:2]	Reserved	000000	Reserved
1	Swap_pins_data_lane	0	Swap P and N pins 0= Swap disabled 1= Swap enabled (DATA2P1, DATA2N1 are swapped)
0	Enable_data_lane	0	Enable data lane 1.2 (DATA1P1 and DATA1N1 0= Disable data lane 1.2 1= Enable data lane 1.2

Register Name	Access	Local Address	Description
data_lane1_reg2	R/W	0x0A	CCP/CSI controls of data lane 1.2

Bit No	Bit Name	DefaultValue	Description
[7:4]	Reserved	0000	Reserved
3	hs_rx_term_e_subLVDS	0	High Speed termination enable for CCP mode (unsused in CSI mode) 0= Disable HS termination 1= Enable HS termination, mandatory for CCP mode
2	hs_rx_e_subLVDS	0	High Speed Receiver enable for CCP mode (unsused in CSI mode) 0= Disable HS receiver 1= Enable HS receiver, mandatory for CCP mode
1	hs_rx_wakeup_subLVDS_data_lane	0	High Speed Receiver wake-up enable for CCP mode (unsused in CSI mode) 0= HS-receiver in low power mode 1= Enable HS receiver, mandatory for CCP mode
0	cntrl_mipi_subLVDS_data_lane	0	Select CSI or CCP mode 0= SMIA CCP 1= MIPI CSI

Register Name	Access	Local Address	Description
data_lane1_reg3	RO	0x0B	CSI status of the data lane 1.2

Bit No	Bit Name	Default Value	Description
[7:2]	Reserved	000000	Reserved
1	ulp_active_not_data_lane	0	Ultra low-power state active 0= The clock lane is not in ULP state or prepare to leave ULP state 1= The clock lane has reached the ULP state.
0	stop_state_data_lane	0	Lane in stop state This signal indicates that the lane module is in STOP state.

Register Name	Access	Local Address	Description
data_lane1_reg4	RO	0x08	CSI proocol error status registers of the data lane 1.2

Bit No	Bit Name	Default Value	Description
[7:6]	Reserved	00	Reserved
5	err_control	0	Unexpected control sequence error
4	err_sync_esc	0	Escape synchronization error
3	err_esc	0	Error during escape command
2	err_eot_sync_hs	0	Error during high-speed end of transmission (EoT)
1	err_sot_sync_hs	0	Synchronization error during high-speed SoT
0	err_sot_hs	0	Error during high-speed start of transmission (SoT)

9.4 Clock lane 2 registers

Register Name	Access	Local Address	Description
clk_lane_reg1_c2	R/W	0x31	General and CSI controls of clock lane2

Bit No	Bit Name	Default Value	Description
7	ui_x4_clk_lane[5]	0	CSI control (unused in CCP mode) :Unit interval time multiplied by four This signal indicates the bit period in units of 0.25 ns. If the unit interval is 3 ns, twelve (0x0C) should be programmed. This value is used to generate delays. Therefore, if the period is not a multiple of 0.25 ns, the value should be rounded down. For example, a 600 Mbit/s single lane linkuses a unit interval of 1.667 ns. Multiplying by four results in 6.667. In this case, a value of 6 (not 7) should be programmed.
6	ui_x4_clk_lane[4]		
5	ui_x4_clk_lane[3]		
4	ui_x4_clk_lane[2]		
3	ui_x4_clk_lane[1]		
2	ui_x4_clk_lane[0]		
1	swap_pins_clk_lane	0	Swap P and N pins 0 = Swap enabled (CLKP2 and CLKN2 are swapped) **1= Swap disabled**
0	Enable	0	Enable clock lane module (CLKP1 and CLKN1) 0= Disable clock lane 1 1= Enable clock lane 1

Register Name	Access	Local Address	Description
clk_lane_reg3_c2	R/W	0x33	CCP/CSI controls of the clock lane 2

Bit No	Bit Name	Default Value	Description
[7:5]	Reserved	000	Reserved
4	hs_rx_term_e_subLVDS_clk_lane	0	High Speed termination enable for CCP mode (unsused in CSI mode) 0= Disable HS termination 1= Enable HS termination, mandatory for CCP mode
3	hs_rx_e_subLVDS_clk_lane	0	High Speed Receiver enable for CCP mode (unsused in CSI mode) 0= Disable HS receiver 1= Enable HS receiver, mandatory for CCP mode
2	hs_rx_wakeup_subLVDS_clk_lane	0	High Speed Receiver wake-up enable for CCP mode (unsused in CSI mode) 0= HS-receiver in low power mode 1= Enable HS receiver, mandatory for CCP mode
1	cntrl_mipi_subLVDS_clk_lane	0	Select CSI or CCP mode 0= SMIA CCP 1= MIPI CSI
0	Reserved	0	Reserved

Register Name	Access	Local Address	Description
clk_lane_wr_reg1_c2	RO	0x39	CSI clock lane 2 status

Bit No	Bit Name	Default Value	Description
[7:2]	Reserved	000000	Reserved
1	ulp_active_not_clk_lane	0	CSI Ultra low-power state active 0= The clock lane is not in ULP state or prepare to leave ULP state 1= The clock lane has reached the ULP state.
0	stop_state_clk_lane	0	CSI Lane in stop state This signal indicates that the lane module is in STOP state.

9.5 Data lane 2 controls

Register Name	Access	Local Address	Description
data_lane3_reg1	R/W	0x34	General controls of data lane 2 (DATA1P2 and DATA1N2)

Bit No	Bit Name	Default Value	Description
[7:2]	Reserved	000000	Reserved
1	Swap_pins_data_lane	0	Swap P and N pins 0= Swap disabled 1= Swap enabled (DATA1P2 and DATA1N2 are swapped)
0	Enable_data_lane	0	Enable data lane 1.1 (DATA1P2 and DATA1N2) 0= Disable data lane 2 1= Enable data lane 2

Register Name	Access	Local Address	Description
data_lane3_reg2	R/W	0x35	CCP/CSI controls of data lane 2

Bit No	Bit Name	Default Value	Description
[7:4]	Reserved	0000	Reserved
3	hs_rx_term_e_subLVDS	0	High Speed termination enable for CCP mode (unsused in CSI mode) 0= Disable HS termination 1= Enable HS termination, mandatory for CCP mode
2	hs_rx_e_subLVDS	0	High Speed Receiver enable for CCP mode (unsused in CSI mode) 0= Disable HS receiver 1= Enable HS receiver, mandatory for CCP mode
1	hs_rx_wakeup_subLVDS_data_lane	0	High Speed Receiver wake-up enable for CCP mode (unsused in CSI mode) 0= HS-receiver in low power mode 1= Enable HS receiver, mandatory for CCP mode
0	cntrl_mipi_subLVDS_data_lane	0	Select CSI or CCP mode 0= SMIA CCP 1= MIPI CSI

Register Name	Access	Local Address	Description
data_lane3_reg3	RO	0x3A	CSI status of data lane 2

Bit No	Bit Name	Default Value	Description
[7:2]	Reserved	000000	Reserved
1	ulp_active_not_data_lane	0(unsused in CSI mode)	CSI Ultra low-power state active 0 = The clock lane is not in ULP state or prepare to leave ULP state 1 = The clock lane has reached the ULP state.
0	stop_state_data_lane	0	CSI Lane in stop state This signal indicates that the lane module is in STOP state.

Register Name	Access	Local Address	Description
data_lane3_reg4	RO	0x3B	CSI protocoleError status registers of data lane 2

Bit No	Bit Name	Default Value	Description
[7:6]	Reserved	0	Reserved
5	err_control	0	Unexpected control sequence error This signal is asserted when an incorrect line state sequence is detected. For example, if a turn-around request or escape mode request is immediately followed by a stop state instead of the required bridge state, this signal is asserted and remains high until the next change in line state.
4	err_sync_esc	0	Escape synchronization error If the number of bits received during a low-power data transmission is not a multiple of eight when the transmis-sion ends, this signal is asserted and remains high until the next change in line state.
3	err_esc	0	Error during escape command If an unrecognized escape entry command is received, this signal is asserted and remains high until the next change in line state.
2	err_eot_sync_hs	0	Error during high-speed end of transmission (EoT)
1	err_sot_sync_hs	0	Synchronization error during high-speed SoT
0	err_sot_hs	0	Error during high-speed start of transmission (SoT)

9.6 CCP RX and error flag registers

Register Name	Access	Local Address	Description
ccp_rx_reg1	R/W	0x0D	CCP Data clock/data strobe mode selection and Error signal control

Bit No	Bit Name	Default Value	Description
7	Delay[4]	0	Error Signals (pulses) generated are valid for short duration (4 input DDR clocks). To be able to capture this in I2C registers working on host clock, these Error pulses need to stretched (duration of pulses need to be increased). This pulse stretching is programmable. Delay value is multiplied by 16 for single lane & by 8 for dual lane. For example: If original pulse width is 4 clocks and Register Value is 3 specifies for dual lane system . The resultant Pulse captured will be 4 (original clocks) + 3 (programmed value) * 8 (dual lane) = 28 clocks
6	Delay[3]		
5	Delay[2]		
4	Delay[1]		
3	Delay[0]		
2	Reserved	0	Reserved
1	Reserved	0	Reserved
0	DS_MODE	0	Selects between CCP Data-Strobe mode and Data-Clock mode for the main camera (unuse in CSI) DC_MODE=0 -> Data clock mode DS_MODE= 1 -> Data strobe mode

Register Name	Access	Local Address	Description
ccp_rx_reg2	R/W	0x0E	CCP controls

Bit No	Bit Name	Default Value	Description
7	Reserved	0	Reserved
6	Clr_glue_sync_error	0	Clear sync error in CCP path
5	pix_width_ccp_rx[3]	0	Pixel width input in CCP mode (unused in CSI). It should be selected between the allowed pixel widths: 6, 7, 8, 10 or 12-bit. Value of this register-slice is binary equivalents of 6, 7, 8, 10 or 12 , other values are invalid.
4	pix_width_ccp_rx[2]		
3	pix_width_ccp_rx[1]		
2	pix_width_ccp_rx[0]		
1	clr_ccp_shift_sync	0	Clear CCP shift sync flag
0	clr_ccp_crc_error	0	Clear CCP CRC error

Register Name	Access	Local Address	Description
ccp_rx_reg3	RO	0x0F	CCP channel and error flags

Bit No	Bit Name	Default Value	
7	Glue_logic_sync_error	0	Incorrect data length error flag
[3-6]	ccp_channel[0-3]	0000	Channel ID extracted from input CCP stream
2	ccp_shift_sync	0	CCP shift sync error flag
1	ccp_false_sync	0	CCP false sync error flag
0	ccp_crc_error	0	CCP CRC error flag

Register Name	Access	Local Address	Description
ccp_rx_reg1_c2	R/W	0x38	Data clock / data strobe selection for the second camera (CLKP2,CLKN2,DATA1P2,DATA1N2)

Bit No	Bit Name	Default Value	Description
[7:1]	Reserved	0000000	Reserved
0	DS MODE	0	Selects between CCP Data-Strobe mode and Data-Clock mode for the second camera (unused in CSI). DC MODE=0 -> Data clock mode DS MODE= 1 -> Data strobe mode

9.7 Mode control registers

Register Name	Access	Local Address	Description
Mode_reg1	R/W	0x14	Chip mode controls

Bit No	Bit Name	Default Value	Description
7	Justification control	0	Data Justification on output Data 0= right justified (data on lower bits of bus) 1= left justified (Data on upper bits) In bypass mode, this control is invalid
6	Bypass_mode[0]	0	1= No bypass 0= Bypass of the pixel generation & the decompression
5	Decompression[2]	0	000 = decompression disabled 001 = 6-10 010 = 7-10 011 = 8-10 100 = 8-12 101= 10-12 110 = 6-12 111 = 7-12
4	Decompression[1]		
3	Decompression[0]		
2	Lane_ctrl[1]	0	Swap data lanes 1.1 and 1.2 0= No swap, lane1 remains lane1 & lane2 remains lane2 1= Lanes swapped, lane1 becomes lane2 & lane2 ->lane1
1	Lane_ctrl[0]	0	0= 1-lane system 1= 2-lane system
0	Ccp/csi	0	Input selector control 0= CSI2 input stream 1= CCP input stream

Register Name	Access	Local Address	Description
Mode_reg2	R/W	0x15	Output Interface controls

Bit No	Bit Name	Default Value	Description
7	Tristate_output	0	Programmation of the parallel interface in ouput or tristate mode 1 = Tristated output 0 = Normal output
6	Clear_Error_Signal	0	Control to reset the error flag output 0 = Reset the Error flag 1 = Do not reset keep value as it is
5	Error_signal_polarity	0	Polarity for Error signal 0 = Non Inverted 1 = Inverted
4	Clock_gating control	0	Continuous or gated clock control 0 = continuous clock 1 = clock gated
3	Output_polarity_clk	0	Polarity control of PCLK signal 0= Non Inverted 1= Inverted
2	Output_polarity_vsync	0	Polarity control of VSYNC signal 0= Non Inverted 1= Inverted
1	Output_polarity_hsync	0	Polarity control of HSYNC signal 0= Non Inverted 1= Inverted
0	Interrupt_polarity	0	Polarity for Interrupt signal 0 = Non Inverted 1 = Inverted

Register Name	Access	Local Address	Description
Mode_reg3	R/W	0x36	Output Interface controls

Bit No	Bit Name	Default Value	Description
[7:6]	Reserved	0	Reserved
5	i2c_comp_leakage	0	Enable compensation macro 0 = Disable IO compensation macro 1= Enable IO compensation macro
4	Reserved	0	Reserved
3	Spec_90_81_c2	0	For second (1 lane) camera 0=0.9 spec of D-PHY 1=0.81 spec of D-PHY
2	Spec_90_81_c1	0	For first (2 lanes) camera 0=0.9 spec of D-PHY 1-0.81 spec of D-PHY
1	Reserved	0	Reserved
0	Camera_select	0	Camera selection 0= Main camera (CLKP1,CLKN1,DATA1P1,DATA1N1,DATA2P1,DATA2N1) 1= Second camera (CLKP2,CLKN2,DATA1P2,DATA1N2)

9.8 Clock control registers

Register Name	Access	Local Address	Description
Clock_control_reg1	R/W	0x16	Clear for INT & ERR

Bit No	Bit Name	Default Value	Description
[7:6]	Reserved	00	Reserved
5	Clr_csi2_interrupt	0	I2C control to clear CSI interrupt
4	Clr_csi2_error	0	I2C control to clear CSI error. It stops streaming data till this bit is reseted.
[3:0]	Reserved	0	Reserved

9.9 System error registers

Register Name	Access	Local Address	Description
Error_regs	RO	0x10	Error output registers

Bit No	Bit Name	Default Value	Description
[7:2]	Reserved	000000	Reserved
1	Checksum_failed	0	Checksum failure status in Low level protocol 0 = OK 1 = Failed
0	ECC_failed	0	ECC in low level protocol status 0 = OK 1 = Failed

9.10 Data pipe information

Register Name	Access	Local Address	Description
Data_ID_Wreg	RO	0x11	Image Data type register extracted from the CSI data stream. It refers to data type in Low Level Protocol. See CSI2 Specification for detailed explanations. The 2 MSB codes the Virtual Channel number, the remaining 6 bits codes the data type.

Register Name	Access	Local Address	Description
Data_ID_Rreg	R/W	0x17	Image Data type register to be programmed: - mandatory in CCP mode - mandatory in CSI if not extracted from the CSI data stream. In CSI mode, the STMIPID02 can be programmed to use data type from this register or from embedded data type information in data stream. It refers to data type in Low Level Protocol. See CSI2 Specification for detailed explanations. The 2 MSB codes the Virtual Channel number, the remaining 6 bits codes the data type.

Register Name	Access	Local Address	Description
Data_ID_Rreg_emb	R/W	0x18	Non-Image Data type register to be programmed in CCP and CSI modes. It refers to data type in Low Level Protocol. See CSI2 Specification for detailed explanations. The 2 MSB codes the Virtual Channel number, the remaining 6 bits codes the data type of the embedded data.

Register Name	Access	Local Address	Description
Data_selection_ctrl	R/W	0x19	Virtual channel, Datatype selection and pixel width control register

Bit No	Bit Name	Default Value	Description
[7:4]	Reserved	0000	Reserved
3	Pixel width selection	0	Selection of pixel width 1 = Pixel width from I2C reg Pix_width_ctrl 0 = Pixel width extracted from data type decided with Data_selection_ctrl[2]
2	Data type	0	Selection of data type 0 = Data type from data stream (readable in Data_ID_Wreg 0x11) 1 = Data type from I2C programmed register (Data_ID_Rreg)
1	VC[1]	0	Virtual channel, whose data to be retrieved and used in subsequent steps. Data for other channel is to be discarded
0	VC[0]		

Register Name	Access	Local Address	Description
Frame_no_lsb	RO	0x12	Frame numer LSByte from Frame sync short packet for CSI2 mode

Bit No	Bit Name	Default Value	Description
[0,7]	Bit 0 to Bit7	00000000	Bit 0 to Bit 7 of frame number

Register Name	Access	Local Address	Description
Frame_no_msb	RO	0x13	Frame number MSByte from Frame sync short packet for CSI2 mode

Bit No	Bit Name	Default Value	Description
[0,7]	Bit 8 to Bit 15	00000000	Bit 8 to Bit 15 of frame number

Register Name	Access	Local Address	Description
Active_line_no_lsb	R/W	0x1B	Number of active lines in image used in CCP mode and decompression mode (LSB)

Bit No	Bit Name	Default Value	Description
[0,7]	Bit 0 to Bit 7	00000000	Bit 0 to Bit 7 of active line number

Register Name	Access	Local Address	Description
Active_line_no _msb	R/W	0x1A	Number of active lines in image used in CCP mode and decompression mode (MSB)

Bit No	Bit Name	Default Value	Description
[0,7]	Bit 8 to Bit15	00000000	Bit 8 to Bit15 of active line number

Register Name	Access	Local Address	Description
SOF_line_no_lsb	R/W	0x1D	Number of embedded lines (status lines) in image used for CCP mode and decom-pression mode (LSB)

Bit No	Bit Name	Default Value	Description
[0,7]	Bit 0 to Bit7	00000000	Bit 0 to Bit7of embedded line number

Register Name	Access	Local Address	Description
SOF_line_no _msb	R/W	0x1C	Number of embedded lines (status lines) in image used for CCP mode and decom-pression mode (MSB)

Bit No	Bit Name	Default Value	Description
[0,7]	Bit 8 to Bit15	00000000	Bit 8 to Bit15 of embedded line number

Register Name	Access	Local Address	Description
Pix_width_ctrl	R/W	0x1E	Pixel width and decompression control of active lines

Bit No	Bit Name	Default Value	Description
[5-7]	Reserved	000	Reserved
4	Dcpx_en for active pixel	0	Decompression enable for active data 0= Decompression OFF 1= Decompression ON
[0-3]	Pix_width[0 to 3]		Pixel width control for active data

Register Name	Access	Local Address	Description
Pix_width_ctrl_emb	R/W	0x1F	Pixel width and decompression control of embedded lines

Bit No	Bit Name	Default Value	Description
[5-7]	Reserved	000	
4	Dcpx_en for emb pixel	0	Decompression enable for embedded data 0= Decompression OFF 1= Decompression ON
[0-3]	Pix_width_emb[0 to 3]		Pixel width control for embedded data. This input will be used by STMIPID02 for recognizing the Pixel width in embedded lines of received stream.

Register Name	Access	Local Address	Description
Data_field_LSB	RO	0x21	LSB of ECC corrected data field

Bit No	Bit Name	Default Value	Description
[0-7]	Bit 0 to 7	00000000	LSB of ECC corrected data field

Register Name	Access	Local Address	Description
Data_Field_MSB	RO	0x20	MSB of ECC corrected data field

Bit No	Bit Name	Default Value	Description
[0-7]	Bit 8 to 15	00000000	MSB of ECC corrected data field

10 Generic script

Below is a generic script which users can start with.
WriteByte(0x0002, 0x15) means that the I2C driver writes 0x15 in register address 0x002.

```
// MAIN CAMERA CLOCK LANE 1 (CLKP1, CLKN1)
WriteByte(0x0002, 0x15);
    // Enable Clock Lane 1 (CLKP1, CLKN1) and UI programmation: 0x15 between 400MHz and 334Mhz, ,
    0x19 between 333 and 286MHz, 0x1D between 285 and 250MHz,0x21 between 249 and 223MHz, 0x25
    between 222 and 200Mhz and so on
WriteByte(0x0004, 0x02);
    // 0x1c CCP mode , 0x02 CSI mode on main camera

//  MAIN CAMERA DATA LANE 1.1 (DATA1P1, DATA1N1)
WriteByte(0x0005, 0x03);
    // 0x03 Enable Data Lane 1.1 (DATA1P1, DATA1N1), 0x00 disable Data lane 1.1
WriteByte(0x0006, 0x01);
    // 0x01 for CSI mode set on Data Lane 1.1 (DATA1P1, DATA1N1), 0x0e for CCP mode on Data Lane 1.1
    (DATA1P1, DATA1N1)

//  MAIN CAMERA DATA LANE 1.2 (DATA2P1, DATA2N1)
WriteByte(0x0009, 0x00);
    // 0x00 disable Data Lane 1.2 (DATA2P1, DATA2N1). CSI dual lane or second lane, Enable Data Lane
    1.2: 0x01
WriteByte(0x000a, 0x01);
    // CSI dual lane or second lane, set CSI mode 0x01, CCP second lane, set CCP 0x0e

// SECOND CAMERA CLOCK LANE 2 (CLKP2, CLKN2)
WriteByte(0x0031, 0x14);
    // Disable second camera: 0x00. Second camera: Enable Clock Lane 2 (CLKP1, CLKN1) and UI
    programmation: 0x17 between 400MHz and 334Mhz, , 0x1B between 333 and 286MHz, 0x1F between
    285 and 250MHz,0x23 between 249 and 223MHz, 0x27 between 222 and 200Mhz and so on
WriteByte(0x0033, 0x1c);
    // Second camera CCP/CSI(CLKP2, CLKN2, DATAP2, DATAN2) : CCP 0x1c or CSI 0x02

// SECOND CAMERA DATA LANE 2 (DATA1P2, DATA1N2)
WriteByte(0x0034, 0x00);
    // 0x00 Disable Data Lane2 , Enable Data lane 2: 0x01 (for CCP or CSI)
WriteByte(0x0035, 0x0e);
    // CCP 0x0e, CSI 0x01 on second camera

// CCP MODE (unused in CSI mode)
WriteByte(0x000d, 0x00);
// For CCP main camera,CCP Data clock mode 0x00, CCP data strobe mode 0x01

WriteByte(0x000e, 0x28);
    // For CCP mode, Pixel width: 0x30 for 12bits, 0x28 for 10bits,0x20 for 8bits, 0x1C for 7bits,0x18 for 6bits
WriteByte(0x0038, 0x00);
    // For CCP 2nd camera, CCP Data clock mode 0x00, CCP data strobe mode 0x01

// MODE CONTROL
WriteByte(0x0014, 0x40);
    // No decompression: 0x41  For CCP, 0x40 for CSi single lane, 0x42 for CSi dual lane. Decompression
    mode please refer to datasheet/register map.
WriteByte(0x0015, 0x00);
    // Normal (non Tristated output), continious clock, clock polarity and synchronization signals not inverted
WriteByte(0x0036, 0x20);
    // Enable compensation macro, 0.90Rev of DPHY. 0x20 for main camera, 0x21 for second camera
    // Enable compensation macro, 0.81Rev of DPHY. 0x24 for main camera, 0x29 for second camera
WriteByte(0x0017, 0x00);
    // Data type: 0x1E YUV422 8-bit, 0x1F YUV422 10-bit, 0x22 RGB565, 0x2A RAW8, 0x2B RAW10,
    0x2C RAW12, for other mode please refer to CSI specifications
WriteByte(0x0018, 0x00);
    // Data type of embedded data: 0x1E YUV422 8-bit, 0x1F YUV422 10-bit, 0x22 RGB565, 0x2A RAW8,
    0x2B RAW10, 0x2C RAW12, for other mode please refer to CSI specifications
WriteByte(0x0019, 0x00);
    // 0X00 Data type and pixel width extracted from data stream, 0x04 Data type programmed, pixel width
    extracted from data type, 0x0c Data type and pixel width programmed

// MANDATORY FOR CCP MODE AND DECOMPRESSION MODE (unused for uncompressed image
format in CSI mode)
WriteByte(0x001b, 0x00); // LSB of the active lines number
WriteByte(0x001a, 0x00);  // MSB of the active lines number
WriteByte(0x001d, 0x00); // LSB of the embedded lines number (aka status lines number)
WriteByte(0x001c, 0x00);  // MSB of the embedded lines number (aka status lines number)

// PIXEL WIDTH and decompression ON/OFF
WriteByte(0x001e, 0x00);
    //  Image data not compressed: 0x06 for Raw6, 0x07 for Raw7, 0x08 for 8 bits, 0x0A for 10bits, 0x0c for
    Raw12. Image data compressed:0x1a for 12-10, 0x18 for 12-8 and 10-8, 0x17 for 12-7 and 10-7, 0x16 for
    12-6 and 10-6
WriteByte(0x001f, 0x00);
    // Embedded data not compressed: 0x06 for Raw6, 0x07 for Raw7, 0x08 for 8 bits, 0x0A for 10bits, 0x0c
    for Raw12. Embedded data compressed:0x1a for 12-10, 0x18 for 12-8 and 10-8, 0x17 for 12-7 and 10-7,
    0x16 for 12-6 and 10-6
```

11 Electrical characteristics

For all CSI2 electrical characteristics, please refer to the MIPI Camera Serial Interface Version 2 (CSI-2).

11.1 Absolute maximum ratings

Table 5. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DDE_1V8}	Digital I/O supply	-0.5 to 2.8	V
V_{DDIN_LDO}	Voltage regulator supply	-0.5 to 2.8	
	Voltage on any signal ball	-0.5 to (V_{DD} + 0.5)	
I_{DD}	Supply current	100	mA
	Current on any signal ball	10	
T_{STO}	Storage temperature	-40 to 150	°C
T_{LEAD}	Lead temperature (soldering, 10 s)	260	

Caution: Stresses above those listed under the “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

11.2 Operating conditions

Table 6. Operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DDE_1V8}	Digital I/O supply	1.7	1.8	1.9	V
V_{DDIN_LDO}	Voltage regulator supply	1.7	1.8	1.9	
T_A	Ambient temperature	-25		70	°C
C_{REG}	LDO output load capacitor, ESR <1Ω @ 100 kHz		1		µF
C_{EXT}	1.2 V decoupling capacitor		10		nF

11.3 Thermal data

Table 7. Thermal data

Symbol	Parameter	Value	Unit
Rth(j-a)	Max. junction-ambient thermal resistance - VFBGA49 (1)	58.4	°C/W

1. *Typical, measured with the component mounted on an evaluation PC board in free air*

11.4 DC electrical characteristics

The values below apply over the operating conditions unless otherwise specified.

Table 8. I/O electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low voltage		-0.3		0.3 V_{DD} (1)	V
V_{IH}	Input high voltage		0.7 V_{DD} (1)		V_{DD} + 0.3 (1)	
V_{OL}	Output low voltage	I_{OL} < 2 mA, I_{OL} < 3 mA on SDA			V_{DD} + 0.2 (1)	
V_{OH}	Output high voltage	-I_{OH} < 2 mA, -I_{OL} < 3 mA on SDA	0.8 V_{DD} (1)			
I_{IL}/I_{IH}	Input leakage current, input balls	V_{SS} < V_{IN} < V_{DD}			20	µA
	Input leakage current,I/O balls				10	
$V_{EXTCLKDC}$	Clock input amplitude, DC	DC coupled square wave	1.5	1.8	2.4	V
$V_{EXTCLKAC}$	Clock input amplitude, AC	AC coupled sine wave	0.5	1	1.2	Vpp
C_{IN}	SCL input capacitance	T_A = 25 °C, freq. = 1 MHz			10	pF
$C_{I/O}$	SDA input / output capacitance				10	

1. *V_{DD} refers to the supply voltage (VDDE_1V8, VDDIN_LDO) to which the signal is referenced*

Table 9. Power supply specifications for VDDIN_LDO

Symbol	Parameter	Test conditions	Typ.	Max.	Unit
I_{DDPD}	V_{DD} supply current in Power down mode	V_{DD} = max; XSDN < V_{IL}	1	5	µA
$I_{DDBYPASS}$	V_{DD} supply current in Bypass mode	V_{DD} = max; image format = RAW8; input/ouput data rate = 1.6 Gbps CSI dual	25	30	mA
$I_{DDNORMAL}$	V_{DD} supply current in Normal mode	V_{DD} = max; CCP RAW10 640 Mbps	18	40	
		V_{DD} = max; CSI single RAW10 800 Mbps	20	45	
		V_{DD} = max; CSI dual RAW12 1.6 Gbps	25	50	

Table 10. Power supply specifications for VDDE_1V8

Symbol	Parameter	Test conditions	Typ.	Max.	Unit
I_{DDPD}	V_{DD} supply current in Power down mode	V_{DD} = max; PDN < V_{IL}	1	50	µA
$I_{DDBYPASS}$	V_{DD} supply current in Bypass mode	V_{DD} = max; image format = RAW8; input/ouput data rate = 1.6 Gbps CSI dual	11	15	mA
$I_{DDNORMAL}$	V_{DD} supply current in Normal mode	V_{DD} = max; CCP RAW10 640 Mbps	11	25	
		V_{DD} = max; CSI single RAW10 800 Mbps	12	25	
		V_{DD} = max; CSI dual RAW12 1.6 Gbps	18	30	

Table 11. CCP2 class 2 receiver electrical characteristics

For further information on CCP2, please refer to the SMIA 1.0 Part 2: CCP2 Specification Available from http://www.smiaforum.org

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CMI_SMIA}	Input common mode voltage range	Embedded R_{TI} = 100 Ω ± 10 %	0.65	0.95	1.15	V
V_{IDTH_SMIA}	Input differential threshold (V_P - V_N)		±50		±200	mV
t_{PWRUP}/t_{PWRDN}	Power up/-down time				20	µs
R_{TI}	Embedded termination resistance		80	100	125	Ω

11.5 AC electrical characteristics

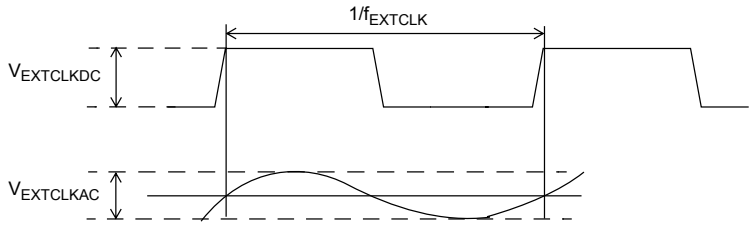
11.5.1 EXTCLK

$V_{EXTCLKAC}$ and $V_{EXTCLKDC}$ are defined in Table 8. I/O electrical characteristics

Table 12. EXTCLK electrical characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{EXTCLK}	Clock frequency input, 50 % duty cycle - VDDE_1V8 referred	6	13	27	MHz

Figure 10. **EXTCLK electrical characteristics**



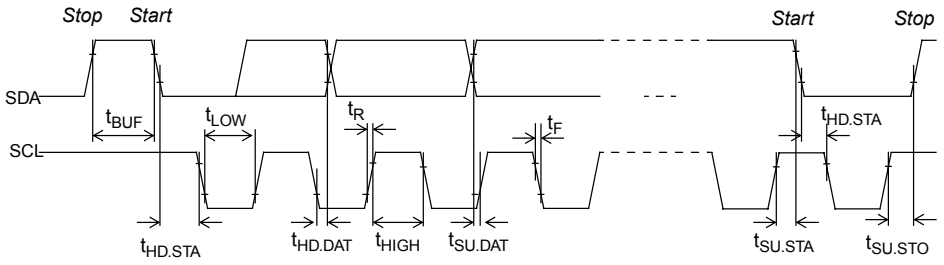
11.5.2 I2C slave timing (SCL, SDA)

Table 13. **I2C slave timing**

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{SCL}	SCL clock frequency	100		400	kHz
t_{LOW}	Clock pulse width low	1.3			µs
t_{HIGH}	Clock pulse width high	0.6			
t_{BUF}	Bus free time between transmissions	1.3			
$t_{HD.STA}$	Start hold time	0.6			
$t_{SU.STA}$	Start setup time	0.6			
$t_{HD.DAT}$	Data hold time	0		0.9	
$t_{SU.DAT}$	Data setup time	100			ns
t_R	SCL / SDA rise time (1)			300	
t_F	SCL / SDA fall time (1)			300	
$t_{SU.STO}$	Stop setup time	0.6			µs

1. *Measured from 0.3 to 0.7 or 0.7 to 0.3 V_{DD}*

Figure 11. **I2C slave timing**



11.5.3 CCP2 serial receiver timing (DATA1P1/N1, CLKP1/N1 and DATA1P2/N2, CLKP2/N2)

Table 14. CCP2 serial receiver data/clock (class 0) input timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{DS}	Data setup time	1	—	—	ns
t_{CKP}	Clock period	4.8			

Figure 12. CCP2 data/clock input timing

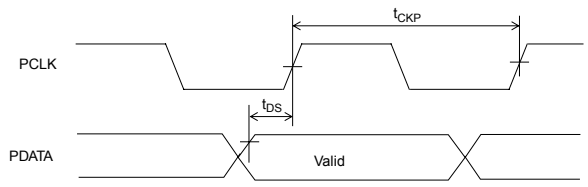
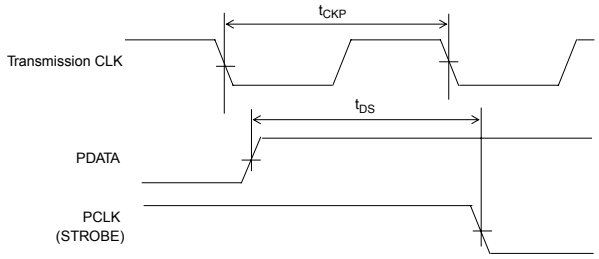


Table 15. CCP2 serial receiver data/strobe (class 2) input timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{DS}	Data to strobe edge setup time	$t_{CKP-780}$	t_{CKP}	$t_{CKP+780}$	ps
t_{CKP}	Transmission clock period	1.56			ns

Figure 13. CCP2 data/strobe input timing



11.5.4 Parallel output interface timing

Figure 14. Parallel output interface timing diagram - inverted clock

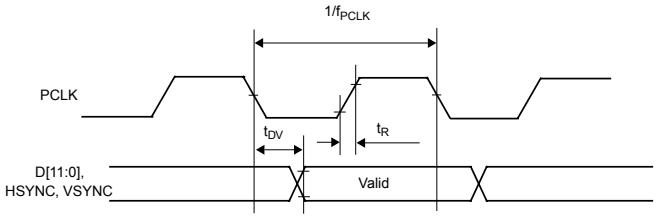
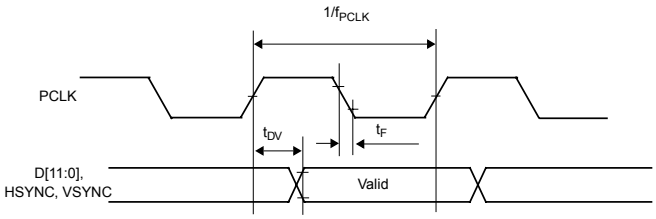


Figure 15. Parallel output interface timing diagram - non inverted clock



Note: For Non-inverted clock mode, the valid edge to capture is the negative (falling) edge
For RAW6/RAW7 dual lane, the bandwith is limited to 800 Mbps.

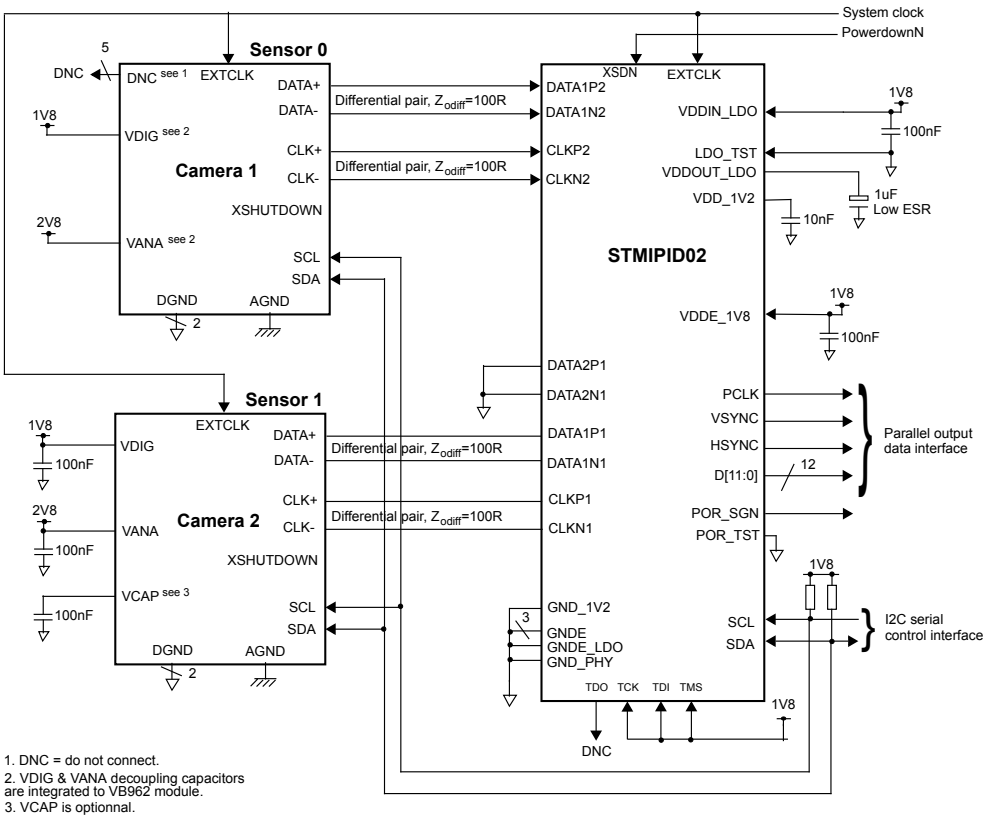
Table 16. Parallel output interface timing

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
f_{PCLK}	PCLK frequency				200	MHz
D_{PCLK}	PCLK duty cycle	No bypass, RAW6 dual lane		50		%
		No bypass, RAW7 dual lane		66		
		No bypass, RAW7 dual lane, jittered clock		50-60		
		No bypass, RAW7 single lane		57.14		
		Bypass and all other modes	45	50	55	
t_R	PCLK rise time, 20 % - 80 %	Load capacitance, C_L = 50 pF			2.1	ns
t_{DV}	PCLK to output valid		0		2	

12 Application schematics

The application schematic given below shows an example of the STMIPID02 application with a CSI-2 sensor.

Figure 16. STMIPID02 recommended schematic with camera 1 (CSI-2) and camera 2 (CCP2)

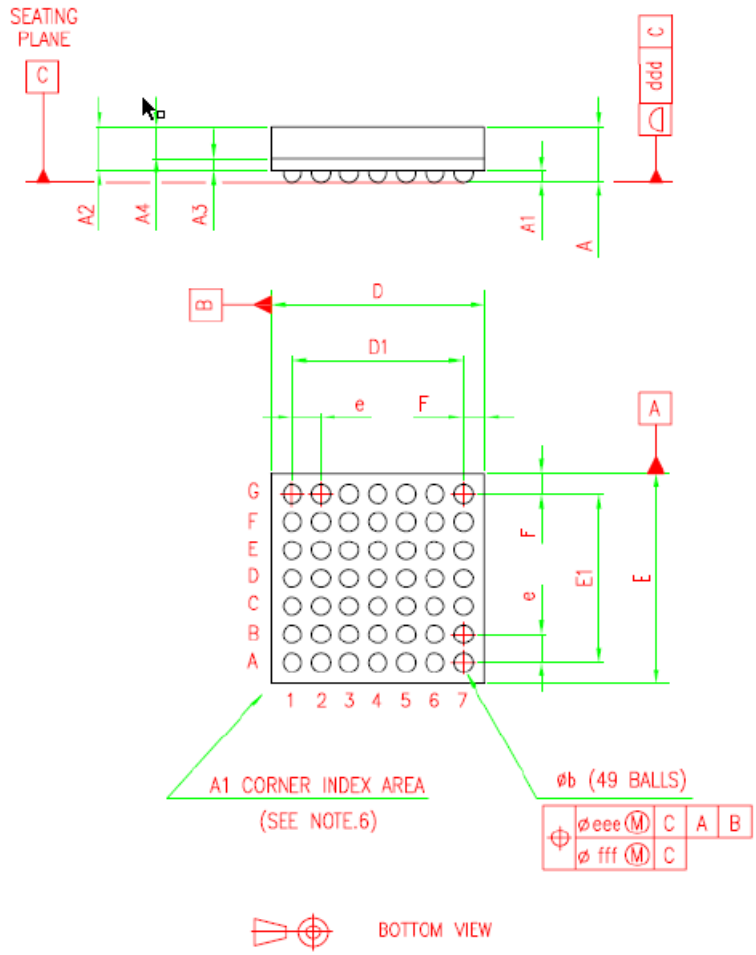


13 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

13.1 VFBGA package information

Figure 17. VFBGA package outline



Note: The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized marking, or other feature of package body or integral heatslug. A distinguishing feature is allowed on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

Table 17. VFBGA mechanical data

Reference	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A (1)			1.00			0.039
A1	0.125			0.005		
A2		0.615			0.024	
A3		0.18			0.007	
A4			0.45			0.018
b (2)	0.22	0.26	0.30	0.009	0.010	0.012
D	2.95	3.00	3.05	0.116	0.118	0.120
D1		2.40			0.094	
E	2.95	3.00	3.05	0.116	0.118	0.120
E1		2.40			0.094	
e		0.40			0.016	
F		0.30			0.012	
ddd			0.08			0.003
eee (3)			0.13			0.005
fff (4)			0.04			0.002

1. *VFBGA stands for very thin profile fine pitch ball grid array. Very thin profile: 0.80 mm < A ≤ 1.00 mm / fine pitch: e < 1.00 mm. The maximum total package height is calculated by the following methodology: A2 Typ. + A1 Typ. + square-root(A1 +A3 +A4 tolerance values).*
2. *The typical ball diameter before mounting is 0.25 mm.*
3. *The tolerance of the position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone, eee, perpendicular to datum C and located on the true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.*
4. *The tolerance of the position that controls the location of the balls within the matrix with respect to each other. For each ball, there is a cylindrical tolerance zone, fff, perpendicular to datum C and located on the true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.*

14 PCB layout guide

The usual good PCB design rules should be observed for the layout of the STMIPID02.

Power and ground planes should be used to supply power to the STMIPID02.

The high-speed signal pairs (CLKP1, CLKN1), (DATA1P1, DATA1N1), (DATA2P1, DATA2N1), (CLKP2, CLKN2) and (DATA1P2, DATA1N2) should be routed as balanced transmission lines with a characteristic differential impedance (Zo_{diff}) of 100 Ω, and matched in length.

The delay difference between Cclock lane, data lane1 and data lane2 should be less than 5 ps.

The total series resistance of the CSI line should be less than 5 Ω.

For more details, please refer to the MIPI Alliance Specification for D-PHY", version 0.90.00, 8 October 2007, Section 7 "Interconnect and Lane Configuration" and Annex B "Interconnect Design Guidelines".

The output interface clock (PCLK) should be 50 Ω adapted.

The output clock (PCLK) and data line length from the STMIPID02 to the host should be as small as possible to avoid reflection effects.

All passive components for the STMIPID02 should be placed in close proximity to the device, including the decoupling capacitors.

The recommended pull up value of the I2C is in the range 2480 Ω to2780 Ω for a bus load capacitance below 100 pF.

The recommended capacitor values are:

- 10 nF on VDD1V2
- 100 nF on VDDIN_LDO and VDDE_1V8
- 1 µF (low ESR <1 Ω) on VDDOUT_LDO

15 ESD characteristics

The device ESD sensitivity is compliant with the following specifications:

- JESD22 A114D, human body model, ±2 kV, class 2 compliant
- JESD22-C101C, charge device model, ±500 V, class III compliant

16 Ordering information

Table 18. **Order code**

Sales type	Package
STMIPID02/TR	VFBGA 49 ball, 3 mm x 3 mm x 1 mm, 0.4 mm pitch, 0.25 mm ball package

Revision history

Table 19. **Document revision history**

Date	Version	Changes
22-Oct-2018	1	Initial public release

Contents