Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	30	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 kΩ)	30	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at T_C = 25°C	80	A
I_D	Drain current (continuous) at T_C = 100°C	60	A
I_{DM} (1)	Drain current (pulsed)	320	A
	Derating factor	1	
P_{TOT}	Total dissipation at T_C = 25°C	150	W
dv/dt (2)	Peak diode recovery voltage slope	7	V/ns
T_J Tstg	Operating junction temperature Storage temperture	-55 to 175	°C

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 20A$, di/dt ≤ 100A/µs, V_{DD} = 80% $V_{(BR)DSS}$

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case Max	1	°C/W
R_{thJA}	Thermal resistance junction-ambient Max	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

Table 3. Avalanche characteristics

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj max)	80	A
E_{AS}	Single pulse avalanche energy (starting Tj=25°C, Id=Iar, Vdd=50V)	600	mJ

2 Electrical characteristics

(T_{CASE} = 25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250µA, V_{GS}= 0	30			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating @125°C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{DS} = ± 20V			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250µA	1	1.7	2.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 40A V_{GS} = 4.5 V, I_D = 40A		0.005	0.006 0.008	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, I_D = 40A	30	50		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse Transfer Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} =0		6500 1500 500		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 24 V, I_D = 80A, V_{GS} = 5V		95 30 44	130	nC nC nC

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 15 V, I_D = 40 A R_G = 4.7Ω V_{GS} = 4.5 V *Figure 12.*		40	55	ns
t_r	Rise time			260	350	ns
$t_{r(Voff)}$ t_f t_c	Off-voltage rise time Fall time Cross over time	V_{DD} = 24 V, I_D = 80 A, R_G = 4.7Ω, V_{GS} = 5V *Figure 12.*		70 165 250	95 220 340	ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				80 320	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 80A, V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 80 A, di/dt = 100A/µs, V_{DD} = 15 V, T_J = 150°C *Figure 15.*		75 0.14 4		ns nC A

1. Pulse with limited by safe operating area
2. Pulsed: pulse duration = 300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

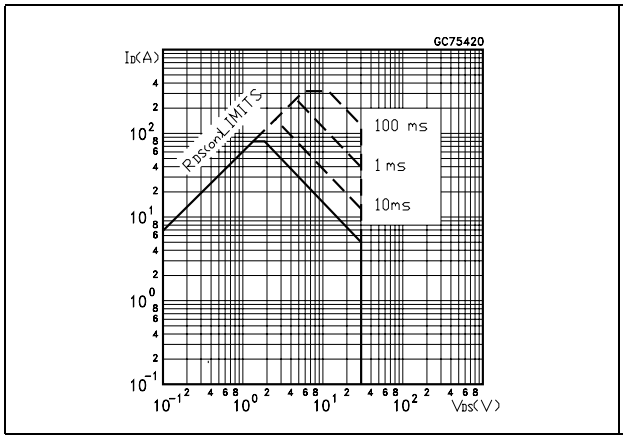


Figure 2. Thermal impedance

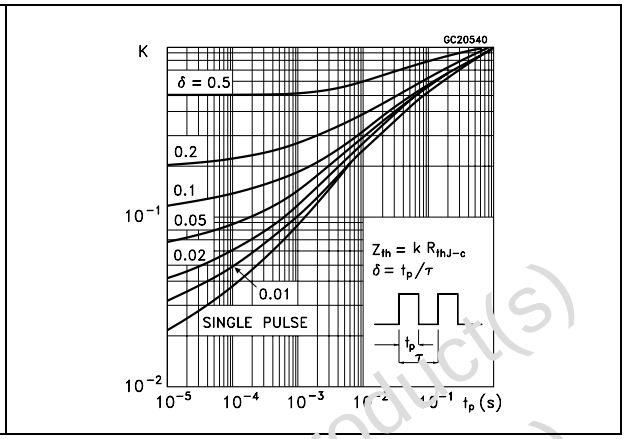


Figure 3. Output characterisics

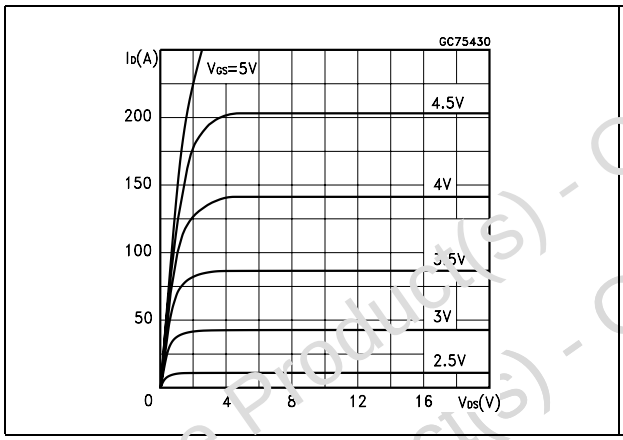


Figure 4. Transfer characteristics

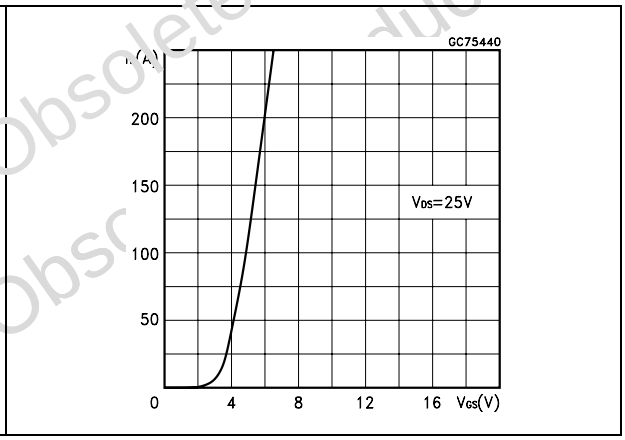


Figure 5. Transconductance

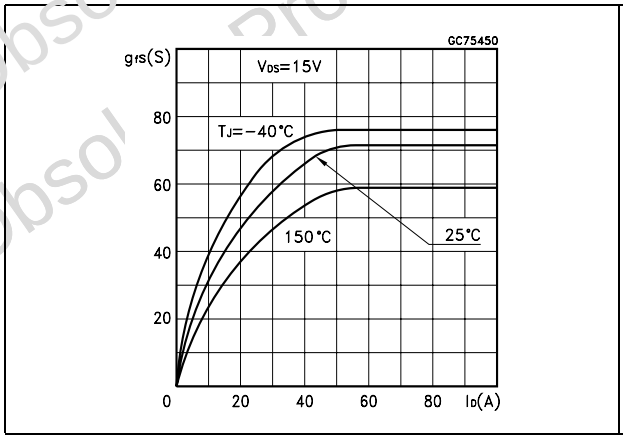


Figure 6. Static drain-source on resistance

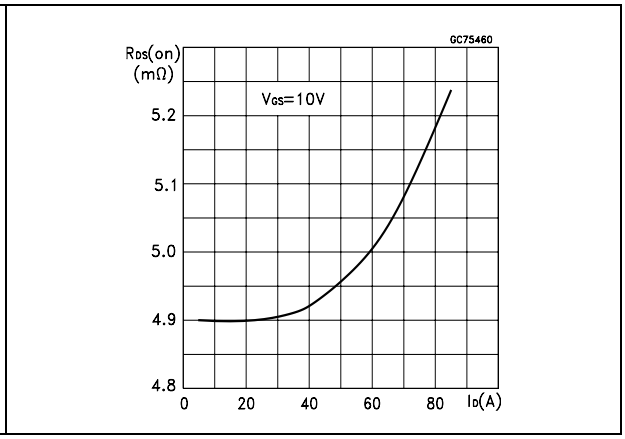


Figure 7. Gate charge vs gate-source voltage

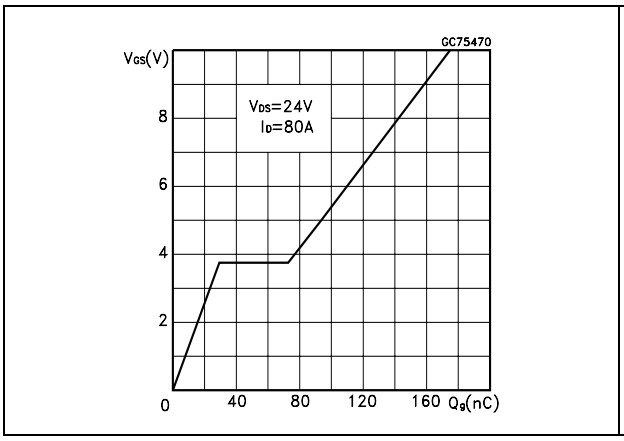


Figure 8. Capacitance variations

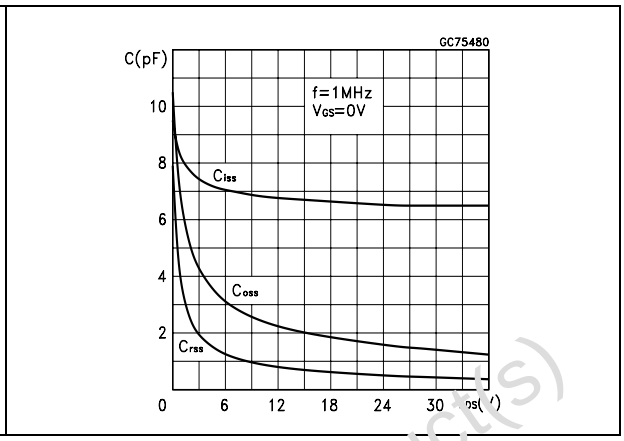


Figure 9. Normalized gate threshold voltage vs temperature

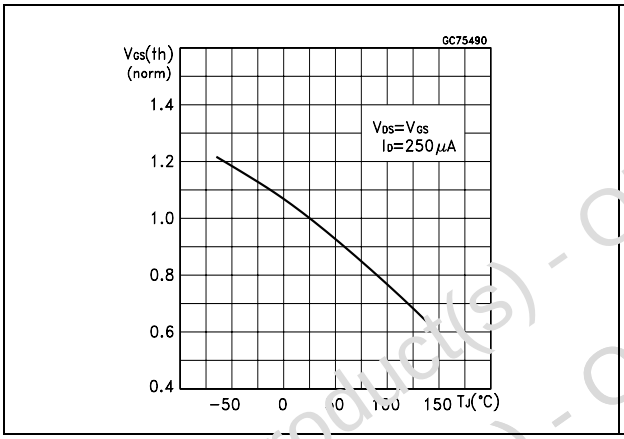


Figure 10. Normalized on resistance vs temperature

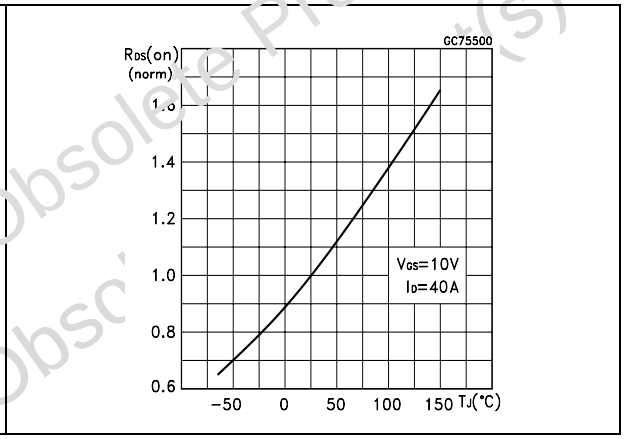
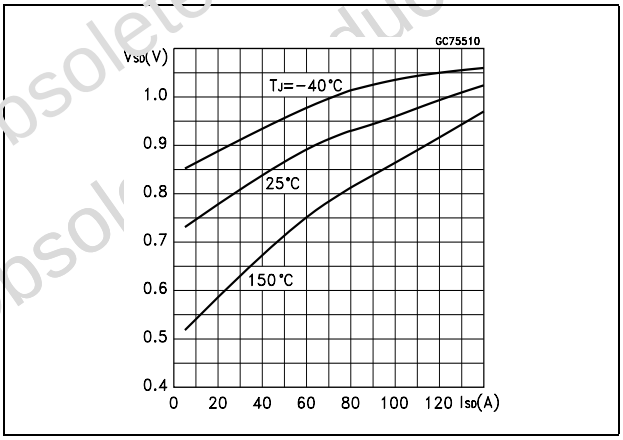


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load

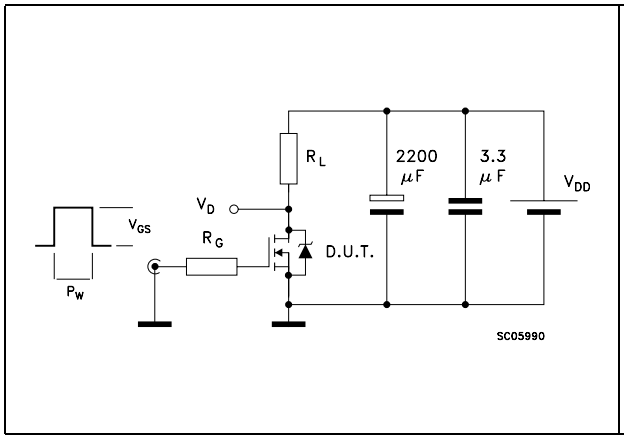


Figure 13. Gate charge test circuit

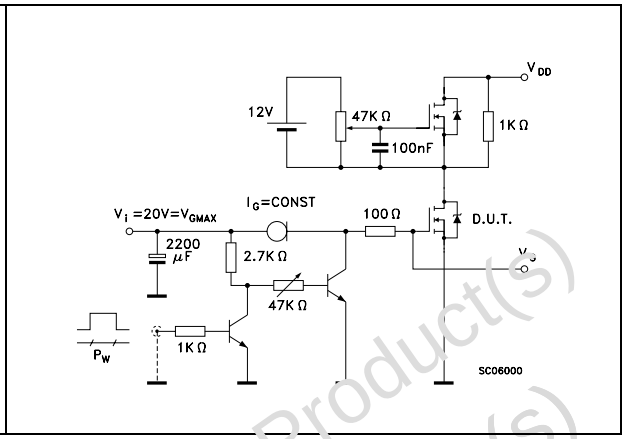


Figure 14. Test circuit for inductive load switching and diode recovery times

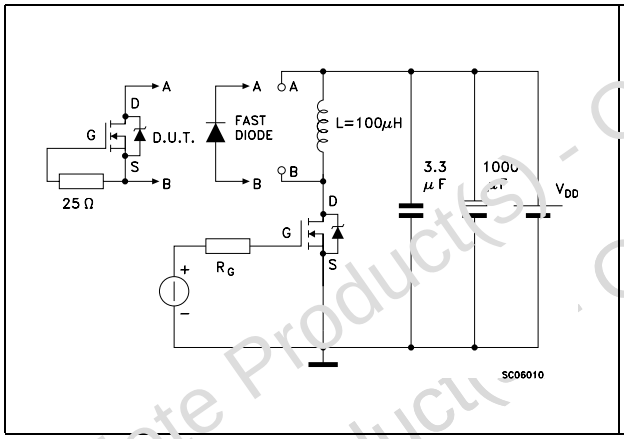


Figure 15. Unclamped inductive load test circuit

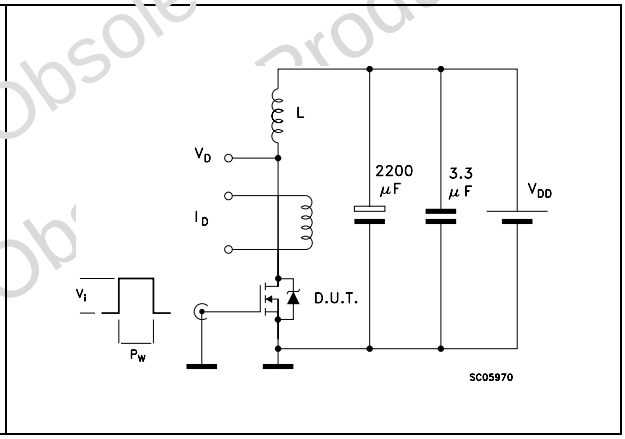
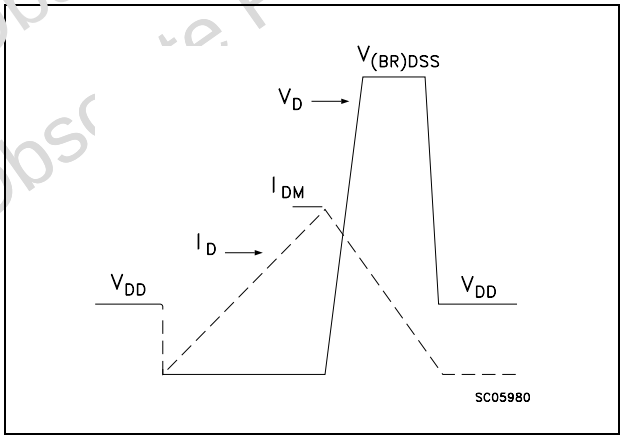


Figure 16. Unclamped inductive waveform

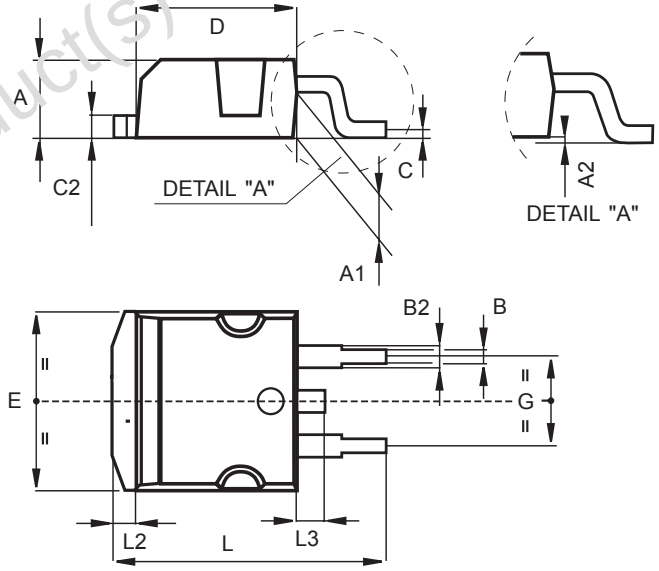


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-263 (D^2PAK) MECHANICAL DATA

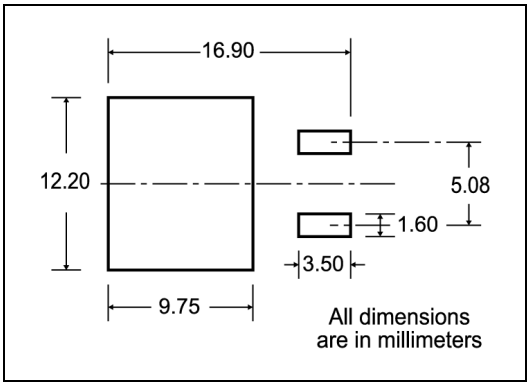
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
E	10		10.4	0.393		0.409
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.624
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068



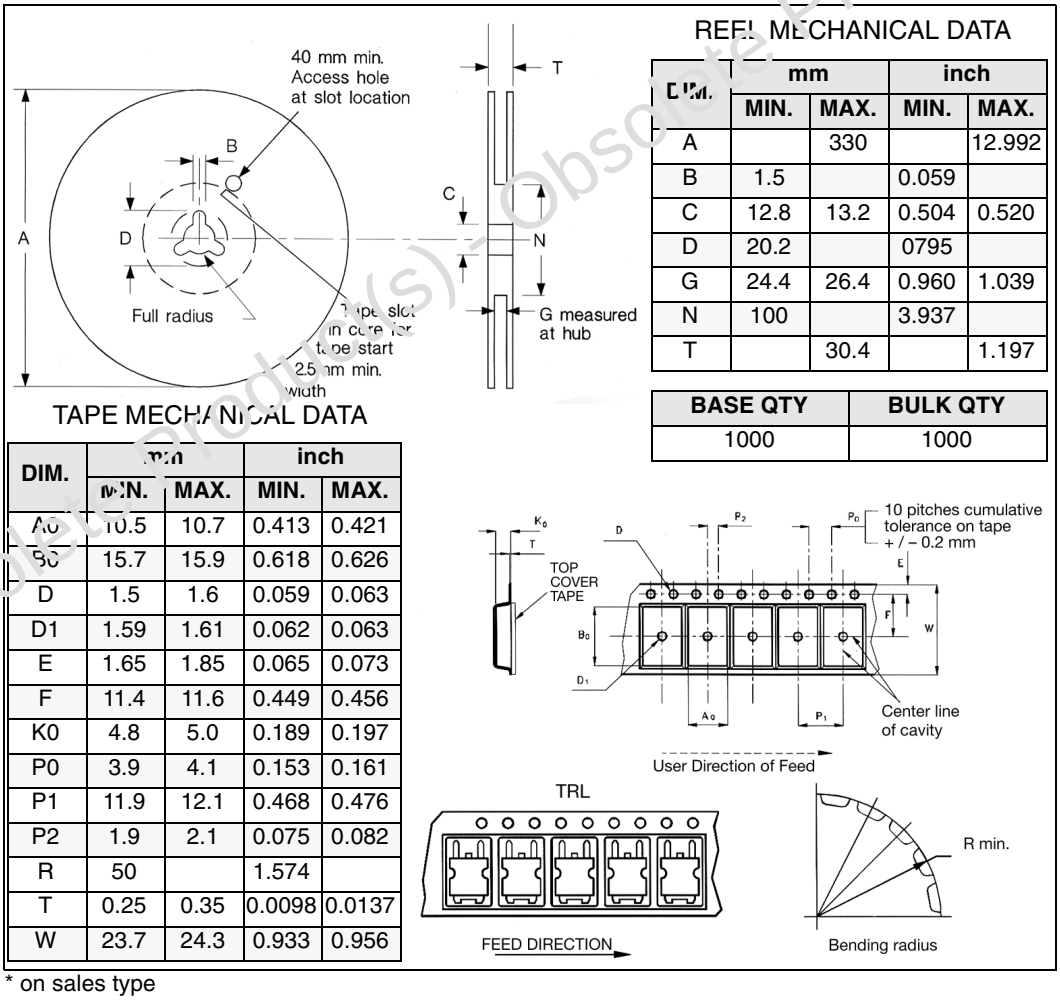
P011P6/F

5 Packaging mechanical data

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956

* on sales type

6 Revision history

Table 8. Revision history

Date	Revision	Changes
21-Jun-2004	5	Preliminary version
25-Jul-2006	6	New template, SOA updated

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