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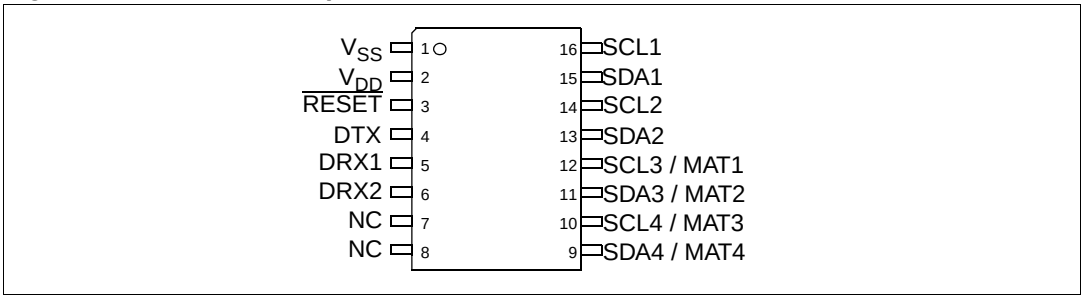
1 Pin description

Figure 2. SO16 narrow pinout



1. NC = Not Connected

See *Table 2* for a description of the pin functions.

Table 2. Pin functions

Pin number SO16	Function name	Function description
1	V_{SS}	Ground
2	V_{DD}	Power Supply (+5 volts)
3	RESET	Reset (active low) input
4	DTX	DiSEqC data transmit output
5	DRX1(1)	DiSEqC-ST(2) and legacy DiSEqC(3) 1.0 data receive input
6	DRX2	DiSEqC-ST data receive input and DiSEqC- 1.0 with 13 to 18V transition (if a DiSEqC- command is sent before on DRX1)
7,8	-	Not used (4)
9	SDA4 / MAT4	I^2C data line 4 / legacy matrix control line 4
10	SCL4 / MAT3(5)	I^2C clock line 4 / legacy matrix control line 3
11	SDA3 / MAT2	I^2C data line 3 / legacy matrix control line 2
12	SCL3 / MAT1	I^2C clock line 3 / legacy matrix control line 1
13	SDA2	I^2C data line 2
14	SCL2	I^2C clock line 2
15	SDA1	I^2C data line 1
16	SCL1	I^2C clock line 1

1. If only one input is required by the application, DRX1 must be used by default.
2. DiSEqC-ST: special DiSEqC command set for SaTCRs control (refer to *Section 3.2* for more details).
3. DiSEqC 1.0: refer to *Section 3.3*.
4. Unused pins must be tied to ground.
5. During normal operation this pin must not be pulled-down.

2 Implementation

2.1 SaTCRs mapping

The ST7LNB1Y0 could communicate through I^2C with up to 8 SaTCRs (refer to *Table 3*). The following hardware implementation of SaTCRs must be respected:

Table 3. SaTCRs implementation

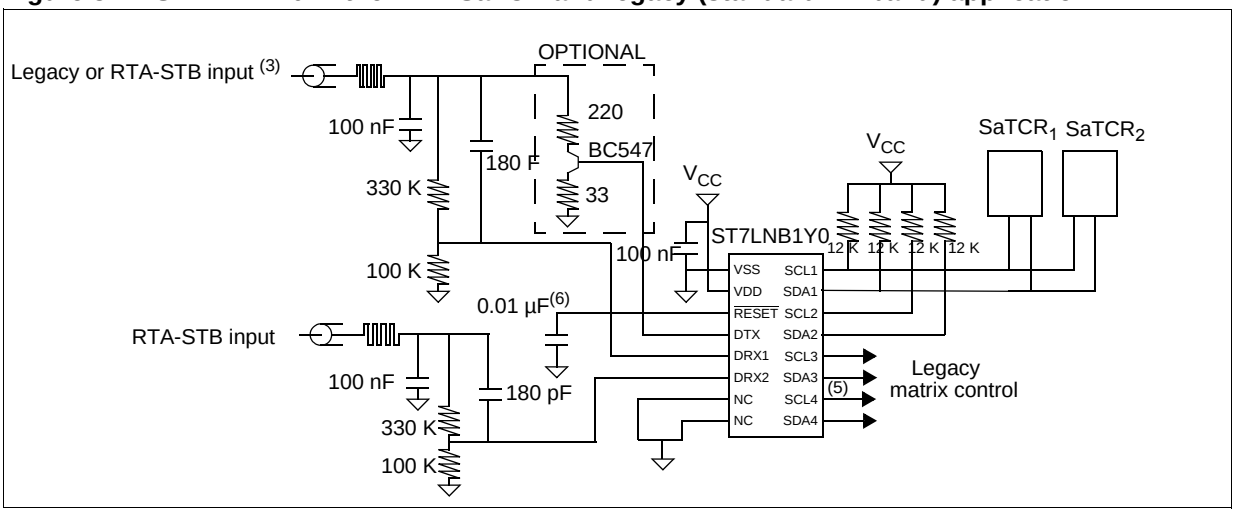
SaTCR number	SaTCR(1)	SaTCR address	I^2C line
0	$SaTCR_1$	C8h	I^2C 1
1	$SaTCR_2$	CAh	
2	$SaTCR_3$	C8h	I^2C 2
3	$SaTCR_4$	CAh	
4	$SaTCR_5$	C8h	I^2C 3
5	$SaTCR_6$	CAh	
6	$SaTCR_7$	C8h	I^2C 4
7	$SaTCR_8$ / legacy SaTCR (for wide RF band applications)	CAh	

1. As a convention, SaTCR1 must be associated to the BPF having the lowest center frequency of the application, SaTCR2 to the BPF having the next higher center frequency and so on.

2.2 Application example

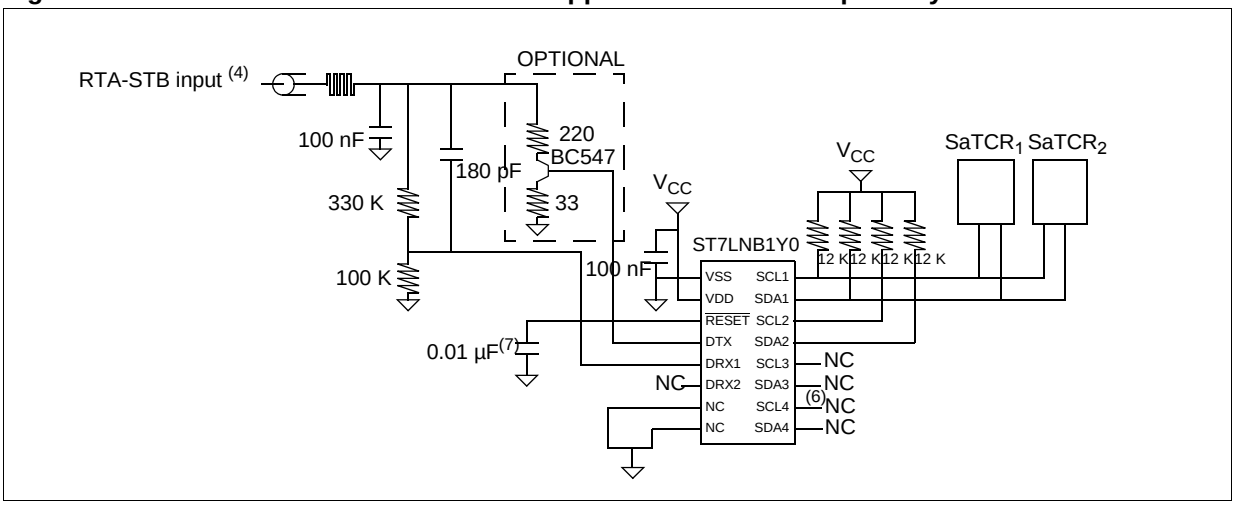
Figure 3 and *Figure 4* show example application circuits for the ST7LNB1Y0 with and without legacy signal.

Figure 3. ST7LNB1Y0 in the Twin SaTCR and legacy (standard RF band) application



1. The divider chain connected to the DRX1 and DRX2 pins must have the following resistance values: 330KΩ and 100 KΩ.
2. Unused I^2C lines (14,13) have to be linked to V_{CC} through 12 KΩ resistors.
3. RTA-STB: remote tuning able set-top box (STB supporting SaTCR control).
4. The transistor is optional, it is used for EEPROM parameters bytes reading using DiSEqC.
5. During normal operation this pin must not be pulled-down.
6. When the LVD is enabled (default state), it is mandatory not to connect a pull-up resistor. A 10 nF pull-down capacitor is recommended to filter noise on the reset line.

Figure 4. ST7LNB1Y0 in the Twin SaTCR application with one input only



1. NC = Not Connected.
2. The divider chain connected to the DRX1 pins must have the following resistance values: 330 KΩ and 100 KΩ.
3. Unused I^2C lines (SCL2,SDA2) have to be linked to V_{CC} through 12 KΩ resistors.
4. RTA-STB: Remote Tuning Able Set Top Box (STB supporting SaTCR control).
5. The transistor is optional, it is used for EEPROM parameters bytes reading using DiSEqC.
6. During normal operation this pin must not be pulled-down.
7. When the LVD is enabled (default state), it is mandatory not to connect a pull-up resistor. A 10 nF pull-down capacitor is recommended to filter noise on the reset line.

3 Functional description

3.1 ST7LNB1Y0 applications

The ST7LNB1Y0 is intended to be used in different LNB switcher applications supporting SaTCRs.

Three main types of applications could be distinguished (see *Table 4*).

Table 4. Application types

Num	Application type	Description
0	SaTCR control(1) (see *Figure 5*)	– Control through I^2C of up to 8 SaTCRs
1	SaTCR and legacy (standard RF band) (see *Figure 6*)	– The ST7LNB1Y0 controls through I^2C up to 4 SaTCRs – Control of a legacy matrix using up to 4 pins
2	SaTCR and legacy (wide RF band) (see *Figure 7*)	– Control though I^2C of up to 6 SaTCRs + legacy – Control of a dedicated SaTCR for the legacy support

1. This application could support up to 8 RF feeds. (applications 1 and 2 are limited to 4 RF feeds).

An EEPROM parameter will be used for configuring the ST7LNB1Y0 for a particular application type (refer to *Section 4* for more details on how to program the EEPROM parameter).

Figure 5. SaTCR control block diagram

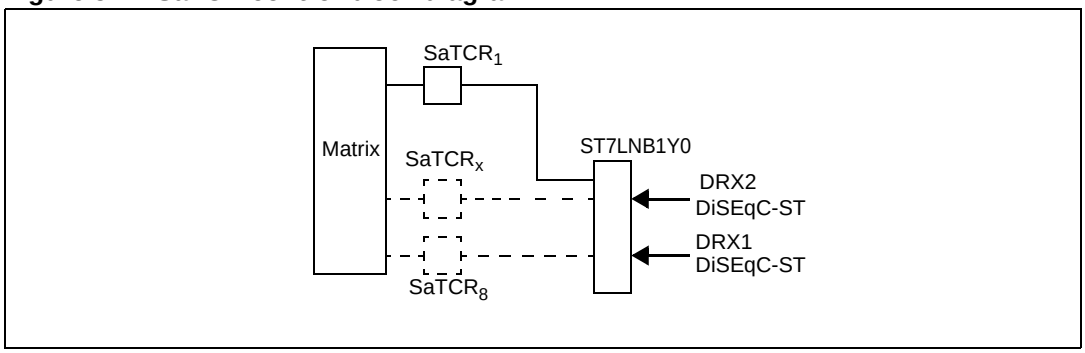


Figure 6. SaTCR control and legacy (standard RF band)

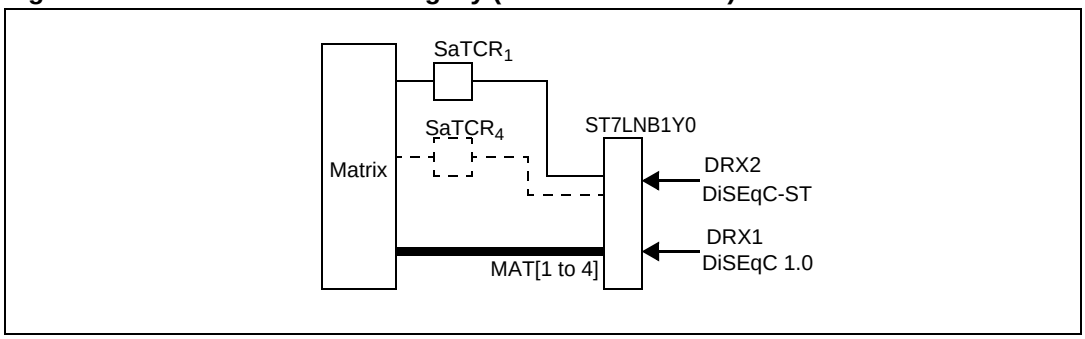
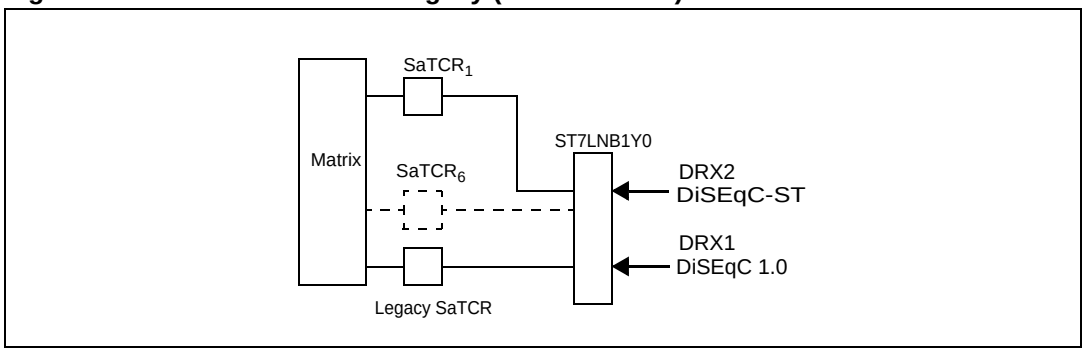


Figure 7. SaTCR control and legacy (wide RF band)



3.2 DiSEqC-ST commands

To control SaTCR based LNBs and switchers, two new DiSEqC commands are used:

- ODU_SatCR_Op (5Ah): this command is used during LNB or switcher normal operation.
- ODU_SatCR_Inst (5Bh): this command is used only during the LNB or switcher installation.

Both commands frames must have the following DiSEqC format:

Table 5. DiSEqC-ST command format

E0h / E2h(1)	DiSEqC Slave address	5Ah /5Bh	DATA1	DATA2

1. All commands accept E0h or E2h framing. Whatever the command, if E2h framing is used, then the MCU sends at least the response E4h (refer to *Section 4.2*).

Different subcommands are defined, depending on the data bytes which are sent (refer to *Table 6* and *Table 7*).

Table 6. ODU_SaTCR_Op (5Ah)

Sub-command	DATA1						DATA2	Command Description
	7	6	5	4:2	1	0		
ODU_ChangeChannel	SaTCR(1)			Feed(2)	Tun[9](3)	Tun[8]	Tun[7:0]	This command is used for the channel selection.
ODU_PowerOff	SaTCR			0			00h	This command is used to put a SaTCR in low power mode.

1. SaTCR: SaTCR number [0 to 7] (refer to *Table 3*).
2. Feed: matrix RF input [0 to 7] (refer to *Table 9*).
3. Tun[9:0]: tuning word.

Table 7. ODU_SaTCR_Inst(5Bh)

Sub-command	DATA1								DATA2	Command Description
	7	6	5	4	3	2	1	0		
ODU_Config(1)	SaTCR			0	0	0	0	1	AppliNum(2)	This command is sent by an RTA-STB in order to determine the ST7LNB1Y0 application number.
ODU_Lofreq(3)	SaTCR			0	0	0	1	0	LOfreqNum(4)	This command is sent by the RTA-STB in order to determine the L.O frequencies present in the LNB.
ODU_SaTCRxSignalOn	xx			00					xxh	When receiving this command the ST7LNB1Y0 commands all the SaTCRs to send a tone in order to indicate their respective BPF center frequencies.

1. ODU_Config: When receiving this command the ST7LNB1Y0 checks if the Polonium indicated in data1 corresponds to the ST7LNB1Y0 application number, if it is the case the ST7LNB1Y0 commands SaTCR indicated in data1 to send a tone having as frequency F = $Fbpf_{SaTCR}$ else F = $Fbpf_{SaTCR}$ + 20 MHz.
2. AppliNum: application number [1 to FFh] (refer to *Table 11*).
3. ODU_Lofreq: When receiving this command the ST7LNB1Y0 checks if the LOfreqNum indicated in data1 corresponds to the one of the L.Os present in the application, if it is the case the ST7LNB1Y0 commands SaTCR indicated in data1 to send a tone having as frequency F = $Fbpf_{SaTCR}$ else F = $Fbpf_{SaTCR}$ + 20 MHz.
4. LofreqNum: Local oscillator table entry number [1 to FFh] (refer to *Table 10*).

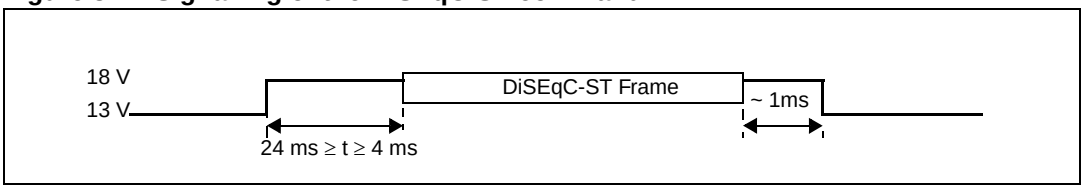
Table 8. DiSEqC-ST command examples

LNB	DiSEqC Frame	Description
ODU_Config	E0 00 5B 01 02	The STB asks if the application number is 2, the reply tone is expected from $SaTCR_1$.
ODU_Lofreq	E0 10 5B 42 04	The STB asks if the LO frequency number 4 is present on the LNB, the reply tone is expected from $SaTCR_3$.
ODU_Change_Channel	E0 00 5A 24 55	The STB asks for a channel_change on $SaTCR_2$ with a Tuning = 055h from matrix RF input = Feed1.

3.2.1 Command signalling

In order to be detected, the DiSEqC-ST commands must be sent after a voltage change from 13 to 18 V. A delay time, t, between 4 ms and 24 ms must be respected before sending the DiSEqC-ST commands (see *Figure 8*).

Figure 8. Signalling of the DiSEqC-ST command



3.2.2 Look up tables

Table 9. Feeds(1)

Feed	RF input		
	Band	Polarization	Satellite
0	Low	Vertical	A
1	High	Vertical	A
2	Low	Horizontal	A
3	High	Horizontal	A
4	Low	Vertical	B
5	High	Vertical	B
6	Low	Horizontal	B
7	High	Horizontal	B

1. Applications supporting legacy are limited to one satellite only (satellite A).

Table 10. Local oscillator frequencies

LofreqNum (hex)		Local oscillator frequency
Standard RF band	00	none
	01	Not Known
	02	9.750 GHz
	03	10.000 GHz
	04	10.600 GHz
	05	10.750 GHz
	06	11.000 GHz
	07	11.250 GHz
	08	11.475 GHz
	09	20.250 GHz
	0A	5.150 GHz
	0B	1.585 GHz
	0C	13.850 GHz
	0D	not allocated
	0E	not allocated
	0F	not allocated

Table 10. Local oscillator frequencies (continued)

LofreqNum (hex)		Local oscillator frequency
Wide RF band	10	none (switcher)
	11	10.000 GHz
	12	10.200 GHz
	13	13.250 GHz
	14	13.450 GHz
	15 to 1F	not allocated

Table 11. ST7LNB1Y0 applications

Application number (AppliNum)	Application
01	Single SatCR and legacy (standard RF band)
02	Twin SatCR (standard RF band)
03	Twin SatCR and legacy (standard RF band)
04	Quad SatCR (standard RF band)
05	Double Twin SatCR (standard RF band)
06	Twin SatCR (wide RF band)
07	Twin SatCR and legacy (wide RF band)
08	Quad SatCR (wide RF band)
09	8 SatCR (standard RF band)
0Ah	6 SatCR (standard RF band)
0Bh	Quad SatCR and legacy (standard RF band)
0Ch to FFh	TBD(1)

1. TBD stands for to be defined.

3.3 DiSEqC 1.0 command for legacy support

The DiSEqC 1.0 commands for the control of the legacy are the following:

- **00h**: this command is used to restore the backwards compatibility.
- **38h**: this command is used to write to port group command.

For application supporting the legacy (except for application 1), the backwards signalling (13/18 V, 22 kHz tone) is recognized until a valid DiSEqC 1.0 command is detected.

The following table presents the truth table for the legacy commands:

Table 12. Legacy commands

Command 38h	Equivalent backwards signalling	Selected feed	Band	Polarity	Satellite
E0 xx 38 F0	13v / 0 kHz	0	Low	Vertical	A
E0 xx 38 F1	13v / 22 kHz	1	High	Vertical	A
E0 xx 38 F2	18v / 0 kHz	2	Low	Horizontal	A
E0 xx 38 F3	18v / 22 kHz	3	High	Horizontal	A

4 ST7LNB1Y0 configuration

To configure the ST7LNB1Y0 for the required target application, a dedicated DiSEqC command is implemented. This configuration is stored in the ST7LNB1Y0 embedded EEPROM location.

4.1 Command 0Fh

ST7LNB1Y0 devices are shipped to customers with a default parameter value. These parameters can be updated using a dedicated 0Fh DiSEqC command.

This command has the following format where “data” is the parameter value to be programmed at the “index” location as shown in *Table 16*.

Note: The special command E0 xx 0F FF FF protects the EEPROM data from any subsequent write access (where xx is the corresponding DiSEqC slave address).

Table 13. Command 0Fh format

E0h	DiSEqC slave address	0Fh	index	data

4.2 Command 0Dh

For reading a parameter inside the EEPROM a dedicated 0Dh command has been added.

The command format is described in *Table 14*, where “index” is the address of the byte to be read from EEPROM.

Table 14. Command 0Dh format

E2h(1)	DiSEqC slave address	0Dh(2)	index

1. E2h framing (and E4h response) is supported from version 1.1 of the LNB1 software (previously, the command 0Dh was implemented with E0h framing and the data response was without E4h framing).
2. After the Command 0Dh, there is a delay of 10ms before getting the reply frame.

The format of the reply frame is given in *Table 15*, format where “data” is the byte read from EEPROM.

Table 15. Reply frame format

E4h	data

Timings

The time required to update a byte parameter (write and read operation) is 130 ms, while the time required to update all parameters is about 3.5 s.

Table 16. ST7LNB1Y0 EEPROM parameters

Index	Parameter	Description	Default value
00	Slave Address	DiSEqC slave address(1)	11h
01	$SaTCR_1$ BPF (lsb)	(2)	5Dh
02	$SaTCR_1$ BPF (msb)		02h
03	$SaTCR_2$ BPF (lsb)		C6h
04	$SaTCR_2$BPF (msb)		02h
05	$SaTCR_3$ BPF (lsb)		48h
06	$SaTCR_3$ BPF (msb)		03h
07	$SaTCR_4$ BPF (lsb)		FCh
08	$SaTCR_4$ BPF (msb)		03h
09	$SaTCR_5$ BPF (lsb)		FFh
0A	$SaTCR_5$BPF (msb)		FFh
0B	$SaTCR_6$ BPF (lsb)		FFh
0C	$SaTCR_6$ BPF (msb)		FFh
0D	$SaTCR_7$ BPF(lsb) / legacy SaTCR Low band (msb)	(3)	FFh
0E	$SaTCR_7$ BPF(msb) / legacy SaTCR Low band (lsb)		FFh
0F	$SaTCR_8$ BPF(lsb) / legacy SaTCR High band (msb)		FFh
10	$SaTCR_8$ BPF(msb) / legacy SaTCR High band (lsb)		FFh
11	Applitype	Application type number (refer to *Table 4*)	00h
12	AppliNum	Application number (refer to *Table 11*)	04h
13	High L.O freq Number	refer to *Table 10*	04h
14	Low L.O freq Number	refer to *Table 10*	02h

Table 16. ST7LNB1Y0 EEPROM parameters (continued)

Index	Parameter	Description	Default value
15	$SaTCR_1$ matrix truth table	(4)	ACh
16			35h
17	$SaTCR_2$ matrix truth table		59h
18			6Ah
19	$SaTCR_3$ matrix truth table		56h
1A			9Ah
1B	$SaTCR_4$ matrix truth table		95h
1C			A6h
1D	$SaTCR_5$ matrix truth table		FFh
1E			FFh
1F	$SaTCR_6$ matrix truth table		FFh
20			FFh
21	$SaTCR_7$ matrix truth table		FFh
22			FFh
23	$SaTCR_8$ matrix truth table / legacy matrix		FFh
24			FFh
25	SaTCRs GAIN(5)	SaTCRs 1 to 4 Gain	FFh
26		SaTCRs 5 to 8 Gain	FFh
27	SaTCRs number	(6)	04h
28	Tuning step size (unit= 1MHz)		04h
29	Software Version Number		14h
2A / 2B	RESERVED(7)		

1. Besides the address defined in the EEPROM at index 00h, addresses 10h and 00h are recognized also as valid addresses.
2. $SaTCR_X$ BPF = BPF_X center frequency (MHz) / 2.
3. When an application supports the wide RF band only one local oscillator with a frequency F_{LO} is present in the LNB. In this case the selection of the high or the low band for the legacy output is performed by a dedicated SaTCR.
   Two parameters are needed for the band selection:
   - The tuning word for the low band selection = $[(F_{LO\ (MHz)} - F_{Low\ (MHz)})/ 4] - 350$: where F_{Low} corresponds to the Low LO frequency.
   - The tuning word for the high band selection = $[(F_{LO\ (MHz)} - F_{High\ (MHz)})/4] - 350$: where F_{High} corresponds to the High band LO frequency.
   Example: in a wide band application with F_{LO}= 13250 MHz, for emulating a low band local oscillator at 9750 MHz, index 0Dh and index 0Eh must be loaded with the decimal value D = dec [0D:0E] = round ((13250-9750)/4) - 350 = 525.
4. Matrix truth table for SaTCRx or legacy:
   - If 4 RF inputs are implemented then the matrix truth table has the following coding on 2 bytes: “aaaabbbb ccccdddd” where:
   aaaa= selection of Feed1 on SaTCRx, aaaa = [MAT4, MAT3, MAT2, MAT1]
   bbbb= selection of Feed0 on SaTCRx, bbbb = [MAT4, MAT3, MAT2, MAT1]
   cccc = selection of Feed3 on SaTCRx, cccc = [MAT4, MAT3, MAT2, MAT1]
   dddd= selection of Feed2 on SaTCRx,dddd = [MAT4, MAT3, MAT2, MAT1]
   - If 8RF inputs are implemented then the truth table given in *Table 17* is used.

5. In order to enable the support of 8 RF inputs: the value ‘0000h’ has to be programmed in index 15h and 16h. SaTCRs gain value: it has the following format on two bytes: “AaBbCcDd EeFfGgHh” where Aa= gain for $SaTCR_1$, Bb = gain for $SaTCR_2$, Cc= gain for $SaTCR_3$, Dd=gain for $SaTCR_4$, Ee= gain for $SaTCR_5$, Ff= gain for $SaTCR_6$, Gg= gain for $SaTCR_7$, Hh=gain for $SaTCR_8$ or legacy SaTCR. Upper case letters and upper case letters indicate LNA and IF gain, respectively.
6. SaTCRs number does not include the legacy SaTCR for the wide RF band applications.
7. RESERVED bytes: do not write to this location.

Table 17. Truth table for support of 8 RF inputs

Feed	MAT1	MAT2	MAT3	MAT4
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 5 V for the 4.5 V ≤ V_{DD} ≤ 5.5 V voltage range. They are given only as design guidelines and are not tested.

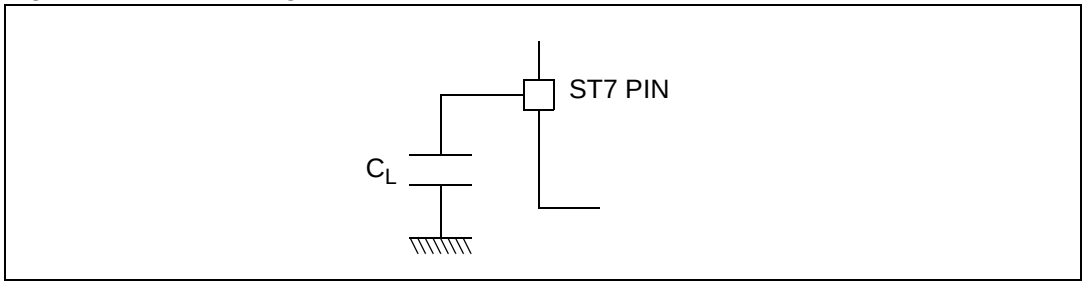
5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

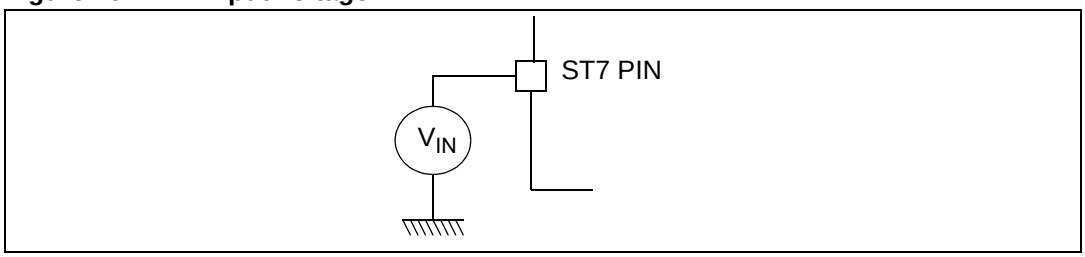
Figure 9. Pin loading conditions



5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 10. Pin input voltage



5.2 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 18. Voltage characteristics

Symbol	Ratings	Maximum value	Unit
V_{DD} - V_{SS}	Supply voltage	7.0	V
V_{IN}	Input voltage on any pin(1)(2)	V_{SS}–0.3 to V_{DD}+0.3	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	see *Section 5.5.3: Absolute maximum ratings (electrical sensitivity)*	

1. Directly connecting the I/O pins to V_{DD} or V_{SS} could damage the device if an unexpected change of the I/O configuration occurs (for example, due to a corrupted program counter). To guarantee safe operation, this connection has to be done through a pull-up or pull-down resistor (typical: 10kΩ for I/Os). Unused I/O pins must be tied in the same way to V_{DD} or V_{SS} according to their reset configuration.
2. When the current limitation is not possible, the V_{IN} absolute maximum rating must be respected, otherwise refer to $I_{INJ(PIN)}$ specification. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.

Table 19. Current characteristics

Symbol	Ratings	Maximum value	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(1)	100	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	100	
I_{IO}	Output current sunk by any standard I/O and control pin	25	
	Output current sunk by any high sink I/O pin	50	
	Output current source by any I/Os and control pin	– 25	
$I_{INJ(PIN)}$(2)(3)	Injected current on $\overline{\text{RESET}}$ pin	± 5	
	Injected current on any other pin(4)(5)	± 5	
$\Sigma I_{INJ(PIN)}$(2)	Total injected current (sum of all I/O and control pins)(4)	± 20	

1. All power (V_{DD}) and ground (V_{SS}) lines must always be connected to the external supply.
2. When the current limitation is not possible, the V_{IN} absolute maximum rating must be respected, otherwise refer to $I_{INJ(PIN)}$ specification. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.
3. Negative injection disturbs the analog performance of the device. In particular, it induces leakage currents throughout the device including the analog inputs. To avoid undesirable effects on the analog functions, care must be taken:
   - Analog input pins must have a negative injection less than 0.8 mA (assuming that the impedance of the analog voltage is lower than the specified limits)
   - Pure digital pins must have a negative injection less than 1.6 mA. In addition, it is recommended to inject the current as far as possible from the analog input pins.
4. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.
5. True open drain I/O port pins do not accept positive injection.

Table 20. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature (see *Section 6.2: Thermal characteristics*)		

5.3 Operating conditions

Table 21. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply voltage		4.5	5.5	V
T_A	Ambient temperature		–40	+85	°C

Table 22. Operating Conditions with Low Voltage Detector (LVD)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IT+(LVD)}$	Reset release threshold (V_{DD} rise)		4.00	4.25	4.50	V
$V_{IT-(LVD)}$	Reset generation threshold (V_{DD} fall)		3.80	4.10	4.30	
V_{hys}	LVD voltage threshold hysteresis	$V_{IT+(LVD)}-V_{IT-(LVD)}$		200		mV
Vt_{POR}	V_{DD} rise time rate(1)		20		20000	µs/V
$t_{g(VDD)}$	Filtered glitch delay on V_{DD}	Not detected by the LVD			150	ns
$I_{DD(LVD)}$	LVD/AVD current consumption			200		µA

1. Not tested in production. The V_{DD} rise time rate condition is needed to ensure a correct device power-on and LVD reset. When the V_{DD} slope is outside these values, the LVD may not ensure a proper reset of the MCU.

Table 23. Operating conditions with the DiSEqC™ signalling

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{DiSEqC}	DiSEqC tone frequency		17.6	22	26.4	kHz
V_{DiSEqC}	DiSEqC tone voltage		100(1)	650		mV_{PP}
$V_{Backward}$	13/18 volt backward compatibility voltage threshold(2)			15		V

1. The MCU is able to detect a DiSEqC signal with an amplitude from 100mV. However it is advised to ensure a DiSEqC amplitude of at least 150 to 200mV to improve robustness against noise.
2. In backwards compatible mode, bus DC voltage is compared with 15 V, if it exceeds this voltage then it is considered as 18 V, otherwise it is considered as 13 V.

5.4 Supply current characteristics

The following current consumption specified for the ST7 functional operating modes over temperature range does not take into account the clock source current consumption. To get the total device consumption, the two current values must be added.

5.4.1 Supply current

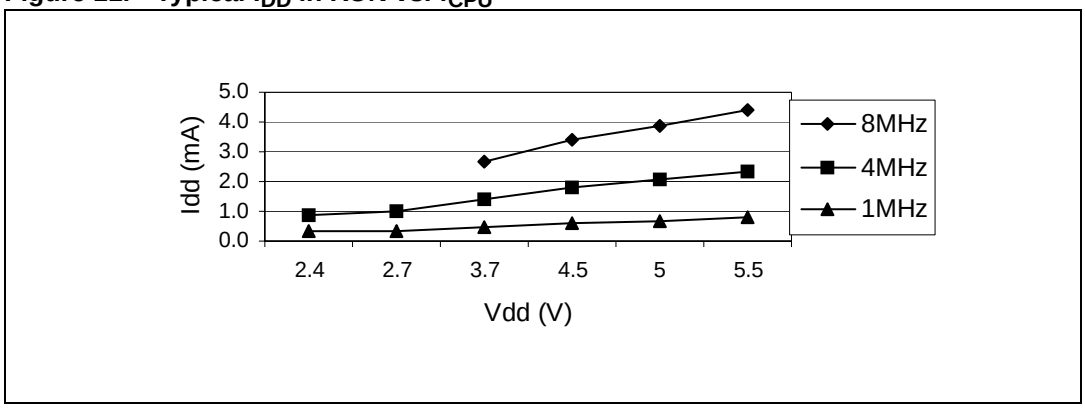
T_A = –0 to +125 °C unless otherwise specified

Table 24. Supply current characteristics

Symbol	Parameter	Conditions	Typ	Max	Unit
I_{DD}	Supply current in RUN mode(1)	V_{DD} = 5.5 V, f_{CPU}=8 MHz	4.50	7	mA
	Supply current for LNB or switcher applications(2)			20	

1. 1. CPU running with memory access, all I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load), all peripherals in reset state; clock input (CLKIN) driven by external square wave, LVD disabled.
2. 2. Data based on typical ST7LNB0 LNB or switcher application software running.

Figure 11. Typical I_{DD} in RUN vs. f_{CPU}



5.5 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

5.5.1 Functional EMS (electromagnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic Discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

- Software recommendations

  The software flowchart must include the management of runaway conditions such as:

  – Corrupted program counter
  – Unexpected reset
  – Critical Data corruption (control registers...)

- Prequalification trials

  Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the RESET pin or the Oscillator pins for 1 second.

  To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 25. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD}=5 V, T_A=+25 °C, f_{OSC}=8 MHz conforms to IEC 1000-4-2	2B
V_{FFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{DD} pins to induce a functional disturbance	V_{DD}=5 V, T_A=+25 °C, f_{OSC}=8 MHz conforms to IEC 1000-4-4	3B

5.5.2 Electromagnetic Interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 26. EMI characteristics(1)

Symbol	Parameter	Conditions	Monitored Frequency Band	Max vs. [f_{OSC}/f_{CPU}]		Unit
				1/4 MHz	1/8 MHz	
S_{EMI}	Peak level	V_{DD}=5V, T_A=+25°C, SO16 package, conforming to SAE J 1752/3	0.1 MHz to 30 MHz	8	14	dBµV
			30 MHz to 130 MHz	27	32	
			130 MHz to 1 GHz	26	28	
			SAE EMI Level	3.5	4	-

1. Data based on characterization results, not tested in production.

5.5.3 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU and DLU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic Discharge (ESD)

Electrostatic Discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the JESD22-A114A/A115A standard.

Table 27. Absolute maximum ratings(1)

Symbol	Ratings	Conditions	Maximum value 1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	T_A=+25 °C	4000	V

1. Data based on characterization results, not tested in production.

Static and Dynamic latch-up

- **LU**: 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.
- **DLU**: Electrostatic discharges (one positive then one negative test) are applied to each pin of 3 samples when the micro is running to assess the latch-up performance in dynamic mode. Power supplies are set to the typical values, the oscillator is connected as near as possible to the pins of the micro and the component is put in reset mode. This test conforms to the IEC1000-4-2 and SAEJ1752/3 standards. For more details, refer to the application note AN1181.

Table 28. Electrical sensitivities(1)

Symbol	Parameter	Conditions	Class 1)
LU	Static latch-up class	T_A=+25°C	A
DLU	Dynamic latch-up class	V_{DD}=5.5 V, f_{OSC}=4 MHz, T_A=+25 °C	A

1. 1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to Class A it exceeds the JEDEC standard. B Class strictly covers all the JEDEC criteria (international standard).

5.6 I/O port pin characteristics

5.6.1 General characteristics

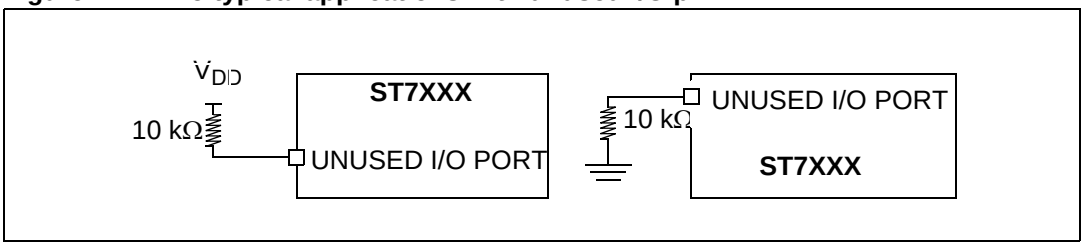
Subject to general operating conditions for V_{DD}, f_{OSC}, and T_A unless otherwise specified.

Table 29. General characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage				$0.3V_{DD}$	V
V_{IH}	Input high level voltage		$0.7V_{DD}$			
V_{hys}	Schmitt trigger voltage hysteresis(1)			400		mV
I_L	Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$			±1	µA
I_S	Static current consumption(2)	Floating input mode			200	
R_{PU}	Weak pull-up equivalent resistor(3)	$V_{IN}=V_{SS}$, $V_{DD}=5$ V	50	120	250	kΩ
C_{IO}	I/O pin capacitance			5		pF
$t_{f(IO)out}$	Output high to low level fall time(1)	C_L=50 pF Between 10% and 90%		25		ns
$t_{r(IO)out}$	Output low to high level rise time(1)			25		

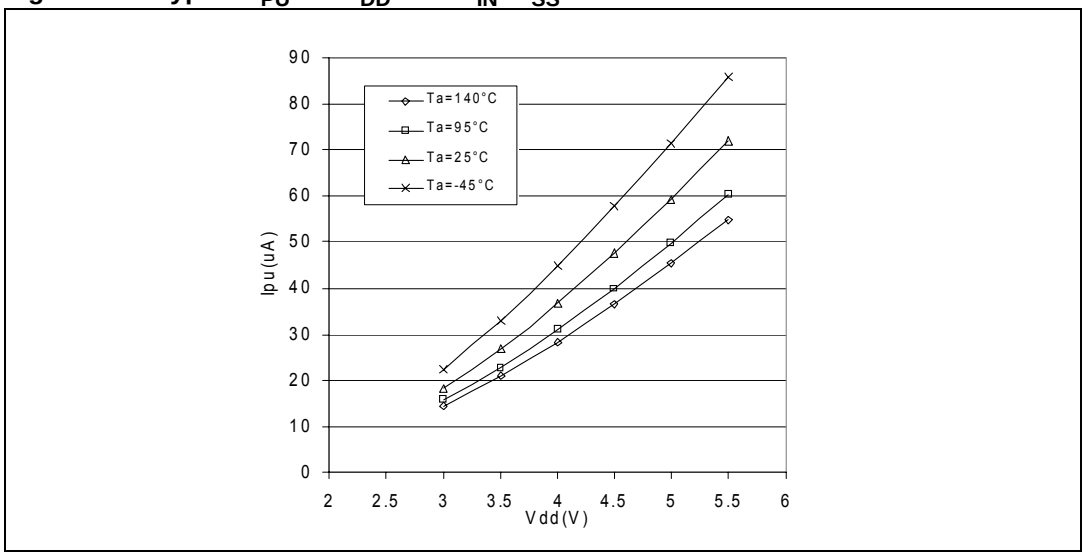
1. Data based on characterization results, not tested in production.
2. Configuration not recommended, all unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor (see *Figure 12*). Data based on design simulation and/or technology characteristics, not tested in production.
3. The R_{PU} pull-up equivalent resistor is based on a resistive transistor (corresponding I_{PU} current characteristics described in *Figure 13*).

Figure 12. Two typical applications with unused I/O pin



1. Only external pull-up allowed on ICCCLK pin.

Figure 13. Typical I_{PU} vs. V_{DD} with $V_{IN}=V_{SS}$



5.6.2 Output driving current

Subject to general operating conditions for V_{DD}, f_{CPU}, and T_A unless otherwise specified.

Table 30. Output driving current characteristics

Symbol	Parameter	Conditions		Min	Max	Unit
V_{OL}(1)	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time (see *Figure 14*)	V_{DD}=5V	I_{IO}=+5 mA		1.0	V
			I_{IO}=+2 mA		0.4	
	Output low level voltage for a high sink I/O pin when 4 pins are sunk at same time (see *Figure 15*)		I_{IO}=+20 mA		1.3	
			I_{IO}=+8 mA		0.75	
V_{OH}(2)	Output high level voltage for an I/O pin when 4 pins are sourced at same time (see *Figure 16*)		I_{IO}=-5 mA	V_{DD}–1.5		
			I_{IO}=-2 mA	V_{DD}–0.8		

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 19* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Table 19* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}. True open drain I/O pins does not have V_{OH}.

Figure 14. Typical V_{OL} at V_{DD}=5 V (standard)

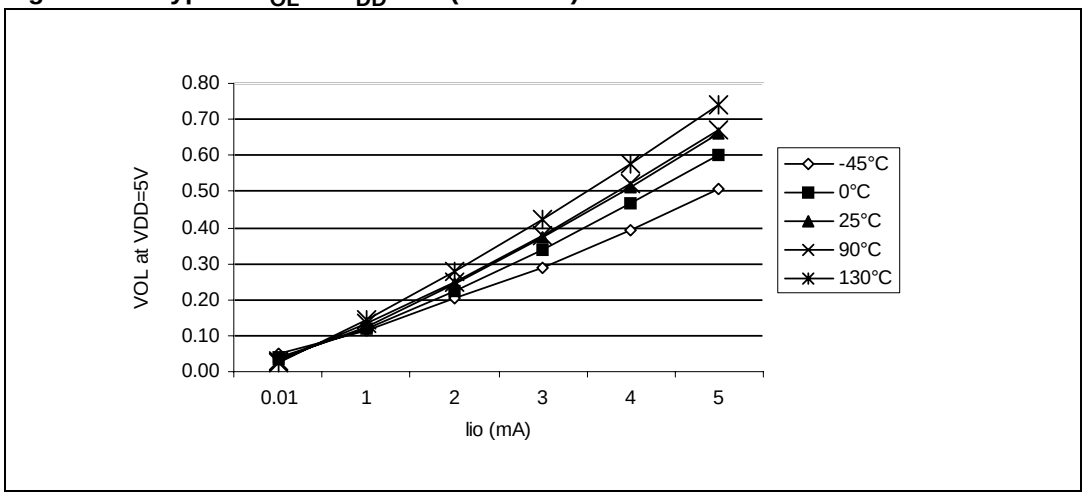


Figure 15. Typical V_{OL} at V_{DD}=5V (high sink)

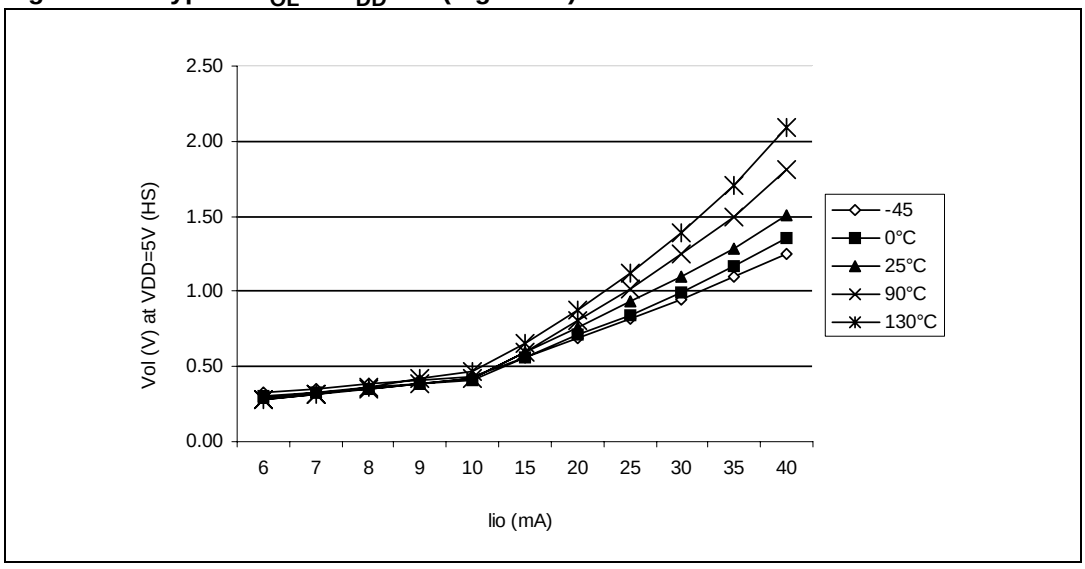
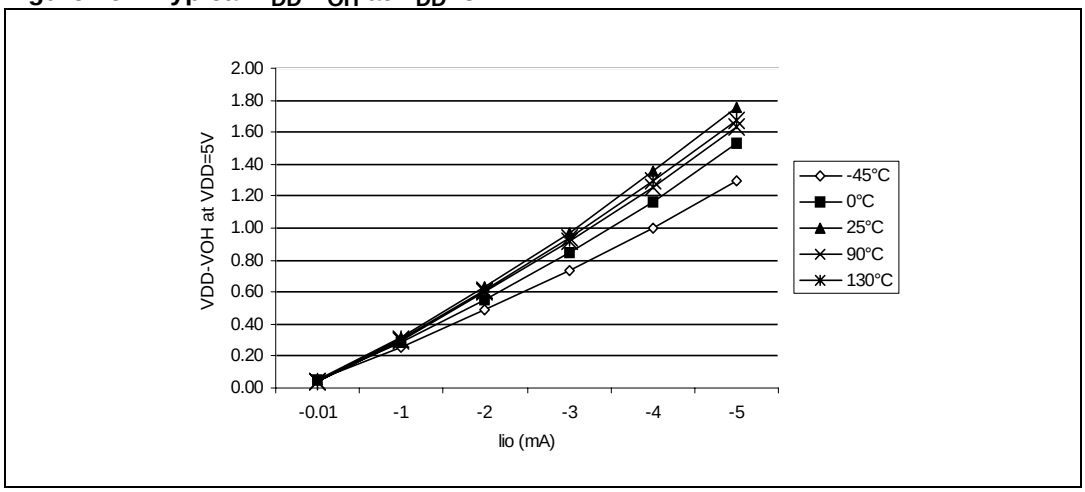


Figure 16. Typical V_{DD}-V_{OH} at V_{DD}=5 V



5.7 Control pin characteristics

5.7.1 Asynchronous $\overline{\text{RESET}}$ pin

Table 31. Asynchronous $\overline{\text{RESET}}$ pin characteristics(1)(2)(3)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}	Input low level voltage					$0.3V_{DD}$	V
V_{IH}	Input high level voltage			$0.7V_{DD}$			
V_{hys}	Schmitt trigger voltage hysteresis(4)				1		V
V_{OL}	Output low level voltage(5)	V_{DD}=5 V	I_{IO}=+5mA		0.5	1.0	V
			I_{IO}=+2mA		0.2	0.4	
R_{ON}	Pull-up equivalent resistor(4)(6)	V_{DD}=5V		20	40	80	kΩ
$t_{w(RSTL)out}$	Generated reset pulse duration	Internal reset sources			30		µs
$t_{h(RSTL)in}$	External reset pulse hold time(7)			20			µs
$t_{g(RSTL)in}$	Filtered glitch duration(8)				200		ns

1. The output of the external reset circuit must have an open-drain output to drive the ST7 reset pad. Otherwise the device can be damaged when the ST7 generates an internal reset (LVD or watchdog).
2. Whatever the reset source is (internal or external), the user must ensure that the level on the $\overline{\text{RESET}}$ pin can go below the V_{IL} max. level specified in *Section 5.7.1 on page 31*. Otherwise the reset will not be taken into account internally.
3. Because the reset circuit is designed to allow the internal RESET to be output in the $\overline{\text{RESET}}$ pin, the user must ensure that the current sunk on the $\overline{\text{RESET}}$ pin (by an external pull-up for example) is less than the absolute maximum value specified for $I_{INJ(RESET)}$ in *Section Table 19. on page 22*.
4. Data based on characterization results, not tested in production.
5. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Table 19* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
6. The R_{ON} pull-up equivalent resistor is based on a resistive transistor. Specified for voltage on $\overline{\text{RESET}}$ pin between V_{ILmax} and V_{DD}.
7. To guarantee the reset of the device, a minimum pulse has to be applied to the $\overline{\text{RESET}}$ pin. All short pulses applied on $\overline{\text{RESET}}$ pin with a duration below $t_{h(RSTL)in}$ can be ignored.
8. The reset network protects the device against parasitic resets.

6 Package characteristics

6.1 Package mechanical data

Figure 17. SO16 16-pin plastic small outline -150mil width, package outline

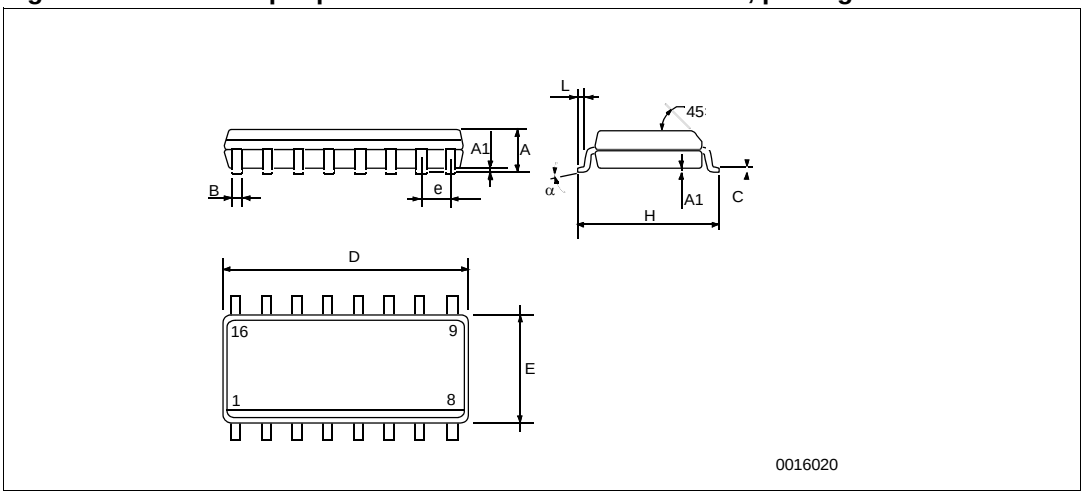


Table 32. SO16 16-pin plastic small outline-150mil width, package mechanical data

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	9.80		10.00	0.386		0.394
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
α	0°		8°	0°		8°
L	0.40		1.27	0.016		0.050
	Number of Pins					
N	16					

6.2 Thermal characteristics

Table 33. Thermal characteristics

Symbol	Ratings		Value	Unit
R_{thJA}	Package thermal resistance (junction to ambient)	SO16	85	°C/W
T_{Jmax}	Maximum junction temperature(1)		150	°C
P_{Dmax}	Power dissipation(2)	SO16	300	mW

1. The maximum chip-junction temperature is based on technology characteristics.
2. The maximum power dissipation is obtained from the formula $P_D = (T_J - T_A) / R_{thJA}$.
The power dissipation of an application can be defined by the user with the formula: $P_D=P_{INT}+P_{PORT}$ where P_{INT} is the chip internal power ($I_{DD}xV_{DD}$) and P_{PORT} is the port power dissipation depending on the ports used in the application.

6.3 Soldering information

In order to meet environmental requirements, ST offers the ST7LNB1Y0 in ECOPACK® package. The package have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at *www.st.com*, together with specific technical application notes covering the main technical aspects related to lead-free conversion (AN2033, AN2034, AN2035, AN2036).

Backward and forward compatibility

The main difference between Pb and Pb-free soldering process is the temperature range.

- ECOPACK LQFP, SDIP, SO and QFN20 packages are fully compatible with Lead (Pb) containing soldering process (see application note AN2034)
- TQFP, SDIP and SO Pb-packages are compatible with Lead-free soldering process, nevertheless it's the customer's duty to verify that the Pb-packages maximum temperature (mentioned on the Inner box label) is compatible with their Lead-free soldering temperature.

Table 34. Soldering compatibility (wave and reflow soldering process)

Package	Plating material devices	Pb solder paste	Pb-free solder paste
SDIP & PDIP	Sn (pure Tin)	Yes	Yes (1)
QFN	Sn (pure Tin)	Yes	Yes(1)
LQFP and SO	NiPdAu (Nickel-palladium-Gold)	Yes	Yes(1)

1. Assemblers must verify that the Pb-package maximum temperature (mentioned on the Inner box label) is compatible with their Lead-free soldering process.

ST7LNB1Y0 DiSEqC™ SLAVE MICROCONTROLLER OPTION LIST
(Last update: July 2007)

Customer . . . . . .
Address . . . . . .
. . . . . .
Contact . . . . . .
Phone No . . . . . .

- Package (tick one box)

ST7LNB1Y0M6 - SO16 narrow (16 pin) [ ]

- EEPROM Parameters (any modified default settings [DEF] should be written in the Custom boxes [CUST])

INDEX	PARAMETER	DEF	CUST	INDEX	PARAMETER	DEF	CUST
00	Slave Address	11h	[h]	**11**	Applitype	00h	[h]
01	SaTCR1 BPF (lsb)	5Dh	[h]	**12**	AppliNum	04h	[h]
02	SaTCR1 BPF (msb)	02h	[h]	**13**	High L.O freq Number	04h	[h]
03	SaTCR2 BPF (lsb)	C6h	[h]	**14**	Low L.O freq Number	02h	[h]
04	SaTCR2BPF (msb)	02h	[h]	**15**	SaTCR1 matrix truth table	ACh	[h]
				16		35h	[h]
05	SaTCR3 BPF (lsb)	48h	[h]	**17**	SaTCR2 matrix truth table	59h	[h]
06	SaTCR3 BPF (msb)	03h	[h]	**18**		6Ah	[h]
07	SaTCR4 BPF (lsb)	FCh	[h]	**19**	SaTCR3 matrix truth table	56h	[h]
				1A		9Ah	[h]
08	SaTCR4 BPF (msb)	03h	[h]	**1B**	SaTCR4 matrix truth table	95h	[h]
09	SaTCR5 BPF (lsb)	FFh	[h]	**1C**		A6h	[h]
0A	SaTCR5BPF (msb)	FFh	[h]	**1D**	SaTCR5 matrix truth table	FFh	[h]
				1E		FFh	[h]
0B	SaTCR6 BPF (lsb)	FFh	[h]	**1F**	SaTCR6 matrix truth table	FFh	[h]
0C	SaTCR6 BPF (msb)	FFh	[h]	**20**		FFh	[h]
0D	SaTCR7 BPF(lsb)/Legacy			**21**	SaTCR7 matrix truth table	FFh	[h]
	SaTCR Low band(msb)	FFh	[h]	**22**		FFh	[h]
0E	SaTCR7 BPF(msb)/Legacy			**23**	SaTCR8 matrix truth table/	FFh	[h]
	SaTCR Low band (lsb)	FFh	[h]	**24**	Legacy matrix	FFh	[h]
0F	SaTCR8 BPF(lsb)/Legacy			**25**	SaTCRs GAIN	FFh	[h]
	SaTCR High band (msb)	FFh	[h]	**26**		FFh	[h]
10	SaTCR8 BPF(msb)/Legacy			**27**	SaTCRs number	04h	[h]
	SaTCR High band (lsb)	FFh	[h]				

(Please refer to *Table 16* in the datasheet for full descriptions and notes of EEPROM Parameters)

Customer . . . . . .
. . . . . .
Notes . . . . . .
. . . . . .
Signature . . . . . .
Date . . . . . .

Please download the latest version of this option list from:
http://www.st.com/mcu > downloads > ST7 microcontrollers > Option list

7 Revision history

Table 35. Document revision history

Date	Revision	Description of Changes
29-Sep-2004	2.0	First release on st.com
10-Nov-2004	3.0	Note added, *Section 4.1: Command 0Fh* E2h and E4h framing added for Command 0Dh, *Section 4.2: Command 0Dh*
06-Dec-2004	4.0	Changed note 6 and *Figure 3* Removed note on page 9. Changed *Table 16: ST7LNB1Y0 EEPROM parameters*
28-Jun-2005	5.0	Changed note 4 in *Section 1: Pin description* Changed note 5 in *Figure 3* Added note 1 to *Section 3.2: DiSEqC-ST commands* Changed timing in *Figure 8: Signalling of the DiSEqC-ST command* Changed *Table 11: ST7LNB1Y0 applications* (added application for 0A and 0B) Added frequencies in wide band part in *Table 10: Local oscillator frequencies* Changed parameters in *Table 16: ST7LNB1Y0 EEPROM parameters*
12-Oct-2005	6.0	Changed package name to SO16 NARROW
31-Jan-2006	7.0	Modified notes for *Table 23: Operating conditions with the DiSEqC™ signalling* related to DiSEqC signal detection levels Capacitors changed from 100pF to 180pF in *Figure 3: ST7LNB1Y0 in the Twin SaTCR and legacy (standard RF band) application*
19-July-2007	8.0	Document reformatted. QFN20 package removed Root part number changed from ST7LBN1 to ST7LNB1Y0. Note 1 removed below *Table 30: Output driving current characteristics*. Additional figure added for single-input application of Twin SaTCR application, *Figure 4: ST7LNB1Y0 in the Twin SaTCR application with one input only*. Thermal characteristics (*Section 6.2*) and Soldering information (*Section 6.3*) updated Option list updated and reformatted. ECOPACK package description updated in *Section 6.3: Soldering information*.

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