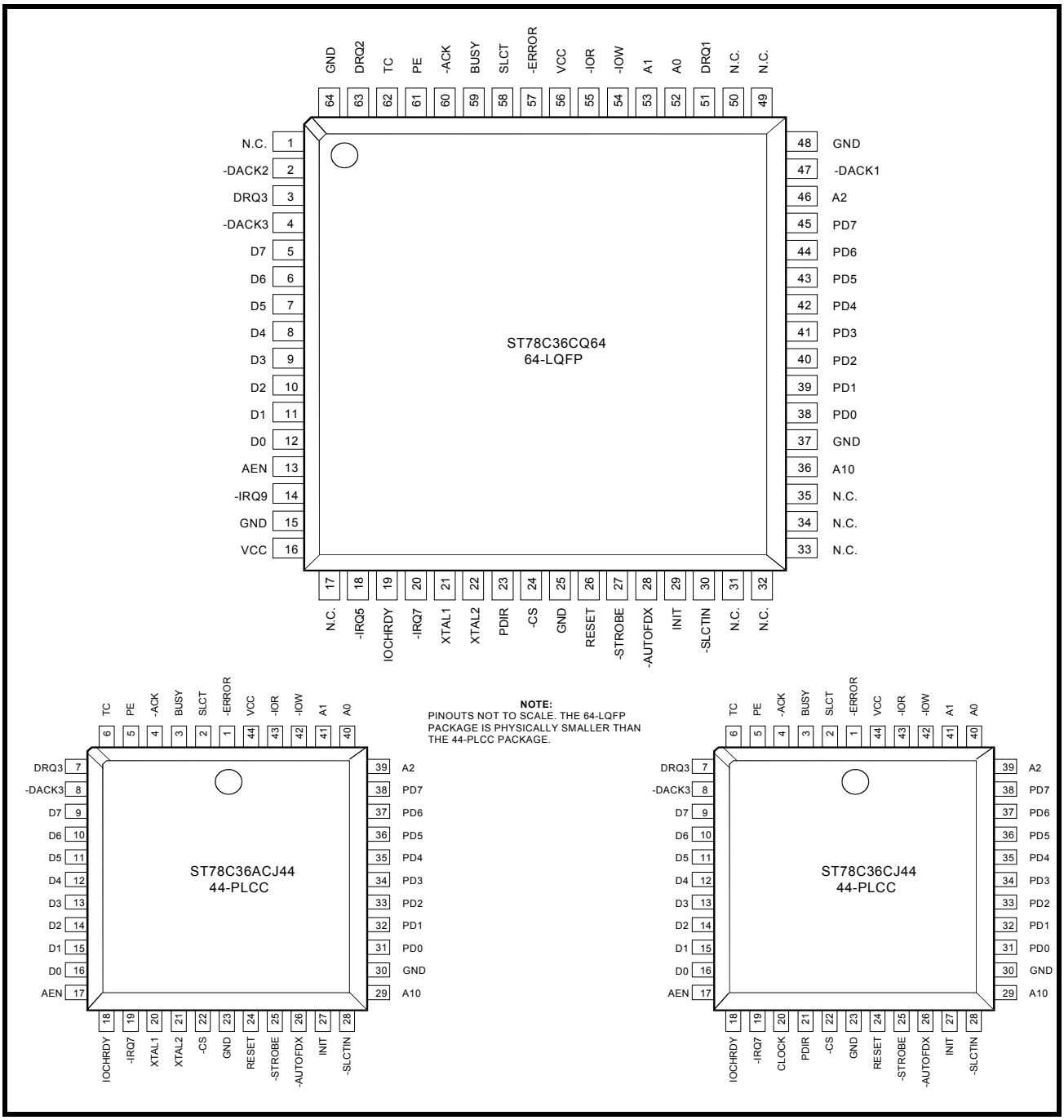
FIGURE 2. ST78C36/36A PIN OUT ASSIGNMENTS



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE	DEVICE STATUS
ST78C36CJ44	44-PLCC	0°C to 70°C	Active
ST78C36ACJ44	44-PLCC	0°C to 70°C	Active
ST78C36CQ64	64-LQFP	0°C to 70°C	EOL

PIN DESCRIPTION

NAME	44-PLCC PIN #	64-LQFP PIN#	TYPE	DESCRIPTION
DATA BUS INTERFACE				
A10 A2 A1 A0	29 39 41 40	36 46 53 52	I	Address Select Lines. A10 places the ECP control/status/data ports at 0x400 offset from the -CS decoded address.
D7 D6 D5 D4 D3 D2 D1 D0	9 10 11 12 13 14 15 16	5 6 7 8 9 10 11 12	I/O	Data bus. Bi-directional data port.
-IOR	43	55	I	Active low AT bus I/O Read strobe.
-IOW	42	54	I	
-CS	22	24	I	Chip select (active LOW). A LOW at this pin enables the parallel port / CPU data transfer operation.
IOCHRDY	18	19	O	I/O Channel ready (internal pull-up / three stated active HIGH). This pin goes low when the device requires addition clock cycles for read and write.
-IRQ9 -IRQ7 -IRQ5	- 19 -	14 20 18	O	Interrupt Request Lines (three stated active low).
AEN	17	13	I	DMA address enable (active HIGH). When this line is HIGH, the DMA controller has control of the address bus.
DRQ3 DRQ2 DRQ1	7 - -	3 63 51	O	Active high AT bus DMA ReQuest for channels 3, 2 and 1 (internal pull-down three stated active HIGH). A request is generated by bringing a DRQx line to a HIGH level. A DRQx line is held HIGH until the corresponding DMA acknowledge “DACKx*” line goes LOW.
-DACK3 -DACK2 -DACK1	8 - -	4 2 47	I	DMA Acknowledge signals for channels 3, 2 and 1 (internal pull-up /three stated active low).
TC	6	62	I	Terminal Count (active HIGH). The ST78C36 terminates the DMA channel when a HIGH pulse is detected.

PIN DESCRIPTION

NAME	44-PLCC PIN #	64-LQFP PIN#	TYPE	DESCRIPTION
PRINTER PORT INTERFACE				
PD7 PD6 PD5 PD4 PD3 PD2 PD1 PD0	38 37 36 35 34 33 32 31	45 44 43 42 41 40 39 38	I/O	Bi-directional parallel port (three-state) to transfer data in or out of the ST78C36 parallel port. PD[7:0] are latched during output mode. Output only for SPP and PPF modes, bi-directional for all other modes.
-STROBE	25	27	O	Data strobe output (internal pull-up / three stated active low). This output indicates to the printer that valid data is available at the printer port (PD0-PD7).
-AUTOFDX	26	28	O	Automatic line feed (internal pull-up / three stated active low). When this signal is low the printer should automatically line feed after each line is printed.
INIT	27	29	O	Initialize line printer (internal pull-up / three stated active low). When this signal is low, it causes the printer to be initialized.
-SLCTIN	28	30	O	Line printer select (internal pull-up / three stated active low). When this signal is low, it selects the printer.
-ERROR	1	57	I	Line printer error (internal pull-up / active low). This is an output from the printer to indicate an error by holding it low during error condition.
SLCT	2	58	I	Line printer selected (internal pull-up / active high). This is an output from the printer to indicate that the line printer has been selected.
BUSY	3	59	I	Line printer busy (internal pull-up / active high). An output from the printer to indicate printer is not ready to accept data.
-ACK	4	60	I	Line printer acknowledge (internal pull-up / active low). This input is pulsed low by the printer to indicate that data has been accepted successfully.
PE	5	61	I	Line printer paper empty (internal pull-up / active high). An output from the printer to indicate out of paper.
PDIR	21	23	O	Printer port direction indicator. HIGH indicates device is in input mode, LOW indicates output mode. (ST78C36CJ44 and ST78C36CQ64 only).
SYSTEM SIGNALS				
CLOCK/ XTAL1	20	21	I	Crystal oscillator input (ST78C36ACJ44, ST78C36CQ64) or External clock input (ST78C36CJ44), nominal 24 MHz.
XTAL2	21	22	O	Crystal oscillator output, nominal 24 MHz. ST78C36ACJ44 and ST78C36CQ64 only.
RESET	24	26	I	System RESET (active HIGH).

PIN DESCRIPTION

NAME	44-PLCC PIN #	64-LQFP PIN#	TYPE	DESCRIPTION
VCC	44	16, 56	Pwr	Power Supply (+5V).
GND	23,30	15, 25, 37, 48, 64	Pwr	Supply Ground.

1.0 OVERVIEW

This device is designed around the Hewlett Packard/Microsoft specification for Extended Capabilities Port Protocol with “ECR mode 100” defined as Enhanced Parallel Port (EPP) mode. The internal timing engines were designed around a 24 MHz reference, which can be supplied from an external source or by the built-in oscillator circuit (ST78C36ACJ and ST78C36CQ64 only) with an appropriate crystal.

At system RESET, the device defaults to standard IBM PC compatible Centronics printer mode (output only). The bi-directional PS/2, EPP, and ECP modes can only be activated by programming the ECR mode field (this requires address bit A10 = 1, which is outside the normal ISA I/O space).

Optional capabilities of the ECP specification are set as follows:

- ECP defined interrupts are pulsed, LOW true (Centronics -ACK is non-pulsed, LOW true).
- PWord size is forced to 1 byte.
- There is 1 byte in the transmitter that does not affect the FIFO full bit (ECP modes).
- RLE compression is not supported in hardware.
- IRQ channel is selectable as 5, 7, or 9 (ST78C36CQ64 only).
- DMA channel is selectable as 1, 2, or 3 (ST78C36CQ64 only).
- FIFO THRESHOLD is set at 8 (used only for non-DMA access to the FIFO).

PORT	ADDRESS	R/W	MODE	FUNCTION
DATA	000	R/W	000, 001	Data Register
ECP-AFIFO	000	W	011	ECP FIFO (Address)
DSR	001	R	All	Status Register
DCR	002	R/W	All	Control Register
EPP-APort	003	R/W	100	EPP Port (Address)
EPP-DPort	004 - 007	R/W	100	EPP Port (Data)
C-FIFO	400	W	010	Parallel Port Data FIFO
ECP-DFIFO	400	R/W	011	ECP FIFO (Data)
T-FIFO	400	R/W	110	Test FIFO
Cnfg-A	400	R	111	Configuration Register A
Cnfg-B	401	R/W	111	Configuration Register B
ECR	402	R/W	All	Extended Control Register

2.0 STANDARD DEFINITIONS

- **Forward direction only.**
  - Compatible Mode: “Centronics” or standard mode.
- **Reverse direction only.**
  - Nibble mode: 4 bits at a time using status lines for data “Hewlett Packard Bi-tronics”.
- **Bi-directional.**
  - EPP: Enhanced Parallel port-used primarily by non-printer peripherals.
  - ECP: Extended Capability Port-used primarily by new generation of printers and scanners.

3.0 INTERNAL REGISTERS

3.1 DATA REGISTER (DATA)

DATA Bits 7-0:

For host output cycles in SPP mode (ECR mode 000) or PS/2 mode (ECR mode 001), data from the host is registered at the trailing edge of -IOW. On host input cycles, data at the peripheral port is passed through to the host data bus.

3.2 ECP FIFO ADDRESS (ECP-AFIFO)

ECP-AFIFO Bits 7-0:

This port is only available for programmed I/O (non-DMA), and only has significance for host write. Data written to this port is stored in the FIFO if FIFO-F = 0 and will be lost if FIFO-F = 1. A 9th FIFO bit (tag) is set low on write. A read from this port is the same as a read at 400.

3.3 STATUS REGISTER (DSR)

This status register is read-only except for bit-0, and all bits are latched for the duration of -IOR.

DSR Bit-0:

If EPP mode is not selected, this bit returns logic one. During EPP mode, bit-0 will return a high if the EPP 10 msecond TimeOut elapsed during the last EPP read or write cycle (this TimeOut also aborts the EPP cycle). This status bit is cleared by exiting EPP mode or by the host writing a high to bit-0 of this register.

DSR Bits 2-1:

Reserved, logic one.

DSR Bit-3:

The true state of the -ERROR pad.

DSR Bit-4:

The true state of the SLCT pad.

DSR Bit-5:

The true state of the PE(mpty) pad.

DSR Bit-6:

The true state of the -ACK pad.

DSR Bit-7:

The complement of the BUSY pad.

3.4 CONTROL REGISTER (DCR)

DCR Bit-0:

The complement of this bit drives -STROBE, and the complement of the pad state is returned for read.

DCR Bit-1:

The complement of this bit drives -AUTOFD, and the complement of the pad state is returned for read.

DCR Bit-2:

This bit drives INIT, and the pad state is returned for read.

DCR Bit-3:

The complement of this bit drives -SLCTIN, and the complement of the pad state is returned for read.

DCR Bit-4:

Ack Interrupt Enable set to a high will generate an interrupt when -ACK is low. When either returns to a high state, this interrupt source will go in-active. This interrupt is not pulsed.

DCR Bit-5:

Peripheral port direction, OUT = 0 and IN = 1.

This bit is forced to logic zero by ECR modes 000 or 010. It can be written only in ECR mode 001, and will maintain that state if the ECR mode is changed to 011, 100, or 110. This bit must be set low for EPP mode, which allows the host to control direction with -IOR and -IOW. The final port direction also drives PDIR.

DCR Bits 6-7:

Reserved, logic zero.

3.5 EPP ADDRESS PORT (EPP-APort)

When EPP mode is enabled, a host read or write with this port will result in a data transfer directly to/from the peripheral with -SLCTIN active. Direction is set by host read/write and will drive -STROBE low during a write if DCR bit 5 (DIR) is not set high.

3.6 EPP DATA PORT (EPP-DPort)

When EPP mode is enabled, a host read or write with this port will result in a data transfer directly to/from the peripheral with -AUTOFD active. Direction is set by host read/write and will drive -STROBE low during a write if DCR bit 5 (DIR) is not set high.

3.7 PARALLEL PORT DATA (C-FIFO)

This port is available for programmed I/O and DMA access. Data written to this port is stored in the FIFO if FIFO-F = 0 and will be lost if FIFO-F = 1.

Data written to this port will be automatically transferred to the peripheral with -STROBE handshaking with BUSY. This port is only defined for write, host reads will interfere with FIFO read sequencing.

3.8 ECP DATA FIFO (ECP-DFIFO)

This port is available for programmed I/O and DMA access. Data written to this port is stored in the FIFO if FIFO-F = 0 and will be lost if FIFO-F = 1. A 9th FIFO bit (tag) is set high on write.

Data read from this port will undergo de-compression if the FIFO tag bit and data bit-7 are both low. The byte containing the RLE count is loaded into the RLE counter and the succeeding byte in the FIFO will be returned to the host RLE count + 1 times before the FIFO read address is incremented. If a FIFO under-run is incurred during host read, the last data byte is returned and FIFO-E remains coherent.

3.9 TEST FIFO (T-FIFO)

This port is available for programmed I/O and DMA access. Data written to this port is stored in the FIFO if FIFO-F = 0 and will be lost if FIFO-F = 1. During a read cycle from this port a FIFO under-run will return last data read and FIFO-E remains coherent.

3.10 CONFIGURATION REGISTER A (Cnfg-A)

This read-only register is available in ECR mode 111 only.

Cnfg-A Bits 1-0:

Forced to logic zero, this field is don't care for PWord = 1 byte.

Cnfg-A Bit-2:

When transmitting, there is 1 byte waiting to be transmitted that does not affect FIFO-F.

Cnfg-A Bit-3:

Reserved, logic zero.

Cnfg-A Bits 6-4:

Indicates PWord = 1 byte (8-bit implementation).

Cnfg-A Bit-7:

Indicates ECP interrupts are pulsed.

3.11 CONFIGURATION REGISTER B (Cnfg-B)

This register is available in ECR mode 111 only, and returns bits 0-5 as logic zero for the ST78C36CJ44. The ST78C36CQ64 will allow programmed selection of the Interrupt and DMA channels after a system RESET state of 001011 (bits 0-5).

Cnfg-B Bits 2-0:

With bit 2 forced low, select an 8-bit DMA channel per the following table:

TABLE 1: DMA CHANNEL SELECTION: CNFG-B BITS[2:0]

WRITE TO FIFO	READ FROM FIFO	DMA CHANNEL
X00	000	3
X01	001	1
X10	010	2
X11	011	3 (Default)

Cnfg-B Bits 5-3:

Select an IRQ channel per the following table:

TABLE 2: IRQ SELECTION: CNFG-B BITS[5:3]

WRITE TO FIFO	READ FROM FIFO	IRQ
000	001	7
001	001	7 (Default)
010	010	9
011	001	7
100	001	7
101	001	7
110	001	7
111	111	5

Cnfg-B Bit-6:

Returns the true value of the selected IRQ pad.

Cnfg-B Bit-7:

Indicates RLE compression is not supported.

3.12 EXTENDED CONTROL REGISTER (ECR)

The Extended Control Register has a system RESET state of 10010101. The significance of the bits is defined by the ECP specification as:

ECR Bit-0:

This read-only bit returns FIFO empty status (FIFO-E) and is forced high unless PPF, ECP, or TST mode is selected.

0 = At least one byte of data contains in the FIFO.

1 = FIFO is empty.

ECR Bit-1:

This read-only bit returns FIFO full status (FIFO-F) and is forced low unless PPF, ECP, or TST mode is selected.

0 = At least one empty location is available in the FIFO.

1 = FIFO is full.

ECR Bit-2:

When low, this bit (ServiceIntr) enables a pulsed interrupt and enables DMA requests (if bit-3 is set). If the enabled interrupt occurs, this bit is automatically returned to a high. The interrupt conditions are:

ECR Bit-3 = DMA

DCR Bit-5 = DIRection

TABLE 3: DMA CONDITION

DMA	DIR	CONDITION
0	0	8 empty bytes in the FIFO
0	1	8 filled bytes in the FIFO
1	X	DMA Terminal Count (TC).

ECR BIT-3:

This bit disables DMA when set low. When set high, a low on ServiceIntr will enable DMA requests.

0 = DMA disabled, DRQx pin is three-stated.

1 = DMA enabled

ECR Bit-4:

When low, this bit (-ErrIntrEn) enables a pulsed interrupt if -ERROR (-Fault) is low. The interrupt is only enabled in ECP mode.

ECR Bits 7-5:

This field can be set to any value if the current value is 000 or 001. If the current value is not 000 or 001, then the field can only be written to 000 or 001. The modes are defined as:

TABLE 4: DESCRIPTION OF PARALLEL PORT MODES

MODE	NAME	DESCRIPTION
000	SPP	Standard Centronics, output only. DCR bit-5 is forced to "0".
001	PS2	Bi-directional PS/2 parallel port. FIFO is disabled
010	PPF	FIFOed, output only. DCR Bit-5 is forced to “0”.
011	ECP	ECP FIFOed port with RLE de-compression. FIFO direction is controlled by DCR Bit-5.
100	EPP	EPP mode.
101	-	Reserved.
110	TST	FIFO test mode. FIFO is accessible via TFIFO register.
111	CFG	Configuration A/B register enable.

4.0 DEVICE OPERATION

4.1 SPP MODE

This is ECR mode 000 (system RESET mode).

In this output-only mode the host data is registered to PD[7:0] at the trailing edge of -IOW; PDIR is driven low; -STROBE, -AUTOFD, INIT, and -SLCTIN are open-drain; and all timing is managed by the host through DSR and DCR registers.

4.2 PS2 MODE

This is ECR mode 001.

In this bi-directional mode the host output data is registered to PD[7:0] at the trailing edge of -IOW, PDIR is driven by DIR to allow peripheral data input, -AUTOFD, INIT, and -SLCTIN are totem-pole, and all timing is managed by the host through DSR and DCR registers.

4.3 PPF MODE

This is ECR mode 010.

In this output-only mode the host data is written to the FIFO with I/O writes to address 400 or by DMA writes; PDIR is driven low; -AUTOFD, INIT, and -SLCTIN are totem-pole.

FIFO data is automatically registered to PD[7:0] whenever the FIFO-E bit is low (data available), and timing is generated by controller logic that handshakes -STROBE (controller) with BUSY (peripheral).

4.4 ECP MODE

This is ECR mode 011.

In this bi-directional mode the host data is written to the FIFO with I/O writes to address 000, 400 or DMA; PDIR is driven by DIR (can only be set in ECR mode 001); -AUTOFD, INIT, and -SLCTIN are totem-pole. I/O writes to address 000 will write a low into the FIFO tag bit, while I/O writes to address 400 or DMA will insert a high.

4.4.1 ECP FORWARD MODE (PDIR = 0)

FIFO data is automatically registered to PD[7:0] whenever the FIFO-E bit is low (data available), and timing is generated by controller logic that handshakes -STROBE (controller) with BUSY (peripheral). Data from the FIFO tag bit is output on -AUTOFD after being registered simultaneous with FIFO data.

4.4.2 ECP REVERSE MODE (PDIR = 1)

PD[7:0] data and BUSY are latched into the FIFO and tag bit respectively at the trailing edge of -AUTOFD if FIFO-F = 0. Timing is generated by controller logic that handshakes -ACK (peripheral) with -AUTOFD (controller).

4.5 EPP MODE

This is ECR mode 100.

In this bi-directional mode, I/O writes will latch host output data at the trailing edge of -IOW, and peripheral input data will be latched at the trailing edge of -SLCTIN or -AUTOFD. PDIR, and -STROBE are driven by the state of -IOW (DCR bits 5 and 0 must be set low); -AUTOFD, INIT, and -SLCTIN are totem-pole.

EPP mode allows buffered access between the PC bus and the peripheral with timing provided by the peripheral via BUSY handshake into IOCHRDY. I/O cycles with address 003 - 007 will immediately drive IOCHRDY low. -STROBE will go low and PD[7:0] is allowed to change (write cycles) after BUSY has been low for at least 60n second. (this delay may have elapsed prior to cycle initiation), immediately followed by a low driven on -SLCTIN for address 003 or -AUTOFD (DATASTB*) for address 004 - 007 (read and write cycles). When BUSY returns high for a minimum of 60n second, IOCHRDY and the active strobe will be driven high - allowing the host to complete the I/O transaction.

To prevent a system stall, a 10 msecond TimeOut aborts the cycle if it expires before BUSY returns high. This TimeOut also sets bit 0 of DCR, which is cleared by disabling EPP mode or writing a high to DCR bit 0.

4.6 TST MODE

This is ECR mode 110.

This mode allows data to be transferred (read or write in any direction) between the FIFO and host at address 400 or DMA without activating the control interface (no data is transferred to/from the peripheral). PDIR is driven by DIR (can only be set in ECR mode 001); -AUTOFD, INIT, and -SLCTIN are totem-pole.

Performing I/O cycles in this mode allows software to test for the value of FIFOThreshold (FT) for both output and input directions.

4.7 CFG MODE

This is ECR mode 111.

This mode enables I/O access to the configuration registers CONF-A and CONF-B and disables I/O access to the FIFO.

4.7.1 IRQ

The module has four sources of interrupt which may be directed to -IRQ5, -IRQ7, -IRQ9 (see CONF-B) or externally jumpered.

1. When DCR bit 4 (AIE) is high and -ACK is low the interrupt is active.
2. When ECP mode is active, if ECR bit 4 is low when ERROR transitions low or ECR bit 4 transitions low when -Fault is low an interrupt pulse of at least 200n seconds will be generated.
3. In FIFO modes (PPF, ECP, or TST) with ECR bit 3 (DMA) low, an interrupt pulse of at least 200n seconds will be generated when ECR bit 2 (SI) is set low if there are at least 8 empty bytes in the FIFO and PDIR = 0 or there are at least 8 filled bytes in the FIFO and PDIR = 1. This interrupt will automatically disable itself by setting ECR bit 2 high.
4. In FIFO modes (PPF, ECP, or TST) with (DMA request enabled), an interrupt pulse of at least 200n seconds will be generated when TC is received if PD-ACK is low.

This interrupt will automatically disable itself and the DMA request by setting ECR bit 2 high.

4.7.2 DMA

DMA cycles occur only between the host and the FIFO data port (address 400) for PPF, ECP, or TST modes. The selected DRQ(1, 2, or 3) will be driven high if ECR bit 3 (DMA) is high and ECR bit 2 (SI) is low when {PDIR = 0 and FIFO-F = 0} or {PDIR = 1 and FIFO-E = 0} or TST mode is active.

When the selected D-ACK(1, 2, or 3) is low, -IOW will transfer host data to the FIFO and -IOR will transfer FIFO data to the host.

The selected DRQ will be driven low to terminate the DMA channel when {PDIR = 0 and FIFO-F = 1} or {PDIR = 1 and FIFO-E = 1} or ECR bit 2 (SI) goes high (interrupt condition 4 above) or more than 32 consecutive DMA data cycles (read or write) have occurred.

FIFO-F and FIFO-E terminated cycles will automatically restart when their state returns low. Consecutive cycle termination will automatically restart because the counter is reset when the selected D-ACK goes high. TC terminated cycles can only be restarted by the host setting ECR bit 2 (SI) low again.

4.7.3 RLE

The module does not support RLE compression (indicated by the “0” in CONF-B bit 7) but is required to support RLE de-compression.

The host may send compressed data to the peripheral by writing the RLE length byte (bit 7 = 0) to address 000 (NOTE: DMA cannot be used for this byte) which will place a zero into the FIFO tag bit. This must be followed immediately by the data byte being written to the FIFO at address 400. These bytes will be transferred to the peripheral in the normal manner.

De-compression takes place if PDIR = 1 when data is read from the FIFO at address 000, 400 or DMA. When a byte is read from the FIFO, bits 0-6 (length) are placed in a counter if data bit-7 and the FIFO tag bit are both low. The subsequent byte in the FIFO (data) is presented to the host count + 1 times before the FIFO read pointer is advanced.

TABLE 5: INTERNAL REGISTERS DESCRIPTION

A10	A2	A1	A0	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	Data Port , ECP-AFIFO	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
0	0	0	1	DSR	BUSY	-ACK	PE	SLCT	ERROR	1	1	1
0	0	1	0	DCR	0	0	DIR	INT enable	-SLCTIN	INIT	-AUTO-FD	-STROBE
0	0	1	1	EPP-APort	AP-7	AP-6	AP-5	AP-4	AP-3	AP-2	AP-1	AP-0
1	0	0	0	EPP-DPort	PDA-7	PDA-6	PDA-5	PDA-4	PDA-3	PDA-2	PDA-1	PDA-0
0	1	0	1	EPP-DPort	PDB-7	PDB-6	PDB-5	PDB-4	PDB-3	PDB-2	PDB-1	PDB-0
0	1	1	0	EPP-DPort	PDC-7	PDC-6	PDC-5	PDC-4	PDC-3	PDC-2	PDC-1	PDC-0
0	1	1	1	EPP-DPort	PDD-7	PDD-6	PDD-5	PDD-4	PDD-3	PDD-2	PDD-1	PDD-0
1	X	0	0	CONF-A	ECP INT type	0	0	1	0	FIFO-F	0	0
1	X	0	1	CONF-B	RLE	IRQ Input	IRQ Sel-2	IRQ Sel-1	IRQ Sel-0	DMA Sel-2	DMA Sel-1	DMA Sel-0
1	X	1	0	ECR	MODE Sel-2	MODE Sel-1	MODE Sel-0	FAULT enable	DMA En/Dis	Service INT	FIFO full	FIFO empty

5.0 SIGNAL DESCRIPTIONS IN VARIOUS MODES

TABLE 6: "CENTRONICS, SPP" SIGNAL DESCRIPTIONS

SIGNAL NAME	SIGNAL TYPE	DESCRIPTION
-STROBE	O	Active low. Indicates valid data is on the data lines.
-AUTOFD	O	Active low. Instructs the printer to automatically insert a line feed for each carriage return.
-SLCTIN	O	Active low. Used to indicate to the printer that it is selected.
INIT	O	Active low. Used to reset the printer
-ACK	I	A low asserted pulse used to indicate that the last character was received.
BUSY	I	A high signal asserted by the printer to indicate that it is busy and cannot take data.
PE	I	A high signal indicated that printer Paper is empty.
SLCT	I	A high signal indicates that printer is online.
-ERROR	I	Asserted low to indicate that some error condition exists.
PD0-PD7	O	Data.

TABLE 7: "NIBBLE MODE" SIGNAL DESCRIPTIONS

SIGNAL NAME	SIGNAL TYPE	NIBBLE MODE NAME	DESCRIPTION
-STROBE	O	-STROBE	Not used for reverse data transfer.
-AUTOFD	O	HostBusy	Host nibble mode handshake signal. Set low to indicate host is ready for nibble. Set high to indicate nibble has been received.
-SLCTIN	O	1284Active	Set high when host is in a 1284 transfer mode.
INIT	O	INIT	Not used for reverse data transfer.
-ACK	I	PtrClk	Set low to indicate valid nibble data, set high in response to "HostBusy" going high.
BUSY	I	PtrBusy	Used for Data Bit-3, then Bit-7.
PE	I	AckDataReq	Used for Data Bit-2, then Bit-6.
SLCT	I	Xflag	Used for Data Bit-1, then Bit-5.
-ERROR	I	-DataAvail	Used for Data Bit-0, then Bit-4.
PD0-PD7	O	N/A	Not used.

5.1 NIBBLE Mode Data Transfer Cycle

- Host signals ability to take data by asserting HostBusy low.
- Peripheral responds by placing first nibble on status lines.
- Peripheral signals valid nibble by asserting PtrClk low.
- Host sets HostBusy high to indicate that it has received the nibble and is not ready for another nibble.
- Peripheral sets PtrClk high to acknowledge host.

TABLE 8: "EPP MODE" SIGNAL DESCRIPTIONS

SIGNAL NAME	SIGNAL TYPE	EPP MODE NAME	DESCRIPTION
-STROBE	O	-Write	Active low. Indicates a write operation, high for a read cycle
-AUTOFD	O	-DataStb	Active low. Indicates a Data-Read or Data-Write operation is in process.
-SLCTIN	O	-AddrStb	Active low. Indicates an Address-Read or Address-Write operation is in process.
INIT	O	-Reset	Active low. Peripheral reset.
-ACK	I	-Intr	Peripheral interrupt. Used to generate an interrupt to the host.
BUSY	I	-Wait	Handshake signal. When low it indicates that is okay to start a cycle, when high it indicates that it is okay to end the cycle.
PE	I	User defined	
SLCT	I	User defined	
-ERROR	I	User defined	
PD0-PD7	O	AD0-AD7	Bi-directional address / data lines.

5.2 EPP Mode Data Transfer Cycle

- Program executes an I/O write cycle to EPP Data Port-4.
- The -Write line is asserted and the data is output to the parallel port.
- The -DataStb is asserted, since -Write is asserted low.
- The port waits for the acknowledge from the peripheral, -Write deasserted.
- The -DataStr is deasserted and EPP cycle ends.
- -Write is asserted low to indicate that the next cycle may begin.

TABLE 9: "ECP MODE" SIGNAL DESCRIPTION

SIGNAL NAME	SIGNAL TYPE	ECP MODE NAME	DESCRIPTION
-STROBE	O	HostClk	Used with PeriphAck to transfer data or address information in the forward direction.
-AUTOFD	O	HostAck	Provides Command / Data status in the forward direction. Used with PeriphClk to transfer data in the reverse direction.
-SLCTIN	O	1284Active	Set high when host is in a 1284 transfer mode.
INIT	O	-ReverseReq	Driven low to put the channel in reverse direction.
-ACK	I	PeriphClk	Used with HostAck to transfer data in the reverse direction.
BUSY	I	PeriphAck	Used with HostClk to transfer data or address information in the forward direction. Provides Command / Data status in the reverse direction.
PE	I	-AckReverse	Driven low to acknowledge ReverseRequest.
SLCT	I	Xflag	Extensibility flag.
-ERROR	I	-PeriphReq	Set low by peripheral to indicate that reverse dat is available.
PD0-PD7	I/O	D0-D7	Bi-directional data lines.

5.3 ECP Mode Forward Data and Command Transfer Cycle

- Host places data on the data lines and indicates a data cycle by setting HostAck high.
- Host asserts HostClk low to indicate valid data.
- Peripheral acknowledge host by setting PeriphAck high.
- Host sets HostClk high. This is the edge that should be used to clock the data in to the peripheral.
- Peripheral sets PeriphAck low to indicate that it is ready for the next byte.
- The cycle repeats, but this time it is command cycle because HostAck is low.

5.4 ECP Mode Reverse Data and Command Transfer Cycle

- The Host requests a reverse channel transfer by setting -ReverseReq low.
- The peripheral signals that it is okay to proceed by setting -AckReverse low.
- The peripheral places data on the data lines and indicates a data cycle by setting PeriphAck high.
- Peripheral asserts PeriphClk low to indicate valid data.
- Host acknowledges by setting HostAck high.
- Peripheral sets PeriphClk high. This is the edge that should be used to clock the data in to the host.
- Host sets HostAck low to indicate that it is ready for the next byte.
- The cycle repeats, but this time it is a Command cycle because PeriphAck is low.

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C - 70°C, VCC = 5.0V +/- 10%, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
T1	AEN setup to command active	40			NS
T2	Command width	150			ns
T3	AEN hold from command inactive	60			ns
T4	Data access from -IOR active			100	ns
T5	Data setup to -IOW inactive	40			ns
T6	Data hold from command inactive	60			ns
T7	PD7-0, -STROBE, -AUTOFD, INIT, -SLCTIN delay from -IOW inactive			100	ns
T8	Interrupt delay from -ACK			60	ns
T9	Interrupt pre-charge pulse at release			10	ns
T10	TC pulse width	60			ns
T11	TC active to DRQx inactive			100	ns
T12	DRQx active to -DACKx active	0			ns
T13	DRQx inactive delay from -DACKx active			100	ns
T14	PD7-0 setup to -STROBE active		600		ns
T15	-STROBE width		600		ns
T16	PD7-0 hold from -STROBE inactive		450		ns
T17	PD7-0 hold from BUSY inactive		80		ns
T18	-STROBE active to BUSY active (handshake)			500	ns
T19	BUSY inactive to -STROBE active (cycle delay)		680		ns
T20	PD7-0, -AUTOFD setup to -STROBE active		0	60	ns
T21	PD7-0, -AUTOFD hold from BUSY active		80	180	ns
T22	-STROBE inactive to BUSY inactive		0		ns
T23	BUSY inactive to -STROBE active		80	200	ns
T24	-STROBE active to BUSY active		0		ns
T25	BUSY active to -STROBE inactive		80	180	ns
T26	PD7-0, BUSY setup to -ACK active		0		ns
T27	PD7-0 data hold from -AUTOFD active		0		ns
T28	-ACK inactive to -AUTOFD active		80	200	ns
T29	-AUTOFD active to -ACK active		0		ns
T30	-ACK active to -AUTOFD inactive		80	200	ns

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C - 70°C, VCC = 5.0V +/- 10%, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
T31	-AUTOFD inactive to -ACK inactive		0		ns
T32	Host address setup to -IOW active		40		ns
T33	Host address hold from -IOW active		60		ns
T34	Host data setup to -IOW active		0	20	ns
T35	Host data hold from -IOW active		50		ns
T36	-IOW active to IOCHRDY low		0	20	ns
T37	IOCHRDY high to Host terminate (-IOW inactive)		10		ns
T38	-IOW inactive to Host command active (-IOW or -IOR)		40		ns
T39	IOCHRDY pre-charge width at release			10	ns
T40	Host address setup to -IOR active		40		ns
T41	Host address hold from -IOR active		10		ns
T42	Host data setup to -IOR inactive		0	20	ns
T43	Host data hold from -IOR inactive		0		ns
T44	-IOR active to IOCHRDY low		0	20	ns
T45	IOCHRDY high to Host terminate (-IOR inactive)		10		ns
T46	-IOR inactive to Host command active (-IOW or -IOR)		40		ns

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C - 70°C, VCC = 5.0V +/- 10%, unless otherwise specified.

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
V_{ILCK}	Clock Input Low level	-0.5		0.6	V	
V_{IHCK}	Clock Input High level	3.0		VCC	V	
V_{IL}	Input Low level	-0.5		0.8	V	
V_{IH}	Input High level	2.0		VCC	V	
V_{OL}	Output Low level			0.4	V	DRQ1-3, IOCHRDY: I_{OL} = 14 mA D0-D7: I_{OL} = 12 mA PDIR: I_{OL} = 4 mA All other outputs: I_{OL} = 20mA
V_{OH}	Output High level	2.4			V	D0-D7: I_{OH} = -12mA PDIR: I_{OH} = -1mA All other outputs: I_{OH} = -20mA
ICC	Avg. power supply current		7	9	mA	
I_{IL}	Input leakage			10	µA	
I_{CL}	Clock leakage			10	µA	
I_R	Internal pull up resistor current	-85		-30	µA	For inputs -DACK1-3, -ERROR, SLCT, BUSY, -ACK and PE

NOTE: *Hewlett Packard / Microsoft compliance testing requires all ECP mode drivers to be push-pull and that they have an impedance controlled series resistor of at least 20 Ohms and that the typical on resistance of the combination of the driver-resistor pair is in the 45-65 Ohm range.*

FIGURE 3. GENERAL READ/WRITE TIMING

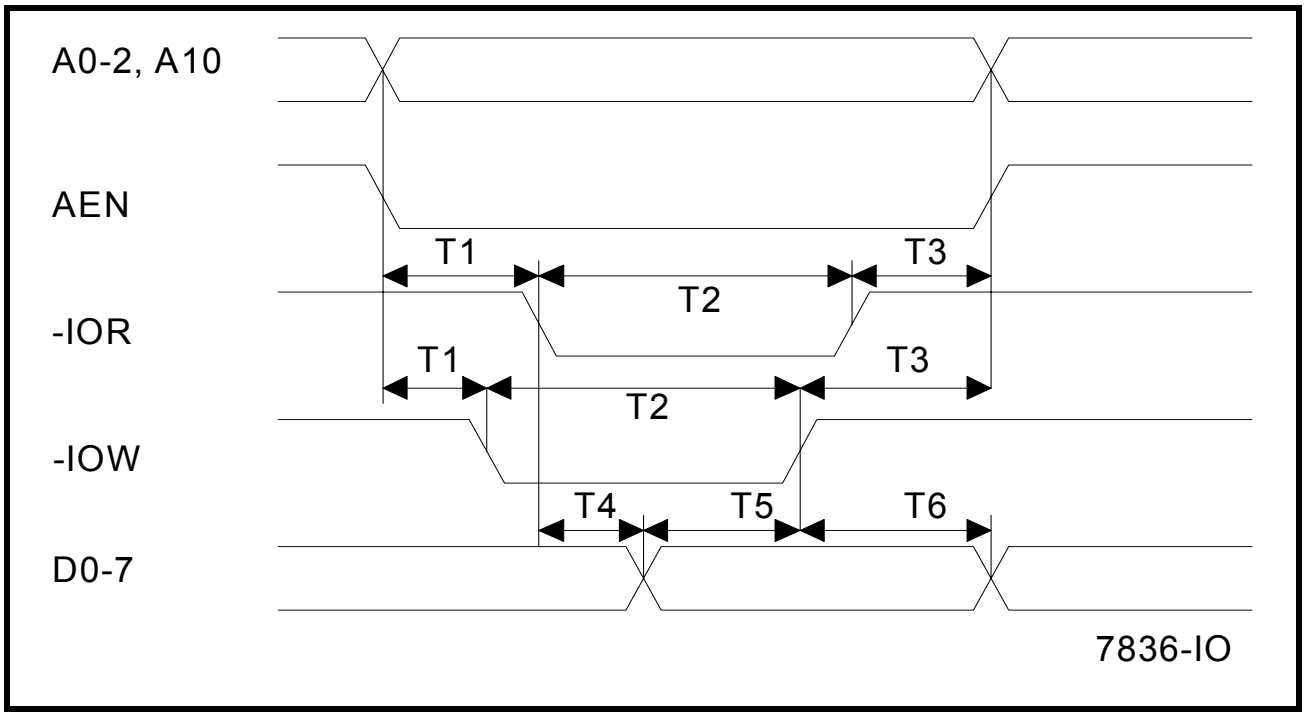


FIGURE 4. PARALLEL PORT TIMING IN SPP, PS/2 MODES

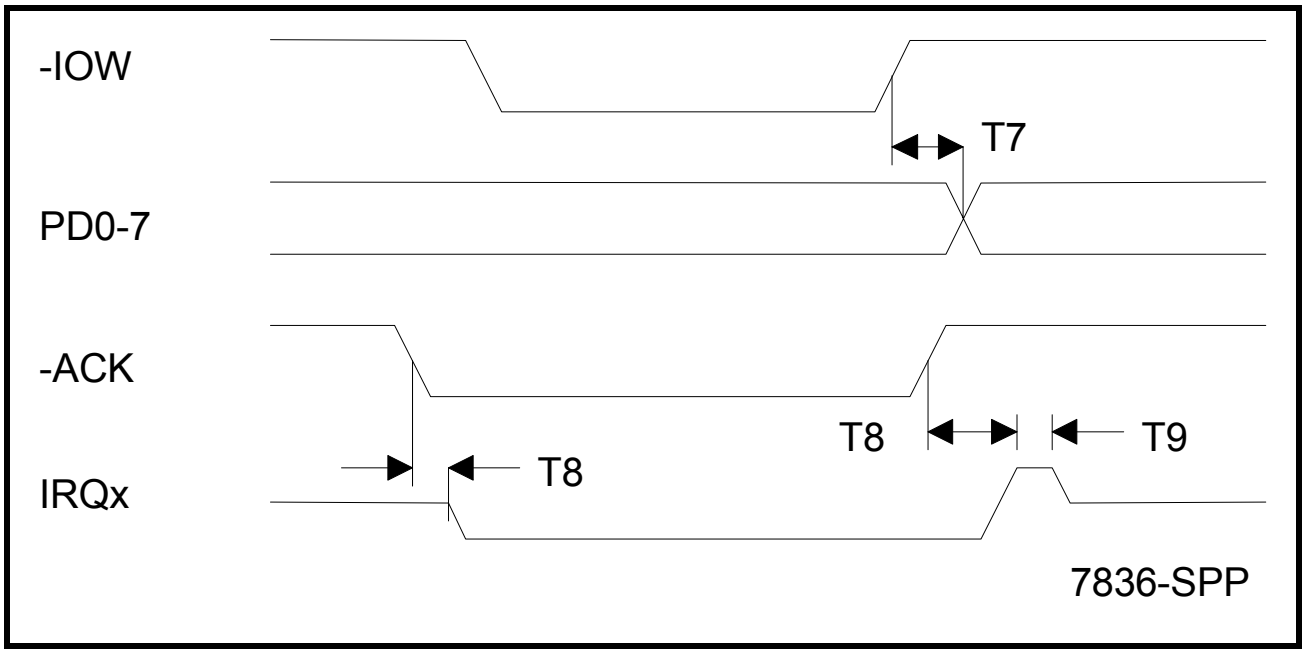


FIGURE 5. HOST DMA TIMING IN ECP MODE

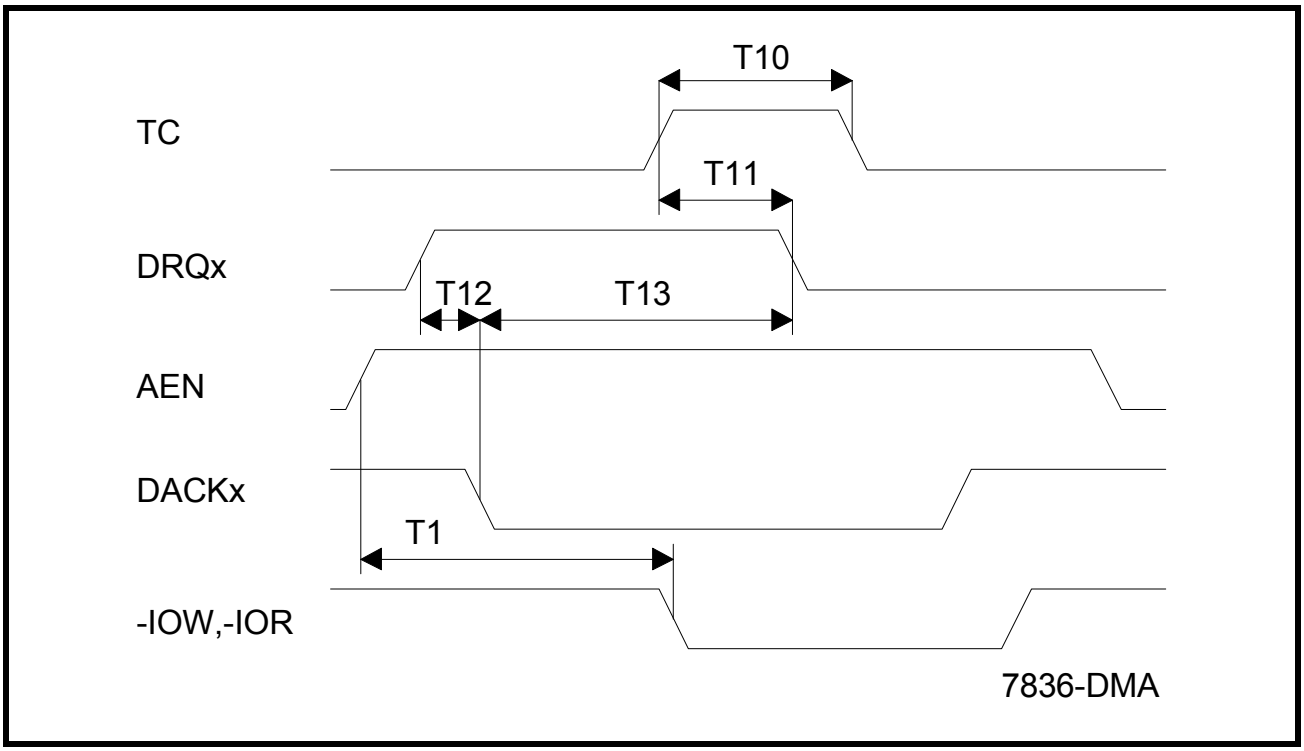


FIGURE 6. PARALLEL PORT FIFO TIMING

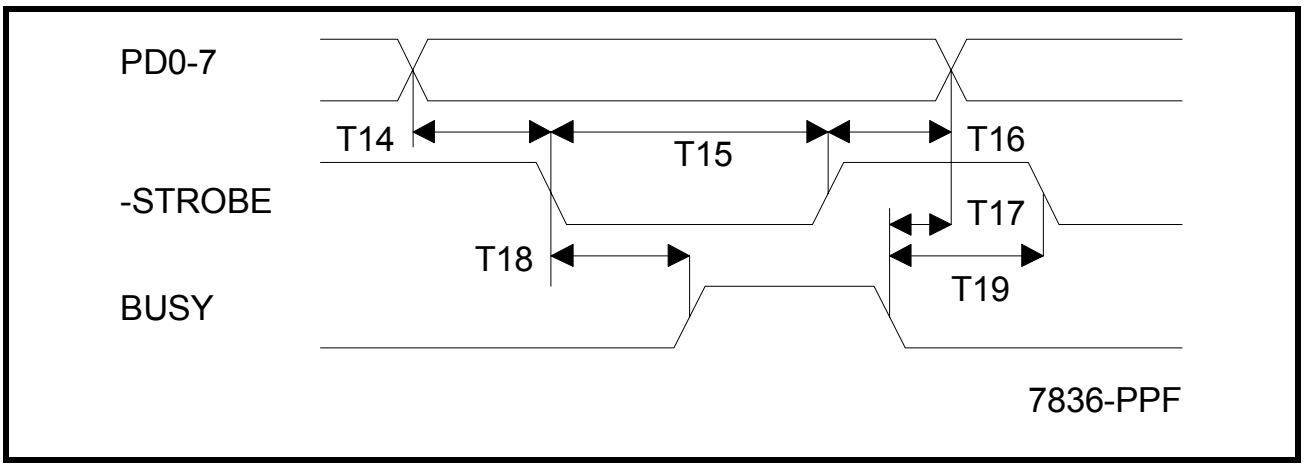


FIGURE 7. PARALLEL PORT FORWARD TIMING IN ECP MODE

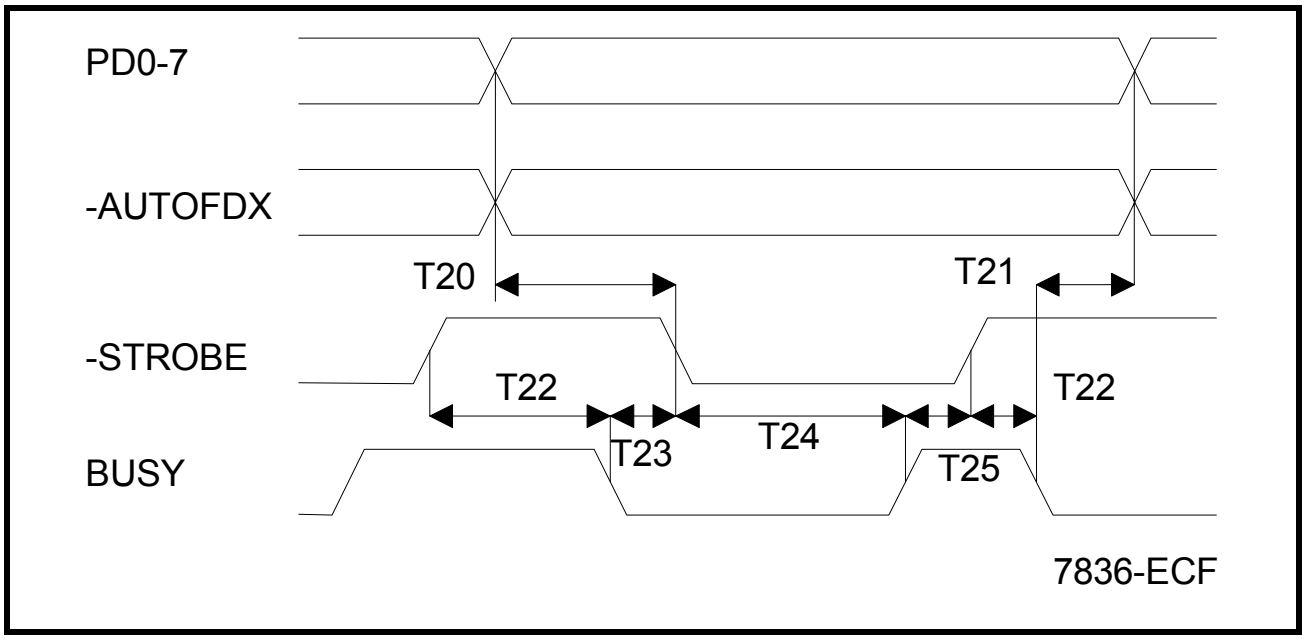


FIGURE 8. PARALLEL PORT REVERSE TIMING IN ECP MODE

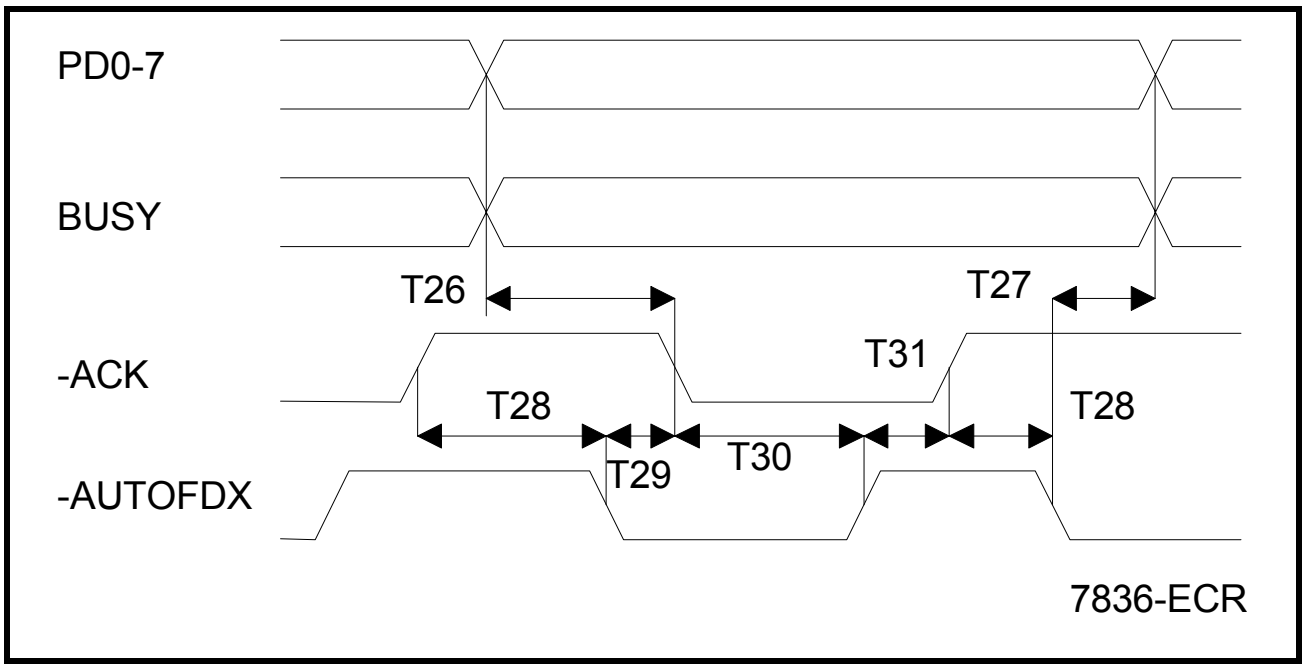


FIGURE 9. ADDRESS OR DATA WRITE TIMING IN EPP MODE

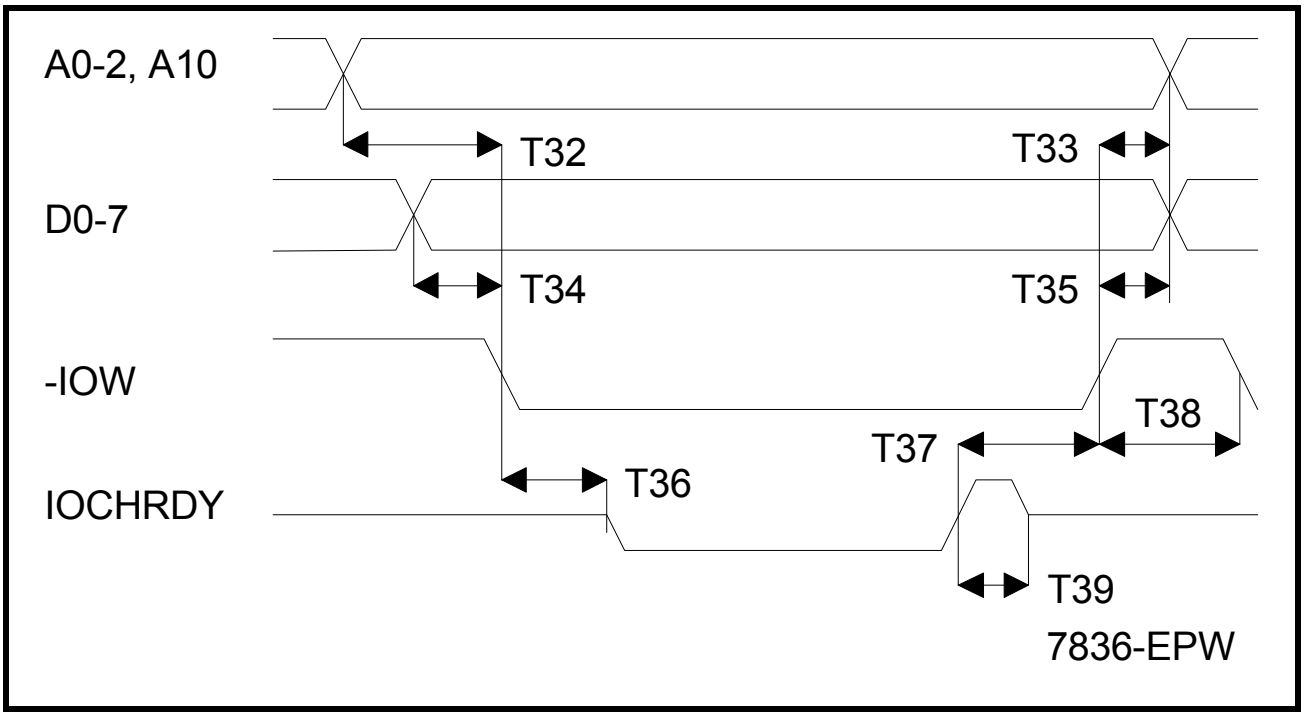
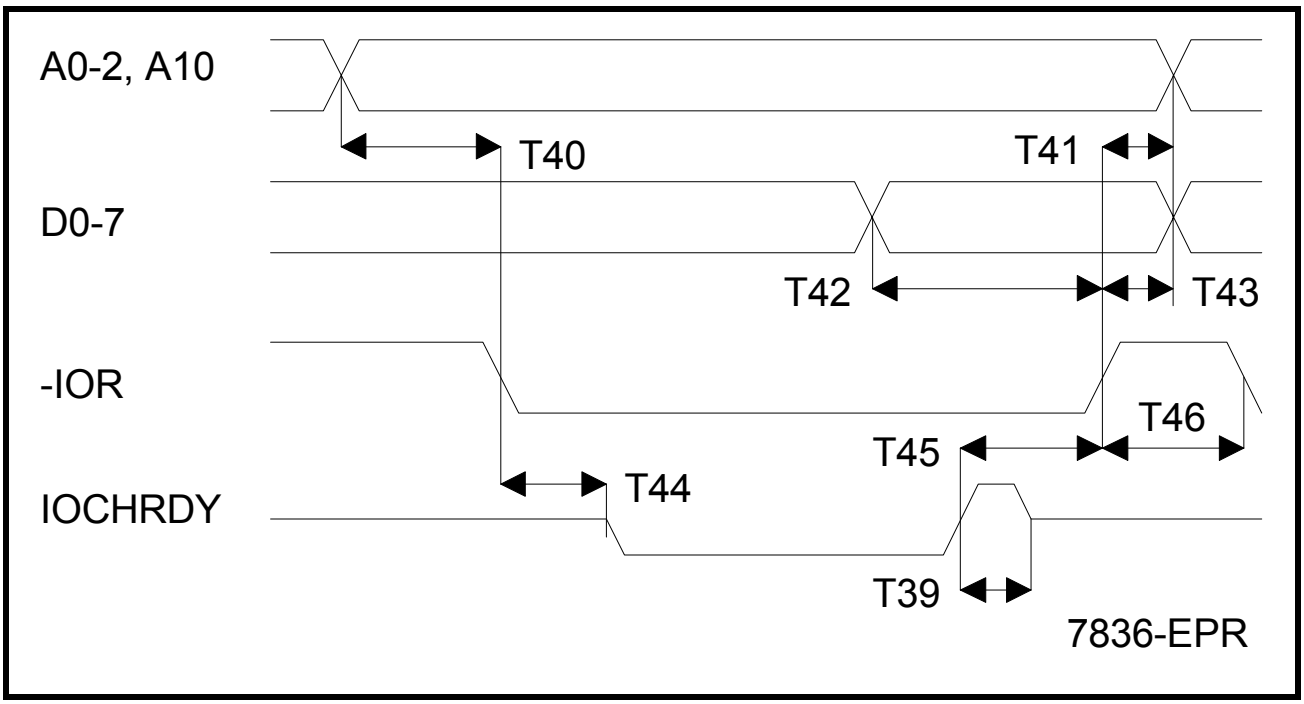


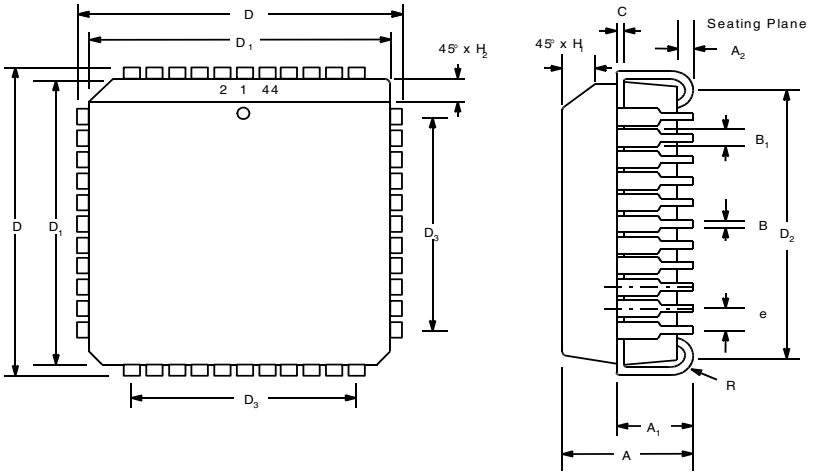
FIGURE 10. ADDRESS OR DATA READ TIMING IN EPP MODE



PACKAGE DIMENSIONS (44 PIN PLCC)

44 LEAD PLASTIC LEADED CHIP CARRIER (PLCC)

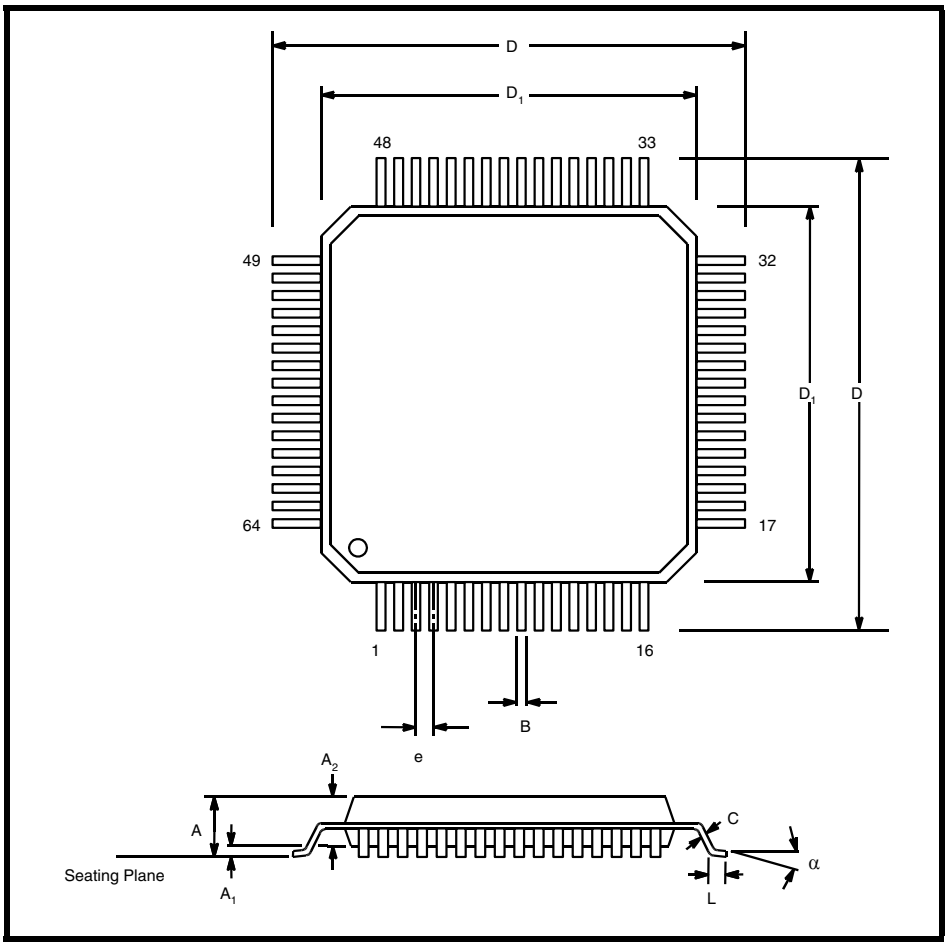
Rev. 1.00



Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A_1	0.090	0.120	2.29	3.05
A_2	0.020	---	0.51	---
B	0.013	0.021	0.33	0.53
B_1	0.026	0.032	0.66	0.81
C	0.008	0.013	0.19	0.32
D	0.685	0.695	17.40	17.65
D_1	0.650	0.656	16.51	16.66
D_2	0.590	0.630	14.99	16.00
D_3	0.500 typ.		12.70 typ.	
e	0.050 BSC		1.27 BSC	
H_1	0.042	0.056	1.07	1.42
H_2	0.042	0.048	1.07	1.22
R	0.025	0.045	0.64	1.14

PACKAGE DIMENSIONS (64-LQFP)



Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A_1	0.002	0.006	0.05	0.15
A_2	0.053	0.057	1.35	1.45
B	0.005	0.009	0.13	0.23
C	0.004	0.008	0.09	0.20
D	0.465	0.480	11.80	12.20
D_1	0.390	0.398	9.90	10.10
e	0.020 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
a	0°	7°	0°	7°

REVISION HISTORY

DATE	REVISION	DESCRIPTION
December 2003	Rev 5.0.0	Changed to standard style format. Added Revision History. Added Device Status to Ordering Information. Updated DC Electrical Characteristics.
February 2004	Rev 5.0.1	Corrected the signal type of the -AUTOFDX pin from I (input) to O (output).
August 2005	Rev 5.0.2	Updated the 1.4mm-thick Quad Flat pack package description from "TQFP" to "LQFP" to be consistent with the JEDEC and Industry norms.
April 2010	Rev 5.1.0	Updated AC Timing specs for T3, T6, T33, and T35. Changed status of ST78C36CQ64 to "EOL" per PDN 090507-01.

NOTICE

EXAR Corporation reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. EXAR Corporation assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contained here in are only for illustration purposes and may vary depending upon a user's specific application. While the information in this publication has been carefully checked; no responsibility, however, is assumed for inaccuracies.

EXAR Corporation does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless EXAR Corporation receives, in writing, assurances to its satisfaction that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; (c) potential liability of EXAR Corporation is adequately protected under the circumstances.

Datasheet April 2010.

Send your UART technical inquiry with technical details to hotline: uarttechsupport@exar.com.