ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Cathode-Anode Reverse Breakdown V_{KA} 20V
Anode-Cathode Forward Current, (<10ms) I_{AK} 1A
Operating Cathode Current I_{KA} 100mA
Reference Input Current I_{REF} 10mA
Continuous Power Dissipation at 25°C PD
TO-92 .... 775mW
SOT-89 .... 1000mW
Storage Temperature T_{STG} ....-65 to 150°C
Lead Temperature (Soldering 10 sec.) T_L...............300°C

OPERATING RATINGS

Input Voltage Range V_{KA}...............................V_{REF} to 20V
Cathode Current I_K 10ma
Junction Temperature Range ....150 °C
Thermal Resistance
0JA (TO-92) ....160°C/W
0JC (TO-92) .... 80°C/W
Typical Derating (TO-92) ....6.3 mW/°C

0JA (SOT-89) ....110°C/W
0JC (SOT-89) .... 8°C/W
Typical Derating (SOT-89) ....9.1 mW/°C

ELECTRICAL SPECIFICATIONS

Specifications with standard type are for an Operating Junction Temperature of T_A = 25°C only; limits applying over the full Operating Junction Temperature range are denoted by a "•". Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_A = 25°C, and are provided for reference purposes only. Unless otherwise indicated, I_K = 10mA V_K = V_{REF}.

Parameter	Min.	Typ.	Max.	Units		Conditions
SPX431LA						
Reference Voltage	2.490	2.503	2.515	V		
ΔVREF withTemp.[1]		0.07	0.20	mV/°C		
Ratio of Change in VREF to Cathode Voltage	-2.7 -2.0	-1.0 -0.4	0.3	mV/V		VREF to 10V VREF to 10V
Reference Input Current		0.7	4.0	µA		
IREF Temp Deviation		0.4	1.2	µA		TJ = 0°C to 105°C
Min IK for Regulation		0.4	1.0	mA		
Off State Leakage		0.04	1.0	µA		VREF = 0V, VKA = 20V
Dynamic Output Impedance		0.15	0.5	Ω		ƒz ≤ 1kHz IK = 1 to 100mA
SPX431L						
Reference Voltage	2.470	2.495	2.520	V		
ΔVREF withTemp.[1]		0.07	0.20	mV/°C		
Ratio of Change in VREF to Cathode Voltage	-2.7 -2.0	-1.0 -0.4	0.3	mV/V		VREF to 10V VREF to 10V
Reference Input Current		0.7	4.0	µA		
IREF Temp Deviation		0.4	1.2	µA		TJ = 0°C to 105°C
Min IK for Regulation		0.4	1.0	mA		
Off State Leakage		0.04	1.0	µA		VREF = 0V, VKA = 20V
Dynamic Output Impedance		0.15	0.5	Ω		ƒz ≤ 1kHz IK = 1 to 100mA
SPX431LC						
Reference Voltage	2.445	2.495	2.520	V		
ΔVREF withTemp.[1]		0.07	0.20	mV/°C		
Ratio of Change in VREF to Cathode Voltage	-2.7 -2.0	-1.0 -0.4	0.3	mV/V		VREF to 10V VREF to 10V
Reference Input Current		0.7	4.0	µA		
IREF Temp Deviation		0.4	1.2	µA		TJ = 0°C to 105°C

Parameter	Min.	Typ.	Max.	Units		Conditions
Min IK for Regulation		0.4	1.0	mA		
Off State Leakage		0.04	1.0	µA		VREF = 0V, VKA = 20V
Dynamic Output Impedance		0.15	0.5	Ω		$f_Z \leq$ 1kHz I_K = 1 to 100mA

Note 1: See appropriate test circuit (Figures 25, 26, 27)

PIN ASSIGNMENT

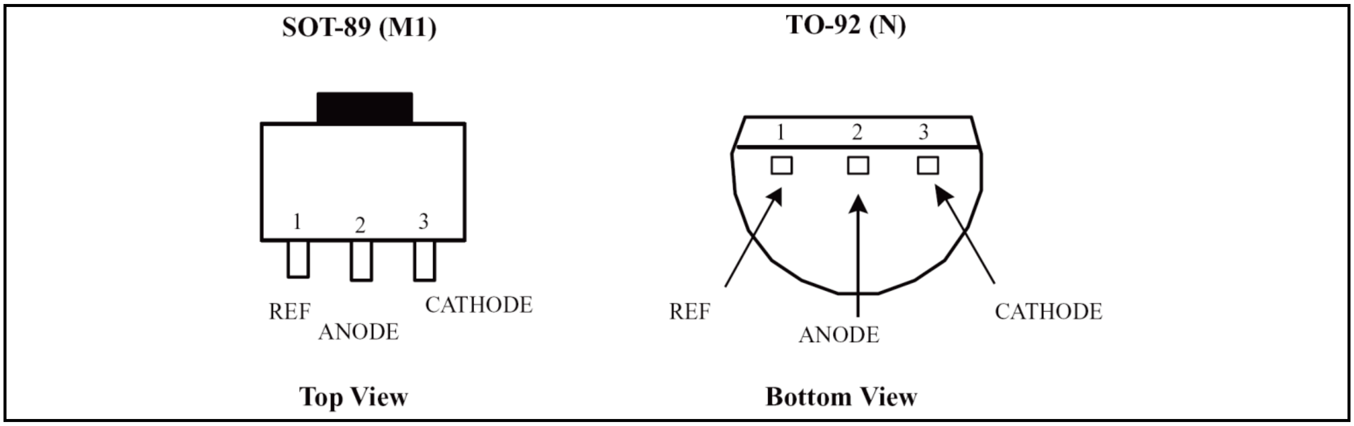


Fig. 2: SPX431L Pin Assignment

PIN DESCRIPTION

Name	Pin Number	Description
NAME	1	Reference
NAME	2	Anode
NAME	3	Cathode

ORDERING INFORMATION

Part Number	Temperature Range	Marking	Package	Packing Quantity	Note 1	Note 2
SPX431LAN-L	0°C to 105°C	Sipex 431LAN 25 YYWWLX	TO-92-3	Bulk	Halogen Free	2.503V 0.5% Acc
SPX431LAN-L/TR				Tape & Reel		
SPX431LM1-L	0°C to 105°C	P011 YYWWXXX	SOT-89-3	Bulk	Halogen Free, bar on left side of marking denotes "-L" lead free product	2.495V 1.0% Acc
SPX431LM1-L/TR				Tape & Reel		
SPX431LN-L	0°C to 105°C	Sipex 431LN 25 YYWWLX	TO-92-3	Bulk	Halogen Free	2.495V 1.0% Acc
SPX431LN-L/TR				Tape & Reel		

"YY" = Year (Last 2 digits) – "Y" = Year (Last Digit)

"WW" = Work Week

"L" = Lead free designator

"X" = Lot Number (example AA234567) – "XXX" = Lot Number (example AA234567)

No bottom marking

TYPICAL PERFORMANCE CHARACTERISTICS

Schematic and BOM from Application Information section of this datasheet. Resistor values are chosen such that the effect to I_{REF} is negligible.

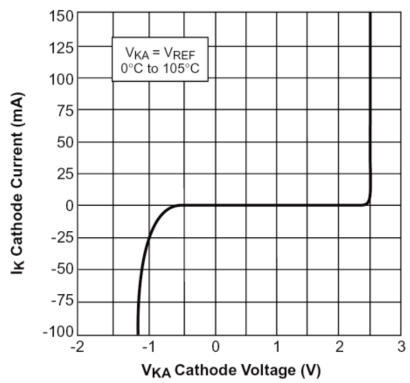


Fig. 3: High Current Operating Characteristics

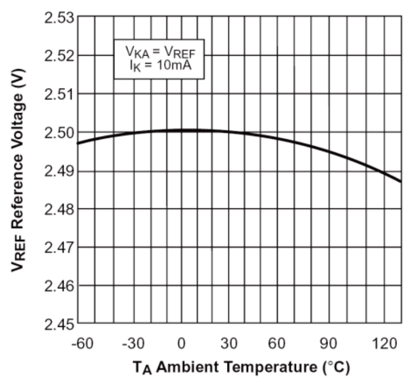


Fig. 4: Reference Voltage VS Ambient Temperature

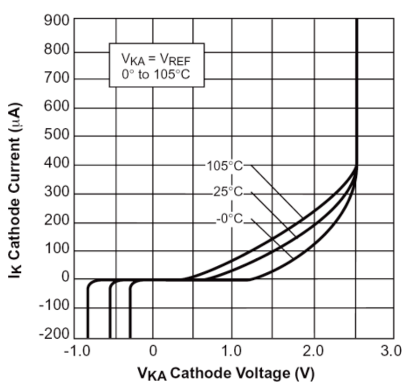


Fig. 5 Low Current Operating Characteristics**.**

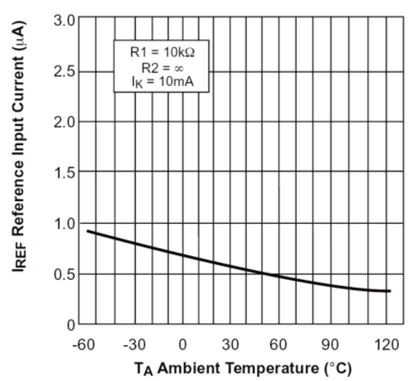


Fig. 6 Reference Input Current VS Ambient Temperature.

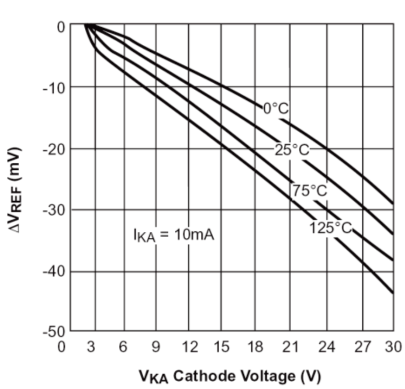


Fig. 7 Reference Voltage Line Regulation VS Cathode Voltage and TAMBIENT

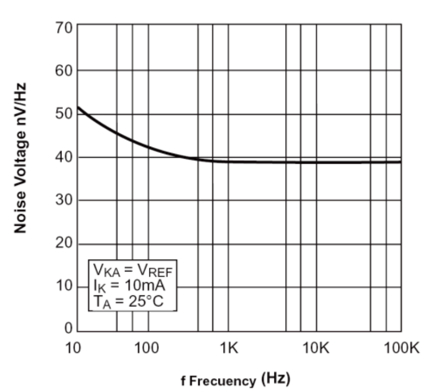


Fig. 8 Noise Voltage VS Frequency

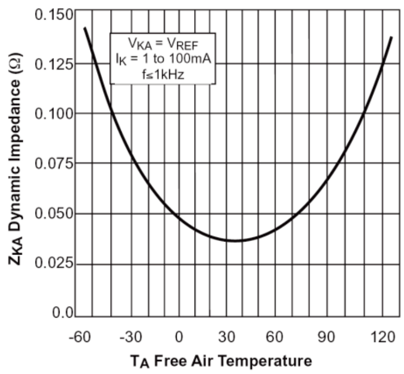


Fig. 9 Low Frequency Dynamic Output Impedance VS TAMBIENT

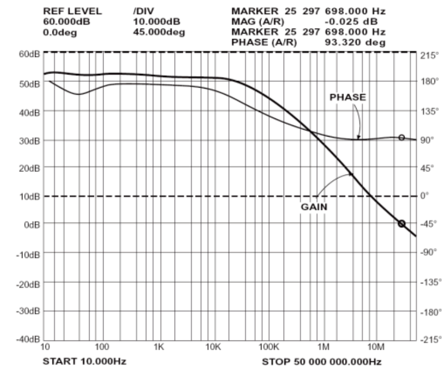


Fig. 10 Small Signal Gain and Phase VS Frequency; I_K = 10mA, T_A = 25°C

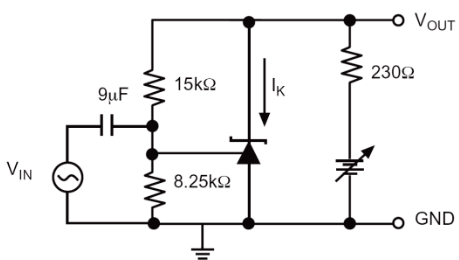


Fig. 11 Test Circuit for Gain and Phase Frequency Response

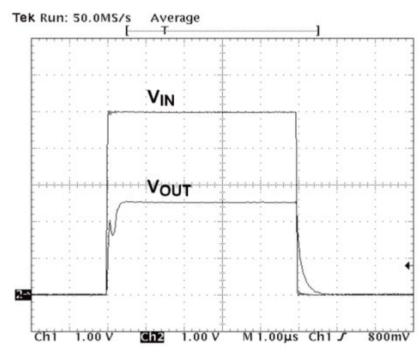


Fig. 2 F_Z = 100kHz, I_K = 10mA, T_A = 25°C

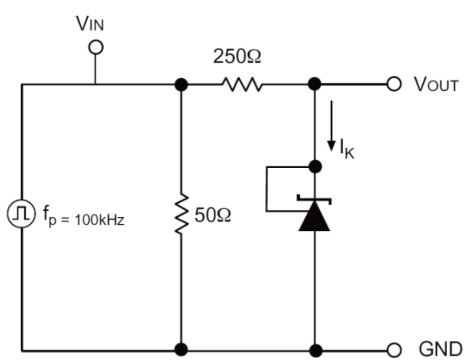


Fig. 33 Test Circuit for Pulse Response

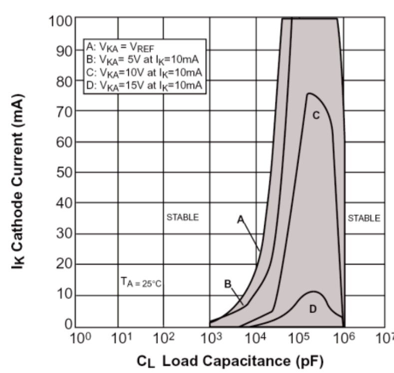


Fig. 44 Stability Boundry Conditions

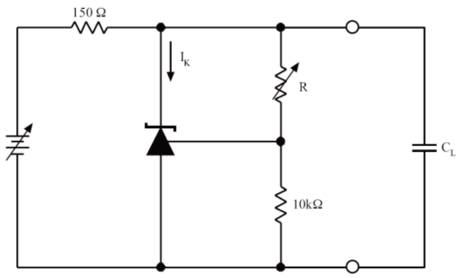


Fig. 55 Test Circuit for Stability

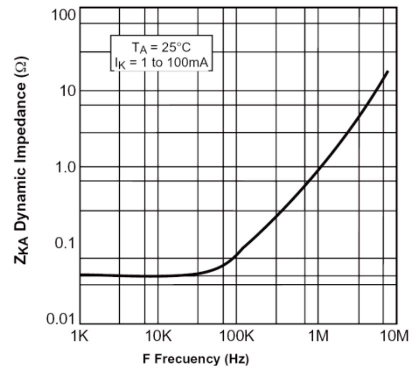


Fig. 66 Dynamic Output Impedance $T_A = 25°C$, $I_K = 1$ to 100mA

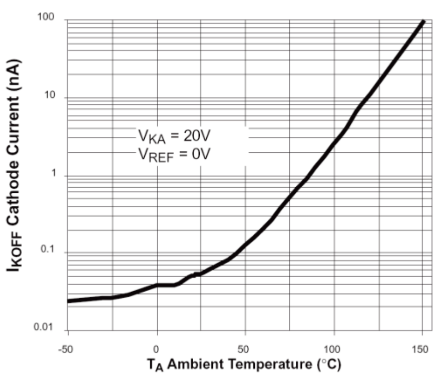


Fig. 77 Off State Leakage

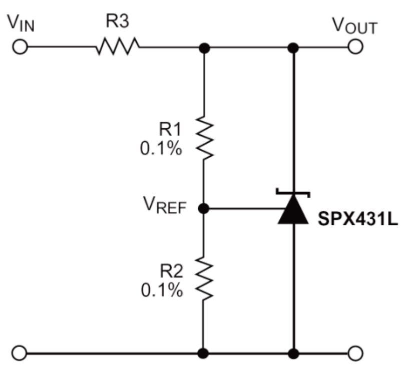


Fig. 88 Shunt Regulator $V_{OUT} = (1+R1/R2)V_{REF}$

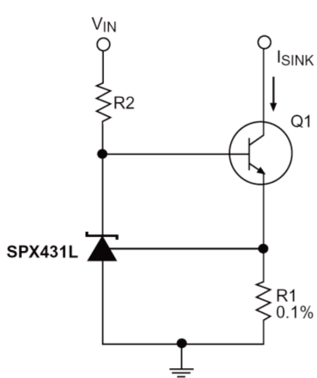


Fig. 199 Constant Current Sink, $I_{SINK} = V_{REF}/R1$

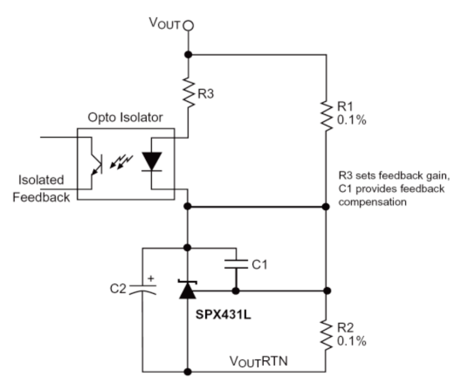


Fig. 100 Reference Amplifier for Isolated Feedback in Off-Line DC-DC Converters

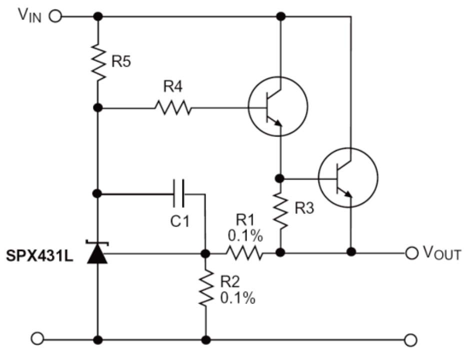


Fig. 111 Precision High Current Series Regulator
$V_{OUT} = (1+R1/R2)V_{REF}$

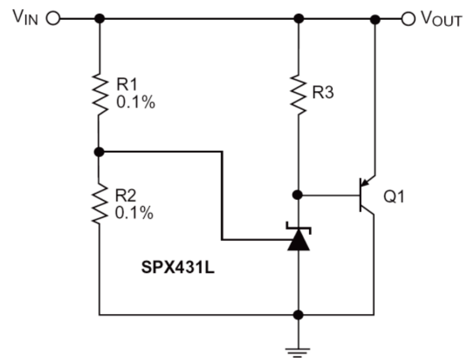


Fig. 122 High Current Shunt regulator
$V_{OUT} = (1+R1/R2)V_{REF}$

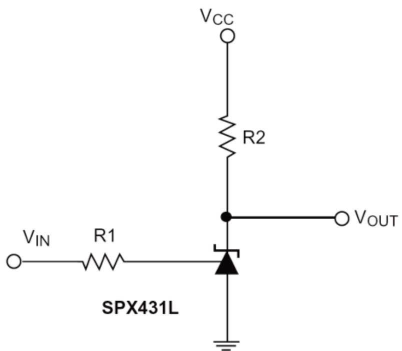
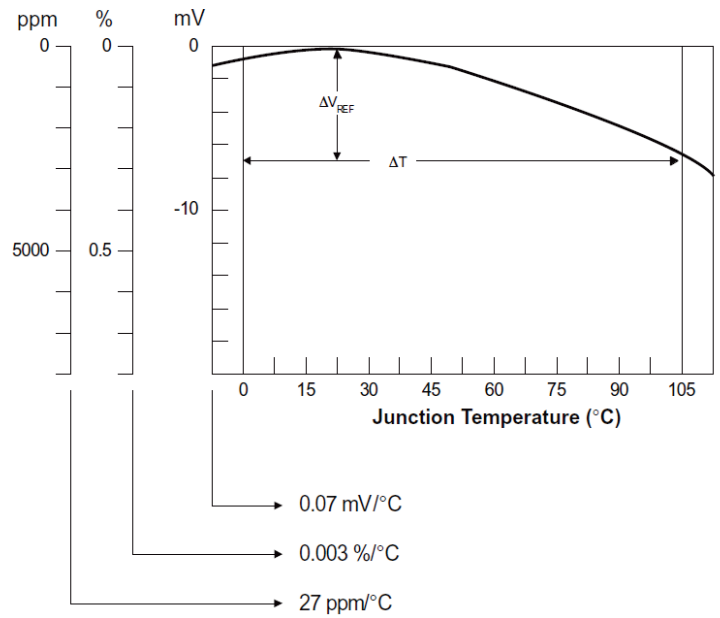


Fig. 133 Single Supply Comparator with Temperature Compensated Threshold. V_{IN} threshold = 2.5V.

APPLICATION INFORMATION

CALCULATING AVERAGE TEMPERATURE COEFFICIENT (TC)



- $$\text{TC in mV/°C} = \frac{\Delta V_{REF}\ (\text{mV})}{\Delta T_A}$$
- $$\text{TC in \%/°C} = \frac{\left(\dfrac{\Delta V_{REF}}{\Delta V_{REF}\ \text{at } 25°C}\right) \times 100}{\Delta T_A}$$
- $$\text{TC in ppm/°C} = \frac{\left(\dfrac{\Delta V_{REF}}{\Delta V_{REF}\ \text{at } 25°C}\right) \times 10^6}{\Delta T_A}$$

Fig. 24: V_{REF} VS Temperature.

TEST CIRCUITS

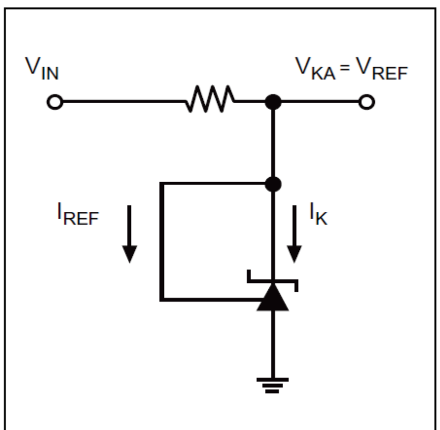


Fig. 25: Test Circuit for V_{KA} = V_{REF}

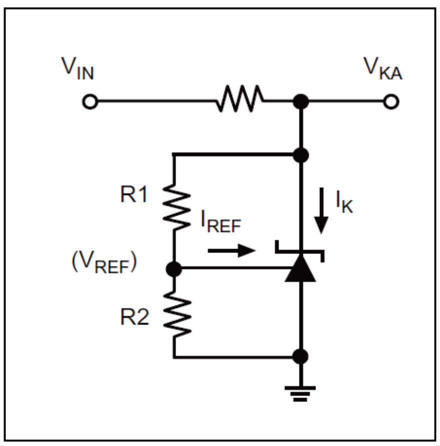


Fig. 26: Test Circuit for V_{KA} > V_{REF}

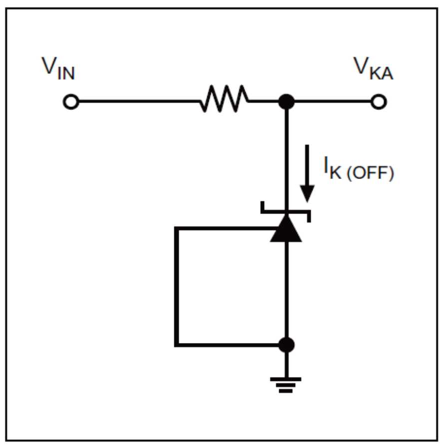
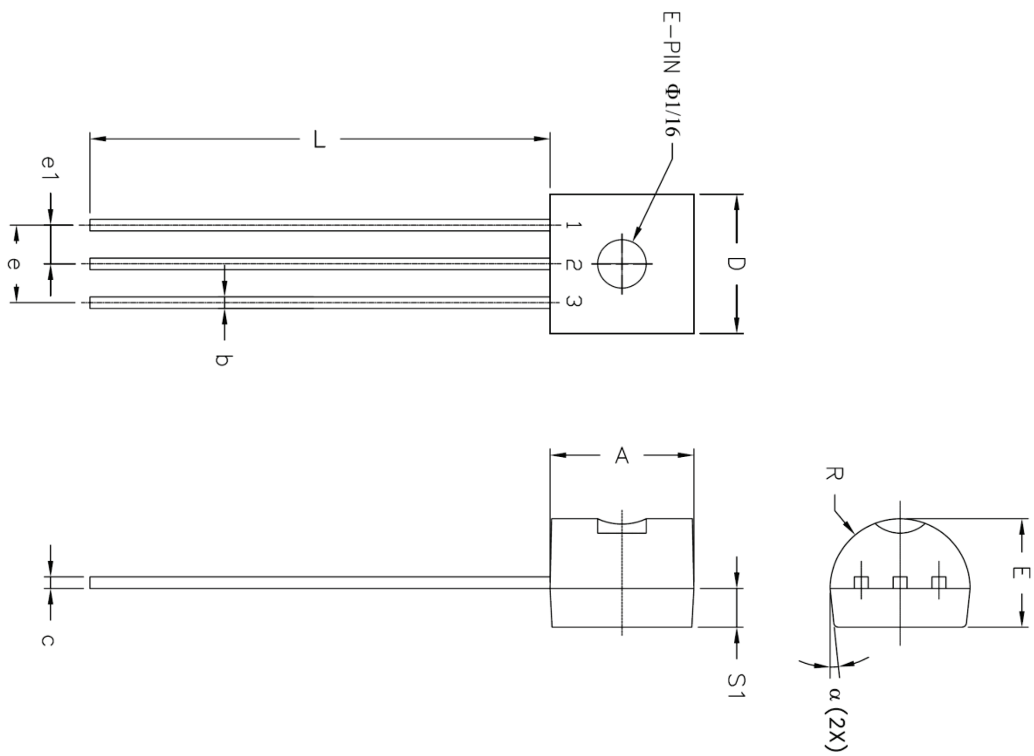


Fig. 27: Test Circuit for I_{KOFF}

PACKAGE SPECIFICATION | 3 PIN TO-92



3 Pin TO–92 (Option 1)* JEDEC TO–226–AA

SYMBOLS	DIMENSIONS IN INCH (Control Unit) MIN	MAX	DIMENSIONS IN MM (Reference Unit) MIN	MAX
A	0.170	0.210	4.32	5.33
b	0.014	0.020	0.36	0.51
c	0.016	0.022	0.41	0.55
D	0.175	0.205	4.45	5.20
E	0.125	0.165	3.18	4.19
e	0.095	0.105	2.42	2.66
e1	0.045	0.055	1.15	1.39
L	0.500	0.610	12.70	15.49
R	0.045	0.095	2.16	2.41
S1	0.045	0.060	1.14	1.52
α	4°	6°	4°	6°
N	3		3	

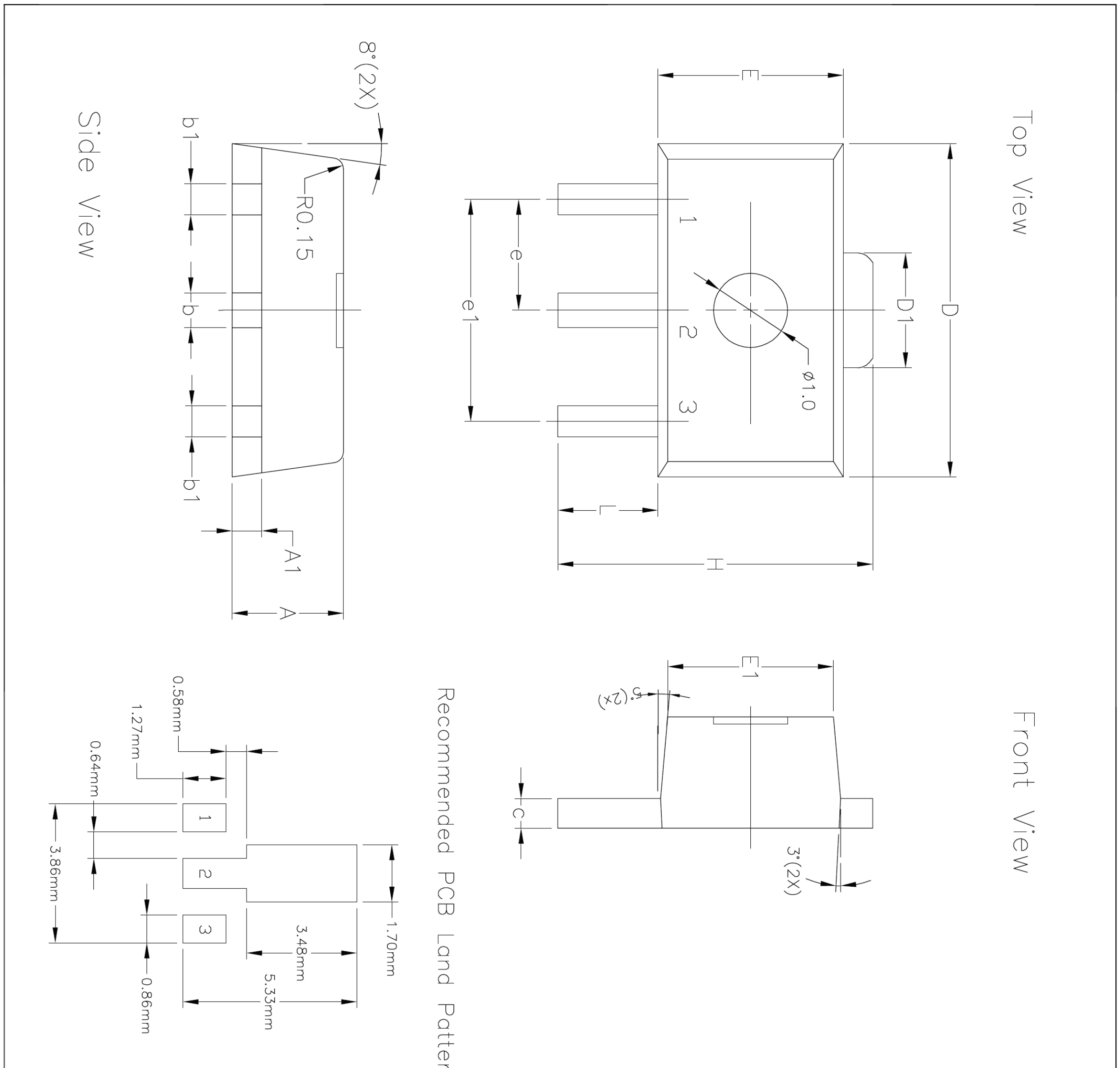
* Refer to product datasheet for POD option being used

REVISION HISTORY

REV.	DESCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	09/23/05	JL
B	DRAWING FORMAT MODIFICATION	08/15/06	JL
C	CHANGE DRAWING LOGO AND COMPANY NAME	11/28/07	JL

EXAR CORPORATION
3 PIN TO–92 PACKAGE OUTLINE
Packaging Approval: | Drawing No: 3–PIN TO–92
By: JL | Date: 11/28/07 | Revision: C | Sheet: 1 OF 2

PACKAGE SPECIFICATION — 3 PIN SOT-89



REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	02/02/06	JL
B	DRAWING FORMAT MODIFICATION	09/11/06	JL
C	CHANGE DRAWING LOGO AND COMPANY NAME	11/28/07	JL
D	ADD RECOMMENDED PCB LAND PATTERN	01/28/10	PC

3 Pin SOT–89 JEDEC TO–243 Variation AA

SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.40	1.50	1.60	0.055	0.059	0.063
A1	0.30	0.40	0.50	0.011	0.015	0.019
b	0.44	0.47	0.56	0.017	0.018	0.022
b1	0.36	0.42	0.48	0.014	0.016	0.019
c	0.35	0.40	0.44	0.014	0.015	0.017
D	4.40	4.50	4.60	0.173	0.177	0.181
D1	1.62	1.60	1.83	0.064	0.062	0.072
E	2.29	2.50	2.60	0.090	0.098	0.102
E1	2.13	—	2.29	0.084	—	0.090
e	1.50 BSC			0.059 BSC		
e1	3.00 BSC			0.118 BSC		
H	3.94	—	4.25	0.155	—	0.167
L	0.89	—	1.20	0.035	—	0.047
N	3			3		

EXAR CORPORATION

3 PIN SOT–89 PACKAGE OUTLINE

Packaging Approval:		Drawing No:	3–PIN SOT–89
By: PC	Date: 01/28/10	Revision: D	Sheet: 1 OF 1

REVSION HISTORY

Revision	Date	Description
2.0.0	06/12/2012	Reformatted Datasheet. Corrected Package Drawing
2.0.1	07/19/2013	Update package marking information and updated corporate logo.

FOR FURTHER ASSISTANCE

Email: customersupport@exar.com

Exar Technical Documentation: http://www.exar.com/TechDoc/default.aspx?

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