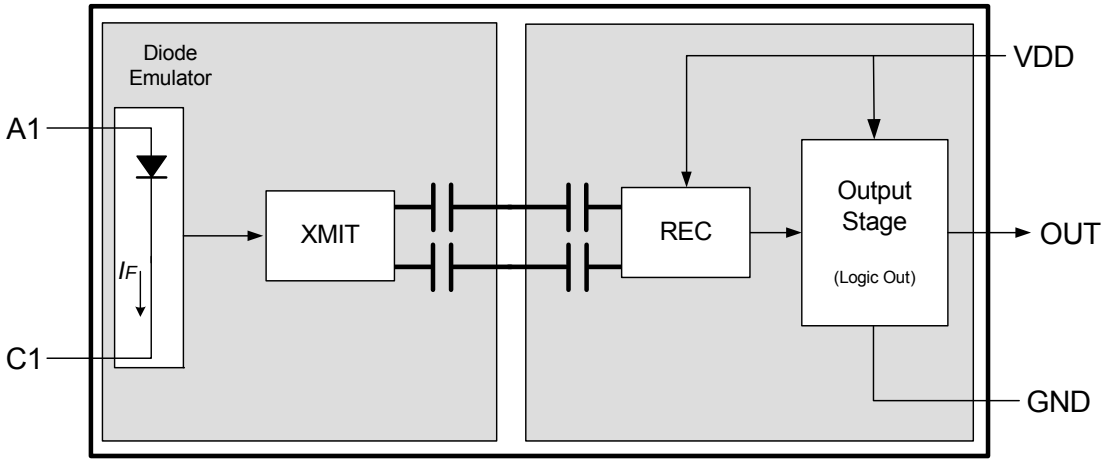
Functional Block Diagram



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Section **Page**

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
V_{DD} Supply Voltage	V_{DD}	2.5	—	5.5	V
Input Current	$I_{F(ON)}$ (See Figure 1)	6	—	30	mA
Operating Temperature (Ambient)	T_A	–40	—	125	°C

Table 2. Electrical Characteristics

V_{DD} = 5 V; GND = 0 V; T_A = –40 to +125 °C; typical specs at 25 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Parameters						
Supply Voltage	V_{DD}	(V_{DD}–GND)	2.5	—	5.5	V
Supply Current	I_{DD}	Output high or low (V_{DD} = 2.5 to 5.5 V)	—	1.5	—	mA
Input Current Threshold	$I_{F(TH)}$		—	—	3.6	mA
Input Current Hysteresis	I_{HYS}		—	0.34	—	mA
Input Forward Voltage (OFF)	$V_{F(OFF)}$	Measured at ANODE with respect to CATHODE.	—	—	1	V
Input Forward Voltage (ON)	$V_{F(ON)}$	Measured at ANODE with respect to CATHODE.	1.4	—	2.8	V
Input Capacitance	C_I	f = 100 kHz, V_F = 0 V, V_F = 2 V	 — —	 15 15	 — —	 pF pF
Logic Low Output Voltage	V_{OL}	I_{OL} = 4 mA	—	0.2	0.4	V
Logic High Output Voltage	V_{OH}	I_{OH} = –4 mA	V_{DD} - 0.4	V_{DD} - 0.2	—	V
Output Impedance	Z_O		—	50	—	Ω
Enable High Min	V_{EH}		V_{DD} - 0.4	—	—	V
Enable Low Max	V_{EL}		—	—	0.4	V
Enable High Current Draw	I_{EH}	V_{DD} = V_{EH} = 5 V	—	0	—	µA
Enable Low Current Draw	I_{EL}	V_{DD} = 5 V, V_{EL} = 0 V	—	–30	0	µA
UVLO Threshold +	VDD_{UV+}	See Figure 8 on page 16. V_{DD} rising	—	2.2	2.35	V
UVLO Threshold –	VDD_{UV-}	See Figure 8 on page 16. V_{DD} falling	—	2	2.25	V
UVLO lockout hysteresis	VDD_{HYS}		50	100	—	mV

Table 2. Electrical Characteristics (Continued)

V_{DD} = 5 V; GND = 0 V; T_A = –40 to +125 °C; typical specs at 25 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC Switching Parameters (V_{DD} = 5 V, C_L = 15 pF)						
Maximum Data Rate	F_{DATA}		DC	—	15	M_{BPS}
Minimum Pulse Width	MPW		66	—	—	ns
Propagation Delay (Low-to-High)	t_{PLH}	C_L = 15 pF	5	—	50	ns
Propagation Delay (High-to-Low)	t_{PHL}	C_L = 15 pF	5	—	50	ns
Pulse Width Distortion	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$	—	—	25	ns
Propagation Delay Skew	$t_{PSK(p-p)}$	$t_{PSK(P-P)}$ is the magnitude of the difference in prop delays between different units operating at same supply voltage, load, and ambient temp.	—	—	25	ns
Rise Time*	t_R	C_L = 15 pF	—	2.5	4	ns
Fall Time*	t_F	C_L = 15 pF	—	2.5	4	ns
Device Startup Time	t_{START}		—	—	40	µs
Common Mode Transient Immunity	CMTI	Output = low or high V_{CM} = 1500 V (See Figure 2) I_F = 6 mA	35	50	—	kV/µs

***Note:** Guaranteed by design and/or characterization

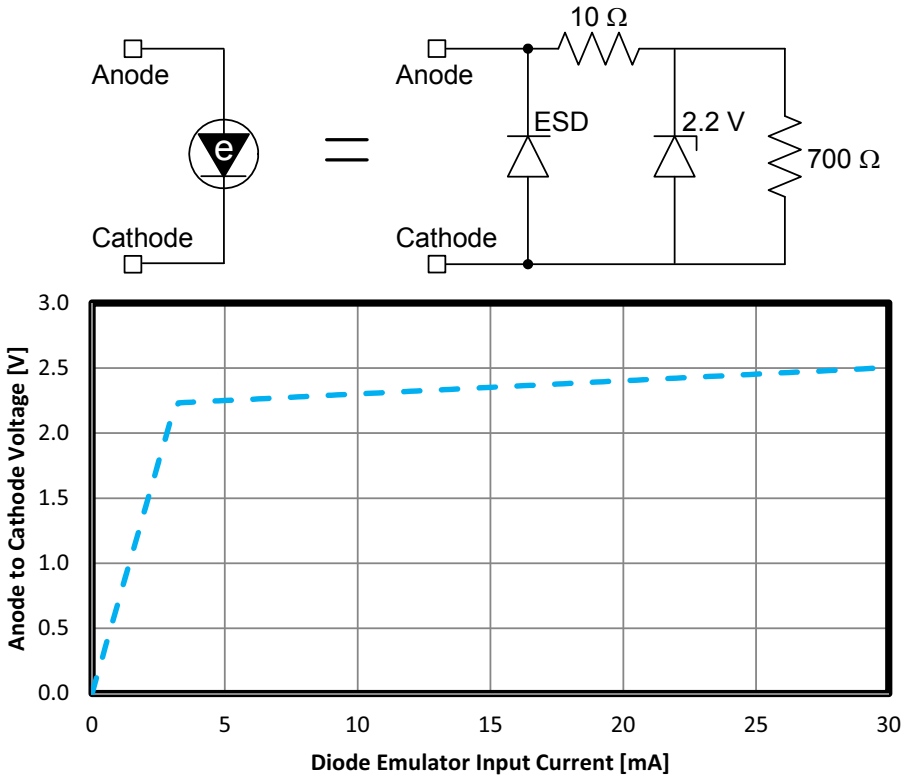


Figure 1. Diode Emulator Model and I-V Curve

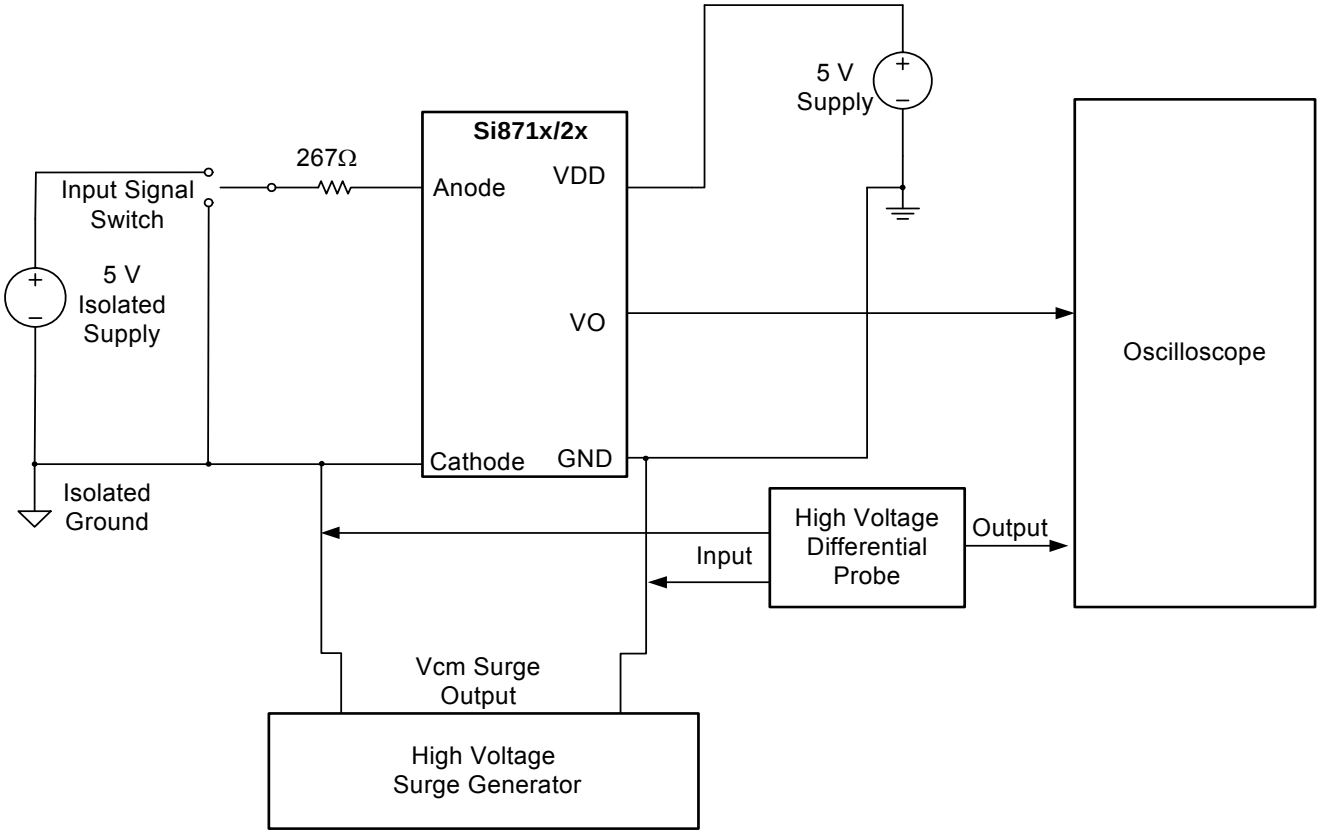


Figure 2. Common Mode Transient Immunity Characterization Circuit

Table 3. Regulatory Information*

CSA
The Si871x/2x is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873.
61010-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 600 V_{RMS} basic insulation working voltage.
60950-1: Up to 1000 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
60601-1: Up to 250 V_{RMS} reinforced insulation working voltage; up to 500 V_{RMS} basic insulation working voltage.
VDE
The Si871x/2x is certified according to IEC60747 and VDE0884. For more details, see File 5006301-4880-0001.
60747-5-2: Up to 1414 V_{peak} for basic insulation working voltage.
VDE0884-10: Up to 1414 V_{peak} for reinforced insulation working voltage.
UL
The Si871x/2x is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 5000 V_{RMS} isolation voltage for basic protection.
CQC
The Si871x/2x is certified under GB4943.1-2011. For more details, see File V2012CQC001041.
Rated up to 1000 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
***Note:** Regulatory Certifications apply to 3.75 kV_{RMS} rated devices which are production tested to 4.5 kV_{RMS} for 1 sec. Regulatory Certifications apply to 5.0 kV_{RMS} rated devices which are production tested to 6.0 kV_{RMS} for 1 sec. For more information, see "8.Ordering Guide" on page 22.

Table 4. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value			Unit
			SOIC-8	DIP8	SDIP6	
Nominal Air Gap (Clearance)	L(IO1)		4.7 min	7.2 min	9.6 min	mm
Nominal External Tracking (Creepage)	L(IO2)		3.9 min	7.0 min	8.3 min	mm
Minimum Internal Gap (Internal Clearance)			0.016	0.016	0.016	mm
Tracking Resistance (Proof Tracking Index)	PTI	IEC60112	600	600	600	V
Erosion Depth	ED		0.031	0.031	0.057	mm
Resistance (Input-Output)*	R_{IO}		10^{12}	10^{12}	10^{12}	Ω
Capacitance (Input-Output)*	C_{IO}	f = 1 MHz	1	1	1	pF
***Note:** To determine resistance and capacitance, the Si871x/2x is converted into a 2-terminal device. Pins 1–4 (1–3, SDIP6) are shorted together to form the first terminal, and pins 5–8 (4–6, SDIP6) are shorted together to form the second terminal. The parameters are then measured between these two terminals.						

Table 5. IEC 60664-1 (VDE 0884) Ratings

Parameter	Test Condition	Specification		
		SOIC-8	DIP8	SDIP6
Basic Isolation Group	Material Group	I	I	I
Installation Classification	Rated Mains Voltages ≤ 150 V_{RMS}	I-IV	I-IV	I-IV
	Rated Mains Voltages ≤ 300 V_{RMS}	I-IV	I-IV	I-IV
	Rated Mains Voltages ≤ 450 V_{RMS}	I-III	I-III	I-IV
	Rated Mains Voltages ≤ 600 V_{RMS}	I-III	I-III	I-IV
	Rated Mains Voltages ≤ 1000 V_{RMS}	I-II	I-II	I-III

Table 6. IEC 60747-5-2 (VDE 0884-10) Insulation Characteristics*

Parameter	Symbol	Test Condition	Characteristic			Unit
			SOIC-8	DIP8	SDIP6	
Maximum Working Insulation Voltage	V_{IORM}		630	891	1140	V peak
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	1181	1671	2138	V peak
Transient Overvoltage	V_{IOTM}	t = 60 sec	6000	6000	8000	V peak
Pollution Degree (DIN VDE 0110, Table 1)			2	2	2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		>10^9	>10^9	>10^9	Ω

***Note:** This isolator is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The Si871x/2x provides a climate classification of 40/125/21.

Table 7. IEC Safety Limiting Values

Parameter	Symbol	Test Condition	Max			Unit
			SOIC-8	DIP8	SDIP6	
Case Temperature	T_S		140	140	140	°C
Input Current	I_S	θ_{JA} = 110 °C/W (SOIC-8), 110 °C/W (DIP8), 105 °C/W (SDIP6), V_F = 2.8 V, T_J = 140 °C, T_A = 25 °C	370	370	390	mA
Output Power	P_S		1	1	1	W
Note: Maximum value allowed in the event of a failure; also see the thermal derating curve in Figures 3, 4,and 5.						

Table 8. Thermal Characteristics

Parameter	Symbol	Typ			Unit
		SOIC-8	DIP8	SDIP6	
IC Junction-to-Air Thermal Resistance	θ_{JA}	110	110	105	°C/W

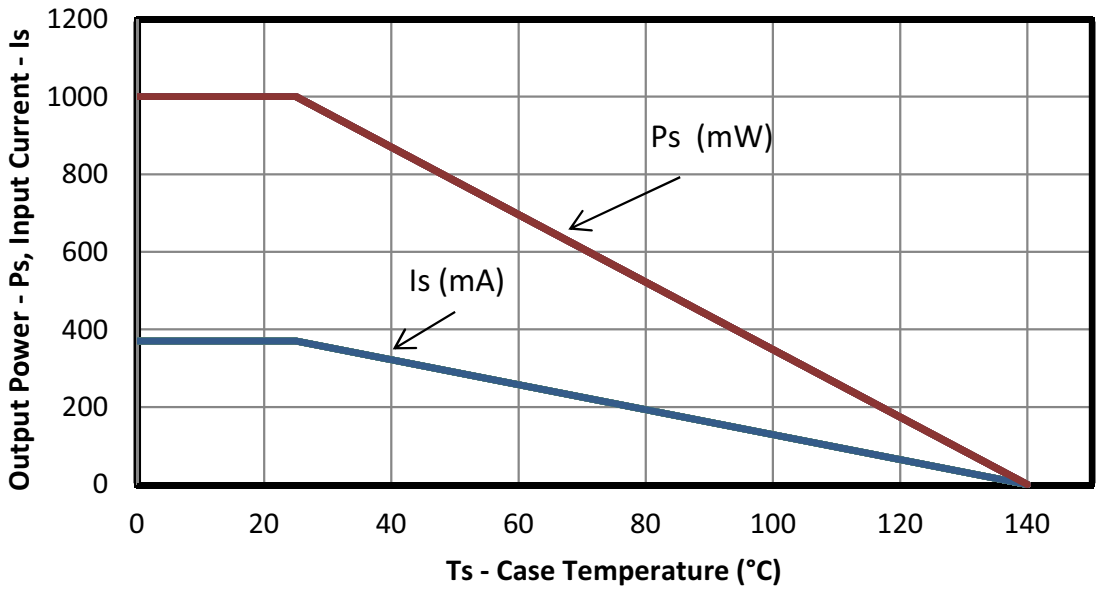


Figure 3. (SOIC-8) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2 and VDE0884-10

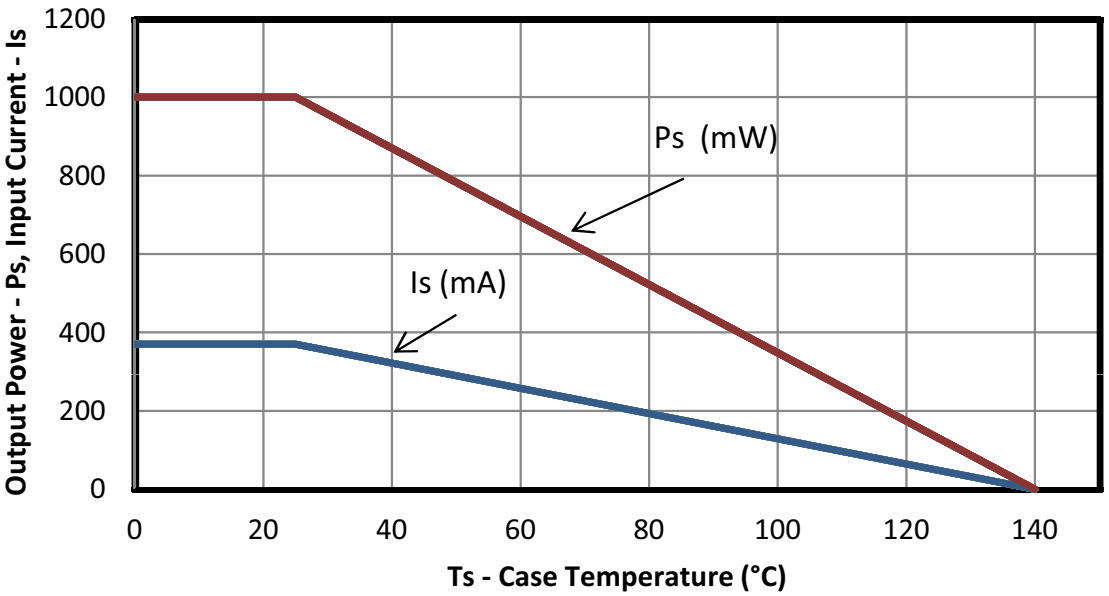


Figure 4. (DIP8) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2 and VDE0884-10

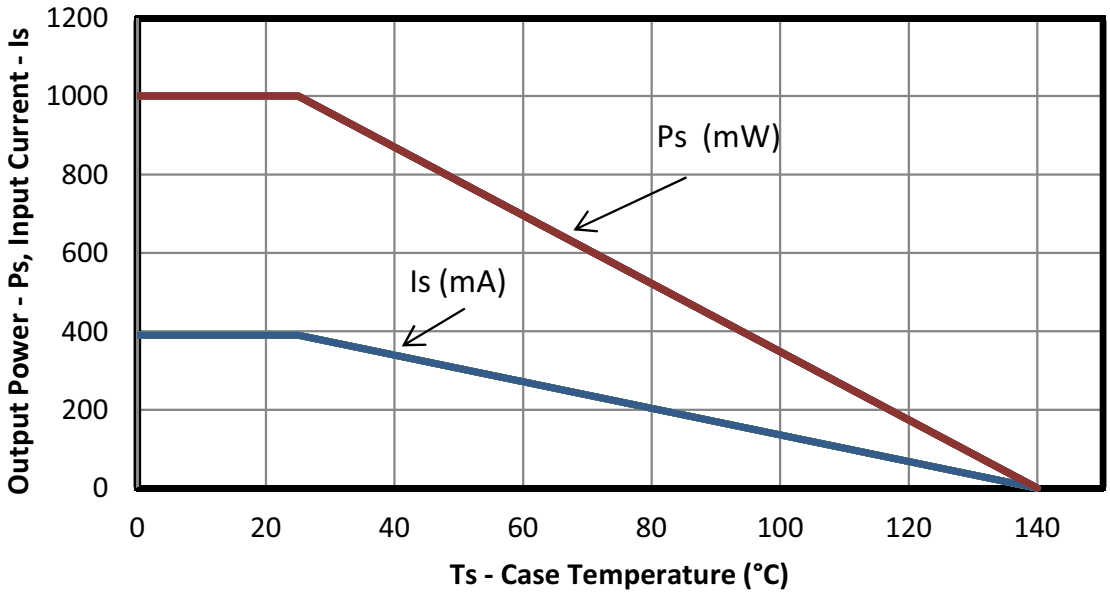


Figure 5. (SDIP6) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2 and VDE0884-10

Table 9. Absolute Maximum Ratings*

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{STG}	–65	+150	°C
Operating Temperature	T_A	–40	+125	°C
Junction Temperature	T_J	—	+140	°C
Average Forward Input Current	$I_{F(AVG)}$	—	30	mA
Peak Transient Input Current (< 1 µs pulse width, 300 pps)	I_{FTR}	—	1	A
Reverse Input Voltage	V_R	—	0.3	V
Supply Voltage	V_{DD}	–0.5	7	V
Output Voltage	V_{OUT}	–0.5	V_{DD}+0.5	V
Enable Voltage	V_{EOUT}	–0.5	V_{DD}+0.5	V
Output Source or Sink Current	I_O	—	22	mA
Input Power Dissipation	P_I	—	90	mW
Output Power Dissipation	P_O	—	163	mW
Total Power Dissipation	P_T	—	253	mW
Lead Solder Temperature (10 s)		—	260	°C
HBM Rating ESD		3	—	kV
Machine Model ESD		250	—	V
CDM		2	—	kV
Maximum Isolation Voltage (1 s) SOIC-8		—	4500	V_{RMS}
Maximum Isolation Voltage (1 s) DIP8		—	4500	V_{RMS}
Maximum Isolation Voltage (1 s) SDIP6		—	6500	V_{RMS}

***Note:** Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions specified in the operational sections of this data sheet.

2. Application Information

2.1. Theory of Operation

The Si871x/2x are pin-compatible, single-channel, drop-in replacements for popular optocouplers with data rates up to 15 Mbps. The operation of an Si871x/2x channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for the Si871x/2x is shown in Figure 6.

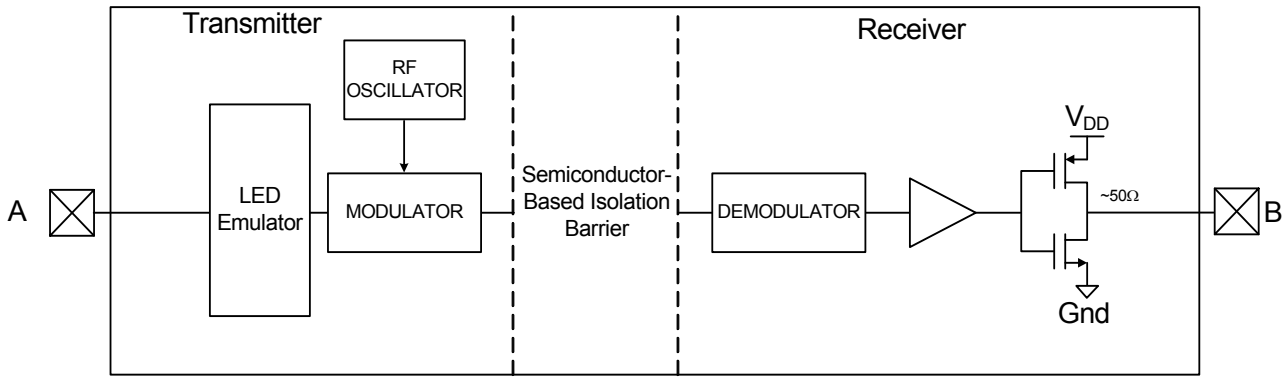


Figure 6. Simplified Channel Diagram

3. Technical Description

3.1. Device Behavior

Truth tables for the Si871x/2x are summarized in Table 10.

Table 10. Si871x/2x Truth Table Summary*

Input	Enable	Output
Si8715 (Non-inverting)		
OFF	N/A	LOW
ON	N/A	HIGH
Si8716 (Inverting)		
OFF	HIGH	HIGH
ON	HIGH	LOW
X	LOW	HIGH
Si8717 (Non-inverting)		
OFF	HIGH	LOW
ON	HIGH	HIGH
X	LOW	HI-Z
Si8718 (Inverting)		
OFF	HIGH	HIGH
ON	HIGH	LOW
X	LOW	HI-Z
Si8719 (Inverting)		
OFF	N/A	HIGH
ON	N/A	LOW
Si8720 (Inverting)		
OFF	HIGH	HIGH
ON	HIGH	LOW
X	LOW	LOW

***Note:** This truth table assumes VDD is powered (VDD> UVLO). If VDD is below UVLO, see "3.3.Under Voltage Lockout (UVLO)" on page 16 for more information. When VDD < UVLO, the output state is not guaranteed. In this condition, the output level is determined by external circuity connected to the output.

3.2. Device Startup

During startup-up, for the Si8716, Output V_O is high until V_{DD} rises above the UVLO+ threshold for a minimum time period of t_{START}. Following this, the output is low when the current flowing from anode to cathode is > $I_{F(ON)}$. Device startup, normal operation, and shutdown behavior for the Si8716 is shown in Figure 7. Note that Figure 7 assumes that Enable is asserted and that the outputs are operating in their normal operating condition (inverting for the Si8716). See Table 10 for more details on the Enable function.

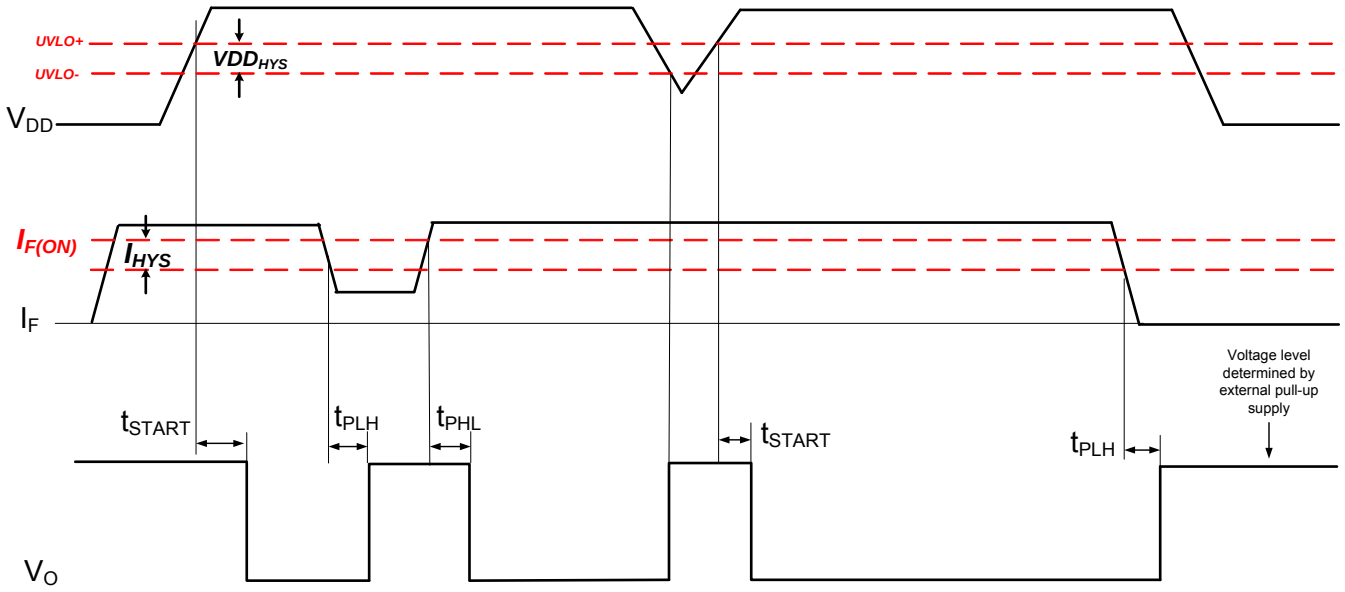


Figure 7. Si8716 Operating Behavior ($I_F \geq I_{F(MIN)}$ when $V_F \geq V_{F(MIN)}$)

3.3. Under Voltage Lockout (UVLO)

The UVLO circuit unconditionally drives V_O to its default state when V_{DD} is below the lockout threshold. Referring to Figure 8, upon power up, the Si871x/2x is maintained in UVLO until VDD rises above VDD_{UV+}. During power down, the Si871x/2x enters UVLO when VDD falls below the UVLO threshold plus hysteresis (i.e., VDD $\leq$ VDD_{UV+} – VDD_{HYS}).

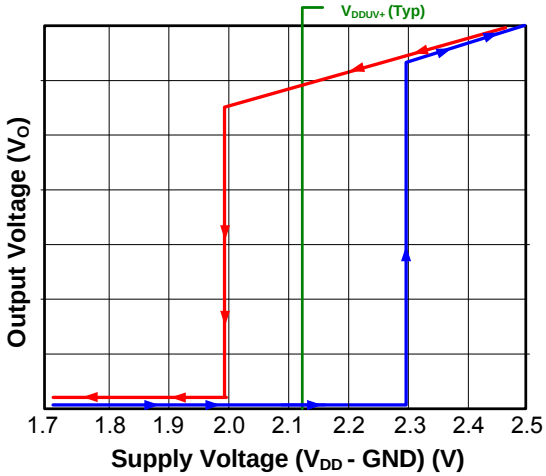


Figure 8. Si871x/2x UVLO Response

4. Applications

The following sections detail the input and output circuits necessary for proper operation of the Si871x/2x family.

4.1. Input Circuit Design

Opto coupler manufacturers typically recommend the circuits shown in Figures 9 and 10. These circuits are specifically designed to improve opto-coupler input common-mode rejection and increase noise immunity.

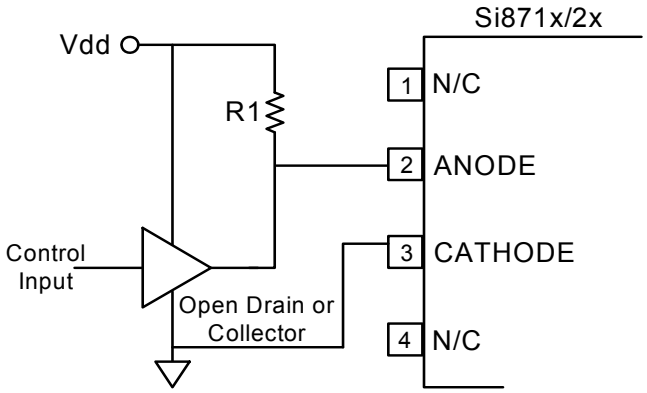


Figure 9. Si871x/2x Input Circuit

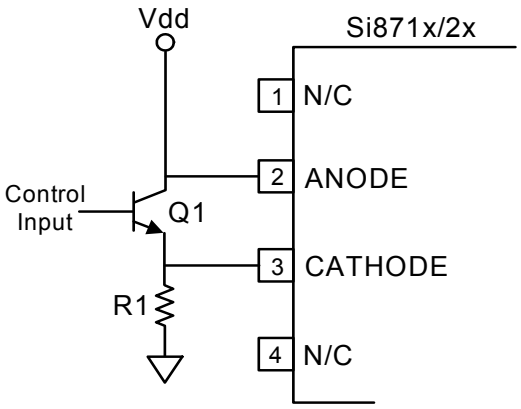


Figure 10. High CMR Si871x/2x Input Circuit

The optically-coupled circuit of Figure 9 turns the LED on when the control input is high. However, internal capacitive coupling from the LED to the power and ground conductors can momentarily force the LED into its off state when the anode and cathode inputs are subjected to a high common-mode transient. The circuit shown in Figure 10 addresses this issue by using a value of R1 sufficiently low to overdrive the LED, ensuring it remains on during an input common-mode transient. Q1 shorts the LED off in the low output state, again increasing common-mode transient immunity.

Some opto coupler applications recommend reverse-biasing the LED when the control input is off to prevent coupled noise from energizing the LED. The Si871x/2x input circuit requires less current and has twice the off-state noise margin compared to opto couplers. However, high CMR opto coupler designs that overdrive the LED (see Figure 10) may require increasing the value of R1 to limit input current I_F to its maximum rating when using the Si871x/2x. In addition, there is no benefit in driving the Si871x/2x input diode into reverse bias when in the off state. Consequently, opto coupler circuits using this technique should either leave the negative bias circuitry unpopulated or modify the circuitry (e.g., add a clamp diode or current limiting resistor) to ensure that the anode pin of the Si871x/2x is no more than –0.3 V with respect to the cathode when reverse-biased.

New designs should consider the input circuit configurations of Figure 11, which are more efficient than those of Figures 9 and 10. As shown, S1 and S2 represent any suitable switch, such as a BJT or MOSFET, analog transmission gate, processor I/O, etc. Also, note that the Si871x/2x input can be driven from the I/O port of any MCU or FPGA capable of sourcing a minimum of 6 mA (see Figure 11B). Additionally, note that the Si871x/2x propagation delay and output drive do not significantly change for values of I_F between $I_{F(MIN)}$ and $I_{F(MAX)}$.

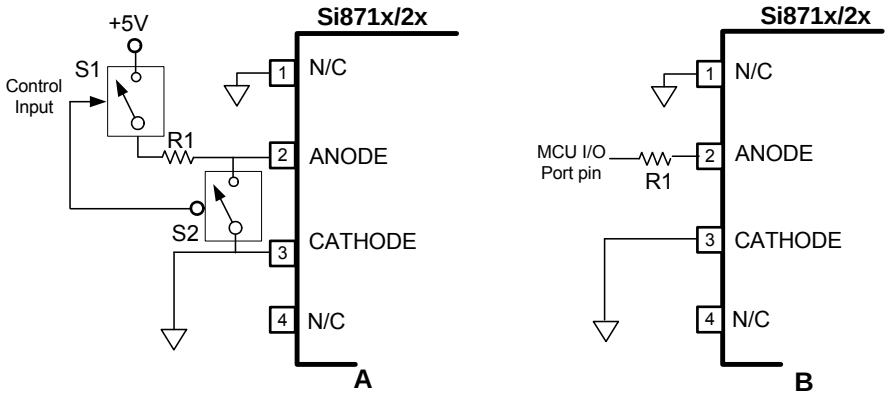
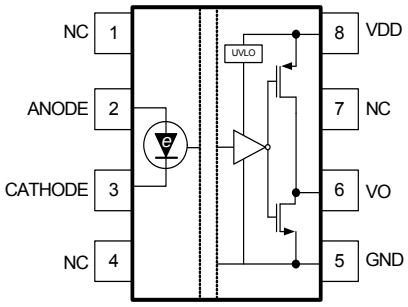


Figure 11. Si871x/2x Other Input Circuit Configurations

4.2. Output Circuit Design and Power Supply Connections

GND can be biased at, above, or below ground as long as the voltage on V_{DD} with respect to GND is a maximum of 5.5 V. V_{DD} decoupling capacitors should be placed as close to the package pins as possible. The optimum values for these capacitors depend on load current and the distance between the chip and its power source. It is recommended that 0.1 and 1 µF bypass capacitors be used to reduce high-frequency noise and maximize performance. Opto replacement applications should limit their supply voltages to 5.5 V or less.

5. Pin Descriptions (SOIC-8, DIP8)



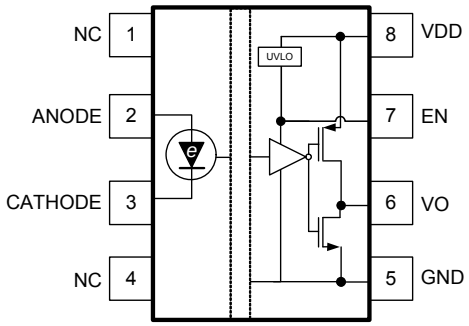
SOIC-8, DIP8
Industry Standard Pinout

Figure 12. Pin Configuration

Table 11. Pin Descriptions (SOIC-8, DIP8)

Pin	Name	Description
1	NC*	No connect.
2	ANODE	Anode of LED emulator. V_O follows the signal applied to this input with respect to the CATHODE input.
3	CATHODE	Cathode of LED emulator. V_O follows the signal applied to ANODE with respect to this input.
4	NC*	No connect.
5	GND	Ground reference for V_{DD}. This terminal is typically connected to ground but may be tied to a negative or positive voltage.
6	V_O	Output signal.
7	NC*	No connect.
8	V_{DD}	Output-side power supply input referenced to GND (5.5 V max).
***Note:** No Connect. These pins are not internally connected. To maximize CMTI performance, these pins should be connected to the ground plane.		

6. Pin Descriptions (SOIC-8, DIP8) with Output Enable



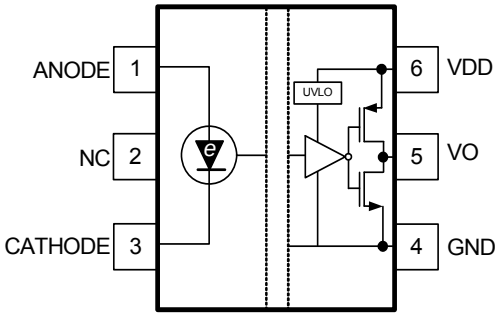
SOIC-8, DIP8 with Output Enable
Industry Standard Pinout

Figure 13. Pin Configuration

Table 12. Pin Descriptions (SOIC-8, DIP8) with Output Enable

Pin	Name	Description
1	NC*	No connect.
2	ANODE	Anode of LED emulator. V_O follows the signal applied to this input with respect to the CATHODE input.
3	CATHODE	Cathode of LED emulator. V_O follows the signal applied to ANODE with respect to this input.
4	NC*	No connect.
5	GND	Ground reference for V_{DD}. This terminal is typically connected to ground but may be tied to a negative or positive voltage.
6	V_O	Output signal.
7	EN	Output enable. Tied to V_{DD} to enable output.
8	V_{DD}	Output-side power supply input referenced to GND (5.5 V max).
***Note:** No Connect. These pins are not internally connected. To maximize CMTI performance, these pins should be connected to the ground plane.		

7. Pin Descriptions (SDIP6)



SDIP6
Industry Standard Pinout

Figure 14. Pin Configuration

Table 13. Pin Descriptions (SDIP6)

Pin	Name	Description
1	ANODE	Anode of LED emulator. V_O follows the signal applied to this input with respect to the CATHODE input.
2	NC*	No connect.
3	CATHODE	Cathode of LED emulator. V_O follows the signal applied to ANODE with respect to this input.
4	GND	Ground reference for V_{DD}. This terminal is typically connected to ground but may be tied to a negative or positive voltage.
5	V_O	Output signal.
6	V_{DD}	Output-side power supply input referenced to GND (5.5 V max).
***Note:** No Connect. These pins are not internally connected. To maximize CMTI performance, these pins should be connected to the ground plane.		

8. Ordering Guide

Table 14. Si871x/2x Ordering Guide[1,2,3]

Ordering Part Number (OPN)	Ordering Options				
	Input/Output Configuration	Data Rate Cross Reference	Insulation Rating	Enable Pin/ Output State when Active	Pkg Type
Logic Output (Available in SOIC-8, DIP8, and SDIP6)					
Si8715BC-A-IS	High CMTI Non-inverting Output	15 Mbps	3.75 kVrms	No, N/A	SOIC-8
Si8716BC-A-IS	High CMTI Inverting Output	15 Mbps ACPL-061L, HCPL-0600, HCPL-0601, HCPL-0611	3.75 kVrms	Yes, High	SOIC-8
Si8717BC-A-IS	High CMTI Non-inverting Output	15 Mbps	3.75 kVrms	Yes, Hi-z	SOIC-8
Si8718BC-A-IS	High CMTI Inverting Output	15 Mbps ACPL-C61L, ACPL-W70L	3.75 kVrms	Yes, Hi-z	SOIC-8
Si8719BC-A-IS	High CMTI Inverting Output	15 Mbps	3.75 kVrms	No, N/A	SOIC-8
Si8720BC-A-IS	High CMTI Inverting Output	15 Mbps	3.75 kVrms	Yes, Low	SOIC-8
Si8715BC-A-IP	High CMTI Non-inverting Output	15 Mbps ACPL-4800, HCPL-2202, HCPL-2212	3.75 kVrms	No, N/A	DIP8/GW
Si8716BC-A-IP	High CMTI Inverting Output	15 Mbps 6N137, HCPL-2601, HCPL-2611	3.75 kVrms	Yes, High	DIP8/GW
Si8717BC-A-IP	High CMTI Non-inverting Output	15 Mbps	3.75 kVrms	Yes, Hi-z	DIP8/GW
Si8718BC-A-IP	High CMTI Inverting Output	15 Mbps	3.75 kVrms	Yes, Hi-z	DIP8/GW
Si8719BC-A-IP	High CMTI Inverting Output	15 Mbps	3.75 kVrms	No, N/A	DIP8/GW
Si8720BC-A-IP	High CMTI Inverting Output	15 Mbps	3.75 kVrms	Yes, Low	DIP8/GW

Notes:
1. All packages are RoHS-compliant with peak solder reflow temperatures of 260 °C according to the JEDEC industry standard classifications.
2. “Si” and “SI” are used interchangeably.
3. AEC-Q100 qualified.

Table 14. Si871x/2x Ordering Guide[1,2,3] (Continued)

Ordering Part Number (OPN)	Ordering Options				
	Input/Output Configuration	Data Rate Cross Reference	Insulation Rating	Enable Pin/ Output State when Active	Pkg Type
Si8715BD-A-IS	High CMTI Non-inverting Output	15 Mbps ACPL-W21L, PS9303L2	5.0 kVrms	No, N/A	SDIP6
Si8719BD-A-IS	High CMTI Inverting Output	15 Mbps ACPL-W61L, ACPL-W481, ACPL-W70L, TLP2766F	5.0 kVrms	No, N/A	SDIP6

Notes:
1. All packages are RoHS-compliant with peak solder reflow temperatures of 260 °C according to the JEDEC industry standard classifications.
2. “Si” and “SI” are used interchangeably.
3. AEC-Q100 qualified.

8.1. Automotive Grade OPNs

Automotive-grade devices are built using automotive-specific flows at all steps in the manufacturing process to ensure robustness and low defectivity. These devices are supported with AIAG-compliant Production Part Approval Process (PPAP) documentation, and feature International Material Data System (IMDS) and China Automotive Material Data System (CAMDS) listing. Qualifications are compliant with AEC-Q100, and a zero-defect methodology is maintained throughout definition, design, evaluation, qualification, and mass production steps.

Table 15. Si87xx Ordering Guide[1,2,3]

Ordering Part Number (OPN)	Ordering Options				
	Input/Output Configuration	Data Rate Cross Reference	Insulation Rating	Enable Pin/Ouptut State when Active	Pkg Type
Si8716BC-AP	High CMTI Inverting Output	15 Mbps 6N137, HCPL-2601, HCPL-2611	3.75 kVrms	Yes, High	DIP8/GW

Notes:
1. All packages are RoHS-compliant.
2. “Si” and “SI” are used interchangeably.
3. An "R" at the end of the part number denotes tape and reel packaging option.
4. Automotive-Grade devices (with an "–A" suffix) are identical in construction materials, topside marking, and electrical parameters to their Industrial-Grade (with a "–I" suffix) version counterparts. Automotive-Grade products are produced utilizing full automotive process flows and additional statistical process controls throughout the manufacturing flow. The Automotive-Grade part number is included on shipping labels.
5. Additional Ordering Part Numbers may be available in Automotive-Grade. Please contact your local Silicon Labs sales representative for further information.

9. Package Outline: 8-Pin Narrow Body SOIC

Figure 15 illustrates the package details for the Si871x/2x in an 8-pin narrow-body SOIC package. Table 16 lists the values for the dimensions shown in the illustration.

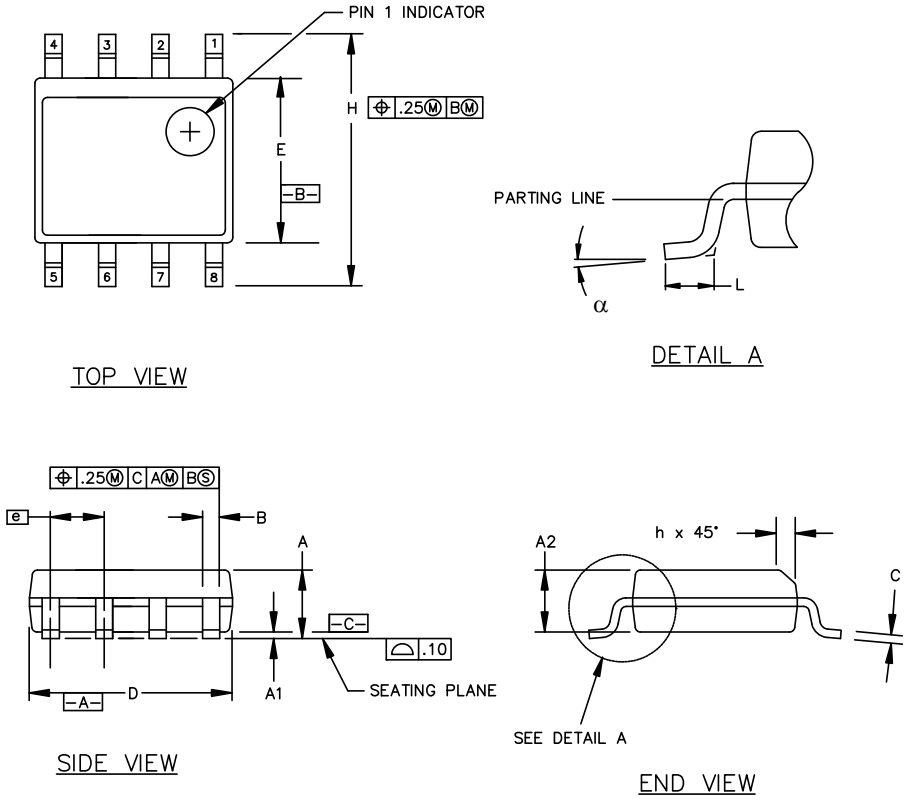


Figure 15. 8-Pin Narrow Body SOIC Package

Table 16. 8-Pin Narrow Body SOIC Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	1.35	1.75
A1	0.10	0.25
A2	1.40 REF	1.55 REF
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
∝	0°	8°

10. Land Pattern: 8-Pin Narrow Body SOIC

Figure 16 illustrates the recommended land pattern details for the Si871x/2x in an 8-pin narrow-body SOIC. Table 17 lists the values for the dimensions shown in the illustration.

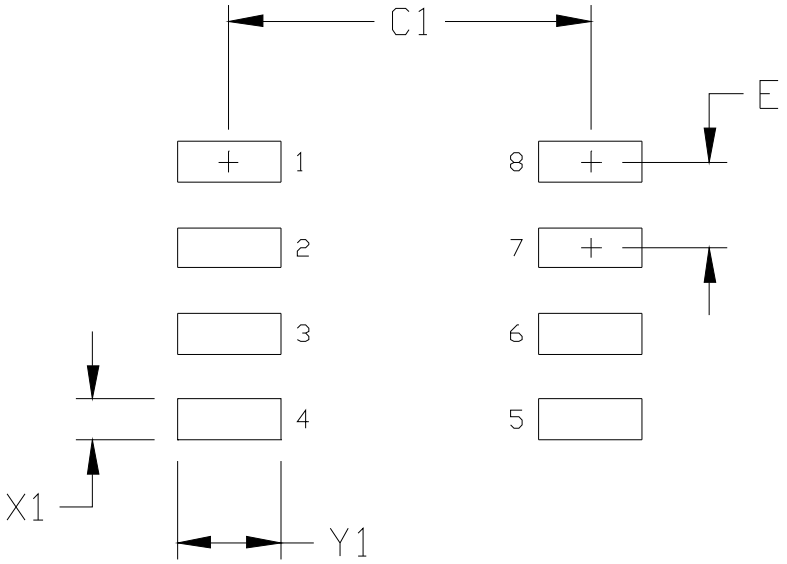


Figure 16. 8-Pin Narrow Body SOIC Land Pattern

Table 17. 8-Pin Narrow Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Notes:
1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

11. Package Outline: DIP8

Figure 17 illustrates the package details for the Si871x/2x in a DIP8 package. Table 18 lists the values for the dimensions shown in the illustration.

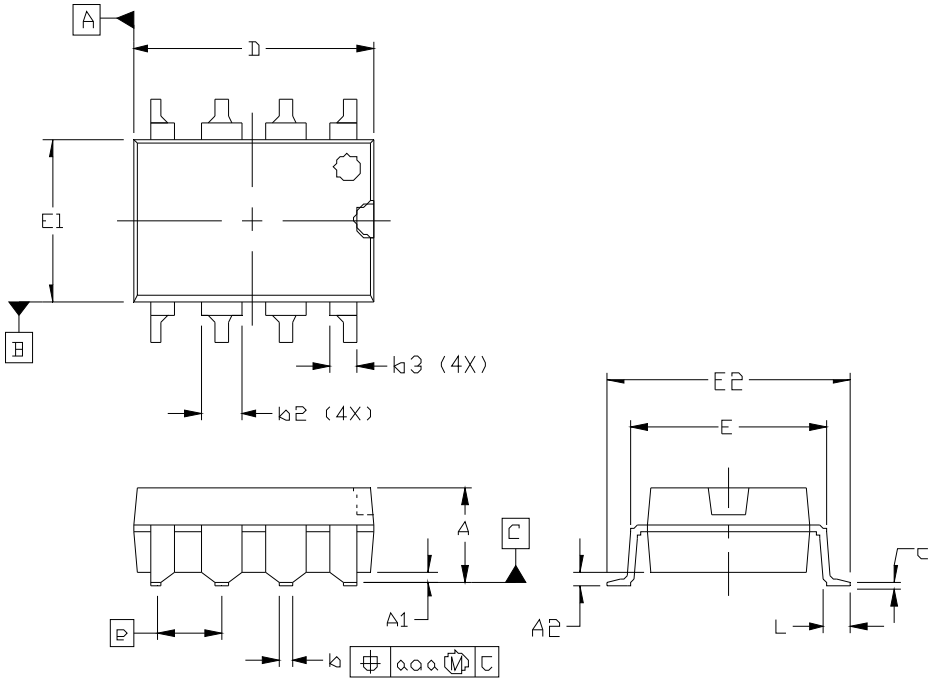


Figure 17. DIP8 Package

Table 18. DIP8 Package Diagram Dimensions

Dimension	Min	Max
A	—	4.19
A1	0.55	0.75
A2	3.17	3.43
b	0.35	0.55
b2	1.14	1.78
b3	0.76	1.14
c	0.20	0.33
D	9.40	9.90
E	7.37	7.87
E1	6.10	6.60
E2	9.40	9.90
e	2.54 BSC.	
L	0.38	0.89
aaa	—	0.25

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

12. Land Pattern: DIP8

Figure 18 illustrates the recommended land pattern details for the Si871x/2x in a DIP8 package. Table 19 lists the values for the dimensions shown in the illustration.

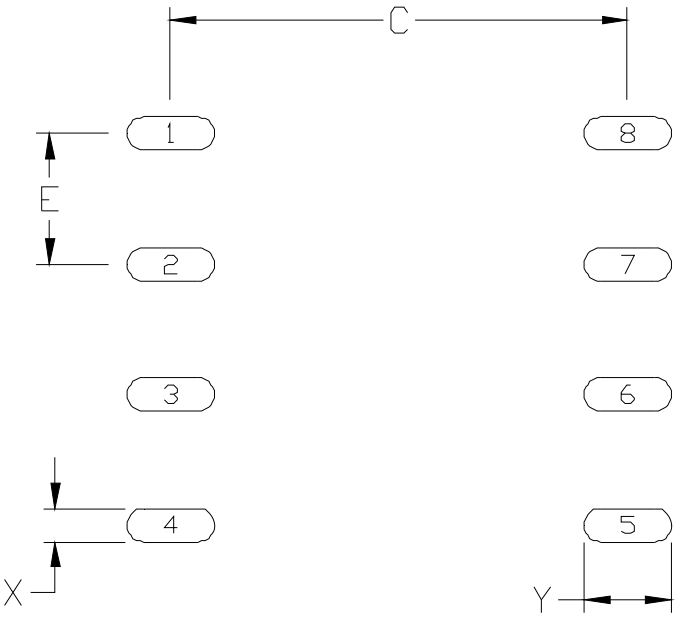


Figure 18. DIP8 Land Pattern

Table 19. DIP8 Land Pattern Dimensions*

Dimension	Min	Max
C	8.85	8.90
E	2.54 BSC	
X	0.60	0.65
Y	1.65	1.70
***Note:** This Land Pattern Design is based on the IPC-7351 specification.		

13. Package Outline: SDIP6

Figure 19 illustrates the package details for the Si871x/2x in an SDIP6 package. Table 20 lists the values for the dimensions shown in the illustration.

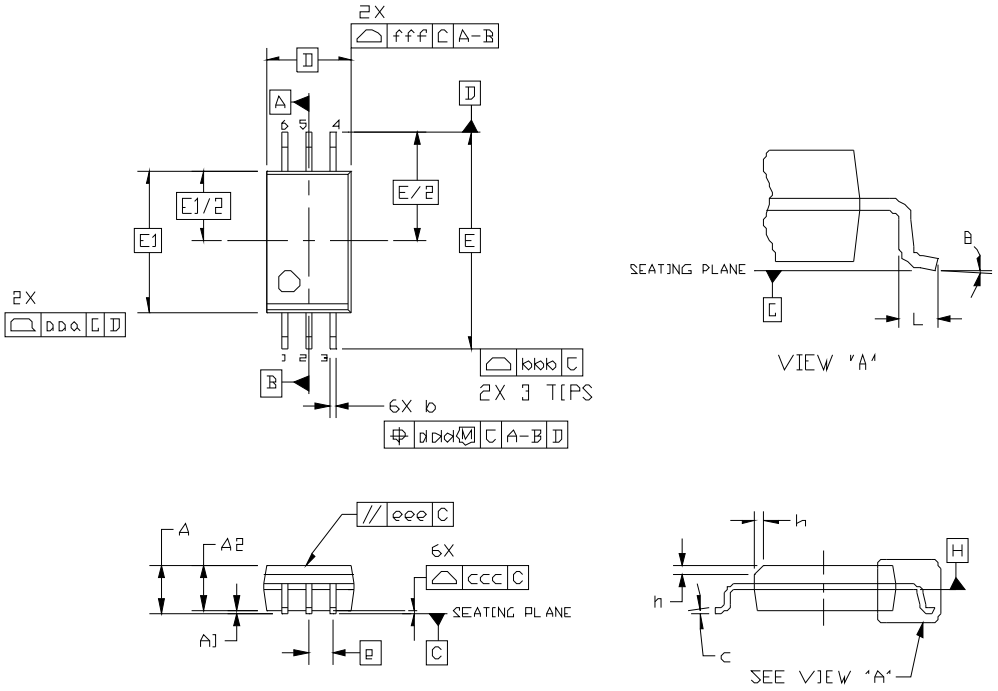


Figure 19. SDIP6 Package

Table 20. SDIP6 Package Diagram Dimensions

Dimension	Min	Max
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.31	0.51
c	0.20	0.33
D	4.58 BSC	
E	11.50 BSC	
E1	7.50 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.75

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

Table 20. SDIP6 Package Diagram Dimensions (Continued)

Dimension	Min	Max
θ	0°	8°
aaa	—	0.10
bbb	—	0.33
ccc	—	0.10
ddd	—	0.25
eee	—	0.10
fff	—	0.20

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

14. Land Pattern: SDIP6

Figure 20 illustrates the recommended land pattern details for the Si871x/2x in an SDIP6 package. Table 21 lists the values for the dimensions shown in the illustration.

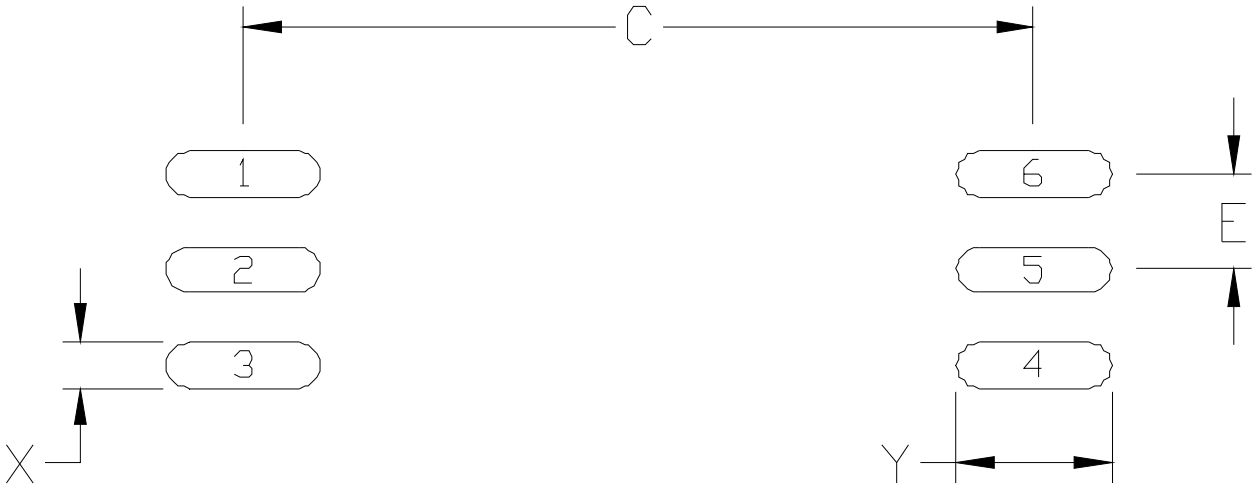


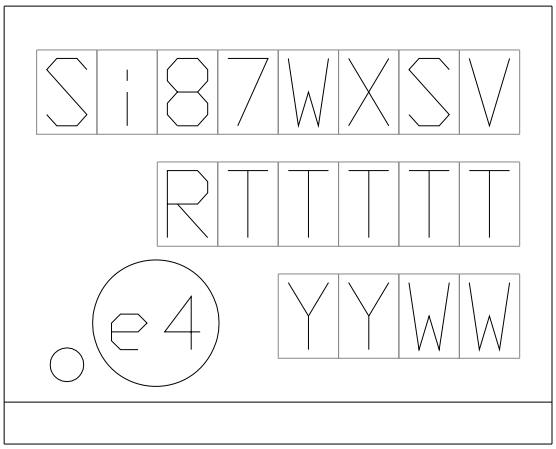
Figure 20. SDIP6 Land Pattern

Table 21. SDIP6 Land Pattern Dimensions*

Dimension	Min	Max
C	10.45	10.50
E	1.27 BSC	
X	0.55	0.60
Y	2.00	2.05
***Note:** This Land Pattern Design is based on the IPC-7351 specification.		

15. Top Markings

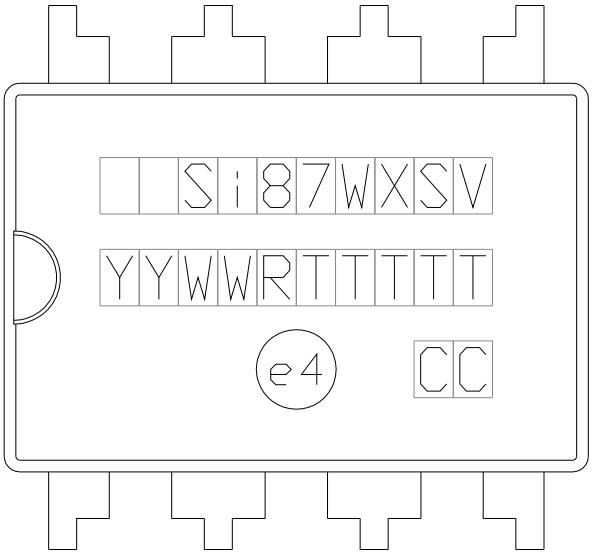
15.1. Top Marking (8-Pin Narrow Body SOIC)



15.2. Top Marking Explanation (8-Pin Narrow Body SOIC)

Line 1 Marking:	Customer Part Number	Si87 = Base name of product series W = Isolator product series (1 or 2) X = Output configuration 5/9 = no enable 6 = enable, output high when active 7/8 = enable, output Hi-z when active 0 = enable, output low when active S = Performance Grade: A = 15 Mbps, 20 kV/µs minimum CMTI B = 15 Mbps, 35 kV/µs minimum CMTI V = Insulation rating C = 3.75 kV
Line 2 Marking:	RTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order form. “R” indicates revision.
Line 3 Marking:	Circle = 43 mils Diameter Left-Justified	“e4” Pb-Free Symbol
	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.

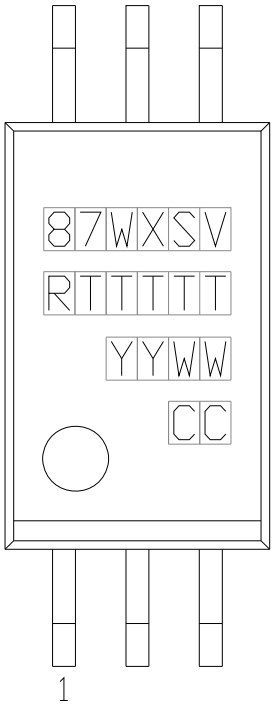
15.3. Top Marking (DIP8)



15.4. Top Marking Explanation (DIP8)

Line 1 Marking:	Customer Part Number	Si87 = Base name of product series W = Isolator product series (1 or 2) X = Output configuration 5/9 = no enable 6 = enable, output high when active 7/8 = enable, output Hi-z when active 0 = enable, output low when active S = Performance Grade: A = 15 Mbps, 20 kV/µs minimum CMTI B = 15 Mbps, 35 kV/µs minimum CMTI V = Insulation rating C = 3.75 kV
Line 2 Marking:	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.
	RTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order form. “R” indicates revision.
Line 3 Marking:	Circle = 51 mils Diameter Center-Justified	“e4” Pb-Free Symbol
	Country of Origin (Iso-Code Abbreviation)	CC

15.5. Top Marking (SDIP6)



15.6. Top Marking Explanation (SDIP6)

Line 1 Marking:	Device	87 = Base name of product series W = Isolator product series (1 or 2) X = Output configuration 5/9 = no enable 6 = enable, output high when active 7/8 = enable, output Hi-z when active 0 = enable, output low when active S = Performance Grade: A = 15 Mbps, 20 kV/µs minimum CMTI B = 15 Mbps, 35 kV/µs minimum CMTI V = Insulation rating C = 3.75 kV; D = 5.0 kV
Line 2 Marking:	RTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order form. “R” indicates revision.
Line 3 Marking:	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.
Line 4 Marking:	Country of Origin (Iso-Code Abbreviation)	CC

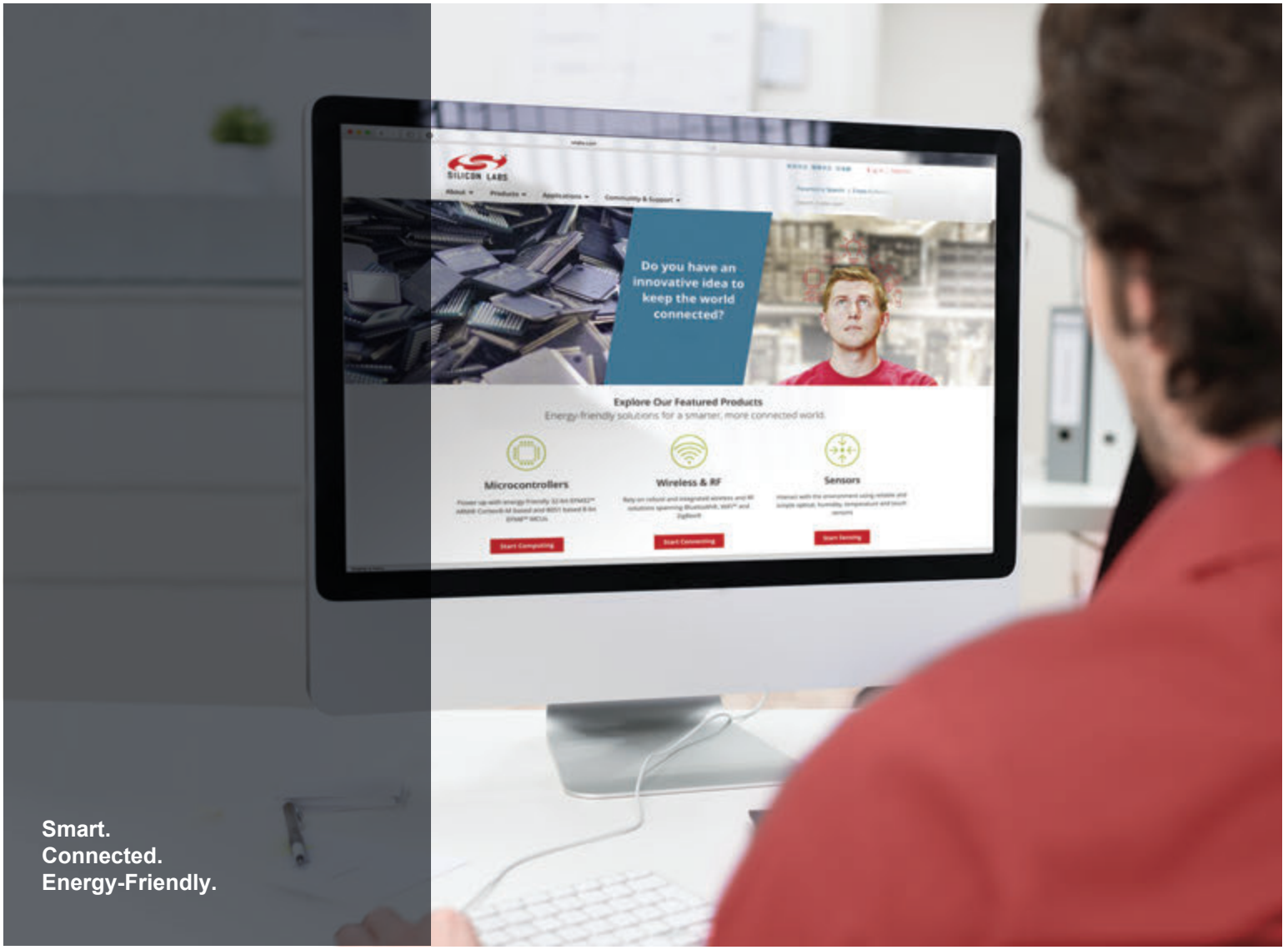
Document Change List

Revision 0.9 to Revision 1.0

- Updated Table 2 on page 4.
- Updated Table 5 on page 9.
- Updated Table 6 on page 9.
- Updated Table 9 on page 13.
- Updated Figure 8 on page 16.

Revision 1.0 to Revision 1.01

- Added "8.1.Automotive Grade OPNs" on page 24.



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