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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Operating Temperature*	T_A	150 Mbps, 15 pF, 5 V	–40	25	125	°C
Supply Voltage	V_{DD1}		2.5	—	5.5	V
	V_{DD2}		2.5	—	5.5	V

***Note:** The maximum ambient temperature is dependent on data frequency, output loading, number of operating channels, and supply voltage.

Table 2. Electrical Characteristics

(V_{DD1} = 5 V ±10%, V_{DD2} = 5 V ±10%, T_A = –40 to 125 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDDUV+	V_{DD1}, V_{DD2} rising	1.95	2.24	2.375	V
VDD Undervoltage Threshold	VDDUV–	V_{DD1}, V_{DD2} falling	1.88	2.16	2.325	V
VDD Negative-Going Lockout Hysteresis	VDD_{HYS}		50	70	95	mV
Positive-Going Input Threshold	VT+	All inputs rising	1.4	1.67	1.9	V
Negative-Going Input Threshold	VT–	All inputs falling	1.0	1.23	1.4	V
Input Hysteresis	V_{HYS}		0.38	0.44	0.50	V
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	4.8	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[1]	Z_O		—	50	—	Ω

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 2. Electrical Characteristics (Continued)
(V_{DD1} = 5 V ±10%, V_{DD2} = 5 V ±10%, T_A = –40 to 125 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Supply Current (All inputs 0 V or at Supply)						
Si8660Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	1.2	1.9	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	3.5	5.3	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	8.8	12.3	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	3.7	5.6	
Si8661Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	1.7	2.7	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	3.4	5.1	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	7.9	11.1	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	4.8	7.2	
Si8662Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	2.2	3.3	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	3.0	4.5	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	7.5	10.5	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	5.6	8.4	
Si8663Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	2.6	3.9	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	2.6	3.9	
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	6.5	9.1	
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	6.5	9.1	
1 Mbps Supply Current (All inputs = 500 kHz square wave, CI = 15 pF on all outputs)						
Si8660Bx, Ex						
V_{DD1}			—	5.0	7.0	mA
V_{DD2}			—	4.2	5.9	
Si8661Bx, Ex						
V_{DD1}			—	4.9	6.9	mA
V_{DD2}			—	4.6	6.4	
Si8662Bx, Ex						
V_{DD1}			—	5.1	7.1	mA
V_{DD2}			—	4.7	6.6	
Si8663Bx, Ex						
V_{DD1}			—	4.9	6.8	mA
V_{DD2}			—	4.9	6.8	

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 2. Electrical Characteristics (Continued)

(V_{DD1} = 5 V ±10%, V_{DD2} = 5 V ±10%, T_A = –40 to 125 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
10 Mbps Supply Current (All inputs = 5 MHz square wave, CI = 15 pF on all outputs)						
Si8660Bx, Ex V_{DD1} V_{DD2}			— —	5.0 5.9	7.0 8.3	mA
Si8661Bx, Ex V_{DD1} V_{DD2}			— —	5.2 6.1	7.3 8.5	mA
Si8662Bx, Ex V_{DD1} V_{DD2}			— —	5.6 5.9	7.9 8.2	mA
Si8663Bx, Ex V_{DD1} V_{DD2}			— —	5.7 5.7	8.0 8.0	mA
100 Mbps Supply Current (All inputs = 50 MHz square wave, CI = 15 pF on all outputs)						
Si8660Bx, Ex V_{DD1} V_{DD2}			— —	5.0 26.2	7.0 34.1	mA
Si8661Bx, Ex V_{DD1} V_{DD2}			— —	8.8 23	11.8 29.8	mA
Si8662Bx, Ex V_{DD1} V_{DD2}			— —	12.8 19.4	16.6 25.2	mA
Si8663Bx, Ex V_{DD1} V_{DD2}			— —	16.4 16.4	21.3 21.3	mA

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 2. Electrical Characteristics (Continued)
(V_{DD1} = 5 V ±10%, V_{DD2} = 5 V ±10%, T_A = –40 to 125 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Timing Characteristics						
Si866xBx, Ex						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	5.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 1	5.0	8.0	13	ns
Pulse Width Distortion $\|t_{PLH} - t_{PHL}\|$	PWD	See Figure 1	—	0.2	4.5	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-Channel Skew	t_{PSK}		—	0.4	2.5	ns
All Models						
Output Rise Time	t_r	C_L = 15 pF See Figure 1	—	2.5	4.0	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 1	—	2.5	4.0	ns
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	See Figure 6	—	350	—	ps
Common Mode Transient Immunity	CMTI	$V_I = V_{DD}$ or 0 V	35	50	—	kV/µs
Startup Time[3]	t_{SU}		—	15	40	µs

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

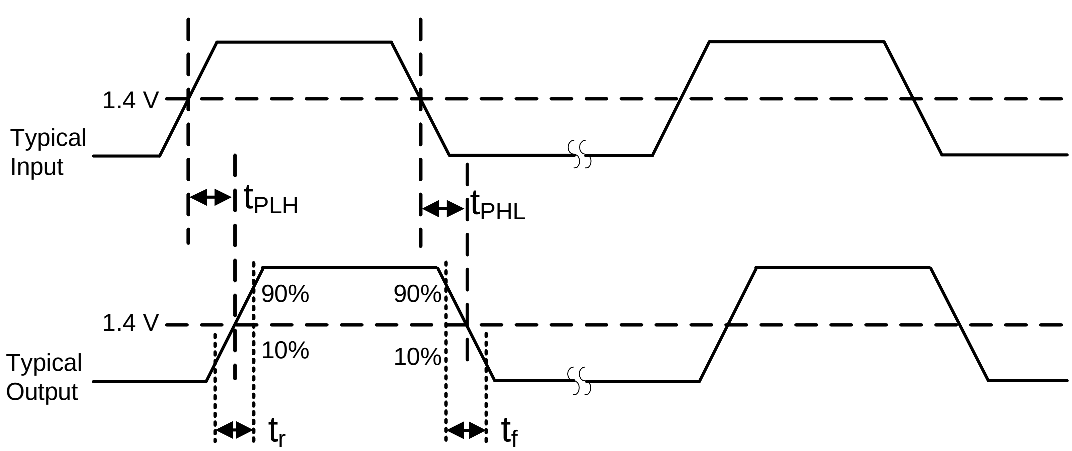

Figure 1. Propagation Delay Timing

Table 3. Electrical Characteristics
(V_{DD1} = 3.3 V ±10%, V_{DD2} = 3.3 V ±10%, T_A = –40 to 125 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDDUV+	V_{DD1}, V_{DD2} rising	1.95	2.24	2.375	V
VDD Undervoltage Threshold	VDDUV–	V_{DD1}, V_{DD2} falling	1.88	2.16	2.325	V
VDD Negative-Going Lockout Hysteresis	VDD_{HYS}		50	70	95	mV
Positive-Going Input Threshold	VT+	All inputs rising	1.4	1.67	1.9	V
Negative-Going Input Threshold	VT–	All inputs falling	1.0	1.23	1.4	V
Input Hysteresis	V_{HYS}		0.38	0.44	0.50	V
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	3.1	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[1]	Z_O		—	50	—	Ω
DC Supply Current (All inputs 0 V or at supply)						
Si8660Bx, Ex V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 V_I = 0(Bx), 1(Ex) V_I = 0(Bx), 1(Ex) V_I = 1(Bx), 0(Ex) V_I = 1(Bx), 0(Ex)	 — — — —	 1.2 3.5 8.8 3.7	 1.9 5.3 12.3 5.6	mA
Si8661Bx, Ex V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 V_I = 0(Bx), 1(Ex) V_I = 0(Bx), 1(Ex) V_I = 1(Bx), 0(Ex) V_I = 1(Bx), 0(Ex)	 — — — —	 1.7 3.4 7.9 4.8	 2.7 5.1 11.1 7.2	mA
Si8662Bx, Ex V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 V_I = 0(Bx), 1(Ex) V_I = 0(Bx), 1(Ex) V_I = 1(Bx), 0(Ex) V_I = 1(Bx), 0(Ex)	 — — — —	 2.2 3.0 7.5 5.6	 3.3 4.5 10.5 8.4	mA
Si8663Bx, Ex V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 V_I = 0(Bx), 1(Ex) V_I = 0(Bx), 1(Ex) V_I = 1(Bx), 0(Ex) V_I = 1(Bx), 0(Ex)	 — — — —	 2.6 2.6 6.5 6.5	 3.9 3.9 9.1 9.1	mA

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 3. Electrical Characteristics (Continued)

(V_{DD1} = 3.3 V ±10%, V_{DD2} = 3.3 V ±10%, T_A = –40 to 125 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
1 Mbps Supply Current (All inputs = 500 kHz square wave, Cl = 15 pF on all outputs)						
Si8660Bx, Ex V_{DD1} V_{DD2}			 — —	 5.0 4.2	 7.0 5.9	 mA
Si8661Bx, Ex V_{DD1} V_{DD2}			 — —	 4.9 4.6	 6.9 6.4	 mA
Si8662Bx, Ex V_{DD1} V_{DD2}			 — —	 5.1 4.7	 7.1 6.6	 mA
Si8663Bx, Ex V_{DD1} V_{DD2}			 — —	 4.9 4.9	 6.8 6.8	 mA
10 Mbps Supply Current (All inputs = 5 MHz square wave, Cl = 15 pF on all outputs)						
Si8660Bx, Ex V_{DD1} V_{DD2}			 — —	 5.0 5.0	 7.0 7.0	 mA
Si8661Bx, Ex V_{DD1} V_{DD2}			 — —	 5.0 5.3	 7.0 7.4	 mA
Si8662Bx, Ex V_{DD1} V_{DD2}			 — —	 5.3 5.2	 7.4 7.3	 mA
Si8663Bx, Ex V_{DD1} V_{DD2}			 — —	 5.2 5.2	 7.3 7.3	 mA

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 3. Electrical Characteristics (Continued)
(V_{DD1} = 3.3 V ±10%, V_{DD2} = 3.3 V ±10%, T_A = –40 to 125 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
100 Mbps Supply Current (All inputs = 50 MHz square wave, Cl = 15 pF on all outputs)						
Si8660Bx, Ex V_{DD1} V_{DD2}			— —	5.0 18.3	7.0 23.8	mA
Si8661Bx, Ex V_{DD1} V_{DD2}			— —	7.4 16.4	9.9 21.3	mA
Si8662Bx, Ex V_{DD1} V_{DD2}			— —	10 14.1	13 18.3	mA
Si8663Bx, Ex V_{DD1} V_{DD2}			— —	12.3 12.3	15.9 15.9	mA
Timing Characteristics						
Si866xBx, Ex						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	5.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 1	5.0	8.0	13	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 1	—	0.2	4.5	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	2.0	4.5	ns
Channel-Channel Skew	t_{PSK}		—	0.4	2.5	ns
All Models						
Output Rise Time	t_r	C_L = 15 pF See Figure 1	—	2.5	4.0	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 1	—	2.5	4.0	ns
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	See Figure 6	—	350	—	ps
Common Mode Transient Immunity	CMTI	V_I = V_{DD} or 0 V	35	50	—	kV/µs
Startup Time[3]	t_{SU}		—	15	40	µs

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 4. Electrical Characteristics

(V_{DD1} = 2.5 V ±5%, V_{DD2} = 2.5 V ±5%, T_A = –40 to 125 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDDUV+	V_{DD1}, V_{DD2} rising	1.95	2.24	2.375	V
VDD Undervoltage Threshold	VDDUV–	V_{DD1}, V_{DD2} falling	1.88	2.16	2.325	V
VDD Negative-Going Lockout Hysteresis	VDD_{HYS}		50	70	95	mV
Positive-Going Input Threshold	VT+	All inputs rising	1.4	1.67	1.9	V
Negative-Going Input Threshold	VT–	All inputs falling	1.0	1.23	1.4	V
Input Hysteresis	V_{HYS}		0.38	0.44	0.50	V
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	2.3	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[1]	Z_O		—	50	—	Ω
DC Supply Current (All inputs 0 V or at supply)						
Si8660Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	1.2	1.9	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	3.5	5.3	mA
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	8.8	12.3	mA
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	3.7	5.6	mA
Si8661Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	1.7	2.7	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	3.4	5.1	mA
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	7.9	11.1	mA
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	4.8	7.2	mA
Si8662Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	2.2	3.3	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	3.0	4.5	mA
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	7.5	10.5	mA
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	5.6	8.4	mA
Si8663Bx, Ex						
V_{DD1}		V_I = 0(Bx), 1(Ex)	—	2.6	3.9	mA
V_{DD2}		V_I = 0(Bx), 1(Ex)	—	2.6	3.9	mA
V_{DD1}		V_I = 1(Bx), 0(Ex)	—	6.5	9.1	mA
V_{DD2}		V_I = 1(Bx), 0(Ex)	—	6.5	9.1	mA

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 4. Electrical Characteristics (Continued)
(V_{DD1} = 2.5 V ±5%, V_{DD2} = 2.5 V ±5%, T_A = –40 to 125 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
1 Mbps Supply Current (All inputs = 500 kHz square wave, Cl = 15 pF on all outputs)						
Si8660Bx, Ex V_{DD1} V_{DD2}			— —	5.0 4.2	7.0 5.9	mA
Si8661Bx, Ex V_{DD1} V_{DD2}			— —	4.9 4.6	6.9 6.4	mA
Si8662Bx, Ex V_{DD1} V_{DD2}			— —	5.1 4.7	7.1 6.6	mA
Si8663Bx, Ex V_{DD1} V_{DD2}			— —	4.9 4.9	6.8 6.8	mA
10 Mbps Supply Current (All inputs = 5 MHz square wave, Cl = 15 pF on all outputs)						
Si8660Bx, Ex V_{DD1} V_{DD2}			— —	5.0 4.6	7.0 6.4	mA
Si8661Bx, Ex V_{DD1} V_{DD2}			— —	5.0 4.9	6.9 6.9	mA
Si8662Bx, Ex V_{DD1} V_{DD2}			— —	5.2 4.9	7.2 6.9	mA
Si8663Bx, Ex V_{DD1} V_{DD2}			— —	5.0 5.0	7.0 7.0	mA

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 4. Electrical Characteristics (Continued)

(V_{DD1} = 2.5 V ±5%, V_{DD2} = 2.5 V ±5%, T_A = –40 to 125 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
100 Mbps Supply Current (All inputs = 50 MHz square wave, CI = 15 pF on all outputs)						
Si8660Bx, Ex						
V_{DD1}			—	5.0	7.0	mA
V_{DD2}			—	14.7	19.1	
Si8661Bx, Ex						
V_{DD1}			—	6.7	9.1	mA
V_{DD2}			—	13.4	17.4	
Si8662Bx, Ex						
V_{DD1}			—	8.7	11.3	mA
V_{DD2}			—	11.7	15.2	
Si8663Bx, Ex						
V_{DD1}			—	10.3	13.4	mA
V_{DD2}			—	10.3	13.4	
Timing Characteristics						
Si866xBx, Ex						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	5.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 1	5.0	8.0	14	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL}\rvert$	PWD	See Figure 1	—	0.2	5.0	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	2.0	5.0	ns
Channel-Channel Skew	t_{PSK}		—	0.4	2.5	ns
All Models						
Output Rise Time	t_r	C_L = 15 pF See Figure 1	—	2.5	4.0	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 1	—	2.5	4.0	ns
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	See Figure 6	—	350	—	ps
Common Mode Transient Immunity	CMTI	$V_I = V_{DD}$ or 0 V	35	50	—	kV/µs
Startup Time[3]	t_{SU}		—	15	40	µs

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 5. Regulatory Information*

CSA
The Si866x is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873.
61010-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 600 V_{RMS} basic insulation working voltage.
60950-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
60601-1: Up to 125 V_{RMS} reinforced insulation working voltage; up to 380 V_{RMS} basic insulation working voltage.
VDE
The Si866x is certified according to IEC 60747-5-2. For more details, see File 5006301-4880-0001.
60747-5-2: Up to 1200 V_{peak} for basic insulation working voltage.
60950-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
UL
The Si866x is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 5000 V_{RMS} isolation voltage for basic protection.
***Note:** Regulatory Certifications apply to 3.75 kV_{RMS} rated devices which are production tested to 4.5 kV_{RMS} for 1 sec. Regulatory Certifications apply to 5.0 kV_{RMS} rated devices which are production tested to 6.0 kV_{RMS} for 1 sec. For more information, see "5. Ordering Guide" on page 26.

Table 6. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value		Unit
			WB SOIC-16	NB SOIC-16	
Nominal Air Gap (Clearance)[1]	L(IO1)		8.0	4.9	mm
Nominal External Tracking (Creepage)[1]	L(IO2)		8.0	4.01	mm
Minimum Internal Gap (Internal Clearance)			0.014	0.011	mm
Tracking Resistance (Proof Tracking Index)	PTI	IEC60112	600	600	V_{RMS}
Erosion Depth	ED		0.019	0.019	mm
Resistance (Input-Output)[2]	R_{IO}		10^{12}	10^{12}	Ω
Capacitance (Input-Output)[2]	C_{IO}	f = 1 MHz	2.0	2.0	pF
Input Capacitance[3]	C_I		4.0	4.0	pF

Notes:

1. The values in this table correspond to the nominal creepage and clearance values. VDE certifies the clearance and creepage limits as 4.7 mm minimum for the NB SOIC-16 package and 8.5 mm minimum for the WB SOIC-16 package. UL does not impose a clearance and creepage minimum for component-level certifications. CSA certifies the clearance and creepage limits as 3.9 mm minimum for the NB SOIC-16 package and 7.6 mm minimum for the WB SOIC-16 package.
2. To determine resistance and capacitance, the Si86xx is converted into a 2-terminal device. Pins 1–8 are shorted together to form the first terminal and pins 9–16 are shorted together to form the second terminal. The parameters are then measured between these two terminals.
3. Measured from input pin to ground.

Table 7. IEC 60664-1 (VDE 0844 Part 2) Ratings

Parameter	Test Conditions	Specification	
		NB SOIC-16	WB SOIC-16
Basic Isolation Group	Material Group	I	I
Installation Classification	Rated Mains Voltages ≤ 150 V_{RMS}	I-IV	I-IV
	Rated Mains Voltages ≤ 300 V_{RMS}	I-III	I-IV
	Rated Mains Voltages ≤ 400 V_{RMS}	I-II	I-III
	Rated Mains Voltages ≤ 600 V_{RMS}	I-II	I-III

Table 8. IEC 60747-5-2 Insulation Characteristics for Si86xxxx*

Parameter	Symbol	Test Condition	Characteristic		Unit
			WB SOIC-16	NB SOIC-16	
Maximum Working Insulation Voltage	V_{IORM}		1200	630	Vpeak
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	2250	1182	
Transient Overvoltage	V_{IOTM}	t = 60 sec	6000	6000	Vpeak
Pollution Degree (DIN VDE 0110, Table 1)			2	2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	$>10^9$	Ω

***Note:** Maintenance of the safety data is ensured by protective circuits. The Si86xxxx provides a climate classification of 40/125/21.

Table 9. IEC Safety Limiting Values[1]

Parameter	Symbol	Test Condition	Min	Typ	Max		Unit
					WB SOIC-16	NB SOIC-16	
Case Temperature	T_S		—	—	150	150	°C
Safety Input, Output, or Supply Current	I_S	θ_{JA} = 105 °C/W (NB SOIC-16), V_I = 5.5 V, T_J = 150 °C, T_A = 25 °C	—	—	220	215	mA
Device Power Dissipation[2]	P_D		—	—	415	415	mW

Notes:
1. Maximum value allowed in the event of a failure; also see the thermal derating curve in Figures 2 and 3.
2. The Si86xx is tested with VDD1 = VDD2 = 5.5 V, TJ = 150 ºC, CL = 15 pF, input a 150 Mbps 50% duty cycle square wave.

Table 10. Thermal Characteristics

Parameter	Symbol	Test Condition	WB SOIC-16	NB SOIC-16	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}		100	105	ºC/W

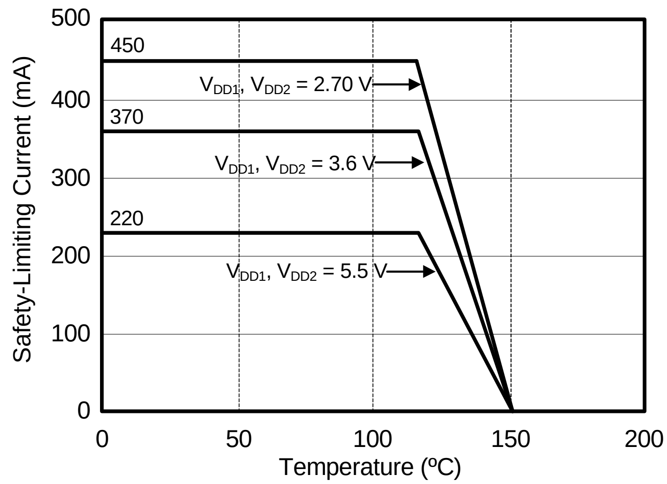

Figure 2. (WB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

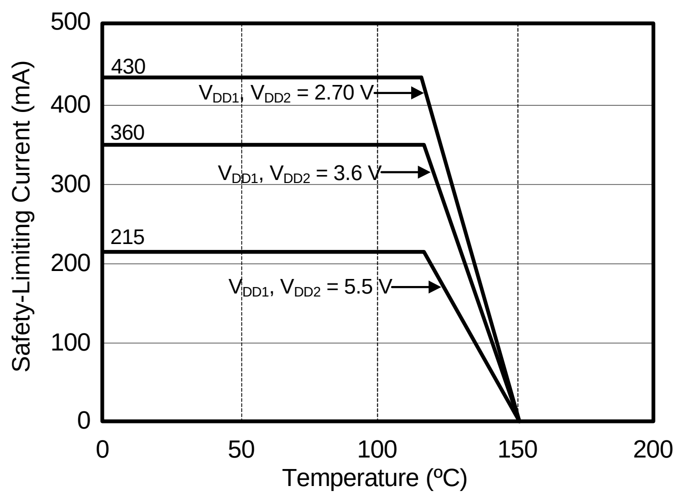

Figure 3. (NB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

Table 11. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Typ	Max	Unit
Storage Temperature[2]	T_{STG}	–65	—	150	°C
Ambient Temperature Under Bias	T_A	–40	—	125	°C
Supply Voltage	V_{DD1}, V_{DD2}	–0.5	—	7.0	V
Input Voltage	V_I	–0.5	—	V_{DD} + 0.5	V
Output Voltage	V_O	–0.5	—	V_{DD} + 0.5	V
Output Current Drive Channel	I_O	—	—	10	mA
Lead Solder Temperature (10 s)		—	—	260	°C
Maximum Isolation (Input to Output) (1 sec) NB SOIC-16		—	—	4500	V_{RMS}
Maximum Isolation (Input to Output) (1 sec) WB SOIC-16		—	—	6500	V_{RMS}

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet.
2. VDE certifies storage temperature from –40 to 150 °C.

2. Functional Description

2.1. Theory of Operation

The operation of an Si866x channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si866x channel is shown in Figure 4.

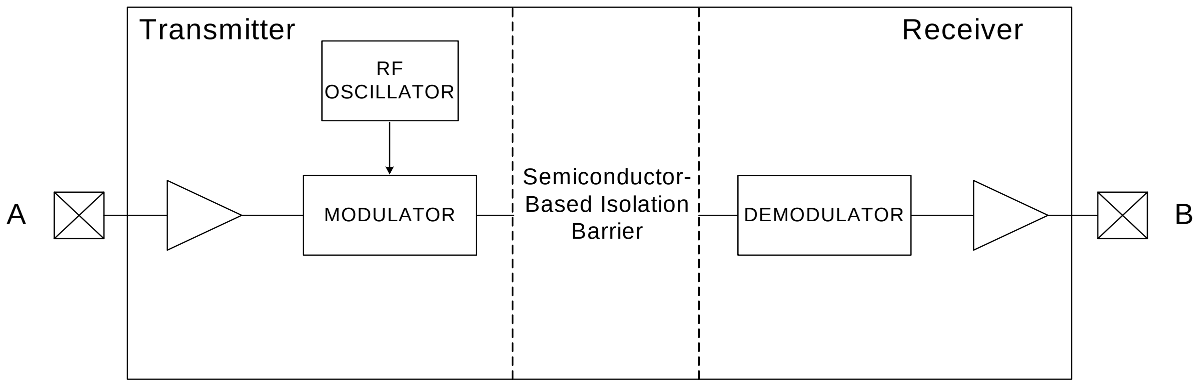

Figure 4. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See Figure 5 for more details.

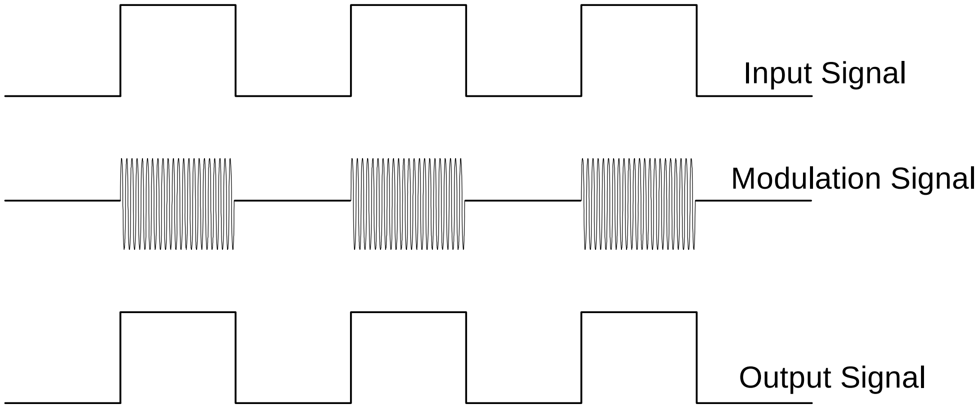

Figure 5. Modulation Scheme

2.2. Eye Diagram

Figure 6 illustrates an eye-diagram taken on an Si8660. For the data source, the test used an Anritsu (MP1763C) Pulse Pattern Generator set to 1000 ns/div. The output of the generator's clock and data from an Si8660 were captured on an oscilloscope. The results illustrate that data integrity was maintained even at the high data rate of 150 Mbps. The results also show that 2 ns pulse width distortion and 350 ps peak jitter were exhibited.

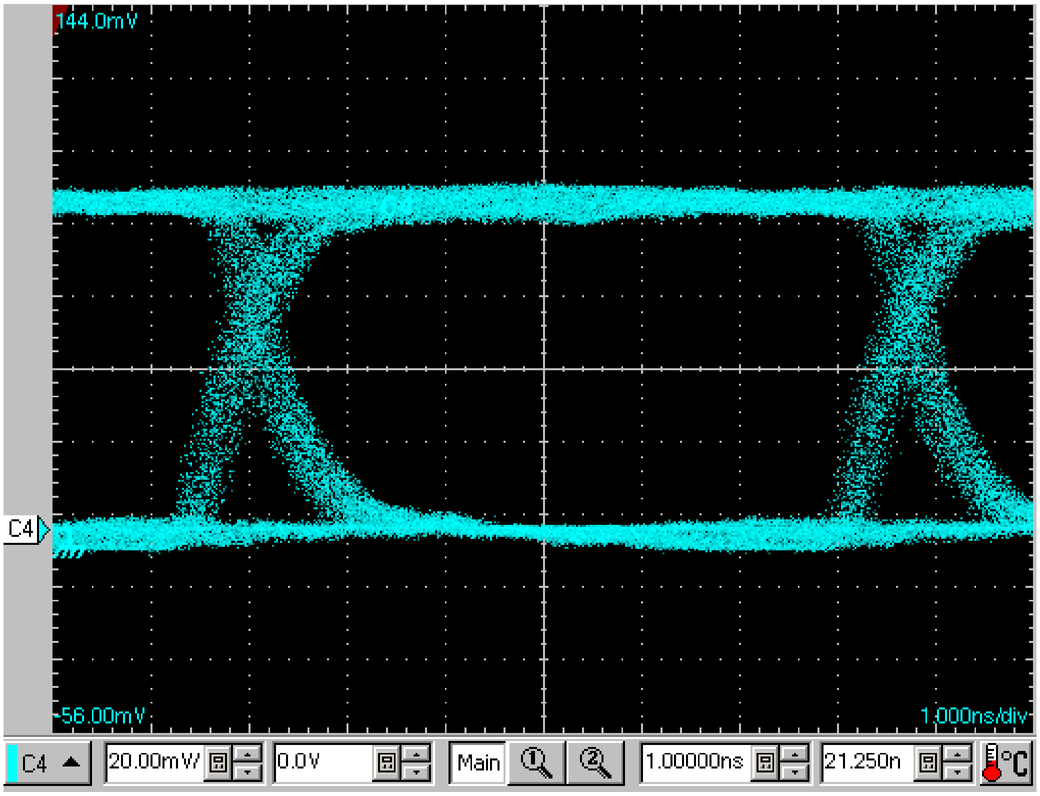

Figure 6. Eye Diagram

3. Device Operation

Device behavior during start-up, normal operation, and shutdown is shown in Figure 7, where UVLO+ and UVLO- are the positive-going and negative-going thresholds respectively. Refer to Table 12 to determine outputs when power supply (VDD) is not present.

Table 12. Si866x Logic Operation

V_I Input[1,2]	VDDI State[1,3,4]	VDDO State[1,3,4]	V_O Output[1,2]	Comments
H	P	P	H	Normal operation.
L	P	P	L	
X[5]	UP	P	L[6] H[6]	Upon transition of VDDI from unpowered to powered, V_O returns to the same state as V_I in less than 1 µs.
X[5]	P	UP	Undetermined	Upon transition of VDDO from unpowered to powered, V_O returns to the same state as V_I within 1 µs.

Notes:
1. VDDI and VDDO are the input and output power supplies. V_I and V_O are the respective input and output terminals.
2. X = not applicable; H = Logic High; L = Logic Low; Hi-Z = High Impedance.
3. “Powered” state (P) is defined as 2.5 V < VDD < 5.5 V.
4. “Unpowered” state (UP) is defined as VDD = 0 V.
5. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current.
6. See "5. Ordering Guide" on page 26 for details. This is the selectable fail-safe operating mode (ordering option). Some devices have default output state = H, and some have default output state = L, depending on the ordering part number (OPN). For default high devices, the data channels have pull-ups on inputs/outputs. For default low devices, the data channels have pull-downs on inputs/outputs.

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3.1. Device Startup

Outputs are held low during powerup until VDD is above the UVLO threshold for time period tSTART. Following this, the outputs follow the states of inputs.

3.2. Undervoltage Lockout

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. Both Side A and Side B each have their own undervoltage lockout monitors. Each side can enter or exit UVLO independently. For example, Side A unconditionally enters UVLO when V_{DD1} falls below $V_{DD1(UVLO–)}$ and exits UVLO when V_{DD1} rises above $V_{DD1(UVLO+)}$. Side B operates the same as Side A with respect to its V_{DD2} supply.

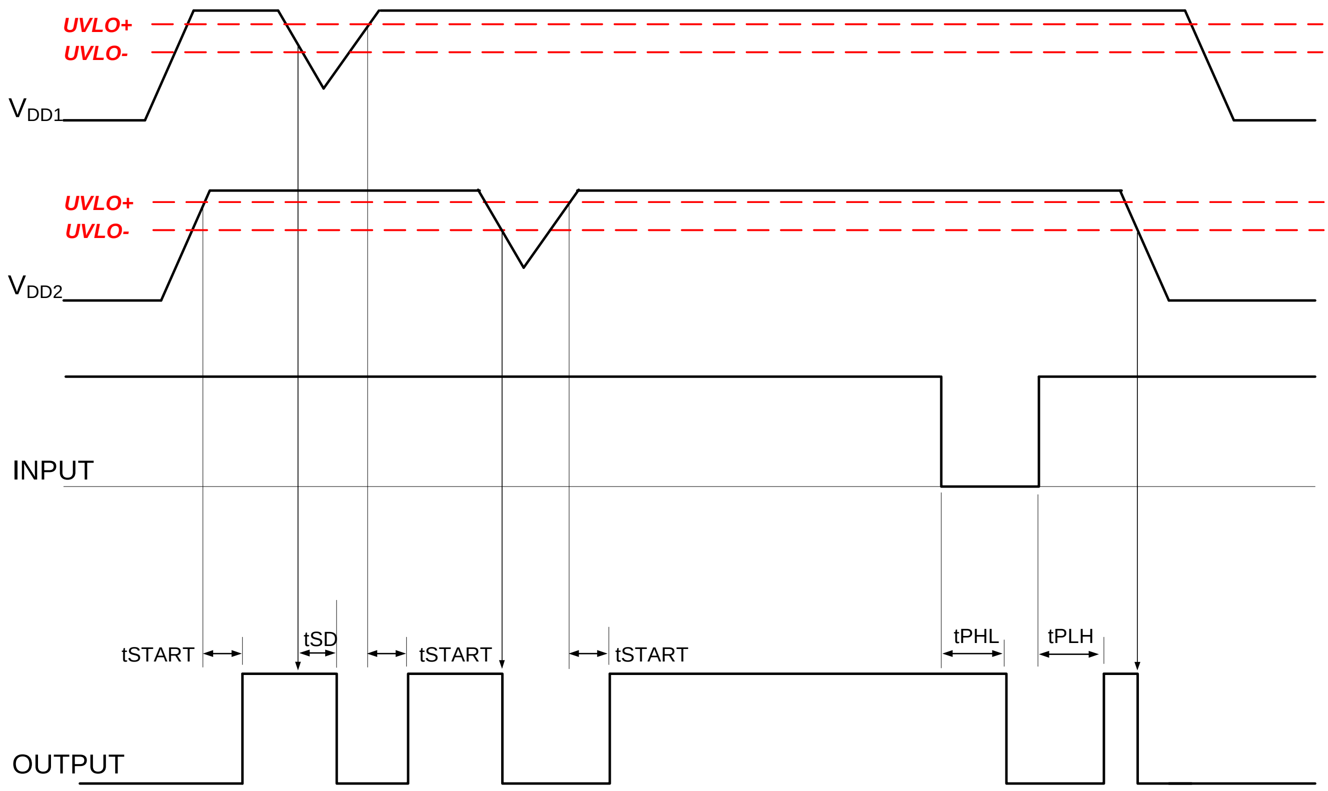


Figure 7. Device Behavior during Normal Operation

3.3. Layout Recommendations

To ensure safety in the end user application, high voltage circuits (i.e., circuits with >30 V_{AC}) must be physically separated from the safety extra-low voltage circuits (SELV is a circuit with <30 V_{AC}) by a certain distance (creepage/clearance). If a component, such as a digital isolator, straddles this isolation barrier, it must meet those creepage/clearance requirements and also provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). Table 5 on page 14 and Table 6 on page 14 detail the working voltage and creepage/clearance capabilities of the Si86xx. These tables also detail the component standards (UL1577, IEC60747, CSA 5A), which are readily accepted by certification bodies to provide proof for end-system specifications requirements. Refer to the end-system specification (61010-1, 60950-1, 60601-1, etc.) requirements before starting any design that uses a digital isolator.

3.3.1. Supply Bypass

The Si866x family requires a 0.1 µF bypass capacitor between V_{DD1} and GND1 and V_{DD2} and GND2. The capacitor should be placed as close as possible to the package. To enhance the robustness of a design, it is further recommended that the user also add 1 µF bypass capacitors and include 100 Ω resistors in series with the inputs and outputs if the system is excessively noisy.

3.3.2. Pin Connections

For narrow-body devices, Pin 2 and Pin 8 GND must be externally connected to respective ground. Pin 9 and Pin 15 must also be connected to external ground. No connect pins are not internally connected. They can be left floating, tied to VDD, or tied to GND.

3.3.3. Output Pin Termination

The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

3.4. Fail-Safe Operating Mode

Si86xx devices feature a selectable (by ordering option) mode whereby the default output state (when the input supply is unpowered) can either be a logic high or logic low when the output supply is powered. See Table 12 on page 20 and "5. Ordering Guide" on page 26 for more information.

3.5. Typical Performance Characteristics

The typical performance characteristics depicted in the following diagrams are for information purposes only. Refer to Tables 2, 3, and 4 for actual specification limits.

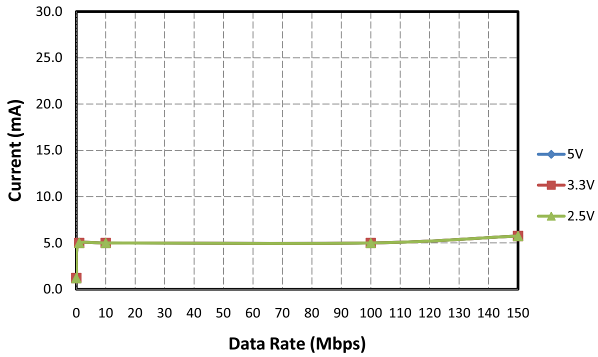


Figure 8. Si8660 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation

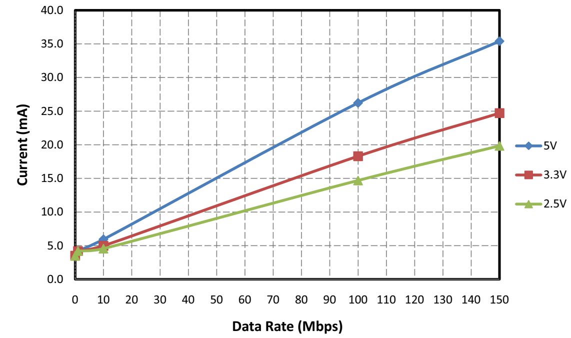


Figure 11. Si8660 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation (15 pF Load)

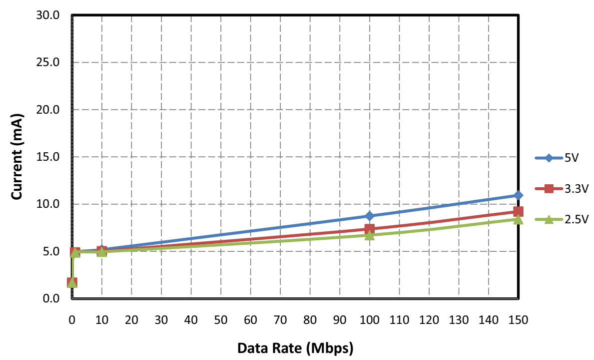


Figure 9. Si8661 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation (15 pF Load)

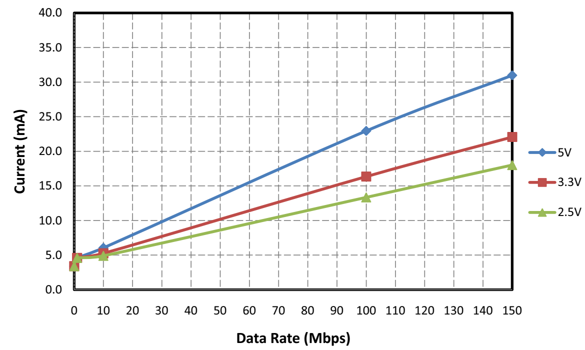


Figure 12. Si8661 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation (15 pF Load)

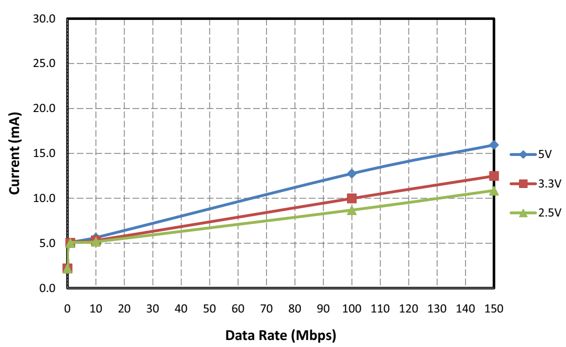


Figure 10. Si8662 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation (15 pF Load)

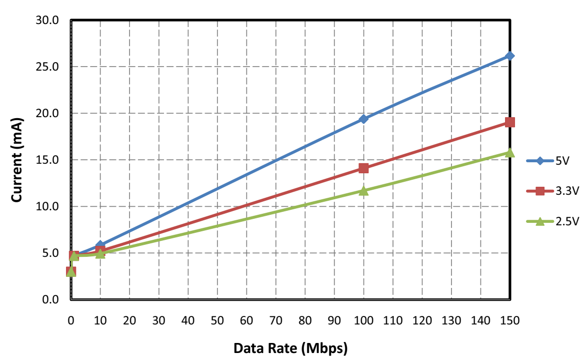


Figure 13. Si8662 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation (15 pF Load)

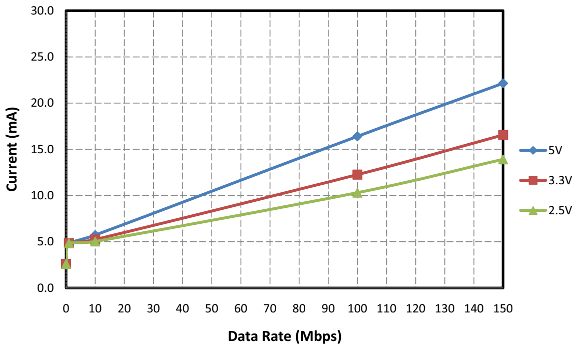


Figure 14. Si8663 Typical V_{DD1} or V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.5 V Operation (15 pF Load)

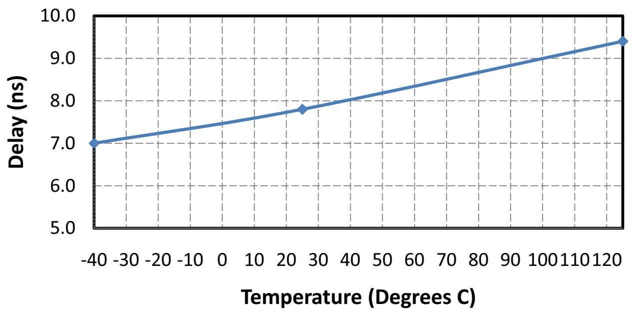
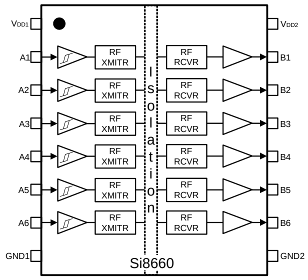
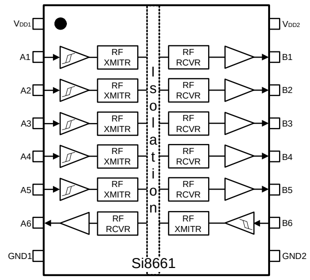
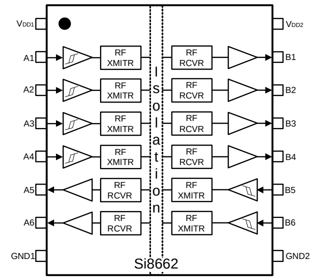


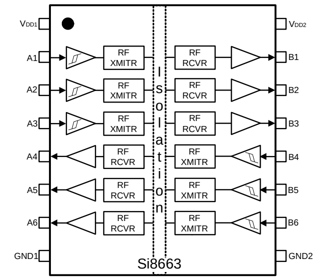
Figure 15. Propagation Delay vs. Temperature

4. Pin Descriptions









Name	SOIC-16 Pin#	Type	Description
V_{DD1}	1	Supply	Side 1 power supply.
A1	2	Digital Input	Side 1 digital input.
A2	3	Digital Input	Side 1 digital input.
A3	4	Digital Input	Side 1 digital input.
A4	5	Digital I/O	Side 1 digital input or output.
A5	6	Digital I/O	Side 1 digital input or output.
A6	7	Digital I/O	Side 1 digital input or output.
GND1	8	Ground	Side 1 ground.
GND2	9	Ground	Side 2 ground.
B6	10	Digital I/O	Side 2 digital input or output.
B5	11	Digital I/O	Side 2 digital input or output.
B4	12	Digital I/O	Side 2 digital input or output.
B3	13	Digital Output	Side 2 digital output.
B2	14	Digital Output	Side 2 digital output.
B1	15	Digital Output	Side 2 digital output.
V_{DD2}	16	Supply	Side 2 power supply.

5. Ordering Guide

Revision B devices are recommended for all new designs.

Table 13. Ordering Guide for Valid OPNs[1]

Ordering Part Number (OPN)	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Max Data Rate (Mbps)	Default Output State	Isolation rating (kV)	Temp (°C)	Package
Revision B Devices[2,3]							
Si8660BA-B-IS1	6	0	150	Low	1.0	–40 to 125 °C	NB SOIC-16
Si8660BC-B-IS1	6	0	150	Low	3.75	–40 to 125 °C	NB SOIC-16
Si8660EC-B-IS1	6	0	150	High	3.75	–40 to 125 °C	NB SOIC-16
Si8660BD-B-IS	6	0	150	Low	5.0	–40 to 125 °C	WB SOIC-16
Si8660ED-B-IS	6	0	150	High	5.0	–40 to 125 °C	WB SOIC-16
Si8661BC-B-IS1	5	1	150	Low	3.75	–40 to 125 °C	NB SOIC-16
Si8661EC-B-IS1	5	1	150	High	3.75	–40 to 125 °C	NB SOIC-16
Si8661BD-B-IS	5	1	150	Low	5.0	–40 to 125 °C	WB SOIC-16
Si8661ED-B-IS	5	1	150	High	5.0	–40 to 125 °C	WB SOIC-16
Si8662BC-B-IS1	4	2	150	Low	3.75	–40 to 125 °C	NB SOIC-16
Si8662EC-B-IS1	4	2	150	High	3.75	–40 to 125 °C	NB SOIC-16
Si8662BD-B-IS	4	2	150	Low	5.0	–40 to 125 °C	WB SOIC-16
Si8662ED-B-IS	4	2	150	High	5.0	–40 to 125 °C	WB SOIC-16
Si8663BC-B-IS1	3	3	150	Low	3.75	–40 to 125 °C	NB SOIC-16
Si8663EC-B-IS1	3	3	150	High	3.75	–40 to 125 °C	NB SOIC-16
Si8663BD-B-IS	3	3	150	Low	5.0	–40 to 125 °C	WB SOIC-16
Si8663ED-B-IS	3	3	150	High	5.0	–40 to 125 °C	WB SOIC-16

Notes:

1. All packages are RoHS-compliant.
   Moisture sensitivity level is MSL3 for wide-body SOIC-16, narrow-body SOIC-16 package with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
2. Revision A devices are supported for existing designs, but Revision B is recommended for all new designs.
3. All devices >1 kV_{RMS} are AEC-Q100 qualified.

Table 13. Ordering Guide for Valid OPNs[1] (Continued)

Ordering Part Number (OPN)	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Max Data Rate (Mbps)	Default Output State	Isolation rating (kV)	Temp (°C)	Package
Revision A Devices[2,3]							
Si8660BA-A-IS1	6	0	150	Low	1.0	–40 to 125 °C	NB SOIC-16
Si8660BC-A-IS1	6	0	150	Low	3.75	–40 to 125 °C	NB SOIC-16
Si8660EC-A-IS1	6	0	150	High	3.75	–40 to 125 °C	NB SOIC-16
Si8660BD-A-IS	6	0	150	Low	5.0	–40 to 125 °C	WB SOIC-16
Si8660ED-A-IS	6	0	150	High	5.0	–40 to 125 °C	WB SOIC-16
Si8661BC-A-IS1	5	1	150	Low	3.75	–40 to 125 °C	NB SOIC-16
Si8661EC-A-IS1	5	1	150	High	3.75	–40 to 125 °C	NB SOIC-16
Si8661BD-A-IS	5	1	150	Low	5.0	–40 to 125 °C	WB SOIC-16
Si8661ED-A-IS	5	1	150	High	5.0	–40 to 125 °C	WB SOIC-16
Si8662BC-A-IS1	4	2	150	Low	3.75	–40 to 125 °C	NB SOIC-16
Si8662EC-A-IS1	4	2	150	High	3.75	–40 to 125 °C	NB SOIC-16
Si8662BD-A-IS	4	2	150	Low	5.0	–40 to 125 °C	WB SOIC-16
Si8662ED-A-IS	4	2	150	High	5.0	–40 to 125 °C	WB SOIC-16
Si8663BC-A-IS1	3	3	150	Low	3.75	–40 to 125 °C	NB SOIC-16
Si8663EC-A-IS1	3	3	150	High	3.75	–40 to 125 °C	NB SOIC-16
Si8663BD-A-IS	3	3	150	Low	5.0	–40 to 125 °C	WB SOIC-16
Si8663ED-A-IS	3	3	150	High	5.0	–40 to 125 °C	WB SOIC-16

Notes:

1. All packages are RoHS-compliant.
   Moisture sensitivity level is MSL3 for wide-body SOIC-16, narrow-body SOIC-16 package with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
2. Revision A devices are supported for existing designs, but Revision B is recommended for all new designs.
3. All devices >1 kV_{RMS} are AEC-Q100 qualified.

6. Package Outline: 16-Pin Wide Body SOIC

Figure 16 illustrates the package details for the Si866x Digital Isolator. Table 14 lists the values for the dimensions shown in the illustration.

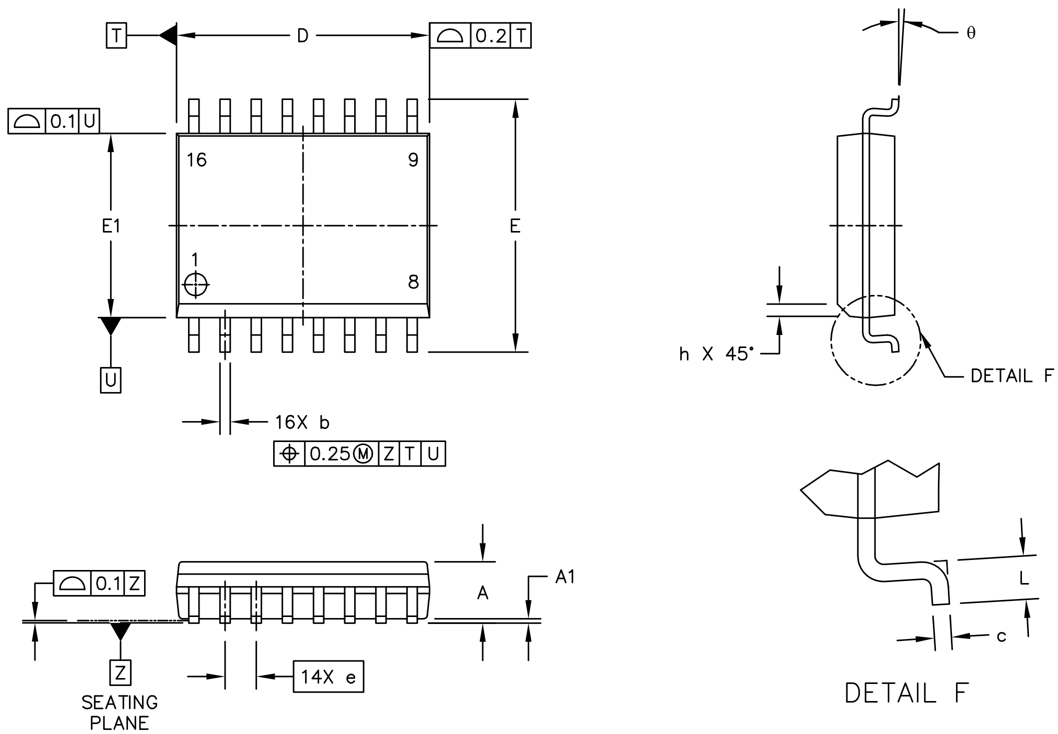


Figure 16. 16-Pin Wide Body SOIC

Table 14. Package Diagram Dimensions

Symbol	Millimeters	
	Min	**Max**
A	—	2.65
A1	0.1	0.3
D	10.3 BSC	
E	10.3 BSC	
E1	7.5 BSC	
b	0.31	0.51
c	0.20	0.33
e	1.27 BSC	
h	0.25	0.75
L	0.4	1.27
θ	0°	7°

7. Land Pattern: 16-Pin Wide-Body SOIC

Figure 17 illustrates the recommended land pattern details for the Si866x in a 16-pin wide-body SOIC. Table 15 lists the values for the dimensions shown in the illustration.

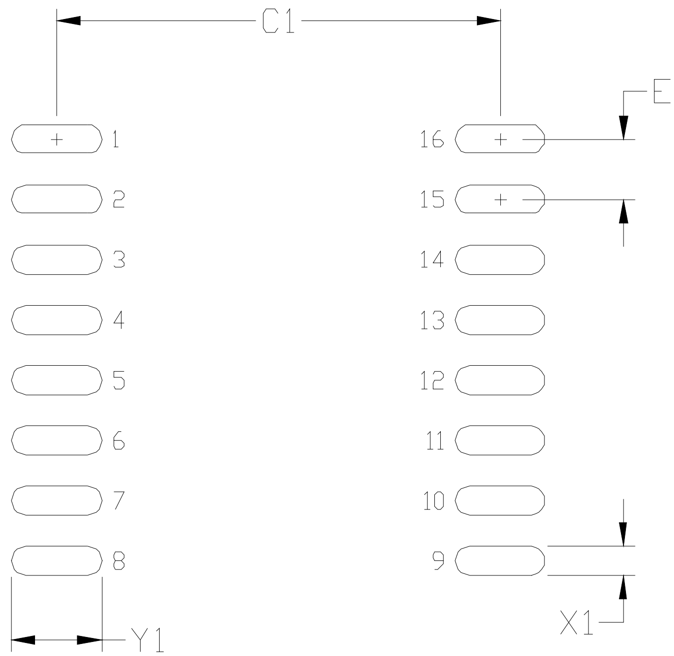


Figure 17. 16-Pin SOIC Land Pattern

Table 15. 16-Pin Wide Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.90

Notes:
1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

8. Package Outline: 16-Pin Narrow Body SOIC

Figure 18 illustrates the package details for the Si866x in a 16-pin narrow-body SOIC (SO-16). Table 16 lists the values for the dimensions shown in the illustration.

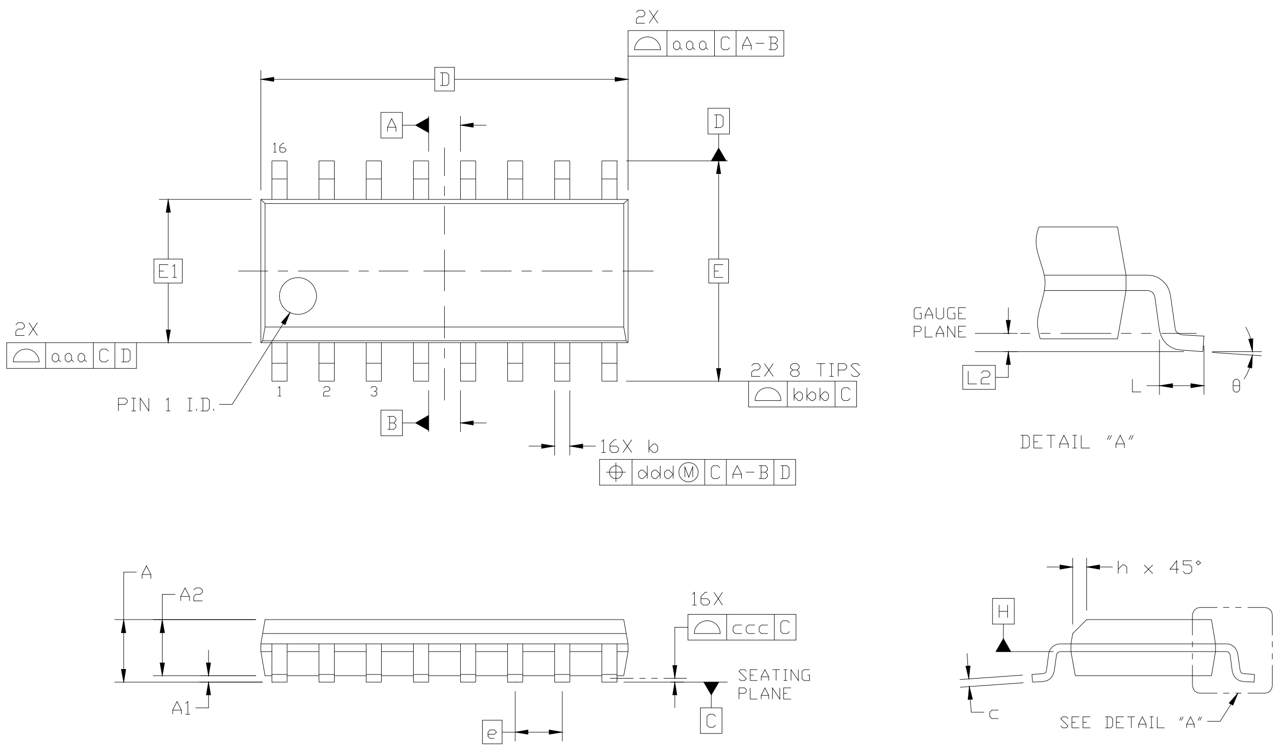


Figure 18. 16-pin Small Outline Integrated Circuit (SOIC) Package

Table 16. Package Diagram Dimensions

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.31	0.51
c	0.17	0.25
D	9.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L2	0.25 BSC	

Table 16. Package Diagram Dimensions (Continued)

Dimension	Min	Max
h	0.25	0.50
θ	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. Land Pattern: 16-Pin Narrow Body SOIC

Figure 19 illustrates the recommended land pattern details for the Si866x in a 16-pin narrow-body SOIC. Table 17 lists the values for the dimensions shown in the illustration.

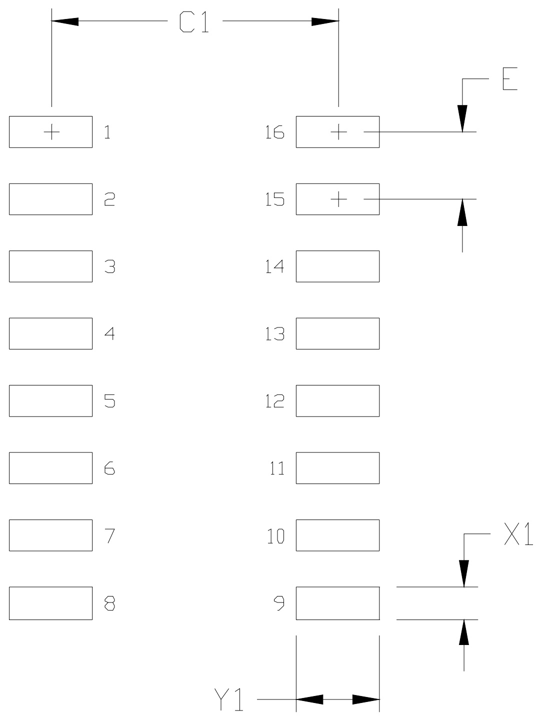


Figure 19. 16-Pin Narrow Body SOIC PCB Land Pattern

Table 17. 16-Pin Narrow Body SOIC Land Pattern Dimensions

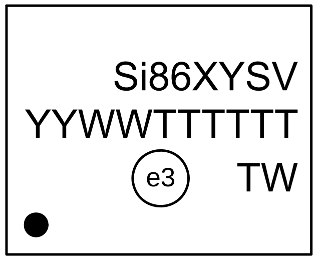
Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Notes:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

10. Top Marking: 16-Pin Wide Body SOIC

10.1. 16-Pin Wide Body SOIC Top Marking

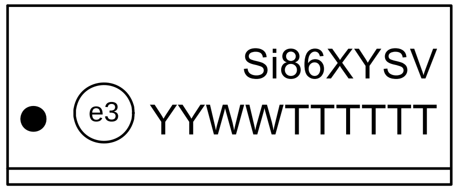


10.2. Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options (See Ordering Guide for more information).	Si86 = Isolator product series XY = Channel Configuration X = # of data channels (6, 5, 4, 3, 2, 1) Y = # of reverse channels (3, 2, 1, 0) S = Speed Grade A = 1 Mbps; B = 150 Mbps (default output = low); E = 150 Mbps (default output = high) V = Insulation rating A = 1 kV; B = 2.5 kV; C = 3.75 kV; D = 5.0 kV
Line 2 Marking:	YY = Year WW = Workweek	Assigned by assembly subcontractor. Corresponds to the year and workweek of the mold date.
	TTTTTT = Mfg Code	Manufacturing code from assembly house.
Line 3 Marking:	Circle = 1.5 mm Diameter (Center-Justified)	“e3” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	TW = Taiwan

11. Top Marking: 16-Pin Narrow Body SOIC

11.1. 16-Pin Narrow Body SOIC Top Marking



11.2. Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options (See Ordering Guide for more information).	Si86 = Isolator product series XY = Channel Configuration X = # of data channels (6, 5, 4, 3, 2, 1) Y = # of reverse channels (3, 2, 1, 0) S = Speed Grade A = 1 Mbps; B = 150 Mbps (default output = low); E = 150 Mbps (default output = high) V = Insulation rating A = 1 kV; B = 2.5 kV; C = 3.75 kV
Line 2 Marking:	Circle = 1.2 mm Diameter	“e3” Pb-Free Symbol
	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.
	TTTTTT = Mfg code	Manufacturing Code from Assembly Purchase Order form.
	Circle = 1.2 mm diameter	“e3” Pb-Free Symbol.

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Document Change List

Revision 0.1 to Revision 1.0

- Added chip graphics on page 1.
- Updated " Features" on page 1.
- Moved Tables 1 and 11 to page 17.
- Updated Tables 2, 3, and 4.
- Updated Table 6, “Insulation and Safety-Related Specifications,” on page 14.
- Updated Table 8, “IEC 60747-5-2 Insulation Characteristics for Si86xxxx*,” on page 15.
- Moved Table 12 to page 20.
- Moved “Typical Performance Characteristics” to page 23.
- Updated "3.5. Typical Performance Characteristics" on page 23.
- Updated Table 4, “Pin Descriptions,” on page 25.
- Updated "5. Ordering Guide" on page 26.
- Removed references to QSOP-16 package.

Revision 1.0 to Revision 1.1

- Reordered spec tables to conform to new convention.
- Removed “pending” throughout document.

Revision 1.1 to Revision 1.2

- Updated High Level Output Voltage VOH to 3.1 V in Table 3, “Electrical Characteristics,” on page 8.
- Updated High Level Output Voltage VOH to 2.3 V in Table 4, “Electrical Characteristics,” on page 11.

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