SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

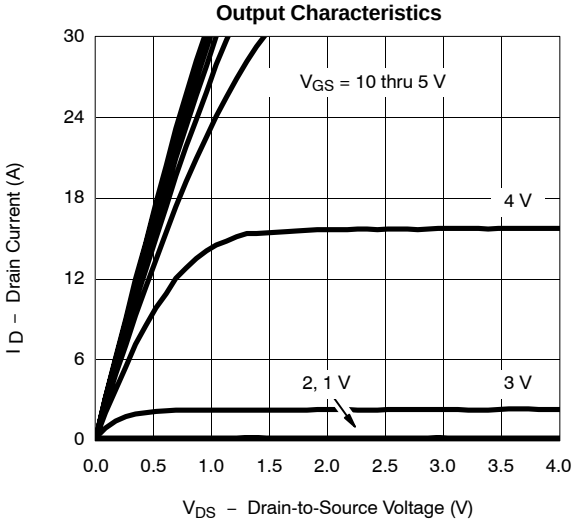
Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1		3	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			1	μA
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55°C			25	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	20			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 5.8 A		0.030	0.037	Ω
		V_{GS} = 4.5 V, I_D = 4.7 A		0.042	0.055	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 5.8 A		13		S
Diode Forward Voltage[b]	V_{SD}	I_S = 1.7 A, V_{GS} = 0 V		0.8	1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 5.8 A		18	25	nC
Gate-Source Charge	Q_{gs}			4.5		
Gate-Drain Charge	Q_{gd}			2.5		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 15 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		10	16	ns
Rise Time	t_r			10	16	
Turn-Off Delay Time	$t_{d(off)}$			27	40	
Fall Time	t_f			24	35	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.7 A, di/dt = 100 A/μs		45	80	

Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

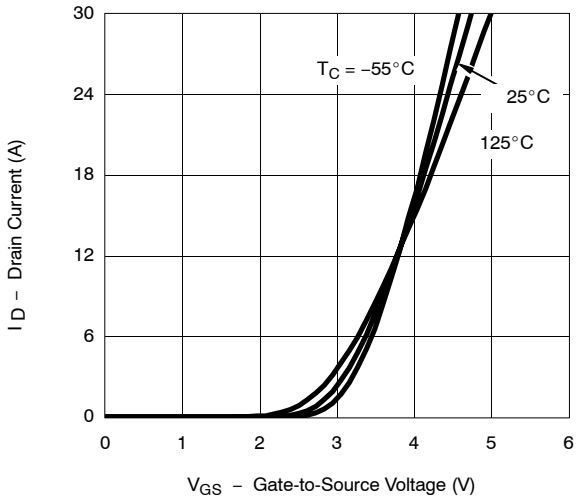
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

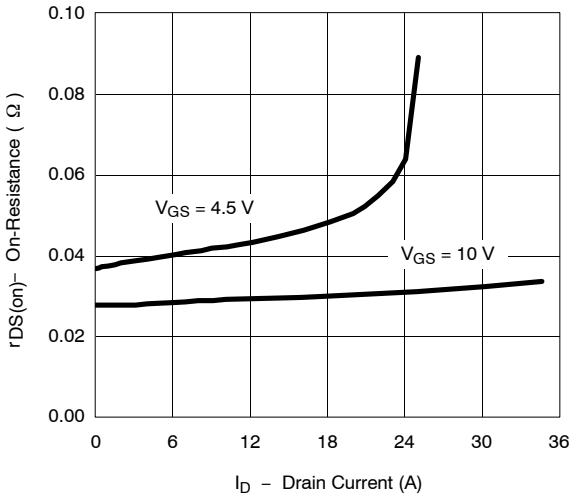
Output Characteristics



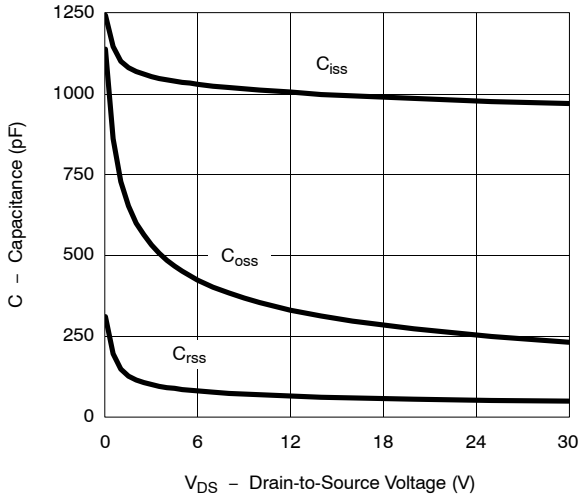
Transfer Characteristics



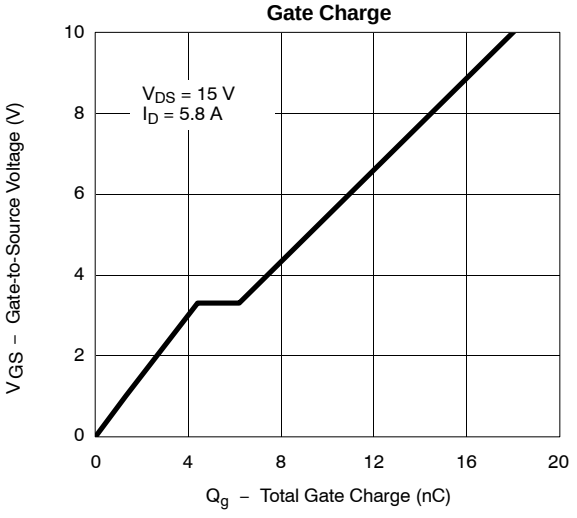
On-Resistance vs. Drain Current



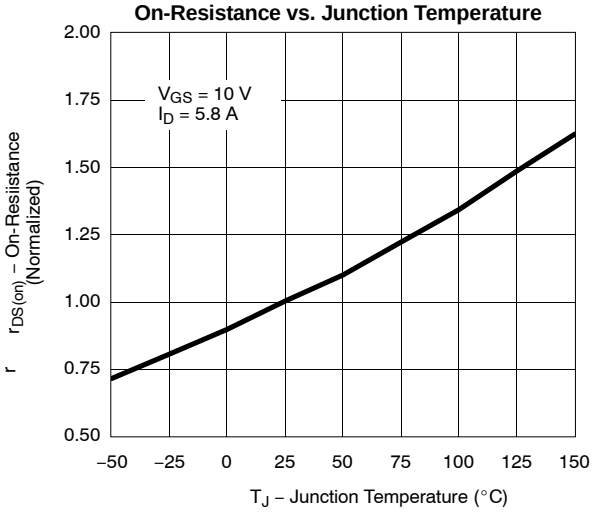
Capacitance



Gate Charge

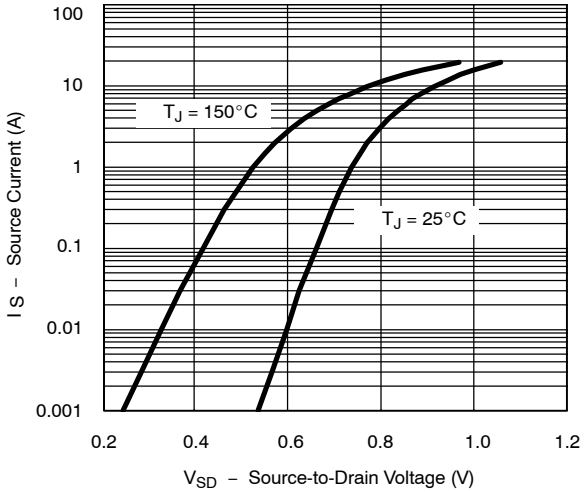


On-Resistance vs. Junction Temperature

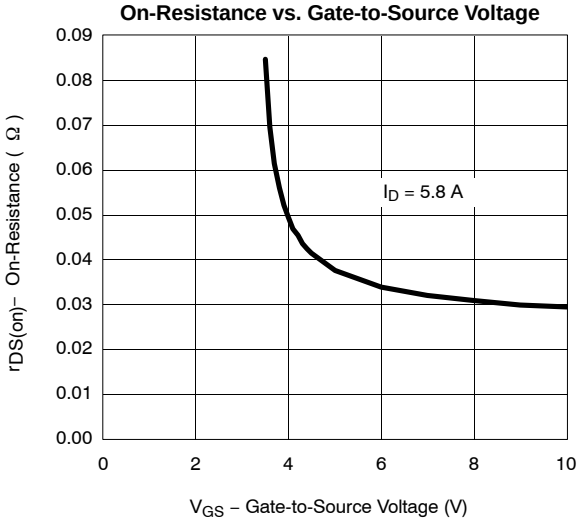


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

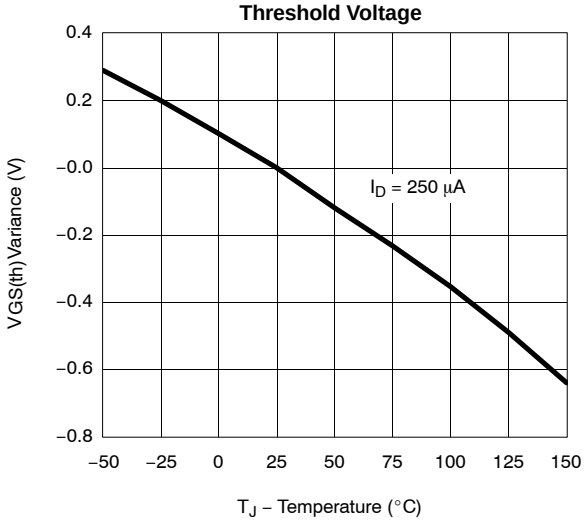
Source-Drain Diode Forward Voltage



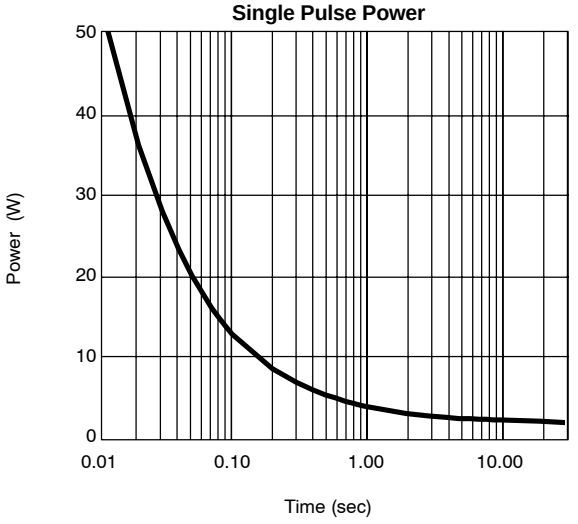
On-Resistance vs. Gate-to-Source Voltage



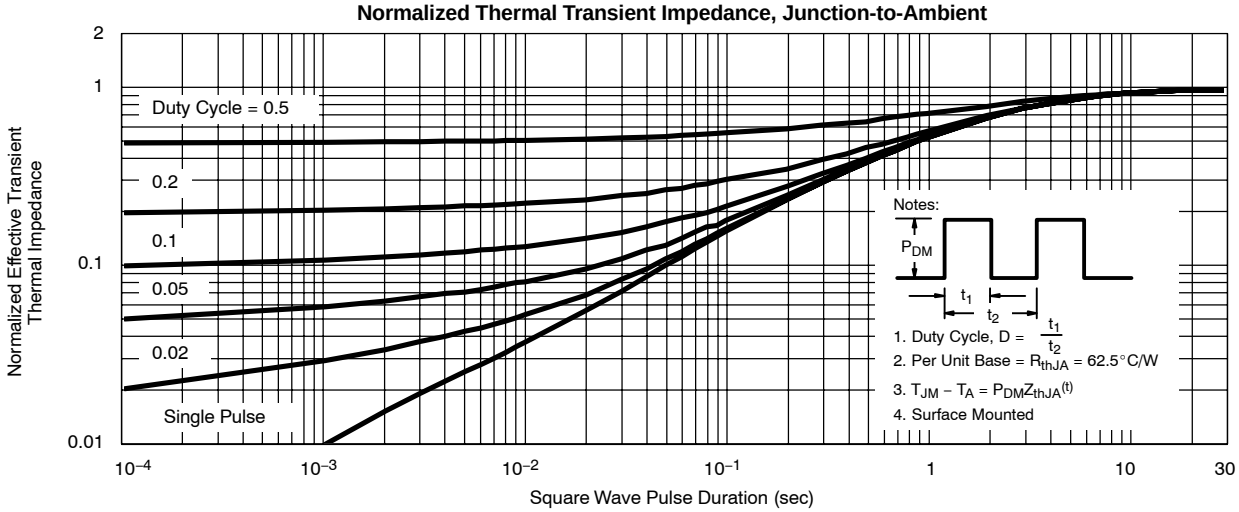
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



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