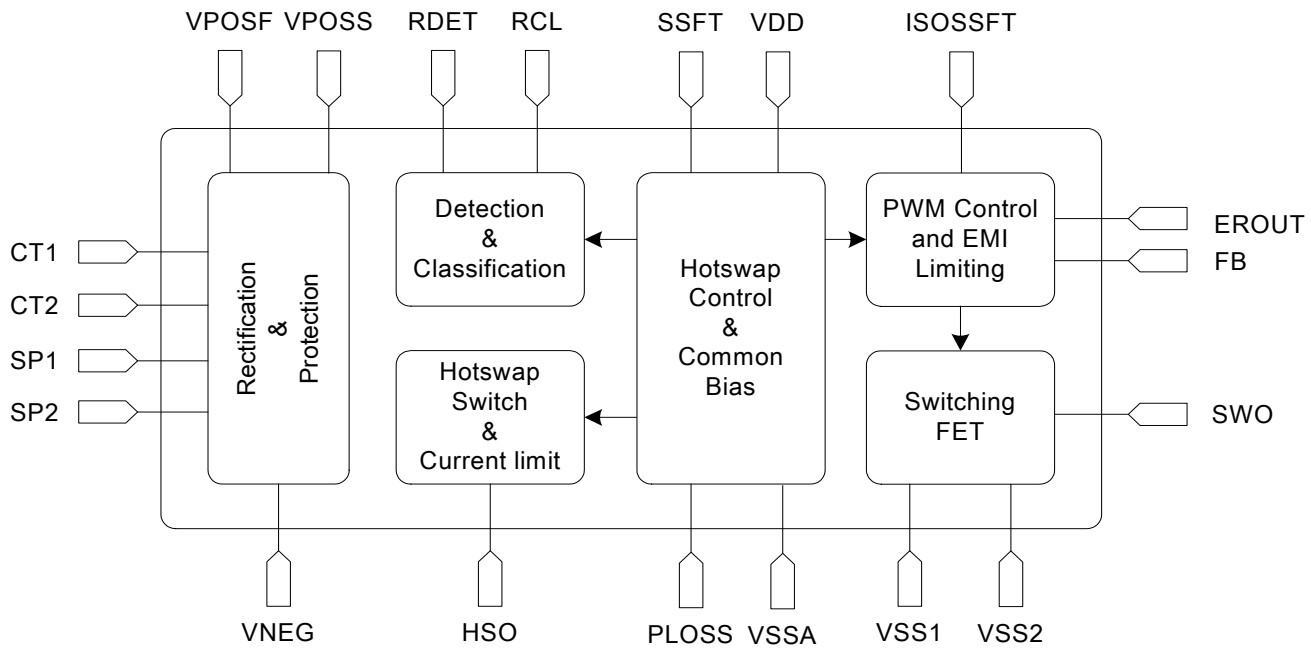
Functional Block Diagram



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Section **Page**

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Description	Symbol	Min	Typ	Max	Units
|CT1 – CT2| or |SP1 – SP2|	VPORT	2.8	—	57	V
Ambient Operating Temperature	TA	–40	25	85	°C

Note: Unless otherwise noted, all voltages referenced to VNEG. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltage and ambient temperature unless otherwise noted.

Table 2. Absolute Maximum Ratings[1]

Type	Description	Rating	Unit
Voltage	CT1 to CT2[2]	–82 to 82	V
	SP1 to SP2[2]	–82 to 82	
	VPOS[3]	–0.7 to 80	
	HSO	–0.7 to 80	
	V_{SS1}, V_{SS2}, or V_{SSA}	–0.7 to 80	
	V_{SS1} to V_{SS2} or V_{SSA}	–0.3 to 0.3	
	SWO[4]	–0.7 to 86	
	$\overline{\text{PLOSS}}$ to VPOS[3]	–80 to 0.7	
	RDET	–0.7 to 80	
	VDD to VSS1, VSS2, or VSSA	–0.3 to 5	
Current	CT1, CT2, SP1, SP2	–5 to 5	A
	VPOS[3]	–5 to 5	
Ambient Temperature	Storage	–65 to 150	°C
	Operating	–40 to 85	

Notes:
1. Unless otherwise noted, all voltages referenced to VNEG. Permanent device damage may occur if the maximum ratings are exceeded. Functional operation should be restricted to those conditions specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may adversely affect device reliability.
2. Transient surge is defined in IEC60060 as a 1000 V impulse of either polarity applied across CT1–CT2 or SP1–SP2. The shape of the impulse shall have a 300 ns full rise time and a 50 µs half fall time, with 201 Ω source impedance.
3. VPOS is equal to VPOSF and VPOSS tied together for test condition purposes.
4. SWO is referenced to V_{SS1} and V_{SS2}, which are normally tied together.

Table 3. Surge Immunity Ratings[1,2,3]

Type	Description	Rating	Unit
CDE[4]	Cable discharge event tolerance	–3.5 to 3.5	kV
ESD (System-Level)	Air discharge (IEC 61000-4-2)	–16.5 to 16.5	kV
	Contact discharge (IEC 61000-4-2)	–8 to 8	kV
ESD (CDM)	JEDEC (JESD22-C101C)	–750 to 750	V
ESD (HBM)	JEDEC (JESD22-A114E)	–2000 to 2000	V
Telephony Voltage Compatibility	IEEE 802.3, Clause 33.5.6	175	Vp

Notes:

1. Permanent device damage may occur if the maximum ratings are exceeded. Functional operation should be restricted to those conditions specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may adversely affect device reliability.
2. For more information regarding system-level surge tolerance, refer to “AN315: Robust Electrical Surge Immunity for PoE PDs through Integrated Protection”.
3. Designs must be compliant with the PCB layout and external component recommendations outlined in the Si3402 EVB User Guide and AN296.
4. J. Deatherage and D. Jones, “Multiple Factors Trigger Cable Discharge Events in Ethernet LANs,” Electronic Design Dec. 4, 2000.

Table 4. Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit
VPORT	Detection	2.7	—	11	V
	Classification	14	—	22	
	UVLO Disabled (Supply turns ON)	—	—	42	
	UVLO Enabled (Supply turns OFF)	30	—	36	
	Transient Surge[1]	62	—	79	
Input Offset Current	VPORT < 10 V	—	—	10	µA
Diode Bridge Leakage	VPORT = 57 V	—	—	25	µA
IPORT Classification[2]	Class 0	0	—	4	mA
	Class 1	9	—	12	
	Class 2	17	—	20	
	Class 3	26	—	30	
	Class 4	36	—	44	
IPORT Operating Current[3]	36 V ≤ VPORT ≤ 57 V	—	2	3.1	mA
Current Limit[4]	Inrush	—	140	—	mA
	Operating	470	—	680	mA
Hotswap FET On-Resistance + R_{SENSE}	36 V ≤ VPORT ≤ 57 V	0.5	—	1.5	Ω
Power Loss VPORT Threshold		27	30	33	V
Switcher Frequency		—	350	—	kHz
Maximum Switcher Duty Cycle[5]	ISOSSFT Connected to VDD	—	50	—	%
Switcher Output Transient Voltage	SWO Voltage with Static Load	—	—	80	V
	SWO Voltage with Switched Load	—	—	86	V
Switching FET On-Resistance		0.3	—	0.86	Ω
Regulated Feedback @ Pin FB[6]	DC Avg.	—	1.23	—	V

Notes:

1. Transient surge defined in IEC60060 as a 1000 V impulse of either polarity applied to CT1–CT2 or SP1–SP2. The shape of the impulse shall have a 300 ns full rise time and a 50 µs half fall time with 201 Ω source impedance.
2. The classification currents are guaranteed only when recommended RCLASS resistors are used, as specified in Table 10.
3. IPORT includes full operating current of switching regulator controller.
4. The PD interface includes dual-level input current limit. At turn-on, before the HSO load capacitor is charged, the current limit is set at the inrush level. After the capacitor has been charged within ~1.25 V of VNEG, the operating current limit is engaged. This higher current limit remains active until the UVLO lower limit has been tripped or until the hotswap switch is sufficiently current-limited to cause a foldback of the HSO voltage.
5. See “AN296: Using the Si3400/1/2 PoE PD Controller in Isolated and Non-Isolated Designs” for more information.
6. Applies to non-isolated applications only (VOUT on schematic in Figure 1).

Table 4. Electrical Characteristics (Continued)

Parameter	Description	Min	Typ	Max	Unit
Regulated Output Voltage Tolerance[6]	Output voltage tolerance @ VOUT	–5	—	5	%
VDD Accuracy @ 0.8 mA	36 V ≤ VPORT ≤ 57 V	4.5	—	5.5	V
Softstart Charging Current	SSFT pin	—	25	—	µA
	ISOSSFT pin	—	13	—	µA
Thermal Shutdown	Junction temperature	—	160	—	ºC
Thermal Shutdown Hysteresis		—	—	25	ºC

Notes:
1. Transient surge defined in IEC60060 as a 1000 V impulse of either polarity applied to CT1–CT2 or SP1–SP2. The shape of the impulse shall have a 300 ns full rise time and a 50 µs half fall time with 201 Ω source impedance.
2. The classification currents are guaranteed only when recommended RCLASS resistors are used, as specified in Table 10.
3. IPORT includes full operating current of switching regulator controller.
4. The PD interface includes dual-level input current limit. At turn-on, before the HSO load capacitor is charged, the current limit is set at the inrush level. After the capacitor has been charged within ~1.25 V of VNEG, the operating current limit is engaged. This higher current limit remains active until the UVLO lower limit has been tripped or until the hotswap switch is sufficiently current-limited to cause a foldback of the HSO voltage.
5. See “AN296: Using the Si3400/1/2 PoE PD Controller in Isolated and Non-Isolated Designs” for more information.
6. Applies to non-isolated applications only (VOUT on schematic in Figure 1).

Table 5. Total Power Dissipation

Description	Test Condition	Min	Typ	Max	Unit
Power Dissipation	VPORT = 50 V, V_{OUT} = 5 V, 2 A	—	1.2	—	W
Power Dissipation*	VPORT = 50 V, V_{OUT} = 5 V, 2 A w/ diode bridges bypassed	—	0.7	—	W

***Note:** Silicon Laboratories recommends the on-chip diode bridges be bypassed when output power requirements are >7 W or in thermally-constrained applications. For more information, see “AN313: Using the Si3402 in High Power Applications”.

Table 6. Package Thermal Characteristics

Parameter	Symbol	Test Condition	Typ	Unit
Thermal Resistance (Junction to Ambient)	θ_{JA}	Still air; assumes a minimum of nine thermal vias are connected to a 2 in^2 heat spreader plane for the package “pad” node (VNEG).	44	°C/W

2. Typical Application Schematics

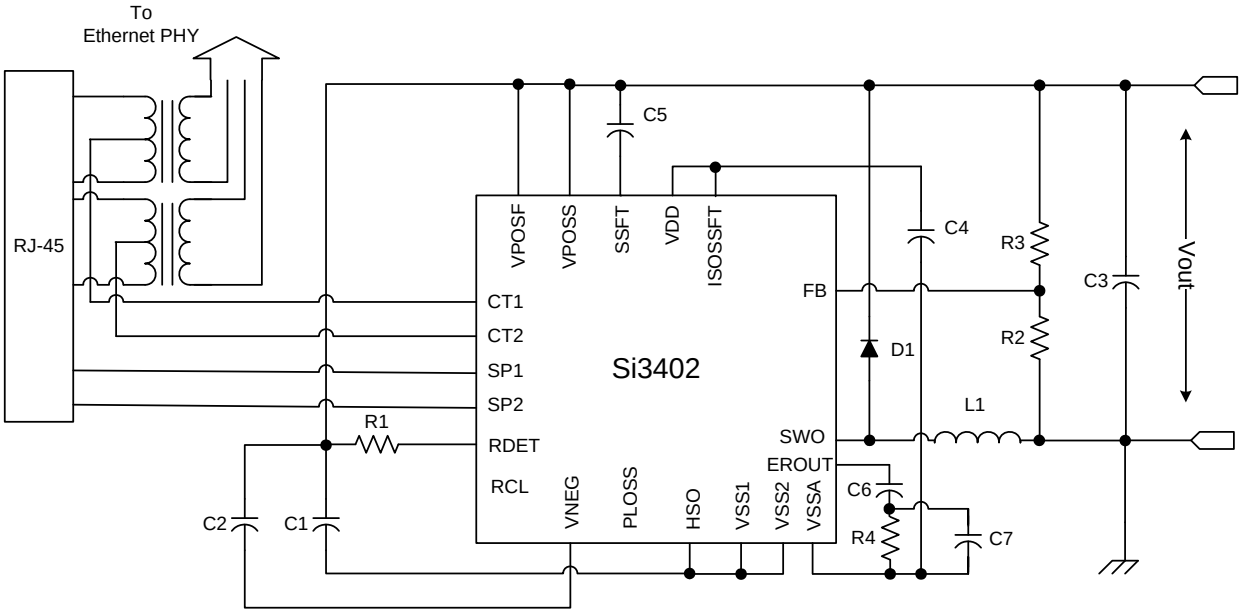

Figure 1. Schematic—Class 0 with Non-Isolated 5 V Output*

***Note:** This is a simplified schematic. See "AN296: Using the Si3400/1/2 PoE PD Controller in Isolated and Non-Isolated Designs" for more details and complete application schematics.

Table 7. Component Listing—Class 0 with 5 V Output

Item	Type	Value	Toler.	Rating	Notes
C1	Capacitor	15 µF	20%	100 V	Switcher supply capacitor. Several parallel capacitors are used for lower ESR.
C2	Capacitor	0.1 µF	20%	100 V	PD input supply capacitor.
C3	Capacitor	1000 µF	20%	10 V	Switcher load capacitor - 1000 µF in parallel with and X5R 22 µF for lower ESR.
C4	Capacitor	0.1 µF	20%	16 V	VDD bypass capacitor.
C5	Capacitor	0.1 µF	10%	16 V	Softstart capacitor.
C6	Capacitor	3.3 nF	10%	16 V	Compensation capacitor.
C7	Capacitor	150 pF	10%	16 V	Compensation capacitor.
R1	Resistor	25.5 kΩ	1%	1/16 W	Detection resistor.
R2	Resistor	8.66 kΩ	1%	1/16 W	Feedback resistor divider.
R3	Resistor	2.87 kΩ	1%	1/16 W	Feedback resistor divider.
R4	Resistor	30.1 kΩ	1%	1/16 W	Feedback compensation resistor.
D1	Diode			100 V	Schottky diode; part no. PDS5100.
L1	Inductor	33 µH	20%	3.5 A	Coilcraft part no. DO5010333.

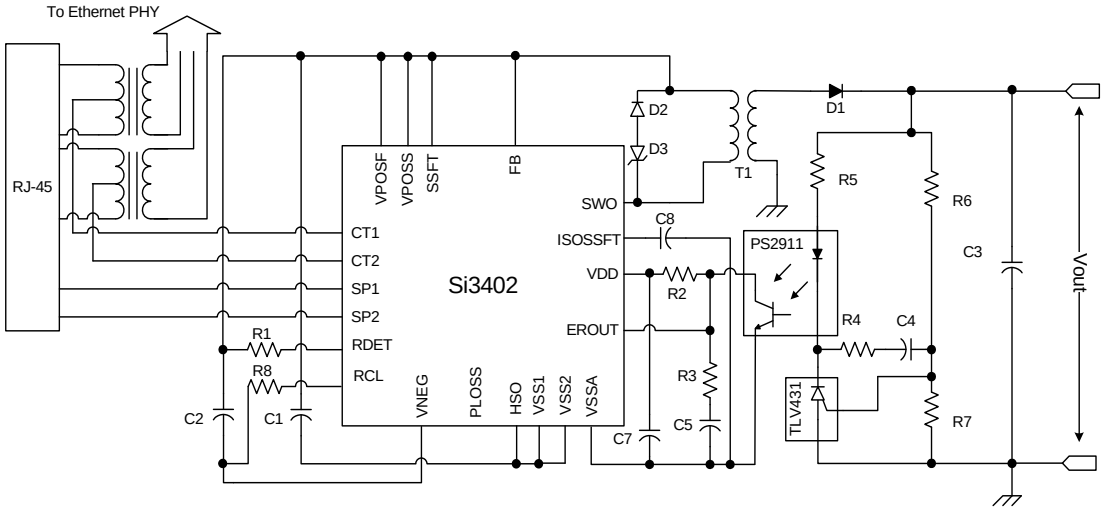

Figure 2. Schematic—Class 1 with Isolated 5.0 V Output*

***Note:** This is a simplified schematic. See "AN296: Using the Si3400/1/2 PoE PD Controller in Isolated and Non-Isolated Designs" for more details and complete application schematics.

Table 8. Components—Class 1 with Isolated 5.0 V Output

Item	Type	Value	Toler.	Rating	Notes
C1	Capacitor	15 µF	20%	100 V	Switcher supply capacitor. Several parallel capacitors are used for lower ESR.
C2	Capacitor	0.1 µF	20%	100 V	PD input supply capacitor.
C3	Capacitor	1100 µF	20%	10 V	Switcher load capacitor. 100 µF in parallel 1000 µF and optional 1 µH inductor for additional filtering.
C4	Capacitor	15 nF	10%	16 V	Feedback compensation.
C5	Capacitor	220 nF	10%	16 V	Feedback compensation.
C7	Capacitor	0.1 µF	20%	16 V	VDD bypass capacitor.
C8	Capacitor	1 µF	20%	16 V	Isolated mode soft start (tie ISOSSFT to VDD if this feature is not used).
R1	Resistor	25.5 kΩ	1%	1/16 W	Detection resistor.
R2	Resistor	4.99 kΩ	1%	1/16 W	Pull-up resistor.
R3	Resistor	100 Ω	1%	1/16 W	Feedback compensation resistor.
R4	Resistor	10 kΩ	1%	1/16 W	Feedback compensation resistor.
R5	Resistor	2.05 kΩ	1%	1/16 W	Pull-up resistor.
R6	Resistor	36.5 kΩ	1%	1/16 W	Feedback resistor divider.
R7	Resistor	12.1 kΩ	1%	1/16 W	Feedback resistor divider.
R8	Resistor	127 Ω	1%	1/16 W	Classification resistor.
D1	Diode	10 A		40 V	Schottky diode; part no. PN PDS1040.
D2	Diode	1 A		100 V	Snubber diode (1N4148)
D3	Diode	15 V		9 A	Snubber diode (DFLT15A)
T1	Transformer	40 µH			Coilcraft part number FA2672 (5 V).
PS2911	Optocoupler				
TLV431	Voltage reference				

3. Functional Description

The Si3402 consists of two major functions: a hotswap controller/interface and a complete pulse-width-modulated switching regulator (controller and power FET).

3.1. Overview

The hotswap interface of the Si3402 provides the complete front end of an 802.3-compliant PD. The Si3402 also includes two full diode bridges, a transient voltage surge suppressor, detection circuit, classification current source, and dual-level hotswap current limiting switch. This high level of integration enables direct connection to the RJ-45 connector, simplifies system design, and provides significant advantages for reliability and protection. The Si3402 requires only four standard external components (detection resistor, optional classification resistor, load capacitor, and input capacitor) to create a fully 802.3-compliant interface. For more information about supporting higher-power applications, see “AN313: Using the Si3402 in High Power Applications” and “AN314: Power Combining Circuit for PoE for up to 18.5 W Output”.

The Si3402 integrates a complete pulse-width modulated switching regulator that includes the controller and power FET. The switching regulator utilizes a constant frequency pulse-width modulated controller optimized for all possible load conditions in PoE applications. The regulator integrates a low on-resistance (Ron) switching power MOSFET that minimizes power dissipation, increases overall regulator efficiency, and simplifies system design. An integrated error amplifier, precision reference, and programmable soft-start current source provide the flexibility of using a non-isolated buck regulator topology or an isolated flyback regulator topology.

The Si3402 is designed to operate with both 802.3-compliant Power Sourcing Equipment (PSE) and pre-standard (legacy) PSEs that do not adhere to the 802.3 specified inrush current limits. The Si3402 is compatible with compliant and legacy PSEs because it uses two levels for the hotswap current limits. By setting the initial inrush current limit to a low level, a PD based on the Si3402 minimizes the current drawn from either a compliant or legacy PSE during startup. After powering up, the Si3402 automatically switches to a higher-level current limit, thereby allowing the PD to consume up to 12.95 W (the max power allowed by the 802.3 specification).

The inrush current limit specified by the 802.3 standard can generate high transient power dissipation in the PD. By properly sizing the devices and implementing on-chip thermal protection, the Si3402 can go through multiple turn-on sequences without overheating the package or damaging the device. The switching regulator power MOSFET has been conservatively designed and sized to withstand the high peak currents created when converting a high-voltage, low-current supply into a low-voltage, high-current supply. Excessive power cycling or short circuit faults will engage the thermal overload protection to prevent the onboard power MOSFETs from exceeding their safe and reliable operating ranges.

3.2. PD Hotswap Controller

The Si3402 hotswap controller changes its mode of operation based on the input voltage applied to the CT1 and CT2 pins or the SP1 and SP2 pins, the 802.3-defined modes of operation, and internal controller requirements. Table 9 defines the modes of operation for the hotswap interface.

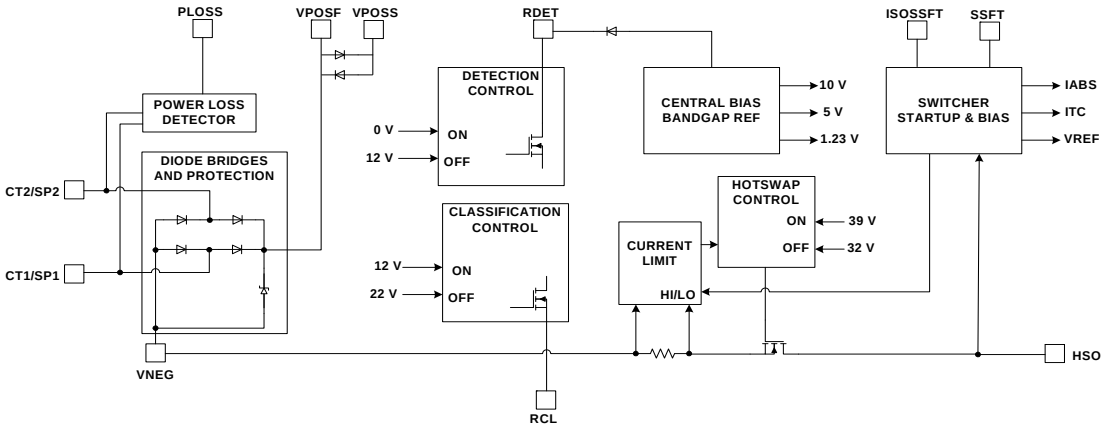

Figure 3. Hotswap Block Diagram

Table 9. Hotswap Interface Modes

Input Voltage (|CT1-CT2| or |SP1-SP2|)	Si3402 Mode
0 to 2.7 V	Inactive
2.7 to 11 V	Detection signature
11 to 14 V	Detection turns off and internal bias starts
14 to 22 V	Classification signature
22 to 42 V	Transition region
42 up to 57 V	Switcher operating mode (hysteresis limit based on rising input voltage)
57 down to 36 V	Switcher operating mode (hysteresis limit based on falling input voltage)

3.2.1. Rectification Diode Bridges and Surge Suppressor

The 802.3 specification defines the input voltage at the RJ-45 connector of the PD with no reference to polarity. In other words, the PD must be able to accept power of either polarity at each of its inputs. This requirement necessitates the use of two sets of diode bridges, one for the CT1 and CT2 pins and one for the SP1 and SP2 pins to rectify the voltage. Furthermore, the standard requires that a PD withstand a high-voltage transient surge consisting of a 1000 V common-mode impulse with 300 ns rise time and 50 µs half fall time. Typically, the diode bridge and the surge suppressor have been implemented externally, adding cost and complexity to the PD system design.

The diode bridge* and the surge suppressor have been integrated into the Si3402, thus reducing system cost and design complexity.

***Note:** Silicon Laboratories recommends that on-chip diode bridges be bypassed when >7 W of output power is required.

By integrating the diode bridges, the Si3402 gains access to the input side of the diode bridge. Monitoring the voltage at the input of the diode bridges instead of the voltage across the load capacitor provides the earliest indication of a power loss. This true early power loss indicator, $\overline{\text{PLOSS}}$, provides a local microcontroller time to save states and shut down gracefully before the load capacitor discharges below the minimum 802.3-specified operating voltage of 36 V. Integration of the surge suppressor enables optimization of the clamping voltage and guarantees protection of all connected circuitry.

As an added benefit, the transient surge suppressor, when tripped, actively disables the hotswap interface and switching regulator, preventing downstream circuits from encountering the high-energy transients.

3.2.2. Detection

In order to identify a device as a valid PD, a PSE will apply a voltage in the range of 2.8 to 10 V on the cable and look for the 25.5 kΩ signature resistor. The Si3402 will react to voltages in this range by connecting an external 25.5 kΩ resistor between VPOS and VNEG. This external resistor and internal low-leakage control circuitry create the proper signature to alert the PSE that a valid PD has been detected and is ready to have power applied. The internal hotswap switch is disabled during this time to prevent the switching regulator and attached load circuitry from generating errors in the detection signature.

Since the Si3402 integrates the diode bridges, the IC can compensate for the voltage and resistance effects of the diode bridges. The 802.3 specification requires that the PSE use a multi-point, $\Delta V/\Delta I$ measurement technique to remove the diode-induced dc offset from the signature resistance measurement. However, the specification does not address the diode's nonlinear resistance and the error induced in the signature resistor measurement. Since the diode's resistance appears in series with the signature resistor, the PD system must find some way of compensating for this error. In systems where the diode bridges are external, compensation is difficult and suffers from errors. Since the diode bridges are integrated in the Si3402, the IC can compensate for this error by offsetting resistance across all operating conditions and thus meeting the 802.3 requirements. An added benefit is that this function can be tested during the IC's automated testing step, guaranteeing system compliance when used in the final PD application. For more information about supporting higher-power applications (above 12.95 W), see "AN313: Using the Si3402 in High Power Applications" and "AN314: Power Combining Circuit for PoE for up to 18.5 W Output".

3.2.3. Classification

Once the PSE has detected a valid PD, the PSE may classify the PD for one of five power levels or classes. A class is based on the expected power consumption of the powered device. An external resistor sets the nominal class current that can then be read by the PSE to determine the proper power requirements of the PD.

When the PSE presents a fixed voltage between 15.5 V and 20.5 V to the PD, the Si3402 asserts the class current from VPOS through the RCL resistor. The resistor values associated with each class are shown in Table 10.

Table 10. Class Resistor Values

Class	Usage	Peak Power Levels	Nominal Class Current	RCL Resistor (1%, 1/16 W)
0	Default	0.44 to 12.95 W	< 4 mA	> 1.33 kΩ (or open circuit)
1	Optional	0.44 to 3.84 W	10.5 mA	127 Ω
2	Optional	3.84 to 6.49 W	18.5 mA	69.8 Ω
3	Optional	6.49 to 12.95 W	28 mA	45.3 Ω
4	PoE+	12.95 to 17 W	40 mA	30.9 Ω

The 802.3 specification limits the classification time to 75 ms to limit the power dissipated in the PD. If the PSE classification period exceeds 75 ms and the die temperature rises above the thermal shutdown limits, the thermal protection circuit will engage and disable the classification current source in order to protect the Si3402. The Si3402 stays in classification mode until the input voltage exceeds 22 V (the upper end of its classification operation region).

3.2.4. Under Voltage Lockout

The 802.3 standard specifies the PD to turn on when the line voltage rises to 42 V and for the PD to turn off when the line voltage falls to 30 V. The PD must also maintain a large on-off hysteresis region to prevent wiring losses between the PSE and the PD from causing startup oscillation.

The Si3402 incorporates an undervoltage lockout (UVLO) circuit to monitor the line voltage and determine when to apply power to the integrated switching regulator. Before the power is applied to the switching regulator, the hotswap switch output (HSO) pin is high-impedance and typically follows VPOS as the input is ramped (due to the discharged switcher supply capacitor). When the input voltage rises above the UVLO turn-on threshold, the Si3402 begins to turn on the internal hotswap power MOSFET. The switcher supply capacitor begins to charge up under the current limit control of the Si3402, and the HSO pin transitions from VPOS to VNEG. The Si3402 includes hysteretic UVLO circuits to maintain power to the load until the input voltage falls below the UVLO turn-off threshold. Once the input voltage falls below 30 V, the internal hotswap MOSFET is turned off.

3.2.5. Dual Current Limit and Switcher Turn-On

The Si3402 implements dual current limits. While the hotswap MOSFET is charging the switcher supply capacitor, the Si3402 maintains a low current limit. The switching regulator is disabled until the voltage across the hotswap MOSFET becomes sufficiently low, indicating the switcher supply capacitor is almost completely charged. When this threshold is reached, the switcher is activated, and the hotswap current limit is increased. This threshold also has hysteresis to prevent systemic oscillation as the switcher begins to draw current and the current limit is increased, which allows resistive losses in the cable to effectively decrease the input supply.

The Si3402 stays in a high-level current limit mode until the input voltage drops below the UVLO turn-off threshold or excessive power is dissipated in the hotswap switch. This dual level current limit allows the system designer to design powered devices for use with both legacy and compliant PoE systems.

An additional feature of the dual current limit circuitry is foldback current limiting in the event of a fault condition. When the current limit is switched to the higher level, 400 mA of current can be drawn by the PD. Should a fault cause more than this current to be consumed, the voltage across the hotswap MOSFET will increase to clamp the maximum amount of power consumed. The power dissipated by the MOSFET can be very high under this condition. If the fault is very low impedance, the voltage across the hotswap MOSFET will continue to rise until the lower current limit level is engaged, further reducing the dissipated power. If the fault condition remains, the thermal overload protection circuitry will eventually engage and shut down the hotswap interface and switching regulator. The foldback current limiting occurs much faster than the thermal overload protection and is, therefore, necessary for comprehensive protection of the hotswap MOSFET.

3.2.6. Power Loss Indicator

A situation can occur in which power is lost at the input of the diode bridge and the hotswap controller does not detect the fault due to the VPOS to VNEG capacitor maintaining the voltage. In such a situation, the PD can remain operational for hundreds of microseconds despite the PSE having removed the line voltage. If it is recognized early enough, the time from power loss to power failure can provide valuable time to gracefully shut down an application.

Due to integration of the diode bridges, the Si3402 is able to instantaneously detect the removal of the line voltage and provide that early warning signal to the PD application. The $\overline{\text{PLOSS}}$ pin is an open drain output that pulls up to VPOS when a line voltage greater than 27 V is applied. When the line voltage falls below 27 V, the output becomes high-impedance, allowing an external pull-down resistor to change the logic state of PLOSS. The benefit of this indicator is that the powered device may include a microcontroller that can quickly save its memory or operational state before draining the supply capacitors and powering itself down. This feature can help improve overall manageability in applications, such as wireless access points.

3.3. Switching Regulator

Power over Ethernet (PoE) applications fall into two broad categories, isolated and non-isolated. Non-isolated systems can be used when the powered device is self-contained and does not provide external conductors to the user or another application. Non-isolated applications include wireless access points and security cameras. In these applications, there is no explicit need for dc isolation between the switching regulator output and the hotswap interface. An isolated system must be used when the powered device interfaces with other self-powered equipment or has external conductors accessible to the user or other applications. For proper operation, the regulated output supply of the switching regulator must not have a dc electrical path to the hotswap interface or switching regulator primary side. Isolated applications include point-of-sale terminals where the user can touch the grounded metal chassis.

The application determines the converter topology. An isolated application will require a flyback transformer-based switching topology while a non-isolated application can use an inductor-based buck converter topology. In the isolated case, dc isolation is achieved through a transformer in the forward path and a voltage reference plus opto-isolator in the feedback path. The application circuit shown in Figure 2 is an example of such a topology. The non-isolated application in Figure 1 makes use of a single inductor as the energy conversion element, and the feedback signal is directly supplied into the internal error amplifier. As can be seen from the application circuits, the isolated topology has an increased number of components, thus increasing the bill of materials (BOM) and system footprint.

To optimize cost and ease implementation, each application should be evaluated for its isolated or non-isolated requirements.

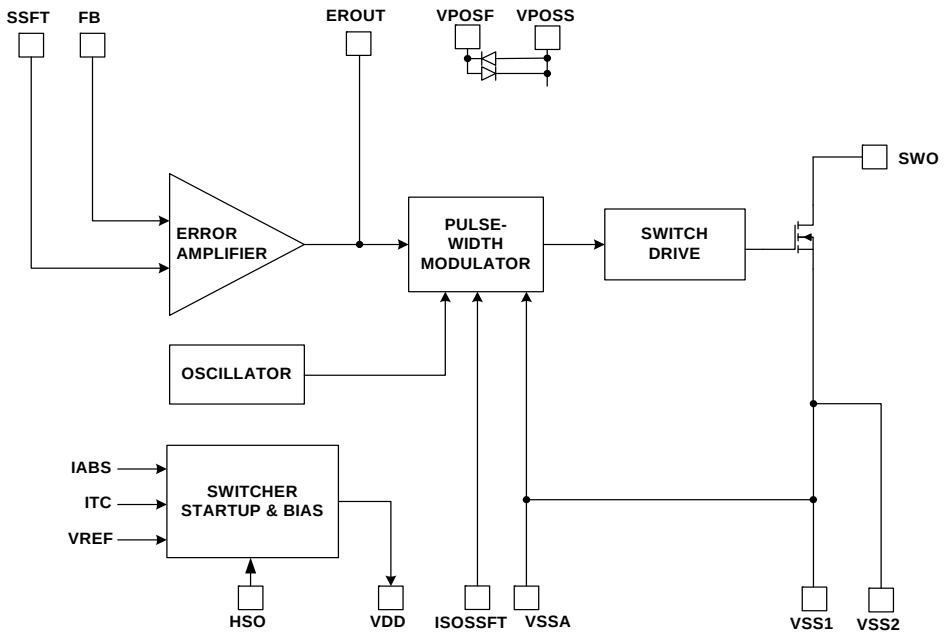

Figure 4. Switcher Block Diagram

3.3.1. Switcher Startup

The switching regulator is disabled until the hotswap interface has both identified itself to the PSE and charged the supply capacitor needed to filter the switching regulator's high-current transients. Once the supply capacitor is charged, the hotswap controller engages the internal bias currents and supplies used by the switcher. Additionally, the soft-start current begins to charge the external soft-start capacitor.

The voltage developed across the soft-start capacitor serves as the error amplifier's reference in the non-isolated application. Ramping this voltage slowly allows the switching regulator to bring up the regulated output voltage in a controlled manner. Controlling the initial startup of the regulated voltage restrains power dissipation in the switching FET and prevents overshoot and ringing in the output supply voltage.

In the isolated mode, a capacitor connected between pins ISOSSFT and VSSA slowly ramps the duty cycle clamp in the PWM circuit. Tie this pin to VDD if it is not used.

3.3.2. Switching Regulator Operation

The switching regulator of the Si3402 is constant-frequency, pulse-width-modulated (PWM), and controller integrated with switching power FETs optimized for the output power range defined by the 802.3 specification.

Once the hotswap interface has ensured proper turn-on of the switching regulator controller, the switcher is fully operational. An internal free-running oscillator and internal precision voltage reference are fed into the pulse-width modulator. The output of the error amplifier (either internal for non-isolated applications or external for isolated applications) is also routed into the PWM and determines the slicing of the oscillator.

The PWM controls the switching FET drive circuitry. A significant advantage of integrating the switching power FET onto the same monolithic IC as the switching regulator controller is the ability to precisely adjust the drive strength and timing to the FET's sizable gate, resulting in high regulator efficiency. Furthermore, current-limiting circuitry prevents the switching FET from sinking too much current, dissipating too much power, and becoming damaged. Thermal overload protection provides a secondary level of protection.

The flexibility of the Si3402's switching regulator allows the system designer to realize either the isolated or non-isolated application circuitry using a single device. In operation, the integration of the switching FET allows tighter control and more efficient operation than a general-purpose switching regulator coupled with a general-purpose external FET.

3.3.3. Flyback Snubber

Extremely high voltages can be generated by the inductive kick associated with the leakage inductance of the primary side of the flyback transformer used in isolated applications.

Refer to “AN296: Using the Si3400/1/2 PoE PD Controller in Isolated and Non-Isolated Designs” for more information on the snubber.

4. Pin Descriptions

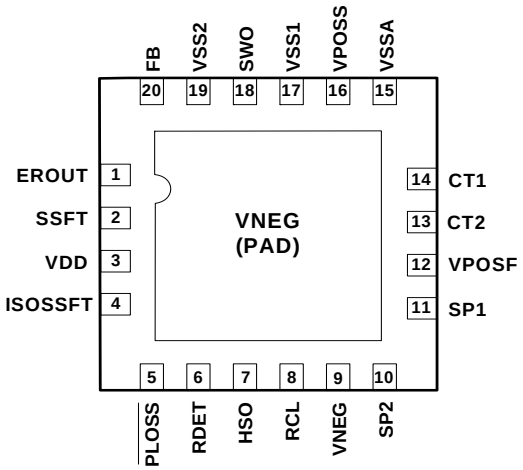

Table 11. Si3402 Pin Descriptions (Top View)

Pin#	Name	Description
1	EROUT	Error-amplifier output and PWM input; directly connected to opto-coupler in isolated application.
2	SSFT	Soft-start output pin ramps voltage across external soft-start capacitor to allow switcher to ramp output slowly.
3	VDD	5 V supply rail for switcher; provides drive for opto-coupler.
4	ISOSSFT	Isolated mode soft start enable input.
5	$\overline{\text{PLOSS}}$	Early power loss indicator; open drain output is pulled to VPOS when VPORT is applied.
6	RDET	Input pin for external precision detection resistor; also used for establishing absolute current reference.
7	HSO	Hotswap switch output; connects to VNEG through hotswap switch.
8	RCL	Input pin for external precision classification resistor; float if optional RCLASS is unused.
9, Pad	VNEG	Rectified high-voltage supply, negative rail. Must be connected to thermal PAD node (VNEG) on package bottom. This thermal pad must be connected to VNEG (pin #9) as well as a 2 in^2 heat spreader plane using a minimum of nine thermal vias.
10	SP2	High-voltage supply input from spare pair; polarity-insensitive.
11	SP1	High-voltage supply input from spare pair; polarity-insensitive.
12	VPOSF	Rectified high-voltage supply, positive rail (force node)
13	CT2	High-voltage supply input from center tap of Ethernet transformer; polarity-insensitive.
14	CT1	High-voltage supply input from center tap of Ethernet transformer; polarity-insensitive.
15	VSSA	Analog ground.
16	VPOSS	Rectified high-voltage supply, positive rail sense node.
17	VSS1	Negative supply rail for switcher; externally tied to HSO.
18	SWO	Switching transistor output; drain of switching N-FET.
19	VSS2	Negative supply rail for switcher; externally tied to HSO.
20	FB	Regulated feedback input in non-isolated application.

5. Package Outline

Figure 5 illustrates the package details for the Si3402. Table 12 lists the values for the dimensions shown in the illustration.

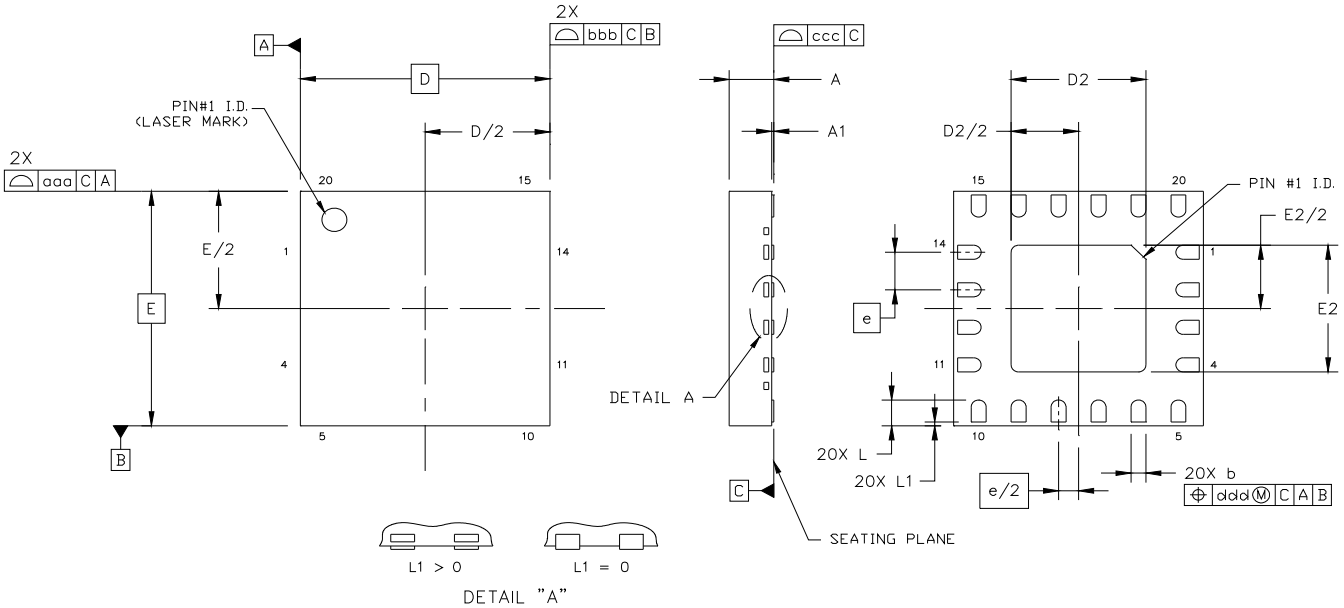

Figure 5. 20-Lead Quad Flat No-Lead Package (QFN)

Table 12. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.25	0.30	0.35
D		5.00 BSC.	
D2	2.60	2.70	2.80
e		0.80 BSC.	
E		5.00 BSC.	
E2	2.60	2.70	2.80
L	0.50	0.55	0.60
L1	0.00	—	0.10
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VHHB-1.

6. Recommended Land Pattern

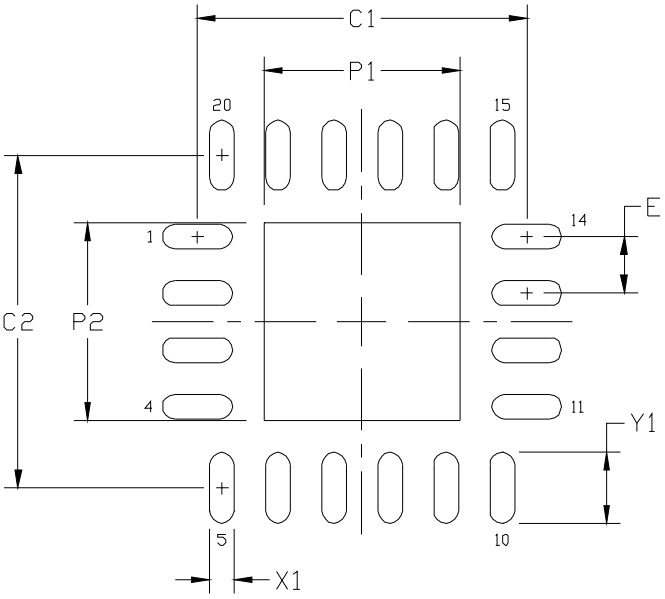

Figure 6. Si3402 Recommended Land Pattern

Table 13. PCB Land Pattern Dimensions

Symbol	Min	Nom	Max
P1	2.70	2.75	2.80
P2	2.70	2.75	2.80
X1	0.25	0.30	0.35
Y1	0.90	0.95	1.00
C1	4.70		
C2	4.70		
E	0.80		

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
8. A 2x2 array of 1.2 mm square openings on 1.4 mm pitch should be used for the center ground pad.

Card Assembly

9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7. Ordering Guide

Part Number[1,2]	Package	Temp Range	Recommended Maximum Output Power[3]
Si3402-A-GM	20-pin QFN, Pb-free; RoHS compliant	–40 to 85 °C	≤ 10 W (IEEE 802.3 systems) 17 W (proprietary high power)

Notes:

1. "X" denotes product revision.
2. Add an "R" at the end of the part number to denote tape and reel option.
3. Refer to "AN313: Using the Si3402 in High Power Applications" and "AN314: Power Combining Circuit for PoE for up to 18.5 W Output" for more information about using the Si3402 in higher power applications.

8. Device Marking Diagram

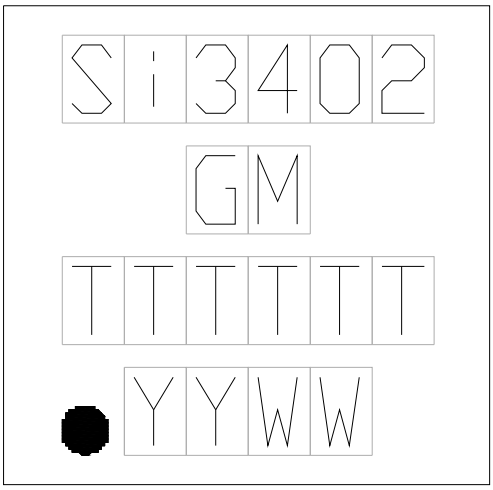

Figure 7. Device Marking Diagram

Table 14. Device Marking Table

Line #	Text Value	Description
1	Si3402	Base part number. This is not the “Ordering Part Number” since it does not contain a specific revision. Refer to "7. Ordering Guide" on page 18 for complete ordering information.
2	GM	G = Industrial temperature range. M = QFN package.
3	TTTTTT	Trace code (assigned by the assembly subcontractor).
4	Circle = 20 mils Diameter (Bottom-Left Justified)	Pin 1 identifier.
	YY	Assembly year.
	WW	Assembly week.

DOCUMENT CHANGE LIST

Revision 1.0 to Revision 1.1

- Added "6. Recommended Land Pattern" on page 17.

Revision 1.1 to Revision 1.2

- Added "8. Device Marking Diagram" on page 19.

Revision 1.2 to Revision 1.3

- Deleted old Table 2 on page 4.
- Updated Table 2, “Absolute Maximum Ratings[1],” on page 4.
- Updated Table 3, “Surge Immunity Ratings[1],[2],[3],” on page 5.
- Updated Table 4, “Electrical Characteristics,” on page 6.

Revision 1.3 to Revision 1.31

- Updated Table 11, “Si3402 Pin Descriptions (Top View),” on page 15.

NOTES:

CONTACT INFORMATION

Silicon Laboratories Inc.

400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Please visit the Silicon Labs Technical Support web page:
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