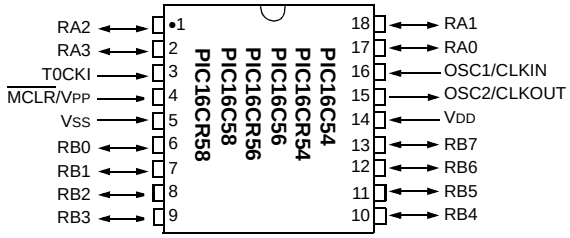
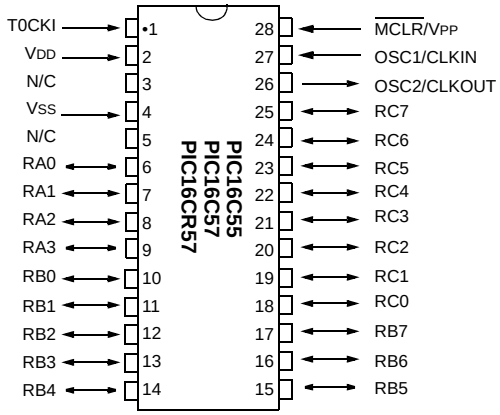
## Pin Diagrams

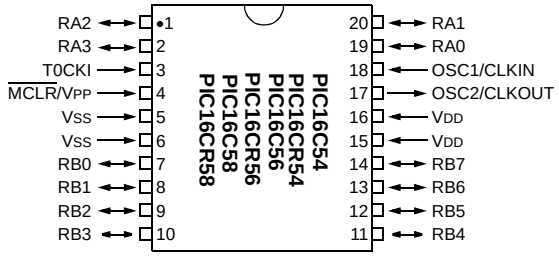
PDIP, SOIC, Windowed CERDIP



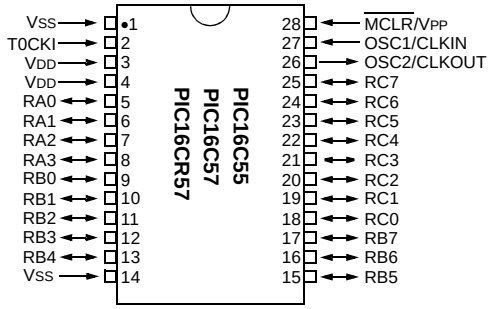

PDIP, SOIC, Windowed CERDIP




SSOP




SSOP




## Device Differences

| Device | Voltage Range | Oscillator Selection (Program) | Oscillator | Process Technology (Microns) | ROM Equivalent | $\overline{\text{MCLR}}$ Filter |
|---|---|---|---|---|---|---|
| PIC16C54 | 2.5-6.25 | Factory | See **Note 1** | 1.2 | PIC16CR54A | No |
| PIC16C54A | 2.0-6.25 | User | See **Note 1** | 0.9 | — | No |
| PIC16C54C | 2.5-5.5 | User | See **Note 1** | 0.7 | PIC16CR54C | Yes |
| PIC16C55 | 2.5-6.25 | Factory | See **Note 1** | 1.7 | — | No |
| PIC16C55A | 2.5-5.5 | User | See **Note 1** | 0.7 | — | Yes |
| PIC16C56 | 2.5-6.25 | Factory | See **Note 1** | 1.7 | — | No |
| PIC16C56A | 2.5-5.5 | User | See **Note 1** | 0.7 | PIC16CR56A | Yes |
| PIC16C57 | 2.5-6.25 | Factory | See **Note 1** | 1.2 | — | No |
| PIC16C57C | 2.5-5.5 | User | See **Note 1** | 0.7 | PIC16CR57C | Yes |
| PIC16C58B | 2.5-5.5 | User | See **Note 1** | 0.7 | PIC16CR58B | Yes |
| PIC16CR54A | 2.5-6.25 | Factory | See **Note 1** | 1.2 | N/A | Yes |
| PIC16CR54C | 2.5-5.5 | Factory | See **Note 1** | 0.7 | N/A | Yes |
| PIC16CR56A | 2.5-5.5 | Factory | See **Note 1** | 0.7 | N/A | Yes |
| PIC16CR57C | 2.5-5.5 | Factory | See **Note 1** | 0.7 | N/A | Yes |
| PIC16CR58B | 2.5-5.5 | Factory | See **Note 1** | 0.7 | N/A | Yes |

**Note 1:** If you change from this device to another device, please verify oscillator characteristics in your application.

**Note:** The table shown above shows the generic names of the PIC16C5X devices. For device varieties, please refer to Section 2.0.

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# 8-Bit EPROM/ROM-Based CMOS Microcontrollers

## 1.0 GENERAL DESCRIPTION

The PIC16C5X from Microchip Technology is a family of low cost, high performance, 8-bit fully static, EPROM/ROM-based CMOS microcontrollers. It employs a RISC architecture with only 33 single word/single cycle instructions. All instructions are single cycle except for program branches which take two cycles. The PIC16C5X delivers performance in an order of magnitude higher than its competitors in the same price category. The 12-bit wide instructions are highly symmetrical resulting in 2:1 code compression over other 8-bit microcontrollers in its class. The easy to use and easy to remember instruction set reduces development time significantly.

The PIC16C5X products are equipped with special features that reduce system cost and power requirements. The Power-on Reset (POR) and Device Reset Timer (DRT) eliminate the need for external RESET circuitry. There are four oscillator configurations to choose from, including the power saving LP (Low Power) oscillator and cost saving RC oscillator. Power saving SLEEP mode, Watchdog Timer and Code Protection features improve system cost, power and reliability.

The UV erasable CERDIP packaged versions are ideal for code development, while the cost effective One Time Programmable (OTP) versions are suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in OTP microcontrollers, while benefiting from the OTP's flexibility.

The PIC16C5X products are supported by a full featured macro assembler, a software simulator, an in-circuit emulator, a low cost development programmer and a full featured programmer. All the tools are supported on IBM® PC and compatible machines.

### 1.1 Applications

The PIC16C5X series fits perfectly in applications ranging from high speed automotive and appliance motor control to low power remote transmitters/receivers, pointing devices and telecom processors. The EPROM technology makes customizing application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages, for through hole or surface mounting, make this microcontroller series perfect for applications with space limitations. Low cost, low power, high performance ease of use and I/O flexibility make the PIC16C5X series very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, replacement of "glue" logic in larger systems, co-processor applications).

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**TABLE 1-1: PIC16C5X FAMILY OF DEVICES**

| Features | PIC16C54 | PIC16CR54 | PIC16C55 | PIC16C56 | PIC16CR56 |
|---|---|---|---|---|---|
| Maximum Operation Frequency | 40 MHz | 20 MHz | 40 MHz | 40 MHz | 20 MHz |
| EPROM Program Memory (x12 words) | 512 | — | 512 | 1K | — |
| ROM Program Memory (x12 words) | — | 512 | — | — | 1K |
| RAM Data Memory (bytes) | 25 | 25 | 24 | 25 | 25 |
| Timer Module(s) | TMR0 | TMR0 | TMR0 | TMR0 | TMR0 |
| I/O Pins | 12 | 12 | 20 | 12 | 12 |
| Number of Instructions | 33 | 33 | 33 | 33 | 33 |
| Packages | 18-pin DIP, SOIC; 20-pin SSOP | 18-pin DIP, SOIC; 20-pin SSOP | 28-pin DIP, SOIC; 28-pin SSOP | 18-pin DIP, SOIC; 20-pin SSOP | 18-pin DIP, SOIC; 20-pin SSOP |
| All PIC® Family devices have Power-on Reset, selectable Watchdog Timer, selectable Code Protect and high I/O current capability. | | | | | |

| Features | PIC16C57 | PIC16CR57 | PIC16C58 | PIC16CR58 |
|---|---|---|---|---|
| Maximum Operation Frequency | 40 MHz | 20 MHz | 40 MHz | 20 MHz |
| EPROM Program Memory (x12 words) | 2K | — | 2K | — |
| ROM Program Memory (x12 words) | — | 2K | — | 2K |
| RAM Data Memory (bytes) | 72 | 72 | 73 | 73 |
| Timer Module(s) | TMR0 | TMR0 | TMR0 | TMR0 |
| I/O Pins | 20 | 20 | 12 | 12 |
| Number of Instructions | 33 | 33 | 33 | 33 |
| Packages | 28-pin DIP, SOIC; 28-pin SSOP | 28-pin DIP, SOIC; 28-pin SSOP | 18-pin DIP, SOIC; 20-pin SSOP | 18-pin DIP, SOIC; 20-pin SSOP |
| All PIC® Family devices have Power-on Reset, selectable Watchdog Timer, selectable Code Protect and high I/O current capability. | | | | |

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## 2.0 PIC16C5X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in this section. When placing orders, please use the PIC16C5X Product Identification System at the back of this data sheet to specify the correct part number.

For the PIC16C5X family of devices, there are four device types, as indicated in the device number:

1. **C**, as in PIC16**C**54C. These devices have EPROM program memory and operate over the standard voltage range.
2. **LC**, as in PIC16**LC**54A. These devices have EPROM program memory and operate over an extended voltage range.
3. **CR**, as in PIC16**CR**54A. These devices have ROM program memory and operate over the standard voltage range.
4. **LCR**, as in PIC16**LCR**54A. These devices have ROM program memory and operate over an extended voltage range.

### 2.1 UV Erasable Devices (EPROM)

The UV erasable versions offered in CERDIP packages, are optimal for prototype development and pilot programs.

UV erasable devices can be programmed for any of the four oscillator configurations. Microchip's PICSTART® Plus**(1)** and PRO MATE® programmers both support programming of the PIC16C5X. Third party programmers also are available. Refer to the Third Party Guide (DS00104) for a list of sources.

### 2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates, or small volume applications.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to the program memory, the configuration bits must be programmed.

**Note 1:** PIC16LC54C and PIC16C54A devices require OSC2 not to be connected while programming with PICSTART® Plus programmer.

### 2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration bit options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

### 2.4 Serialized Quick-Turnaround-Production (SQTP$^{SM}$) Devices

Microchip offers the unique programming service where a few user defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential. The devices are identical to the OTP devices but with all EPROM locations and configuration bit options already programmed by the factory.

Serial programming allows each device to have a unique number which can serve as an entry code, password or ID number.

### 2.5 Read Only Memory (ROM) Devices

Microchip offers masked ROM versions of several of the highest volume parts, giving the customer a low cost option for high volume, mature products.



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## 3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16C5X family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16C5X uses a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12 bits wide making it possible to have all single word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle except for program branches.

The PIC16C54/CR54 and PIC16C55 address 512 x 12 of program memory, the PIC16C56/CR56 address 1K x 12 of program memory, and the PIC16C57/CR57 and PIC16C58/CR58 address 2K x 12 of program memory. All program memory is internal.

The PIC16C5X can directly or indirectly address its register files and data memory. All special function registers including the program counter are mapped in the data memory. The PIC16C5X has a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of ‘special optimal situations’ make programming with the PIC16C5X simple yet efficient. In addition, the learning curve is reduced significantly.

The PIC16C5X device contains an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8 bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the W (working) register. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the `SUBWF` and `ADDWF` instructions for examples.

A simplified block diagram is shown in Figure 3-1, with the corresponding device pins described in Table 3-1 (for PIC16C54/56/58) and Table 3-2 (for PIC16C55/57).



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**FIGURE 3-1: PIC16C5X SERIES BLOCK DIAGRAM**

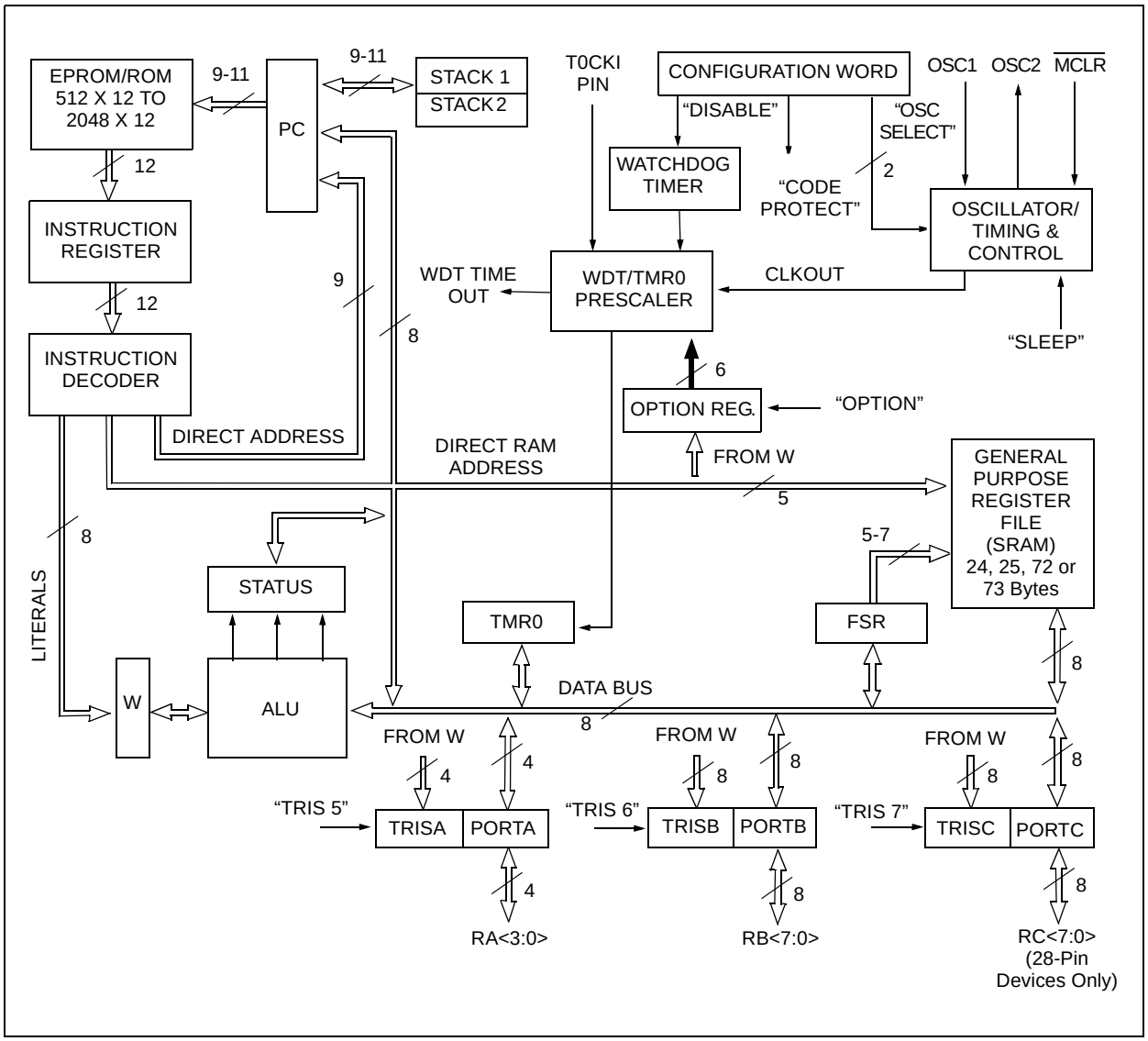


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**TABLE 3-1: PINOUT DESCRIPTION - PIC16C54, PIC16CR54, PIC16C56, PIC16CR56, PIC16C58, PIC16CR58**

| Pin Name | Pin Number | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|
| | DIP | SOIC | SSOP | | | |
| RA0 | 17 | 17 | 19 | I/O | TTL | Bi-directional I/O port |
| RA1 | 18 | 18 | 20 | I/O | TTL | |
| RA2 | 1 | 1 | 1 | I/O | TTL | |
| RA3 | 2 | 2 | 2 | I/O | TTL | |
| RB0 | 6 | 6 | 7 | I/O | TTL | Bi-directional I/O port |
| RB1 | 7 | 7 | 8 | I/O | TTL | |
| RB2 | 8 | 8 | 9 | I/O | TTL | |
| RB3 | 9 | 9 | 10 | I/O | TTL | |
| RB4 | 10 | 10 | 11 | I/O | TTL | |
| RB5 | 11 | 11 | 12 | I/O | TTL | |
| RB6 | 12 | 12 | 13 | I/O | TTL | |
| RB7 | 13 | 13 | 14 | I/O | TTL | |
| T0CKI | 3 | 3 | 3 | I | ST | Clock input to Timer0. Must be tied to VSS or VDD, if not in use, to reduce current consumption. |
| $\overline{MCLR}$/VPP | 4 | 4 | 4 | I | ST | Master clear (RESET) input/programming voltage input. This pin is an active low RESET to the device. Voltage on the $\overline{MCLR}$/VPP pin must not exceed VDD to avoid unintended entering of Programming mode. |
| OSC1/CLKIN | 16 | 16 | 18 | I | ST | Oscillator crystal input/external clock source input. |
| OSC2/CLKOUT | 15 | 15 | 17 | O | — | Oscillator crystal output. Connects to crystal or resonator in crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKOUT, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate. |
| VDD | 14 | 14 | 15,16 | P | — | Positive supply for logic and I/O pins. |
| VSS | 5 | 5 | 5,6 | P | — | Ground reference for logic and I/O pins. |

Legend: I = input, O = output, I/O = input/output, P = power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input



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**TABLE 3-2: PINOUT DESCRIPTION - PIC16C55, PIC16C57, PIC16CR57**

| Pin Name | Pin Number | | | Pin Type | Buffer Type | Description |
|---|---|---|---|---|---|---|
| | DIP | SOIC | SSOP | | | |
| RA0 | 6 | 6 | 5 | I/O | TTL | Bi-directional I/O port |
| RA1 | 7 | 7 | 6 | I/O | TTL | |
| RA2 | 8 | 8 | 7 | I/O | TTL | |
| RA3 | 9 | 9 | 8 | I/O | TTL | |
| RB0 | 10 | 10 | 9 | I/O | TTL | Bi-directional I/O port |
| RB1 | 11 | 11 | 10 | I/O | TTL | |
| RB2 | 12 | 12 | 11 | I/O | TTL | |
| RB3 | 13 | 13 | 12 | I/O | TTL | |
| RB4 | 14 | 14 | 13 | I/O | TTL | |
| RB5 | 15 | 15 | 15 | I/O | TTL | |
| RB6 | 16 | 16 | 16 | I/O | TTL | |
| RB7 | 17 | 17 | 17 | I/O | TTL | |
| RC0 | 18 | 18 | 18 | I/O | TTL | Bi-directional I/O port |
| RC1 | 19 | 19 | 19 | I/O | TTL | |
| RC2 | 20 | 20 | 20 | I/O | TTL | |
| RC3 | 21 | 21 | 21 | I/O | TTL | |
| RC4 | 22 | 22 | 22 | I/O | TTL | |
| RC5 | 23 | 23 | 23 | I/O | TTL | |
| RC6 | 24 | 24 | 24 | I/O | TTL | |
| RC7 | 25 | 25 | 25 | I/O | TTL | |
| T0CKI | 1 | 1 | 2 | I | ST | Clock input to Timer0. Must be tied to $V_{SS}$ or $V_{DD}$, if not in use, to reduce current consumption. |
| $\overline{MCLR}$ | 28 | 28 | 28 | I | ST | Master clear (RESET) input. This pin is an active low RESET to the device. |
| OSC1/CLKIN | 27 | 27 | 27 | I | ST | Oscillator crystal input/external clock source input. |
| OSC2/CLKOUT | 26 | 26 | 26 | O | — | Oscillator crystal output. Connects to crystal or resonator in crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate. |
| $V_{DD}$ | 2 | 2 | 3,4 | P | — | Positive supply for logic and I/O pins. |
| $V_{SS}$ | 4 | 4 | 1,14 | P | — | Ground reference for logic and I/O pins. |
| N/C | 3,5 | 3,5 | — | — | — | Unused, do not connect. |

Legend: I = input, O = output, I/O = input/output, P = power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input

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## 3.1 Clocking Scheme/Instruction Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks, namely Q1, Q2, Q3 and Q4. Internally, the program counter is incremented every Q1 and the instruction is fetched from program memory and latched into the instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow are shown in Figure 3-2 and Example 3-1.

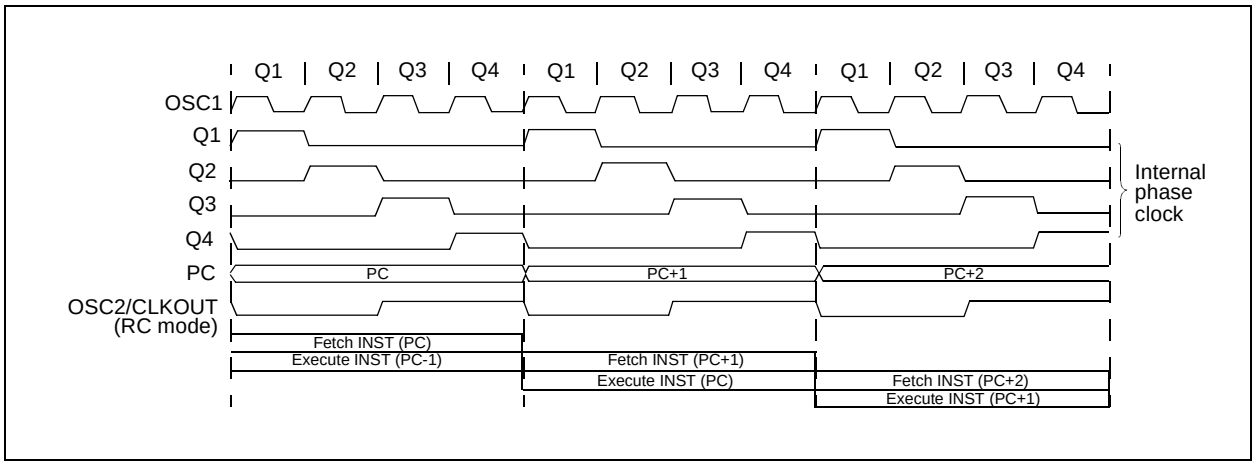
## 3.2 Instruction Flow/Pipelining

An Instruction Cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle, while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., `GOTO`), then two cycles are required to complete the instruction (Example 3-1).

A fetch cycle begins with the program counter (PC) incrementing in Q1.

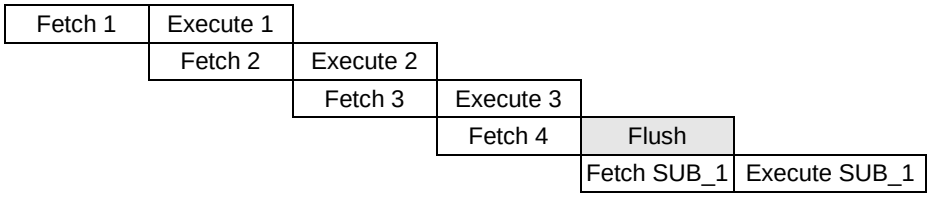
In the execution cycle, the fetched instruction is latched into the Instruction Register in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

**FIGURE 3-2: CLOCK/INSTRUCTION CYCLE**




**EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW**

```
1. MOVLW H'55'
2. MOVWF PORTB
3. CALL  SUB_1
4. BSF   PORTA, BIT3
```




All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is “flushed” from the pipeline, while the new instruction is being fetched and then executed.



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# 4.0 OSCILLATOR CONFIGURATIONS

## 4.1 Oscillator Types

PIC16C5Xs can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1:FOSC0) to select one of these four modes:

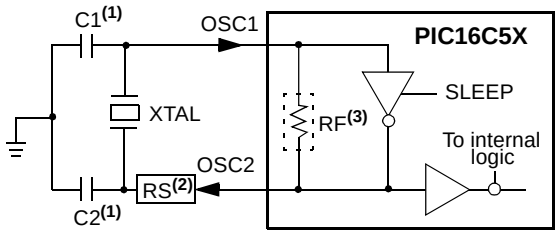
1. LP: Low Power Crystal
2. XT: Crystal/Resonator
3. HS: High Speed Crystal/Resonator
4. RC: Resistor/Capacitor

| | |
|---|---|
| **Note:** | Not all oscillator selections available for all parts. See Section 9.1. |

## 4.2 Crystal Oscillator/Ceramic Resonators

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 4-1). The PIC16C5X oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source drive the OSC1/CLKIN pin (Figure 4-2).

**FIGURE 4-1: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP OSC CONFIGURATION)**




**Note 1:** See Capacitor Selection tables for recommended values of C1 and C2.
**2:** A series resistor (RS) may be required for AT strip cut crystals.
**3:** RF varies with the Oscillator mode chosen (approx. value = 10 MΩ).

**FIGURE 4-2: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)**

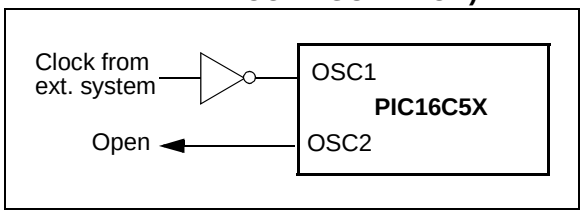



**TABLE 4-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS - PIC16C5X, PIC16CR5X**

| Osc Type | Resonator Freq | Cap. Range C1 | Cap. Range C2 |
|---|---|---|---|
| XT | 455 kHz | 68-100 pF | 68-100 pF |
| | 2.0 MHz | 15-33 pF | 15-33 pF |
| | 4.0 MHz | 10-22 pF | 10-22 pF |
| HS | 8.0 MHz | 10-22 pF | 10-22 pF |
| | 16.0 MHz | 10 pF | 10 pF |

These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

**TABLE 4-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR - PIC16C5X, PIC16CR5X**

| Osc Type | Crystal Freq | Cap.Range C1 | Cap. Range C2 |
|---|---|---|---|
| LP | 32 kHz(1) | 15 pF | 15 pF |
| XT | 100 kHz | 15-30 pF | 200-300 pF |
| | 200 kHz | 15-30 pF | 100-200 pF |
| | 455 kHz | 15-30 pF | 15-100 pF |
| | 1 MHz | 15-30 pF | 15-30 pF |
| | 2 MHz | 15 pF | 15 pF |
| | 4 MHz | 15 pF | 15 pF |
| HS | 4 MHz | 15 pF | 15 pF |
| | 8 MHz | 15 pF | 15 pF |
| | 20 MHz | 15 pF | 15 pF |

**Note 1:** For $V_{DD}$ > 4.5V, C1 = C2 ≈ 30 pF is recommended.

These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

| | |
|---|---|
| **Note:** | If you change from this device to another device, please verify oscillator characteristics in your application. |



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## 4.3 External Crystal Oscillator Circuit

Either a prepackaged oscillator or a simple oscillator circuit with TTL gates can be used as an external crystal oscillator circuit. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used: one with parallel resonance, or one with series resonance.

Figure 4-3 shows an implementation example of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 kΩ resistor provides the negative feedback for stability. The 10 kΩ potentiometers bias the 74AS04 in the linear region. This circuit could be used for external oscillator designs.

**FIGURE 4-3: EXAMPLE OF EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT (USING XT, HS OR LP OSCILLATOR MODE)**

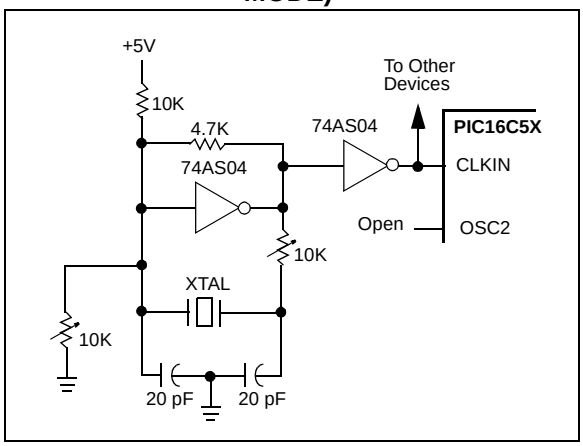
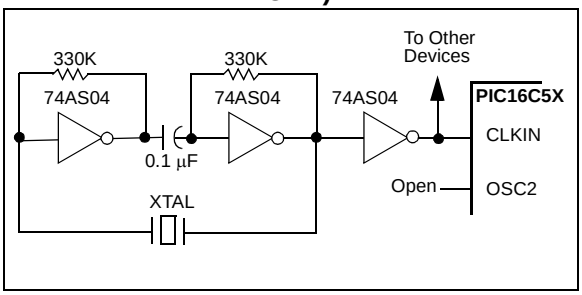



Figure 4-4 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330 kΩ resistors provide the negative feedback to bias the inverters in their linear region.

**FIGURE 4-4: EXAMPLE OF EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT (USING XT, HS OR LP OSCILLATOR MODE)**

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## 4.4 RC Oscillator

For timing insensitive applications, the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low CEXT values. The user also needs to take into account variation due to tolerance of external R and C components used.

Figure 4-5 shows how the R/C combination is connected to the PIC16C5X. For REXT values below 2.2 kΩ, the oscillator operation may become unstable, or stop completely. For very high REXT values (e.g., 1 MΩ) the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend keeping REXT between 3 kΩ and 100 kΩ.

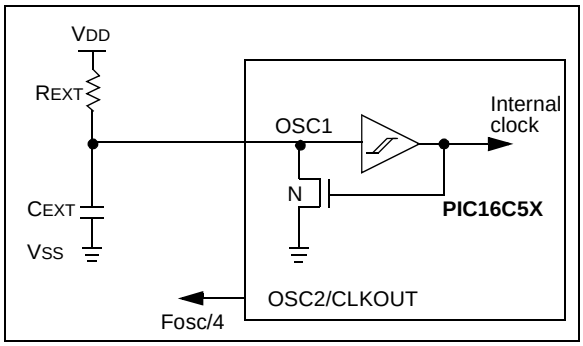
Although the oscillator will operate with no external capacitor (CEXT = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

The Electrical Specifications sections show RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

Also, see the Electrical Specifications sections for variation of oscillator frequency due to VDD for given REXT/CEXT values as well as frequency variation due to operating temperature for given R, C, and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic.

**FIGURE 4-5: RC OSCILLATOR MODE**




| **Note:** | If you change from this device to another device, please verify oscillator characteristics in your application. |
|---|---|



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## 5.0 RESET

PIC16C5X devices may be RESET in one of the following ways:

- Power-On Reset (POR)
- $\overline{MCLR}$ Reset (normal operation)
- $\overline{MCLR}$ Wake-up Reset (from SLEEP)
- WDT Reset (normal operation)
- WDT Wake-up Reset (from SLEEP)

Table 5-1 shows these RESET conditions for the PCL and STATUS registers.

Some registers are not affected in any RESET condition. Their status is unknown on POR and unchanged in any other RESET. Most other registers are reset to a "RESET state" on Power-On Reset (POR), $\overline{MCLR}$ or WDT Reset. A $\overline{MCLR}$ or WDT wake-up from SLEEP also results in a device RESET, and not a continuation of operation before SLEEP.

The $\overline{TO}$ and $\overline{PD}$ bits (STATUS <4:3>) are set or cleared depending on the different RESET conditions (Table 5-1). These bits may be used to determine the nature of the RESET.

Table 5-3 lists a full description of RESET states of all registers. Figure 5-1 shows a simplified block diagram of the On-chip Reset circuit.

**TABLE 5-1: STATUS BITS AND THEIR SIGNIFICANCE**

| Condition | $\overline{TO}$ | $\overline{PD}$ |
|---|---|---|
| Power-On Reset | 1 | 1 |
| $\overline{MCLR}$ Reset (normal operation) | u | u |
| $\overline{MCLR}$ Wake-up (from SLEEP) | 1 | 0 |
| WDT Reset (normal operation) | 0 | 1 |
| WDT Wake-up (from SLEEP) | 0 | 0 |

Legend: u = unchanged, x = unknown, – = unimplemented read as '0'.

**TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH RESET**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR | Value on $\overline{MCLR}$ and WDT Reset |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 03h | STATUS | PA2 | PA1 | PA0 | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C | 0001 1xxx | 000q quuu |

Legend: u = unchanged, x = unknown, q = see Table 5-1 for possible values.



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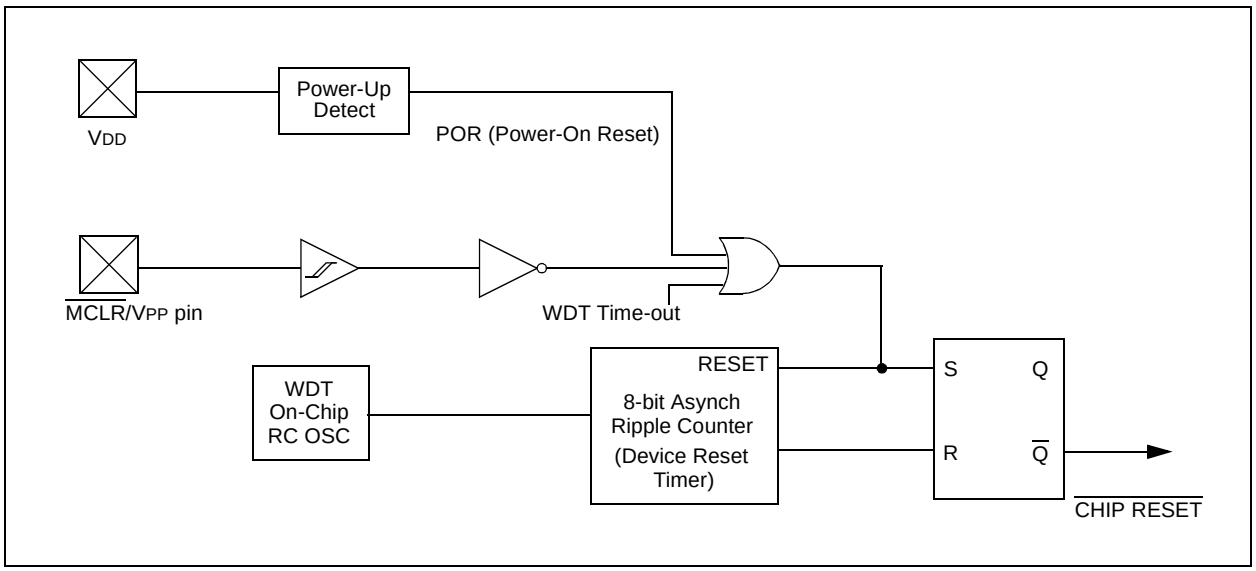
**TABLE 5-3: RESET CONDITIONS FOR ALL REGISTERS**

| Register | Address | Power-On Reset | $\overline{MCLR}$ or WDT Reset |
|---|---|---|---|
| W | N/A | xxxx xxxx | uuuu uuuu |
| TRIS | N/A | 1111 1111 | 1111 1111 |
| OPTION | N/A | --11 1111 | --11 1111 |
| INDF | 00h | xxxx xxxx | uuuu uuuu |
| TMR0 | 01h | xxxx xxxx | uuuu uuuu |
| PCL | 02h | 1111 1111 | 1111 1111 |
| STATUS | 03h | 0001 1xxx | 000q quuu |
| FSR(1) | 04h | 1xxx xxxx | 1uuu uuuu |
| PORTA | 05h | ---- xxxx | ---- uuuu |
| PORTB | 06h | xxxx xxxx | uuuu uuuu |
| PORTC(2) | 07h | xxxx xxxx | uuuu uuuu |
| General Purpose Register Files | 07-7Fh | xxxx xxxx | uuuu uuuu |

Legend: x = unknown u = unchanged - = unimplemented, read as '0'
q = see tables in Table 5-1 for possible values.

**Note 1:** These values are valid for PIC16C57/CR57/C58/CR58. For the PIC16C54/CR54/C55/C56/CR56, the value on RESET is 111x xxxx and for $\overline{MCLR}$ and WDT Reset, the value is 111u uuuu.
**2:** General purpose register file on PIC16C54/CR54/C56/CR56/C58/CR58.

**FIGURE 5-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT**

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## 5.1 Power-On Reset (POR)

The PIC16C5X family incorporates on-chip Power-On Reset (POR) circuitry which provides an internal chip RESET for most power-up situations. To use this feature, the user merely ties the MCLR/VPP pin to VDD. A simplified block diagram of the on-chip Power-On Reset circuit is shown in Figure 5-1.

The Power-On Reset circuit and the Device Reset Timer (Section 5.2) circuit are closely related. On power-up, the RESET latch is set and the DRT is RESET. The DRT timer begins counting once it detects MCLR to be high. After the time-out period, which is typically 18 ms, it will RESET the reset latch and thus end the on-chip RESET signal.

A power-up example where MCLR is not tied to VDD is shown in Figure 5-3. VDD is allowed to rise and stabilize before bringing MCLR high. The chip will actually come out of reset TDRT msec after MCLR goes high.

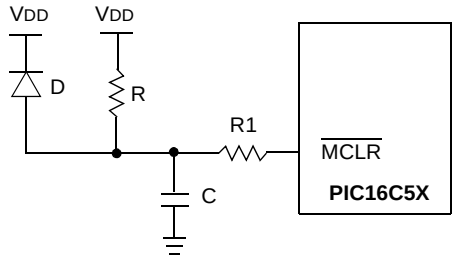
In Figure 5-4, the on-chip Power-On Reset feature is being used (MCLR and VDD are tied together). The VDD is stable before the start-up timer times out and there is no problem in getting a proper RESET. However, Figure 5-5 depicts a problem situation where VDD rises too slowly. The time between when the DRT senses a high on the MCLR/VPP pin, and when the MCLR/VPP pin (and VDD) actually reach their full value, is too long. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip is, therefore, not guaranteed to function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (Figure 5-2).

| | |
|---|---|
| **Note:** | When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met. |

For more information on PIC16C5X POR, see *Power-Up Considerations* - AN522 in the Embedded Control Handbook.

The POR circuit does not produce an internal RESET when VDD declines.

**FIGURE 5-2: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)**




- External Power-On Reset circuit is required only if VDD power-up is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
- R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device electrical specification.
- R1 = 100Ω to 1 kΩ will limit any current flowing into MCLR from external capacitor C in the event of MCLR pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).



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**FIGURE 5-3: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD)**

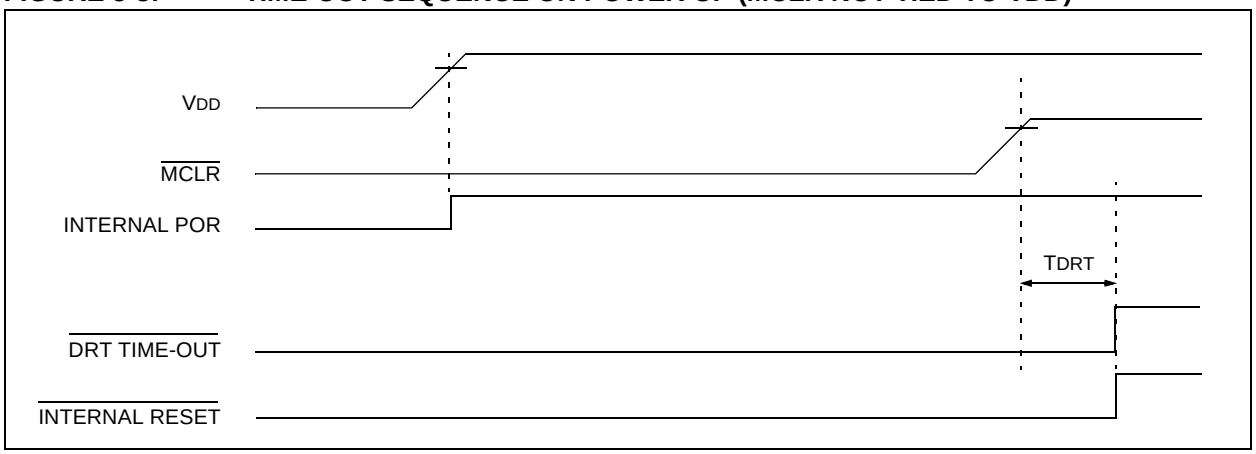



**FIGURE 5-4: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD): FAST VDD RISE TIME**

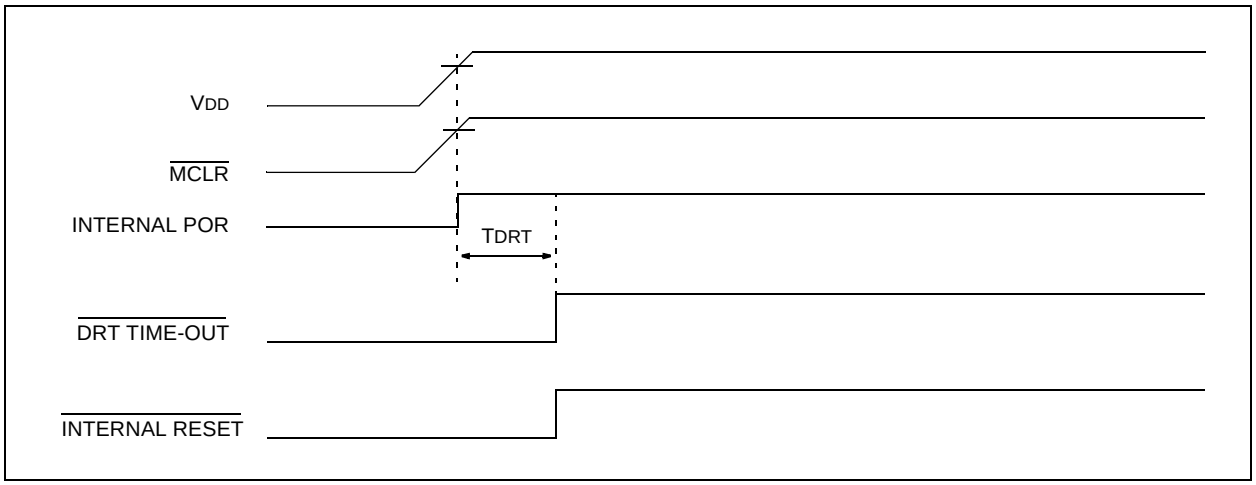
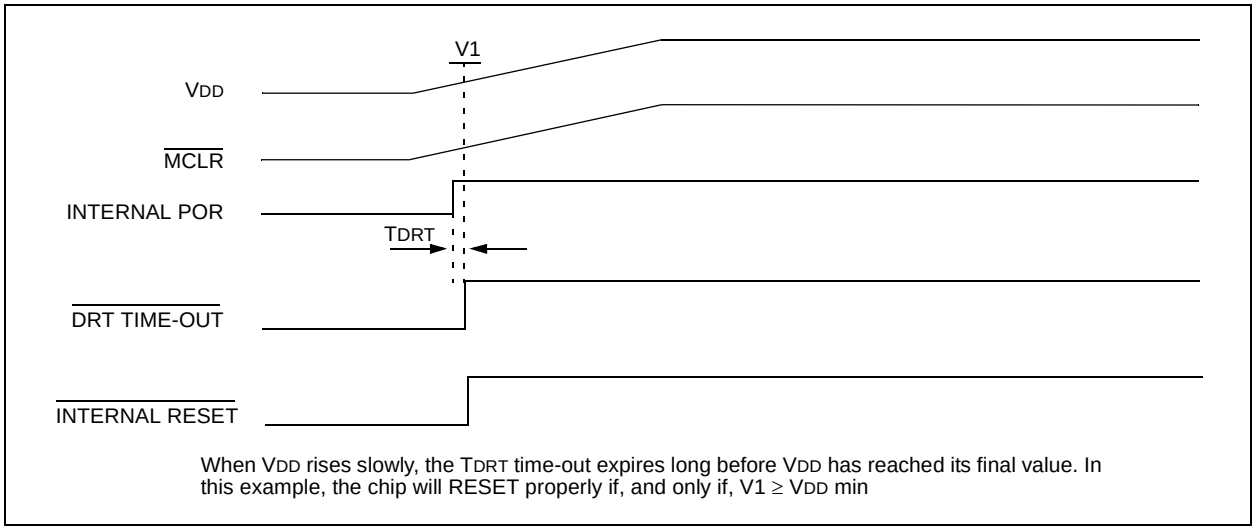



**FIGURE 5-5: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD): SLOW VDD RISE TIME**




When VDD rises slowly, the TDRT time-out expires long before VDD has reached its final value. In this example, the chip will RESET properly if, and only if, V1 ≥ VDD min

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## 5.2 Device Reset Timer (DRT)

The Device Reset Timer (DRT) provides an 18 ms nominal time-out on RESET regardless of Oscillator mode used. The DRT operates on an internal RC oscillator. The processor is kept in RESET as long as the DRT is active. The DRT delay allows VDD to rise above VDD min., and for the oscillator to stabilize.

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. The on-chip DRT keeps the device in a RESET condition for approximately 18 ms after the voltage on the MCLR/VPP pin has reached a logic high (VIH) level. Thus, external RC networks connected to the MCLR input are not required in most cases, allowing for savings in cost-sensitive and/or space restricted applications.

The Device Reset time delay will vary from chip to chip due to VDD, temperature, and process variation. See AC parameters for details.

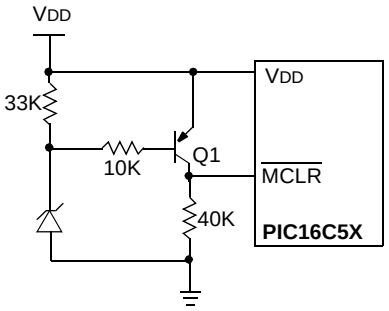
The DRT will also be triggered upon a Watchdog Timer time-out. This is particularly important for applications using the WDT to wake the PIC16C5X from SLEEP mode automatically.

## 5.3 Reset on Brown-Out

A brown-out is a condition where device power (VDD) dips below its minimum value, but not to zero, and then recovers. The device should be RESET in the event of a brown-out.

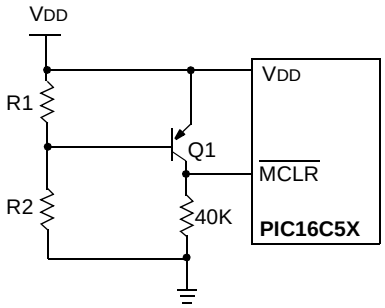
To RESET PIC16C5X devices when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 5-6, Figure 5-7 and Figure 5-8.

**FIGURE 5-6: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1**




This circuit will activate RESET when VDD goes below Vz + 0.7V (where Vz = Zener voltage).

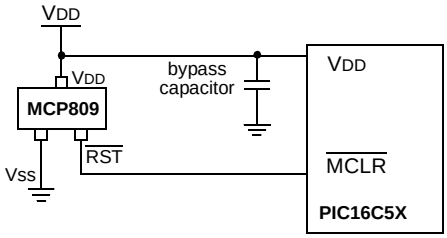
**FIGURE 5-7: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2**




This brown-out circuit is less expensive, although less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \bullet \frac{R1}{R1 + R2} = 0.7V$$

**FIGURE 5-8: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 3**




This brown-out protection circuit employs Microchip Technology's MCP809 microcontroller supervisor. The MCP8XX and MCP1XX families of supervisors provide push-pull and open collector outputs with both "active high and active low" RESET pins. There are 7 different trip point selections to accommodate 5V and 3V systems.



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## 6.0 MEMORY ORGANIZATION

PIC16C5X memory is organized into program memory and data memory. For devices with more than 512 bytes of program memory, a paging scheme is used. Program memory pages are accessed using one or two STATUS Register bits. For devices with a data memory register file of more than 32 registers, a banking scheme is used. Data memory banks are accessed using the File Selection Register (FSR).

### 6.1 Program Memory Organization

The PIC16C54, PIC16CR54 and PIC16C55 have a 9-bit Program Counter (PC) capable of addressing a 512 x 12 program memory space (Figure 6-1). The PIC16C56 and PIC16CR56 have a 10-bit Program Counter (PC) capable of addressing a 1K x 12 program memory space (Figure 6-2). The PIC16CR57, PIC16C58 and PIC16CR58 have an 11-bit Program Counter capable of addressing a 2K x 12 program memory space (Figure 6-3). Accessing a location above the physically implemented address will cause a wraparound.

A NOP at the RESET vector location will cause a restart at location 000h. The RESET vector for the PIC16C54, PIC16CR54 and PIC16C55 is at 1FFh. The RESET vector for the PIC16C56 and PIC16CR56 is at 3FFh. The RESET vector for the PIC16C57, PIC16CR57, PIC16C58, and PIC16CR58 is at 7FFh. See Section 6.5 for additional information using CALL and GOTO instructions.

**FIGURE 6-1: PIC16C54/CR54/C55 PROGRAM MEMORY MAP AND STACK**

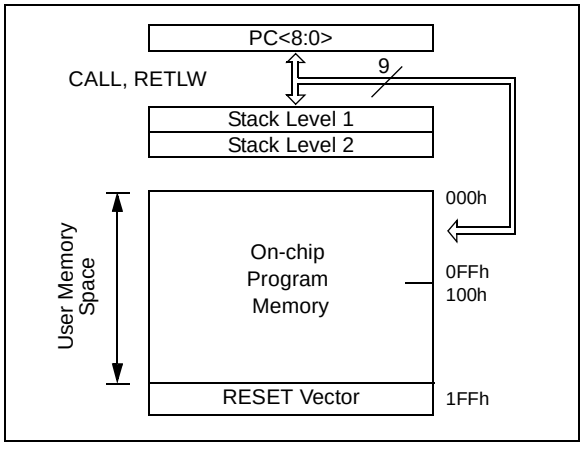



**FIGURE 6-2: PIC16C56/CR56 PROGRAM MEMORY MAP AND STACK**

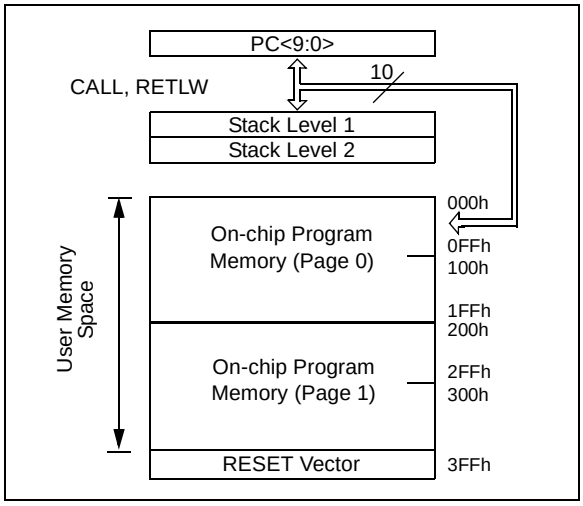
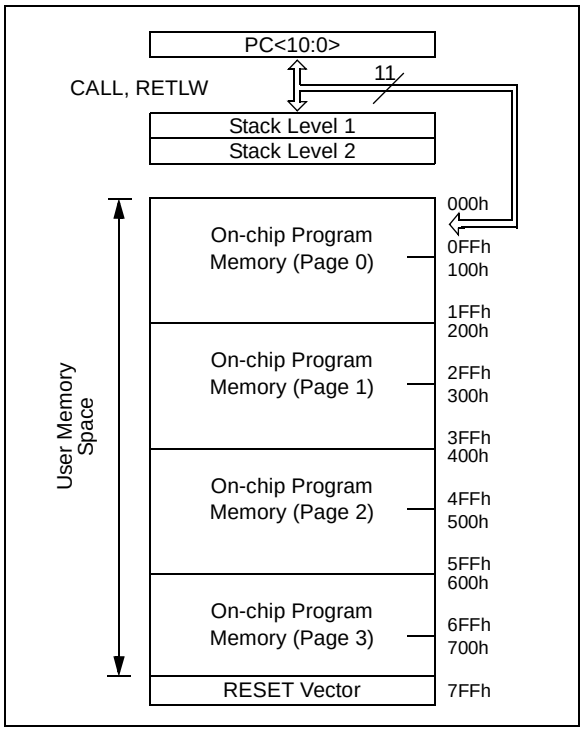



**FIGURE 6-3: PIC16C57/CR57/C58/ CR58 PROGRAM MEMORY MAP AND STACK**



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## 6.2 Data Memory Organization

Data memory is composed of registers, or bytes of RAM. Therefore, data memory for a device is specified by its register file. The register file is divided into two functional groups: Special Function Registers and General Purpose Registers.

The Special Function Registers include the TMR0 register, the Program Counter (PC), the Status Register, the I/O registers (ports) and the File Select Register (FSR). In addition, Special Purpose Registers are used to control the I/O port configuration and prescaler options.

The General Purpose Registers are used for data and control information under command of the instructions.

For the PIC16C54, PIC16CR54, PIC16C56 and PIC16CR56, the register file is composed of 7 Special Function Registers and 25 General Purpose Registers (Figure 6-4).

For the PIC16C55, the register file is composed of 8 Special Function Registers and 24 General Purpose Registers.

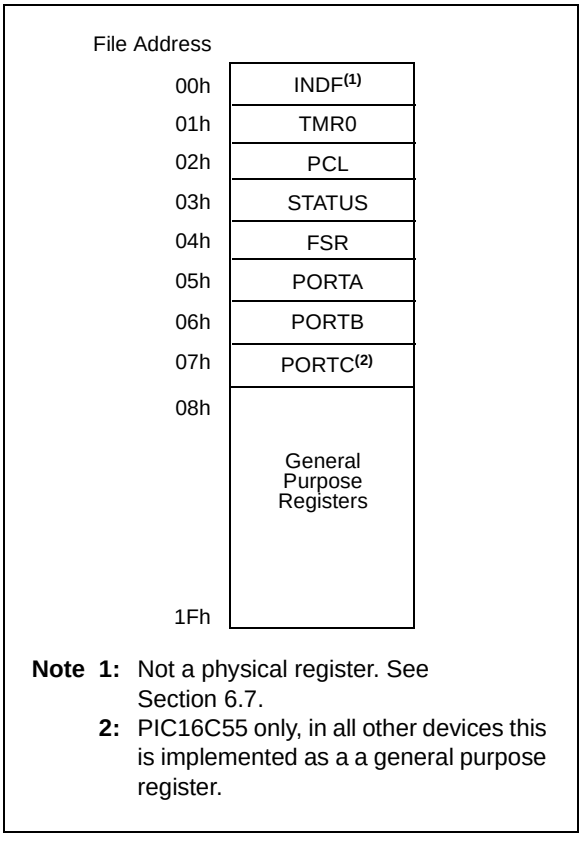
For the PIC16C57 and PIC16CR57, the register file is composed of 8 Special Function Registers, 24 General Purpose Registers and up to 48 additional General Purpose Registers that may be addressed using a banking scheme (Figure 6-5).

For the PIC16C58 and PIC16CR58, the register file is composed of 7 Special Function Registers, 25 General Purpose Registers and up to 48 additional General Purpose Registers that may be addressed using a banking scheme (Figure 6-6).

### 6.2.1 GENERAL PURPOSE REGISTER FILE

The register file is accessed either directly or indirectly through the File Select Register (FSR). The FSR Register is described in Section 6.7.

**FIGURE 6-4: PIC16C54, PIC16CR54, PIC16C55, PIC16C56, PIC16CR56 REGISTER FILE MAP**




**Note 1:** Not a physical register. See Section 6.7.

**2:** PIC16C55 only, in all other devices this is implemented as a a general purpose register.

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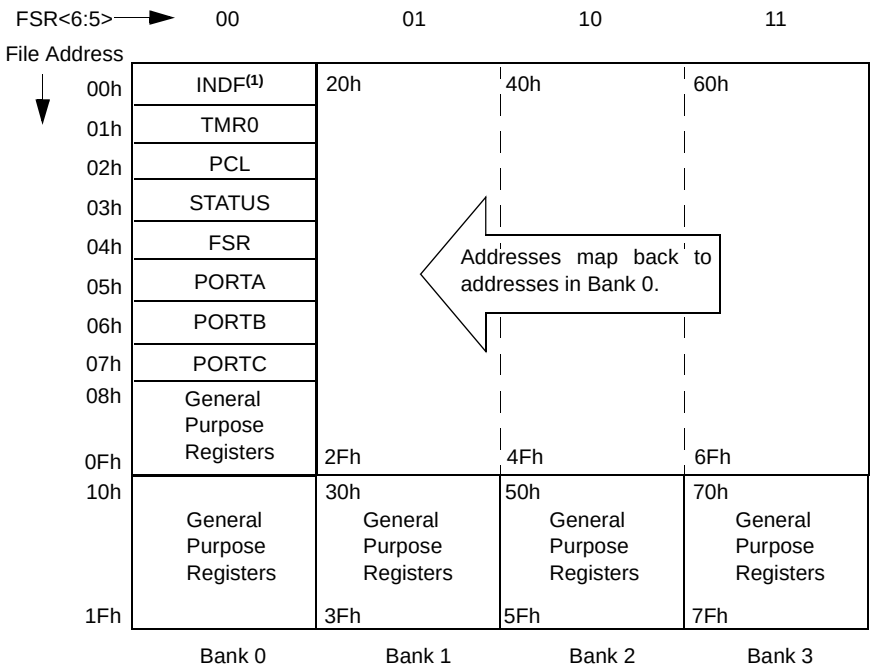
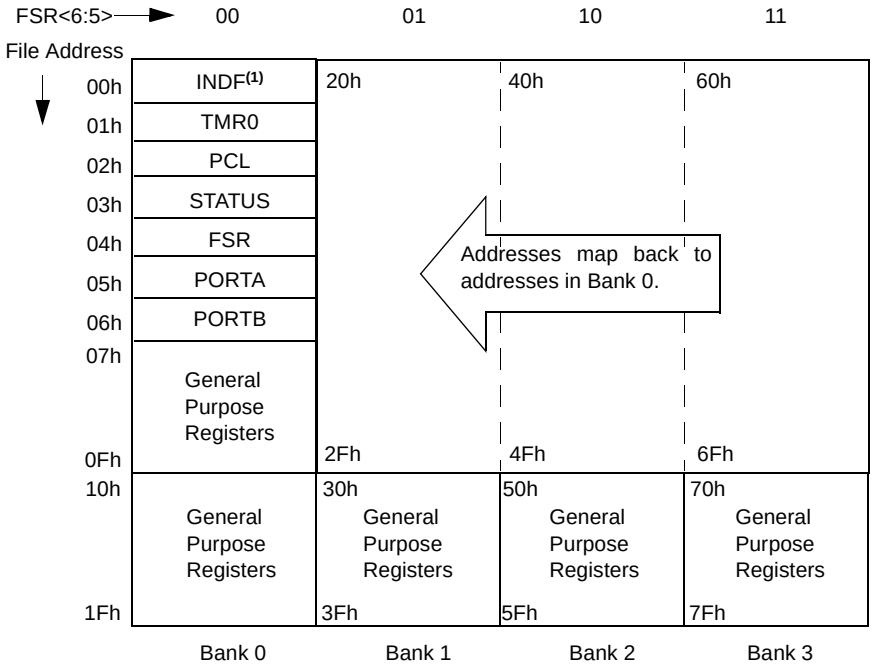
**FIGURE 6-5: PIC16C57/CR57 REGISTER FILE MAP**




**Note 1:** Not a physical register. See Section 6.7.

**FIGURE 6-6: PIC16C58/CR58 REGISTER FILE MAP**




**Note 1:** Not a physical register. See Section 6.7.



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### 6.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions to control the operation of the device (Table 6-1).

The Special Registers can be classified into two sets. The Special Function Registers associated with the “core” functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

**TABLE 6-1: SPECIAL FUNCTION REGISTER SUMMARY**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on Power-on Reset | Details on Page |
|---|---|---|---|---|---|---|---|---|---|---|---|
| N/A | TRIS | I/O Control Registers (TRISA, TRISB, TRISC) | | | | | | | | 1111 1111 | 35 |
| N/A | OPTION | Contains control bits to configure Timer0 and Timer0/WDT prescaler | | | | | | | | --11 1111 | 30 |
| 00h | INDF | Uses contents of FSR to address data memory (not a physical register) | | | | | | | | xxxx xxxx | 32 |
| 01h | TMR0 | Timer0 Module Register | | | | | | | | xxxx xxxx | 38 |
| 02h(1) | PCL | Low order 8 bits of PC | | | | | | | | 1111 1111 | 31 |
| 03h | STATUS | PA2 | PA1 | PA0 | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C | 0001 1xxx | 29 |
| 04h | FSR | Indirect data memory address pointer | | | | | | | | 1xxx xxxx(3) | 32 |
| 05h | PORTA | — | — | — | — | RA3 | RA2 | RA1 | RA0 | ---- xxxx | 35 |
| 06h | PORTB | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 | xxxx xxxx | 35 |
| 07h(2) | PORTC | RC7 | RC6 | RC5 | RC4 | RC3 | RC2 | RC1 | RC0 | xxxx xxxx | 35 |

Legend: x = unknown, u = unchanged, – = unimplemented, read as '0' (if applicable). Shaded cells = unimplemented or unused

**Note 1:** The upper byte of the Program Counter is not directly accessible. See Section 6.5 for an explanation of how to access these bits.

**2:** File address 07h is a General Purpose Register on the PIC16C54, PIC16CR54, PIC16C56, PIC16CR56, PIC16C58 and PIC16CR58.

**3:** These values are valid for PIC16C57/CR57/C58/CR58. For the PIC16C54/CR54/C55/C56/CR56, the value on RESET is 111x xxxx and for $\overline{MCLR}$ and WDT Reset, the value is 111u uuuu.

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## 6.3 STATUS Register

This register contains the arithmetic status of the ALU, the RESET status and the page preselect bits for program memories larger than 512 words.

The STATUS Register can be the destination for any instruction, as with any other register. If the STATUS Register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS Register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS Register as `000u u1uu` (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF` and `MOVWF` instructions be used to alter the STATUS Register because these instructions do not affect the Z, DC or C bits from the STATUS Register. For other instructions which do affect STATUS Bits, see Section 10.0, Instruction Set Summary.

**REGISTER 6-1: STATUS REGISTER (ADDRESS: 03h)**

| R/W-0 | R/W-0 | R/W-0 | R-1 | R-1 | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| PA2 | PA1 | PA0 | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C |
| bit 7 | | | | | | | bit 0 |

bit 7: **PA2**: This bit unused at this time.
Use of the PA2 bit as a general purpose read/write bit is not recommended, since this may affect upward compatibility with future products.

bit 6-5: **PA<1:0>**: Program page preselect bits (PIC16C56/CR56)(PIC16C57/CR57)(PIC16C58/CR58)
`00` = Page 0 (000h - 1FFh) - PIC16C56/CR56, PIC16C57/CR57, PIC16C58/CR58
`01` = Page 1 (200h - 3FFh) - PIC16C56/CR56, PIC16C57/CR57, PIC16C58/CR58
`10` = Page 2 (400h - 5FFh) - PIC16C57/CR57, PIC16C58/CR58
`11` = Page 3 (600h - 7FFh) - PIC16C57/CR57, PIC16C58/CR58
Each page is 512 words.
Using the PA<1:0> bits as general purpose read/write bits in devices which do not use them for program page preselect is not recommended since this may affect upward compatibility with future products.

bit 4: **$\overline{TO}$**: Time-out bit
`1` = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
`0` = A WDT time-out occurred

bit 3: **$\overline{PD}$**: Power-down bit
`1` = After power-up or by the `CLRWDT` instruction
`0` = By execution of the `SLEEP` instruction

bit 2: **Z**: Zero bit
`1` = The result of an arithmetic or logic operation is zero
`0` = The result of an arithmetic or logic operation is not zero

bit 1: **DC**: Digit carry/$\overline{borrow}$ bit (for `ADDWF` and `SUBWF` instructions)
**ADDWF**
`1` = A carry from the 4th low order bit of the result occurred
`0` = A carry from the 4th low order bit of the result did not occur
**SUBWF**
`1` = A borrow from the 4th low order bit of the result did not occur
`0` = A borrow from the 4th low order bit of the result occurred

bit 0: **C**: Carry/$\overline{borrow}$ bit (for `ADDWF`, `SUBWF` and `RRF`, `RLF` instructions)

| ADDWF | SUBWF | RRF or RLF |
|---|---|---|
| `1` = A carry occurred | `1` = A borrow did not occur | Loaded with LSb or MSb, respectively |
| `0` = A carry did not occur | `0` = A borrow occurred | |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | 1 = bit is set | 0 = bit is cleared | x = bit is unknown |



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## 6.4 OPTION Register

The OPTION Register is a 6-bit wide, write-only register which contains various control bits to configure the Timer0/WDT prescaler and Timer0.

By executing the `OPTION` instruction, the contents of the W Register will be transferred to the OPTION Register. A RESET sets the OPTION<5:0> bits.

**REGISTER 6-2: OPTION REGISTER**

| U-0 | U-0 | W-1 | W-1 | W-1 | W-1 | W-1 | W-1 |
|---|---|---|---|---|---|---|---|
| — | — | T0CS | TOSE | PSA | PS2 | PS1 | PS0 |
| bit 7 | | | | | | | bit 0 |

bit 7-6: **Unimplemented**: Read as '0'

bit 5: **T0CS**: Timer0 clock source select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4: **T0SE**: Timer0 source edge select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3: **PSA**: Prescaler assignment bit
1 = Prescaler assigned to the WDT
0 = Prescaler assigned to Timer0

bit 2-0: **PS<2:0>**: Prescaler rate select bits

| Bit Value | Timer0 Rate | WDT Rate |
|---|---|---|
| 000 | 1 : 2 | 1 : 1 |
| 001 | 1 : 4 | 1 : 2 |
| 010 | 1 : 8 | 1 : 4 |
| 011 | 1 : 16 | 1 : 8 |
| 100 | 1 : 32 | 1 : 16 |
| 101 | 1 : 64 | 1 : 32 |
| 110 | 1 : 128 | 1 : 64 |
| 111 | 1 : 256 | 1 : 128 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | 1 = bit is set | 0 = bit is cleared | x = bit is unknown |

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## 6.5 Program Counter

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one, every instruction cycle, unless an instruction changes the PC.

For a GOTO instruction, bits 8:0 of the PC are provided by the GOTO instruction word. The PC Latch (PCL) is mapped to PC<7:0> (Figure 6-7, Figure 6-8 and Figure 6-9).

For the PIC16C56, PIC16CR56, PIC16C57, PIC16CR57, PIC16C58 and PIC16CR58, a page number must be supplied as well. Bit5 and bit6 of the STATUS Register provide page information to bit9 and bit10 of the PC (Figure 6-8 and Figure 6-9).

For a CALL instruction, or any instruction where the PCL is the destination, bits 7:0 of the PC again are provided by the instruction word. However, PC<8> does not come from the instruction word, but is always cleared (Figure 6-7 and Figure 6-8).

Instructions where the PCL is the destination, or modify PCL instructions, include MOVWF PCL, ADDWF PCL, and BSF PCL,5.

For the PIC16C56, PIC16CR56, PIC16C57, PIC16CR57, PIC16C58 and PIC16CR58, a page number again must be supplied. Bit5 and bit6 of the STATUS Register provide page information to bit9 and bit10 of the PC (Figure 6-8 and Figure 6-9).

| **Note:** | Because PC<8> is cleared in the CALL instruction, or any modify PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long). |
|---|---|

**FIGURE 6-7: LOADING OF PC BRANCH INSTRUCTIONS - PIC16C54, PIC16CR54, PIC16C55**

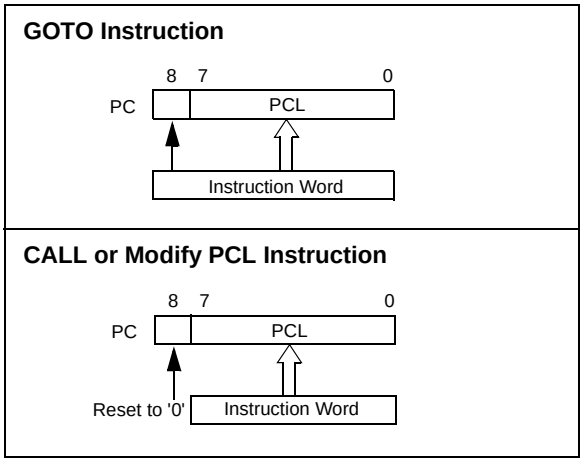



**FIGURE 6-8: LOADING OF PC BRANCH INSTRUCTIONS - PIC16C56/PIC16CR56**

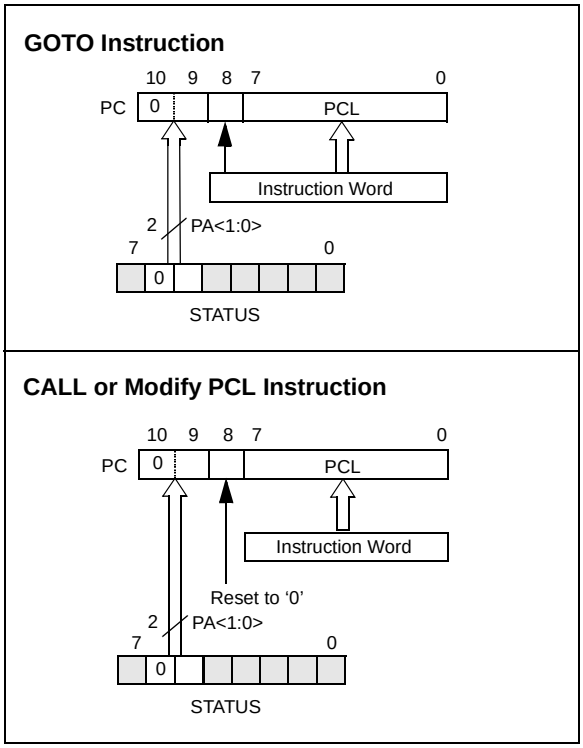
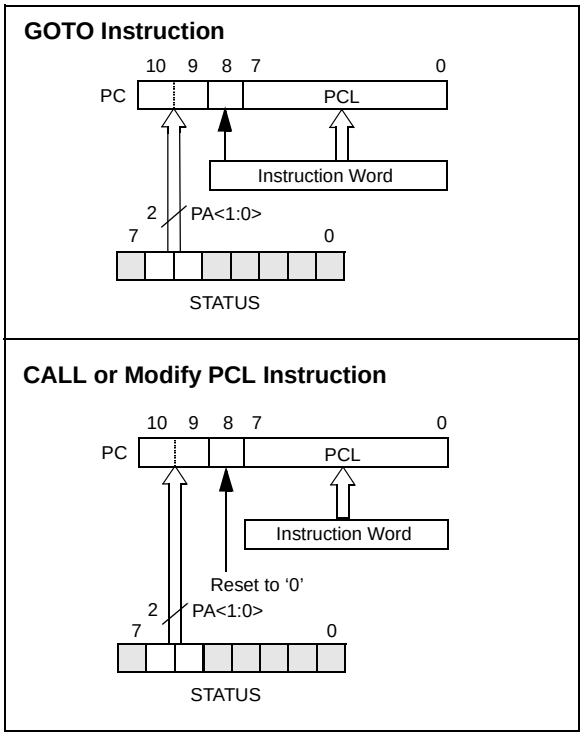



**FIGURE 6-9: LOADING OF PC BRANCH INSTRUCTIONS - PIC16C57/PIC16CR57, AND PIC16C58/ PIC16CR58**



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### 6.5.1 PAGING CONSIDERATIONS – PIC16C56/CR56, PIC16C57/CR57 AND PIC16C58/CR58

If the Program Counter is pointing to the last address of a selected memory page, when it increments it will cause the program to continue in the next higher page. However, the page preselect bits in the STATUS Register will not be updated. Therefore, the next GOTO, CALL or modify PCL instruction will send the program to the page specified by the page preselect bits (PA0 or PA<1:0>).

For example, a NOP at location 1FFh (page 0) increments the PC to 200h (page 1). A GOTO xxx at 200h will return the program to address xxh on page 0 (assuming that PA<1:0> are clear).

To prevent this, the page preselect bits must be updated under program control.

### 6.5.2 EFFECTS OF RESET

The Program Counter is set upon a RESET, which means that the PC addresses the last location in the last page (i.e., the RESET vector).

The STATUS Register page preselect bits are cleared upon a RESET, which means that page 0 is preselected.

Therefore, upon a RESET, a GOTO instruction at the RESET vector location will automatically cause the program to jump to page 0.

## 6.6 Stack

PIC16C5X devices have a 10-bit or 11-bit wide, two-level hardware push/pop stack.

A CALL instruction will push the current value of stack 1 into stack 2 and then push the current program counter value, incremented by one, into stack level 1. If more than two sequential CALL's are executed, only the most recent two return addresses are stored.

A RETLW instruction will pop the contents of stack level 1 into the program counter and then copy stack level 2 contents into level 1. If more than two sequential RETLW's are executed, the stack will be filled with the address previously stored in level 2. Note that the W Register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

For the RETLW instruction, the PC is loaded with the Top of Stack (TOS) contents. All of the devices covered in this data sheet have a two-level stack. The stack has the same bit width as the device PC, therefore, paging is not an issue when returning from a subroutine.

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## 6.7 Indirect Data Addressing; INDF and FSR Registers

The INDF Register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR Register (FSR is a *pointer*). This is indirect addressing.

### EXAMPLE 6-1: INDIRECT ADDRESSING

- Register file 08 contains the value 10h
- Register file 09 contains the value 0Ah
- Load the value 08 into the FSR Register
- A read of the INDF Register will return the value of 10h
- Increment the value of the FSR Register by one (FSR = 09h)
- A read of the INDF register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF Register indirectly results in a no-operation (although STATUS bits may be affected).

A simple program to clear RAM locations 10h-1Fh using indirect addressing is shown in Example 6-2.

### EXAMPLE 6-2: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

```
            MOVLW   H'10'   ;initialize pointer
            MOVWF   FSR     ; to RAM
NEXT        CLRF    INDF    ;clear INDF Register
            INCF    FSR,F   ;inc pointer
            BTFSC   FSR,4   ;all done?
            GOTO    NEXT    ;NO, clear next
CONTINUE
            :               ;YES, continue
```

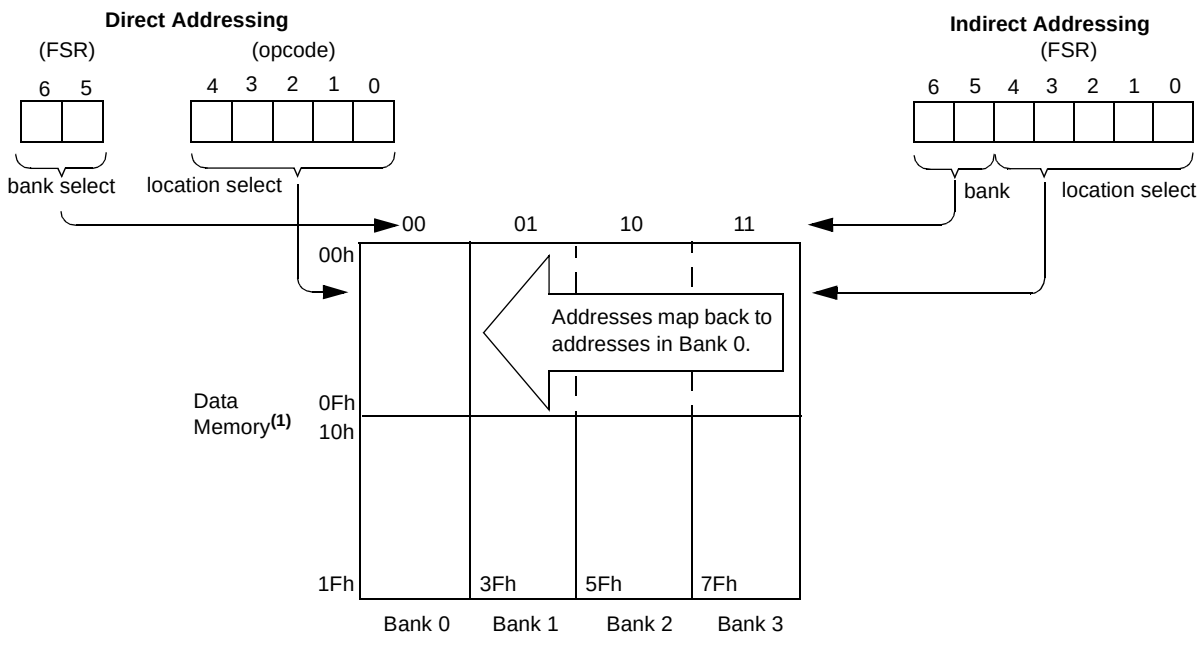
The FSR is either a 5-bit (PIC16C54, PIC16CR54, PIC16C55, PIC16C56, PIC16CR56) or 7-bit (PIC16C57, PIC16CR57, PIC16C58, PIC16CR58) wide register. It is used in conjunction with the INDF Register to indirectly address the data memory area.

The FSR<4:0> bits are used to select data memory addresses 00h to 1Fh.

**PIC16C54, PIC16CR54, PIC16C55, PIC16C56, PIC16CR56:** These do not use banking. FSR<6:5> bits are unimplemented and read as '1's.

**PIC16C57, PIC16CR57, PIC16C58, PIC16CR58:** FSR<6:5> are the bank select bits and are used to select the bank to be addressed (00 = bank 0, 01 = bank 1, 10 = bank 2, 11 = bank 3).

### FIGURE 6-10: DIRECT/INDIRECT ADDRESSING




**Note 1:** For register map detail see Section 6.2.



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**NOTES:**

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## 7.0 I/O PORTS

As with any other register, the I/O Registers can be written and read under program control. However, read instructions (e.g., MOVF PORTB,W) always read the I/O pins independent of the pin's input/output modes. On RESET, all I/O ports are defined as input (inputs are at hi-impedance) since the I/O control registers (TRISA, TRISB, TRISC) are all set.

## 7.1 PORTA

PORTA is a 4-bit I/O Register. Only the low order 4 bits are used (RA<3:0>). Bits 7-4 are unimplemented and read as '0's.

## 7.2 PORTB

PORTB is an 8-bit I/O Register (PORTB<7:0>).

## 7.3 PORTC

PORTC is an 8-bit I/O Register for PIC16C55, PIC16C57 and PIC16CR57.

PORTC is a General Purpose Register for PIC16C54, PIC16CR54, PIC16C56, PIC16CR56, PIC16C58 and PIC16CR58.

## 7.4 TRIS Registers

The Output Driver Control Registers are loaded with the contents of the W Register by executing the TRIS f instruction. A '1' from a TRIS Register bit puts the corresponding output driver in a hi-impedance (input) mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer.

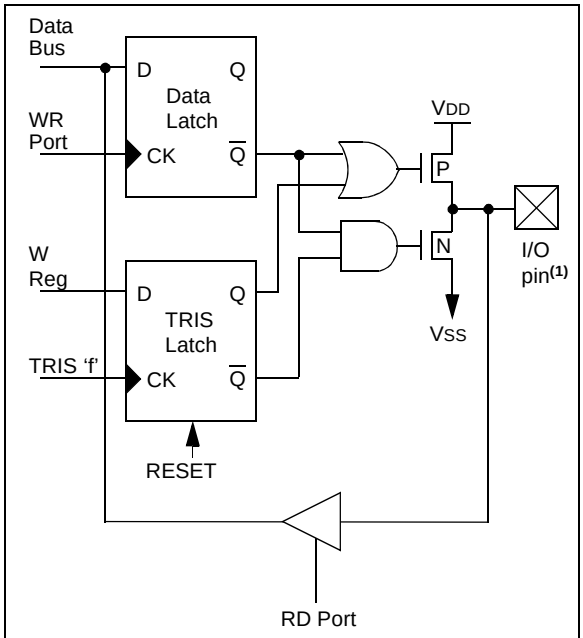
| **Note:** | A read of the ports reads the pins, not the output data latches. That is, if an output driver on a pin is enabled and driven high, but the external system is holding it low, a read of the port will indicate that the pin is low. |
|---|---|

The TRIS Registers are "write-only" and are set (output drivers disabled) upon RESET.

## 7.5 I/O Interfacing

The equivalent circuit for an I/O port pin is shown in Figure 7-1. All ports may be used for both input and output operation. For input operations these ports are non-latching. Any input must be present until read by an input instruction (e.g., MOVF PORTB, W). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit (in TRISA, TRISB, TRISC) must be cleared (= 0). For use as an input, the corresponding TRIS bit must be set. Any I/O pin can be programmed individually as input or output.

**FIGURE 7-1: EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN**




**Note 1:** I/O pins have protection diodes to VDD and VSS.

**TABLE 7-1: SUMMARY OF PORT REGISTERS**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on Power-On Reset | Value on MCLR and WDT Reset |
|---|---|---|---|---|---|---|---|---|---|---|---|
| N/A | TRIS | I/O Control Registers (TRISA, TRISB, TRISC) | | | | | | | | 1111 1111 | 1111 1111 |
| 05h | PORTA | — | — | — | — | RA3 | RA2 | RA1 | RA0 | ---- xxxx | ---- uuuu |
| 06h | PORTB | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 | xxxx xxxx | uuuu uuuu |
| 07h | PORTC | RC7 | RC6 | RC5 | RC4 | RC3 | RC2 | RC1 | RC0 | xxxx xxxx | uuuu uuuu |

Legend: x = unknown, u = unchanged, — = unimplemented, read as '0', Shaded cells = unimplemented, read as '0'



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## 7.6 I/O Programming Considerations

### 7.6.1 BI-DIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU, bit5 to be set and the PORTB value to be written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the Input mode, no problem occurs. However, if bit0 is switched into Output mode later on, the content of the data latch may now be unknown.

Example 7-1 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

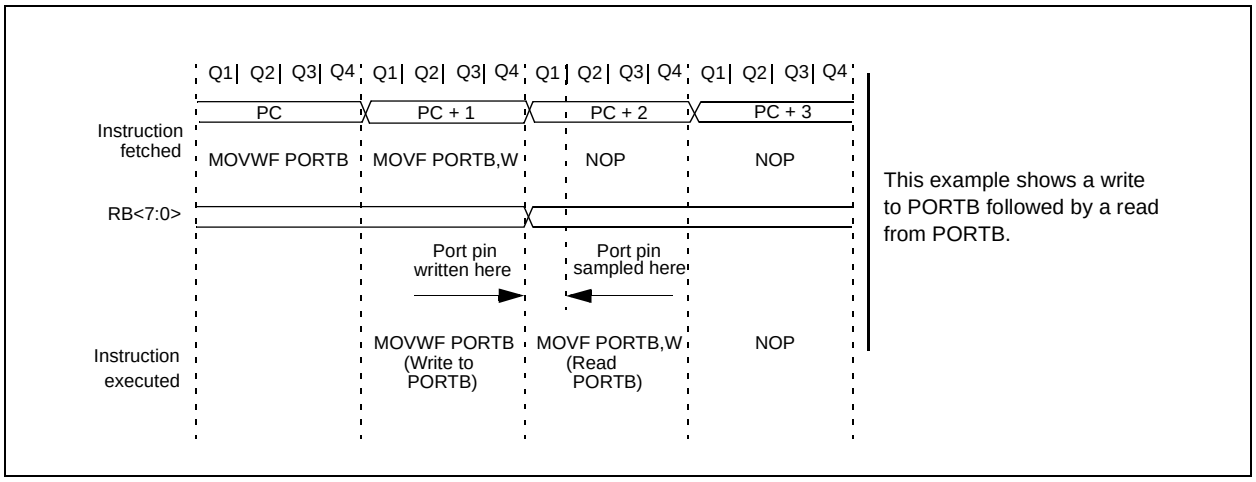
**EXAMPLE 7-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT**

```
;Initial PORT Settings
; PORTB<7:4> Inputs
; PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
;
;                    PORT latch  PORT pins
;                    ----------  ----------
  BCF   PORTB, 7    ;01pp pppp   11pp pppp
  BCF   PORTB, 6    ;10pp pppp   11pp pppp
  MOVLW H'3F'        ;
  TRIS  PORTB       ;10pp pppp   10pp pppp
;
;Note that the user may have expected the pin
;values to be 00pp pppp. The 2nd BCF caused
;RB7 to be latched as the pin value (High).
```

### 7.6.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 7-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction, which causes that file to be read into the CPU, is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

**FIGURE 7-2: SUCCESSIVE I/O OPERATION**

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## 8.0 TIMER0 MODULE AND TMR0 REGISTER

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
  - Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
  - Edge select for external clock

Figure 8-1 is a simplified block diagram of the Timer0 module, while Figure 8-2 shows the electrical structure of the Timer0 input.

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles (Figure 8-3 and Figure 8-4). The user can work around this by writing an adjusted value to the TMR0 register.

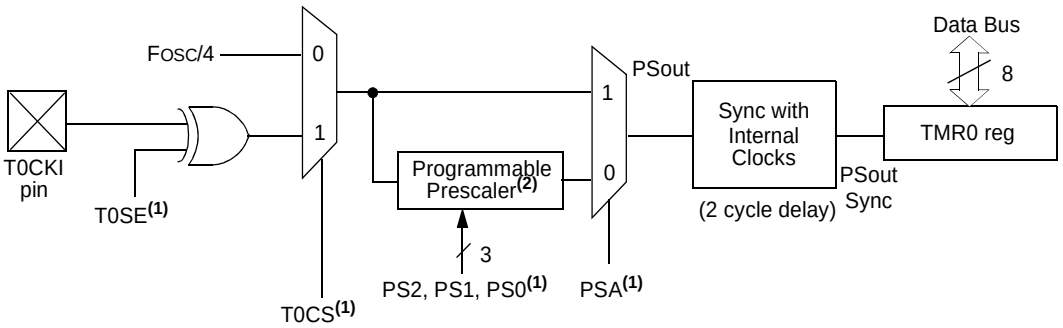
Counter mode is selected by setting the T0CS bit (OPTION<5>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The incrementing edge is determined by the source edge select bit T0SE (OPTION<4>). Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 8.1.

| **Note:** | The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both. |
|---|---|

The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4,..., 1:256 are selectable. Section 8.2 details the operation of the prescaler.

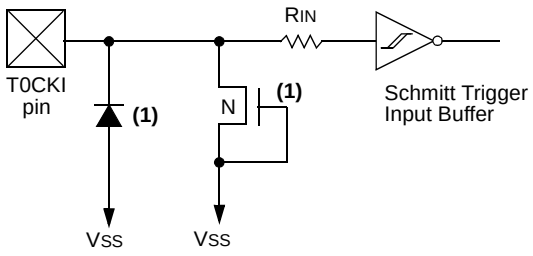
A summary of registers associated with the Timer0 module is found in Table 8-1.

**FIGURE 8-1: TIMER0 BLOCK DIAGRAM**




**Note 1:** Bits T0CS, T0SE, PSA, PS2, PS1 and PS0 are located in the OPTION register (Section 6.4).
**2:** The prescaler is shared with the Watchdog Timer (Figure 8-6).

**FIGURE 8-2: ELECTRICAL STRUCTURE OF T0CKI PIN**




**Note 1:** ESD protection circuits.



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**FIGURE 8-3: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALER**

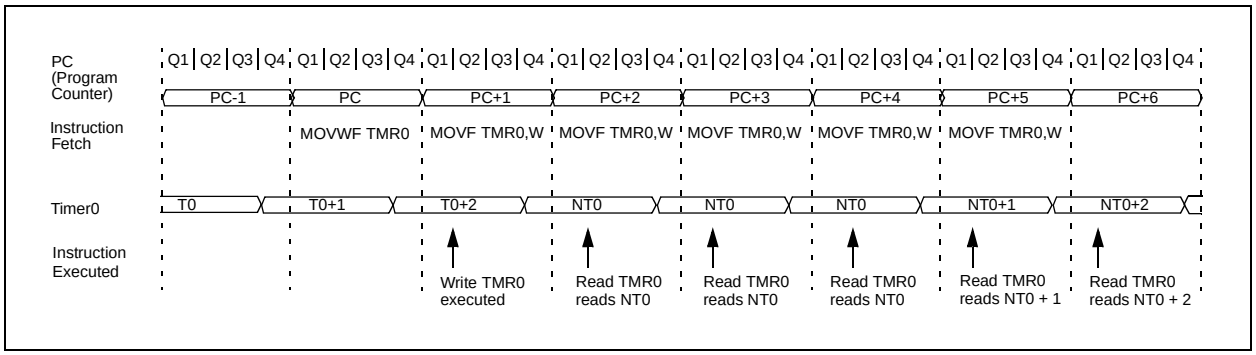


**FIGURE 8-4: TIMER0 TIMING: INTERNAL CLOCK/PRESCALER 1:2**

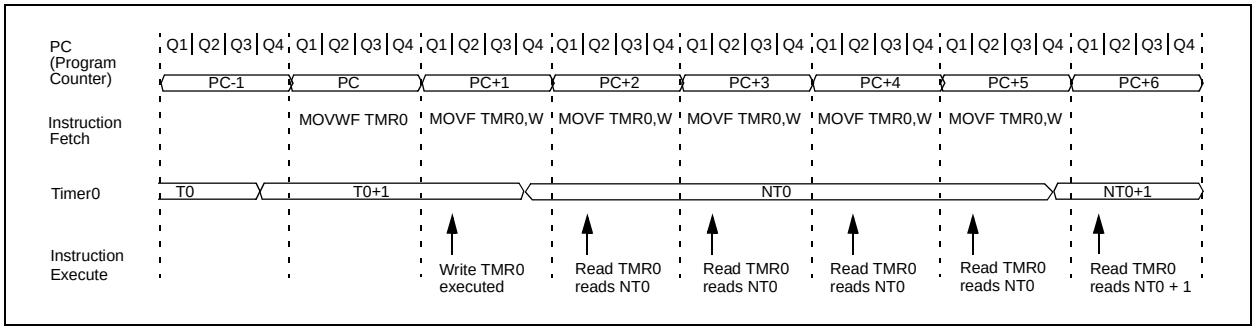


**TABLE 8-1: REGISTERS ASSOCIATED WITH TIMER0**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on Power-on Reset | Value on MCLR and WDT Reset |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 01h | TMR0 | Timer0 - 8-bit real-time clock/counter | | | | | | | | xxxx xxxx | uuuu uuuu |
| N/A | OPTION | — | — | T0CS | T0SE | PSA | PS2 | PS1 | PS0 | --11 1111 | --11 1111 |

Legend: x = unknown, u = unchanged, - = unimplemented. Shaded cells not used by Timer0.

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## 8.1 Using Timer0 with an External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (TOSC) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

### 8.1.1 EXTERNAL CLOCK SYNCHRONIZATION

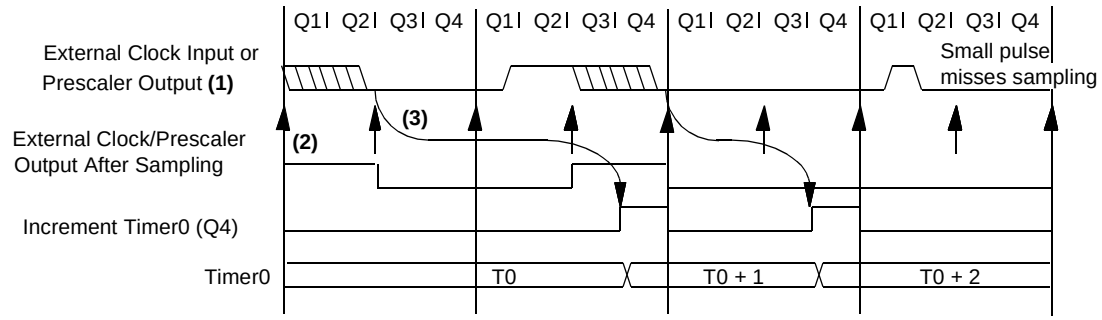
When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 8-5). Therefore, it is necessary for T0CKI to be high for at least 2TOSC (and a small RC delay of 20 ns) and low for at least 2TOSC (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple counter-type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4TOSC (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

### 8.1.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 8-5 shows the delay from the external clock edge to the timer incrementing.

**FIGURE 8-5: TIMER0 TIMING WITH EXTERNAL CLOCK**




**Note 1:** External clock if no prescaler selected, prescaler output otherwise.
**2:** The arrows indicate the points in time where sampling occurs.
**3:** Delay from clock input change to Timer0 increment is 3Tosc to 7Tosc (duration of Q = Tosc). Therefore, the error in measuring the interval between two edges on Timer0 input = ± 4Tosc max.



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## 8.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer (WDT), respectively (Section 9.2.1). For simplicity, this counter is being referred to as “prescaler” throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT, and vice-versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF 1`, `MOVWF 1`, `BSF 1,x`, etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the WDT. The prescaler is neither readable nor writable. On a RESET, the prescaler contains all '0's.

### 8.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed “on the fly” during program execution). To avoid an unintended device RESET, the following instruction sequence (Example 8-1) must be executed when changing the prescaler assignment from Timer0 to the WDT.

**EXAMPLE 8-1: CHANGING PRESCALER (TIMER0→WDT)**

```
CLRWDT              ;Clear WDT
CLRF   TMR0         ;Clear TMR0 & Prescaler
MOVLW  B'00xx1111'  ;Last 3 instructions in
                     this example
OPTION              ;are required only if
                    ;desired
CLRWDT              ;PS<2:0> are 000 or
                    ;001
MOVLW  B'00xx1xxx'  ;Set Prescaler to
OPTION              ;desired WDT rate
```

To change prescaler from the WDT to the Timer0 module, use the sequence shown in Example 8-2. This sequence must be used even if the WDT is disabled. A `CLRWDT` instruction should be executed before switching the prescaler.

**EXAMPLE 8-2: CHANGING PRESCALER (WDT→TIMER0)**

```
CLRWDT                  ;Clear WDT and
                        ;prescaler
MOVLW   B'xxxx0xxx'     ;Select TMR0, new
                        ;prescale value and
                        ;clock source
OPTION
```

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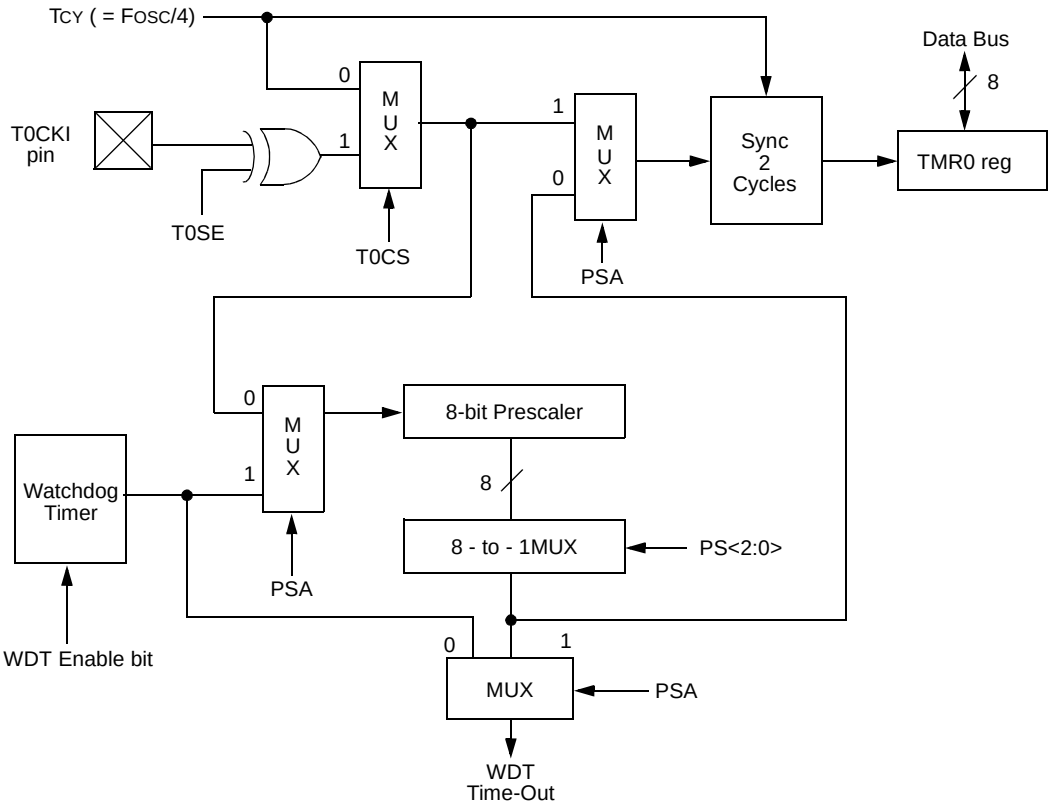
**FIGURE 8-6: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER**




**Note:** T0CS, T0SE, PSA, PS<2:0> are bits in the OPTION register.



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## 9.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits that deal with the needs of real-time applications. The PIC16C5X family of microcontrollers have a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features are:

- Oscillator Selection (Section 4.0)
- RESET (Section 5.0)
- Power-On Reset (Section 5.1)
- Device Reset Timer (Section 5.2)
- Watchdog Timer (WDT) (Section 9.2)
- SLEEP (Section 9.3)
- Code protection (Section 9.4)
- ID locations (Section 9.5)

The PIC16C5X Family has a Watchdog Timer which can be shut off only through configuration bit WDTE. It runs off of its own RC oscillator for added reliability. There is an 18 ms delay provided by the Device Reset Timer (DRT), intended to keep the chip in RESET until the crystal oscillator is stable. With this timer on-chip, most applications need no external RESET circuitry.

The SLEEP mode is designed to offer a very low current Power-down mode. The user can wake up from SLEEP through external RESET or through a Watchdog Timer time-out. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.



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## 9.1 Configuration Bits

Configuration bits can be programmed to select various device configurations. Two bits are for the selection of the oscillator type and one bit is the Watchdog Timer enable bit. Nine bits are code protection bits for the PIC16C54A, PIC16CR54A, PIC16C54C, PIC16CR54C, PIC16C55A, PIC16C56A, PIC16CR56A, PIC16C57C, PIC16CR57C, PIC16C58B, and PIC16CR58B devices (Register 9-1). One bit is for code protection for the PIC16C54, PIC16C55, PIC16C56 and PIC16C57 devices (Register 9-2).

QTP or ROM devices have the oscillator configuration programmed at the factory and these parts are tested accordingly (see "Product Identification System" diagrams in the back of this data sheet).

**REGISTER 9-1: CONFIGURATION WORD FOR PIC16C54A/CR54A/C54C/CR54C/C55A/C56A/ CR56A/C57C/CR57C/C58B/CR58B**

| CP | CP | CP | CP | CP | CP | CP | CP | CP | WDTE | FOSC1 | FOSC0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| bit 11 | | | | | | | | | | | bit 0 |

bit 11-3: **CP**: Code Protection Bit
1 = Code protection off
0 = Code protection on

bit 2: **WDTE**: Watchdog timer enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0: **FOSC1:FOSC0**: Oscillator Selection Bit
00 = LP oscillator
01 = XT oscillator
10 = HS oscillator
11 = RC oscillator

**Note 1:** Refer to the PIC16C5X Programming Specification (Literature Number DS30190) to determine how to access the configuration word.

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | 1 = bit is set | 0 = bit is cleared | x = bit is unknown |

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**REGISTER 9-2: CONFIGURATION WORD FOR PIC16C54/C55/C56/C57**

| — | — | — | — | — | — | — | — | CP | WDTE | FOSC1 | FOSC0 |
|---|---|---|---|---|---|---|---|---|---|---|---|

bit 11 bit 0

bit 11-4: **Unimplemented**: Read as '0'

bit 3: **CP:** Code protection bit.
1 = Code protection off
0 = Code protection on

bit 2: **WDTE:** Watchdog timer enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0: **FOSC1:FOSC0:** Oscillator selection bits(2)
00 = LP oscillator
01 = XT oscillator
10 = HS oscillator
11 = RC oscillator

**Note 1:** Refer to the PIC16C5X Programming Specifications (Literature Number DS30190) to determine how to access the configuration word.
**2:** PIC16LV54A supports XT, RC and LP oscillator only.

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | 1 = bit is set | 0 = bit is cleared | x = bit is unknown |



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## 9.2 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins have been stopped, for example, by execution of a SLEEP instruction. During normal operation or SLEEP, a WDT Reset or Wake-up Reset generates a device RESET.

The $\overline{TO}$ bit (STATUS<4>) will be cleared upon a Watchdog Timer Reset (Section 6.3).

The WDT can be permanently disabled by programming the configuration bit WDTE as a '0' (Section 9.1). Refer to the PIC16C5X Programming Specifications (Literature Number DS30190) to determine how to access the configuration word.

### 9.2.1 WDT PERIOD

An 8-bit counter is available as a prescaler for the Timer0 module (Section 8.2), or as a postscaler for the Watchdog Timer (WDT), respectively. For simplicity, this counter is being referred to as “prescaler” throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT, and vice-versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine prescaler assignment and prescale ratio (Section 6.4).

The WDT has a nominal time-out period of 18 ms (with no prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, time-out a period of a nominal 2.3 seconds can be realized. These periods vary with temperature, VDD and part-to-part process variations (see Device Characterization).

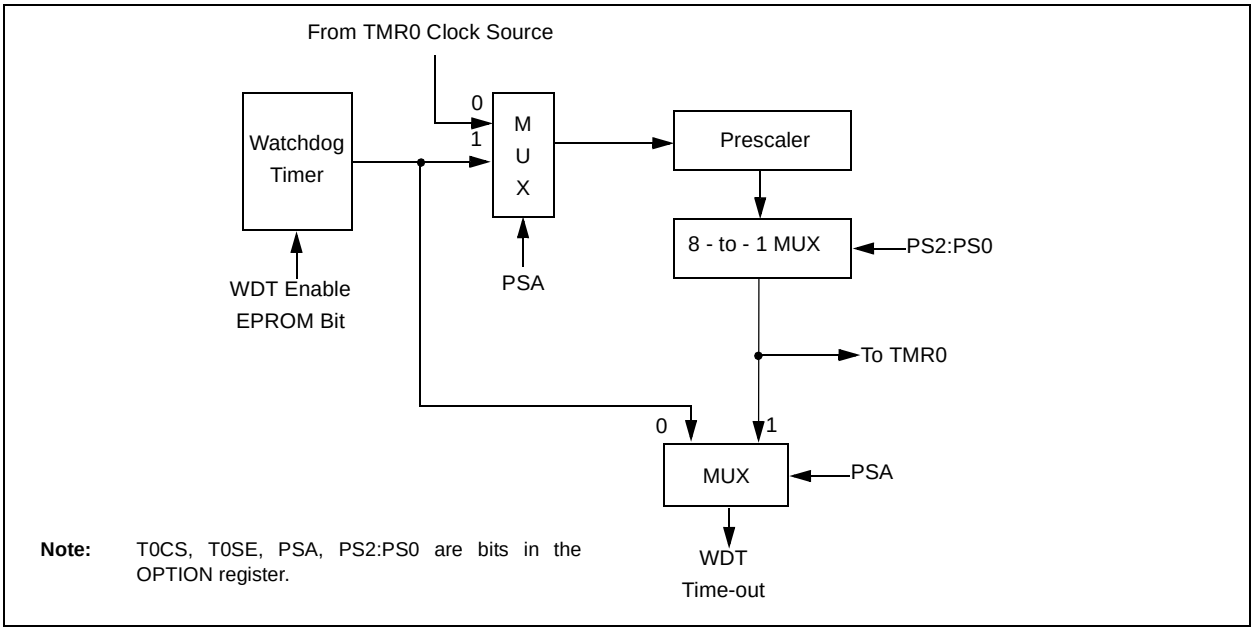
Under worst case conditions (VDD = Min., Temperature = Max., WDT prescaler = 1:128), it may take several seconds before a WDT time-out occurs.

### 9.2.2 WDT PROGRAMMING CONSIDERATIONS

The CLRWDT instruction clears the WDT and the prescaler, if assigned to the WDT, and prevents it from timing out and generating a device RESET.

The SLEEP instruction RESETS the WDT and the prescaler, if assigned to the WDT. This gives the maximum SLEEP time before a WDT Wake-up Reset.

**FIGURE 9-1: WATCHDOG TIMER BLOCK DIAGRAM**




**Note:** T0CS, T0SE, PSA, PS2:PS0 are bits in the OPTION register.

**TABLE 9-1: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on Power-On Reset | Value on MCLR and WDT Reset |
|---|---|---|---|---|---|---|---|---|---|---|---|
| N/A | OPTION | — | — | Tosc | Tose | PSA | PS2 | PS1 | PS0 | --11 1111 | --11 1111 |

Legend: u = unchanged, - = unimplemented, read as '0'. Shaded cells not used by Watchdog Timer.

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## 9.3 Power-Down Mode (SLEEP)

A device may be powered down (SLEEP) and later powered up (Wake-up from SLEEP).

### 9.3.1 SLEEP

The Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the $\overline{TO}$ bit (STATUS<4>) is set, the $\overline{PD}$ bit (STATUS<3>) is cleared and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, driving low, or hi-impedance).

It should be noted that a RESET generated by a WDT time-out does not drive the $\overline{MCLR}/V_{PP}$ pin low.

For lowest current consumption while powered down, the T0CKI input should be at $V_{DD}$ or $V_{SS}$ and the $\overline{MCLR}/V_{PP}$ pin must be at a logic high level ($\overline{MCLR} = V_{IH}$).

### 9.3.2 WAKE-UP FROM SLEEP

The device can wake up from SLEEP through one of the following events:

1. An external RESET input on $\overline{MCLR}/V_{PP}$ pin.
2. A Watchdog Timer Time-out Reset (if WDT was enabled).

Both of these events cause a device RESET. The $\overline{TO}$ and $\overline{PD}$ bits can be used to determine the cause of device RESET. The $\overline{TO}$ bit is cleared if a WDT time-out occurred (and caused wake-up). The $\overline{PD}$ bit, which is set on power-up, is cleared when SLEEP is invoked.

The WDT is cleared when the device wakes from SLEEP, regardless of the wake-up source.

## 9.4 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

| | |
|---|---|
| **Note:** | Microchip does not recommend code protecting windowed devices. |

## 9.5 ID Locations

Four memory locations are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify.

Use only the lower 4 bits of the ID locations and always program the upper 8 bits as '1's.

| | |
|---|---|
| **Note:** | Microchip will assign a unique pattern number for QTP and SQTP requests and for ROM devices. This pattern number will be unique and traceable to the submitted code. |



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## 10.0 INSTRUCTION SET SUMMARY

Each PIC16C5X instruction is a 12-bit word divided into an OPCODE, which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC16C5X instruction set summary in Table 10-2 groups the instructions into byte-oriented, bit-oriented, and literal and control operations. Table 10-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator is used to specify which one of the 32 file registers in that bank is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8 or 9-bit constant or literal value.

**TABLE 10-1: OPCODE FIELD DESCRIPTIONS**

| Field | Description |
|---|---|
| f | Register file address (0x00 to 0x1F) |
| W | Working register (accumulator) |
| b | Bit address within an 8-bit file register |
| k | Literal field, constant data or label |
| x | Don't care location (= 0 or 1)<br>The assembler will generate code with x = 0.<br>It is the recommended form of use for compatibility with all Microchip software tools. |
| d | Destination select;<br>d = 0 (store result in W)<br>d = 1 (store result in file register 'f')<br>Default is d = 1 |
| label | Label name |
| TOS | Top of Stack |
| PC | Program Counter |
| WDT | Watchdog Timer Counter |
| $\overline{TO}$ | Time-out bit |
| $\overline{PD}$ | Power-down bit |
| dest | Destination, either the W register or the specified register file location |
| [ ] | Options |
| ( ) | Contents |
| → | Assigned to |
| < > | Register bit field |
| ∈ | In the set of |
| *italics* | User defined term (font is courier) |

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time would be 1 μs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time would be 2 μs.

Figure 10-1 shows the three general formats that the instructions can have. All examples in the figure use the following format to represent a hexadecimal number:

0xhhh

where 'h' signifies a hexadecimal digit.

**FIGURE 10-1: GENERAL FORMAT FOR INSTRUCTIONS**

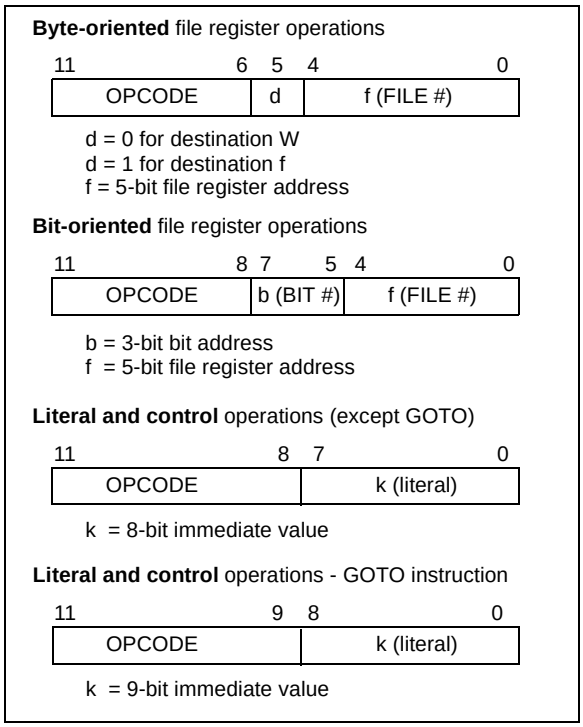




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**TABLE 10-2: INSTRUCTION SET SUMMARY**

| Mnemonic, Operands | | Description | Cycles | 12-Bit Opcode MSb | | LSb | Status Affected | Notes |
|---|---|---|---|---|---|---|---|---|
| ADDWF | f,d | Add W and f | 1 | 0001 | 11df | ffff | C,DC,Z | 1,2,4 |
| ANDWF | f,d | AND W with f | 1 | 0001 | 01df | ffff | Z | 2,4 |
| CLRF | f | Clear f | 1 | 0000 | 011f | ffff | Z | 4 |
| CLRW | – | Clear W | 1 | 0000 | 0100 | 0000 | Z | |
| COMF | f, d | Complement f | 1 | 0010 | 01df | ffff | Z | |
| DECF | f, d | Decrement f | 1 | 0000 | 11df | ffff | Z | 2,4 |
| DECFSZ | f, d | Decrement f, Skip if 0 | 1(2) | 0010 | 11df | ffff | None | 2,4 |
| INCF | f, d | Increment f | 1 | 0010 | 10df | ffff | Z | 2,4 |
| INCFSZ | f, d | Increment f, Skip if 0 | 1(2) | 0011 | 11df | ffff | None | 2,4 |
| IORWF | f, d | Inclusive OR W with f | 1 | 0001 | 00df | ffff | Z | 2,4 |
| MOVF | f, d | Move f | 1 | 0010 | 00df | ffff | Z | 2,4 |
| MOVWF | f | Move W to f | 1 | 0000 | 001f | ffff | None | 1,4 |
| NOP | – | No Operation | 1 | 0000 | 0000 | 0000 | None | |
| RLF | f, d | Rotate left f through Carry | 1 | 0011 | 01df | ffff | C | 2,4 |
| RRF | f, d | Rotate right f through Carry | 1 | 0011 | 00df | ffff | C | 2,4 |
| SUBWF | f, d | Subtract W from f | 1 | 0000 | 10df | ffff | C,DC,Z | 1,2,4 |
| SWAPF | f, d | Swap f | 1 | 0011 | 10df | ffff | None | 2,4 |
| XORWF | f, d | Exclusive OR W with f | 1 | 0001 | 10df | ffff | Z | 2,4 |
| **BIT-ORIENTED FILE REGISTER OPERATIONS** | | | | | | | | |
| BCF | f, b | Bit Clear f | 1 | 0100 | bbbf | ffff | None | 2,4 |
| BSF | f, b | Bit Set f | 1 | 0101 | bbbf | ffff | None | 2,4 |
| BTFSC | f, b | Bit Test f, Skip if Clear | 1 (2) | 0110 | bbbf | ffff | None | |
| BTFSS | f, b | Bit Test f, Skip if Set | 1 (2) | 0111 | bbbf | ffff | None | |
| **LITERAL AND CONTROL OPERATIONS** | | | | | | | | |
| ANDLW | k | AND literal with W | 1 | 1110 | kkkk | kkkk | Z | |
| CALL | k | Call subroutine | 2 | 1001 | kkkk | kkkk | None | 1 |
| CLRWDT | k | Clear Watchdog Timer | 1 | 0000 | 0000 | 0100 | $\overline{TO}$, $\overline{PD}$ | |
| GOTO | k | Unconditional branch | 2 | 101k | kkkk | kkkk | None | |
| IORLW | k | Inclusive OR Literal with W | 1 | 1101 | kkkk | kkkk | Z | |
| MOVLW | k | Move Literal to W | 1 | 1100 | kkkk | kkkk | None | |
| OPTION | k | Load OPTION register | 1 | 0000 | 0000 | 0010 | None | |
| RETLW | k | Return, place Literal in W | 2 | 1000 | kkkk | kkkk | None | |
| SLEEP | – | Go into standby mode | 1 | 0000 | 0000 | 0011 | $\overline{TO}$, $\overline{PD}$ | |
| TRIS | f | Load TRIS register | 1 | 0000 | 0000 | 0fff | None | 3 |
| XORLW | k | Exclusive OR Literal to W | 1 | 1111 | kkkk | kkkk | Z | |

**Note 1:** The 9th bit of the program counter will be forced to a '0' by any instruction that writes to the PC except for `GOTO` (see Section 6.5 for more on program counter).

**2:** When an I/O register is modified as a function of itself (e.g. `MOVF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

**3:** The instruction `TRIS f`, where f = 5, 6 or 7 causes the contents of the W register to be written to the tristate latches of PORTA, B or C respectively. A '1' forces the pin to a hi-impedance state and disables the output buffers.

**4:** If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared (if assigned to TMR0).

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**ADDWF** **Add W and f**

Syntax: [ *label* ] ADDWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (W) + (f) → (dest)

Status Affected: C, DC, Z

Encoding:

| 0001 | 11df | ffff |
|---|---|---|

Description: Add the contents of the W register and register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example:
```
ADDWF  TEMP_REG, 0
```
Before Instruction
W = 0x17
TEMP_REG = 0xC2
After Instruction
W = 0xD9
TEMP_REG = 0xC2

**ANDWF** **AND W with f**

Syntax: [ *label* ] ANDWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (W) .AND. (f) → (dest)

Status Affected: Z

Encoding:

| 0001 | 01df | ffff |
|---|---|---|

Description: The contents of the W register are AND'ed with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example:
```
ANDWF  TEMP_REG, 1
```
Before Instruction
W = 0x17
TEMP_REG = 0xC2
After Instruction
W = 0x17
TEMP_REG = 0x02

**ANDLW** **AND literal with W**

Syntax: [ *label* ] ANDLW k

Operands: $0 \le k \le 255$

Operation: (W).AND. (k) → (W)

Status Affected: Z

Encoding:

| 1110 | kkkk | kkkk |
|---|---|---|

Description: The contents of the W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example:
```
ANDLW  H'5F'
```
Before Instruction
W = 0xA3
After Instruction
W = 0x03

**BCF** **Bit Clear f**

Syntax: [ *label* ] BCF f,b

Operands: $0 \le f \le 31$
$0 \le b \le 7$

Operation: 0 → (f<b>)

Status Affected: None

Encoding:

| 0100 | bbbf | ffff |
|---|---|---|

Description: Bit 'b' in register 'f' is cleared.

Words: 1

Cycles: 1

Example:
```
BCF    FLAG_REG,  7
```
Before Instruction
FLAG_REG = 0xC7
After Instruction
FLAG_REG = 0x47



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**BSF** **Bit Set f**

Syntax: [ *label* ] BSF f,b

Operands: 0 ≤ f ≤ 31
0 ≤ b ≤ 7

Operation: 1 → (f<b>)

Status Affected: None

Encoding:

| 0101 | bbbf | ffff |
|---|---|---|

Description: Bit 'b' in register 'f' is set.

Words: 1

Cycles: 1

Example:
```
BSF     FLAG_REG,    7
```
Before Instruction
FLAG_REG = 0x0A
After Instruction
FLAG_REG = 0x8A

**BTFSC** **Bit Test f, Skip if Clear**

Syntax: [ *label* ] BTFSC f,b

Operands: 0 ≤ f ≤ 31
0 ≤ b ≤ 7

Operation: skip if (f<b>) = 0

Status Affected: None

Encoding:

| 0110 | bbbf | ffff |
|---|---|---|

Description: If bit 'b' in register 'f' is 0 then the next instruction is skipped.
If bit 'b' is 0 then the next instruction fetched during the current instruction execution is discarded, and a `NOP` is executed instead, making this a 2-cycle instruction.

Words: 1

Cycles: 1(2)

Example:
```
HERE    BTFSC   FLAG,1
FALSE   GOTO    PROCESS_CODE
TRUE    •
        •
        •
```
Before Instruction
PC = address `(HERE)`
After Instruction
if FLAG<1> = 0,
PC = address `(TRUE)`;
if FLAG<1> = 1,
PC = address `(FALSE)`

**BTFSS** **Bit Test f, Skip if Set**

Syntax: [ *label* ] BTFSS f,b

Operands: 0 ≤ f ≤ 31
0 ≤ b < 7

Operation: skip if (f<b>) = 1

Status Affected: None

Encoding:

| 0111 | bbbf | ffff |
|---|---|---|

Description: If bit 'b' in register 'f' is '1' then the next instruction is skipped.
If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is discarded and a `NOP` is executed instead, making this a 2-cycle instruction.

Words: 1

Cycles: 1(2)

Example:
```
HERE    BTFSS   FLAG,1
FALSE   GOTO    PROCESS_CODE
TRUE    •
        •
        •
```
Before Instruction
PC = address `(HERE)`
After Instruction
If FLAG<1> = 0,
PC = address `(FALSE)`;
if FLAG<1> = 1,
PC = address `(TRUE)`

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**CALL** **Subroutine Call**

Syntax: [ *label* ] CALL k

Operands: 0 ≤ k ≤ 255

Operation: (PC) + 1→ TOS;
k → PC<7:0>;
(STATUS<6:5>) → PC<10:9>;
0 → PC<8>

Status Affected: None

Encoding:

| 1001 | kkkk | kkkk |
|---|---|---|

Description: Subroutine call. First, return address (PC+1) is pushed onto the stack. The eight bit immediate address is loaded into PC bits <7:0>. The upper bits PC<10:9> are loaded from STATUS<6:5>, PC<8> is cleared. CALL is a two-cycle instruction.

Words: 1

Cycles: 2

Example: HERE CALL THERE

Before Instruction
PC = address (HERE)
After Instruction
PC = address (THERE)
TOS = address (HERE + 1)

**CLRF** **Clear f**

Syntax: [ *label* ] CLRF f

Operands: 0 ≤ f ≤ 31

Operation: 00h → (f);
1 → Z

Status Affected: Z

Encoding:

| 0000 | 011f | ffff |
|---|---|---|

Description: The contents of register 'f' are cleared and the Z bit is set.

Words: 1

Cycles: 1

Example: CLRF FLAG_REG

Before Instruction
FLAG_REG = 0x5A
After Instruction
FLAG_REG = 0x00
Z = 1

**CLRW** **Clear W**

Syntax: [ *label* ] CLRW

Operands: None

Operation: 00h → (W);
1 → Z

Status Affected: Z

Encoding:

| 0000 | 0100 | 0000 |
|---|---|---|

Description: The W register is cleared. Zero bit (Z) is set.

Words: 1

Cycles: 1

Example: CLRW

Before Instruction
W = 0x5A
After Instruction
W = 0x00
Z = 1

**CLRWDT** **Clear Watchdog Timer**

Syntax: [ *label* ] CLRWDT

Operands: None

Operation: 00h → WDT;
0 → WDT prescaler (if assigned);
1 → $\overline{TO}$;
1 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

| 0000 | 0000 | 0100 |
|---|---|---|

Description: The CLRWDT instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

Words: 1

Cycles: 1

Example: CLRWDT

Before Instruction
WDT counter = ?
After Instruction
WDT counter = 0x00
WDT prescaler = 0
$\overline{TO}$ = 1
$\overline{PD}$ = 1



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**COMF** **Complement f**

Syntax: [ *label* ] COMF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: $(\bar{f}) \rightarrow (dest)$

Status Affected: Z

Encoding:

| 0010 | 01df | ffff |
|---|---|---|

Description: The contents of register 'f' are complemented. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example:
```
COMF   REG1,0
```
Before Instruction
REG1 = 0x13
After Instruction
REG1 = 0x13
W = 0xEC

**DECF** **Decrement f**

Syntax: [ *label* ] DECF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f) – 1 → (dest)

Status Affected: Z

Encoding:

| 0000 | 11df | ffff |
|---|---|---|

Description: Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example:
```
DECF    CNT, 1
```
Before Instruction
CNT = 0x01
Z = 0
After Instruction
CNT = 0x00
Z = 1

**DECFSZ** **Decrement f, Skip if 0**

Syntax: [ *label* ] DECFSZ f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f) – 1 → d; skip if result = 0

Status Affected: None

Encoding:

| 0010 | 11df | ffff |
|---|---|---|

Description: The contents of register 'f' are decremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.
If the result is 0, the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a two-cycle instruction.

Words: 1

Cycles: 1(2)

Example:
```
HERE      DECFSZ   CNT, 1
          GOTO     LOOP
CONTINUE  •
          •
          •
```
Before Instruction
PC = address (HERE)
After Instruction
CNT = CNT - 1;
if CNT = 0,
PC = address (CONTINUE);
if CNT ≠ 0,
PC = address (HERE+1)

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**GOTO** **Unconditional Branch**

Syntax: [ *label* ] GOTO k

Operands: $0 \le k \le 511$

Operation: $k \rightarrow PC<8:0>$;
STATUS<6:5> → PC<10:9>

Status Affected: None

Encoding:

| | | |
|---|---|---|
| 101k | kkkk | kkkk |

Description: GOTO is an unconditional branch. The 9-bit immediate value is loaded into PC bits <8:0>. The upper bits of PC are loaded from STATUS<6:5>. GOTO is a two-cycle instruction.

Words: 1

Cycles: 2

Example:
```
GOTO THERE
```
After Instruction
PC = address (THERE)

**INCF** **Increment f**

Syntax: [ *label* ] INCF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f) + 1 → (dest)

Status Affected: Z

Encoding:

| | | |
|---|---|---|
| 0010 | 10df | ffff |

Description: The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

Words: 1

Cycles: 1

Example:
```
INCF  CNT,  1
```
Before Instruction
CNT = 0xFF
Z = 0
After Instruction
CNT = 0x00
Z = 1

**INCFSZ** **Increment f, Skip if 0**

Syntax: [ *label* ] INCFSZ f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f) + 1 → (dest), skip if result = 0

Status Affected: None

Encoding:

| | | |
|---|---|---|
| 0011 | 11df | ffff |

Description: The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.
If the result is 0, then the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a two-cycle instruction.

Words: 1

Cycles: 1(2)

Example:
```
HERE     INCFSZ   CNT, 1
         GOTO     LOOP
CONTINUE •
         •
         •
```
Before Instruction
PC = address (HERE)
After Instruction
CNT = CNT + 1;
if CNT = 0,
PC = address (CONTINUE);
if CNT ≠ 0,
PC = address (HERE +1)



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**IORLW** **Inclusive OR literal with W**

Syntax: [ *label* ] IORLW k

Operands: $0 \le k \le 255$

Operation: (W) .OR. (k) → (W)

Status Affected: Z

Encoding:

| | | |
|---|---|---|
| 1101 | kkkk | kkkk |

Description: The contents of the W register are OR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example:
```
IORLW  0x35
```
Before Instruction
W = 0x9A
After Instruction
W = 0xBF
Z = 0

**IORWF** **Inclusive OR W with f**

Syntax: [ *label* ] IORWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (W).OR. (f) → (dest)

Status Affected: Z

Encoding:

| | | |
|---|---|---|
| 0001 | 00df | ffff |

Description: Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

Words: 1

Cycles: 1

Example:
```
IORWF          RESULT, 0
```
Before Instruction
RESULT = 0x13
W = 0x91
After Instruction
RESULT = 0x13
W = 0x93
Z = 0

**MOVF** **Move f**

Syntax: [ *label* ] MOVF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f) → (dest)

Status Affected: Z

Encoding:

| | | |
|---|---|---|
| 0010 | 00df | ffff |

Description: The contents of register 'f' is moved to destination 'd'. If 'd' is 0, destination is the W register. If 'd' is 1, the destination is file register 'f'. 'd' is 1 is useful to test a file register since status flag Z is affected.

Words: 1

Cycles: 1

Example:
```
MOVF   FSR,   0
```
After Instruction
W = value in FSR register

**MOVLW** **Move Literal to W**

Syntax: [ *label* ] MOVLW k

Operands: $0 \le k \le 255$

Operation: k → (W)

Status Affected: None

Encoding:

| | | |
|---|---|---|
| 1100 | kkkk | kkkk |

Description: The eight bit literal 'k' is loaded into the W register.

Words: 1

Cycles: 1

Example:
```
MOVLW  0x5A
```
After Instruction
W = 0x5A

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**MOVWF** **Move W to f**

Syntax: [ *label* ] MOVWF f

Operands: $0 \le f \le 31$

Operation: (W) → (f)

Status Affected: None

Encoding:

| 0000 | 001f | ffff |
|---|---|---|

Description: Move data from the W register to register 'f'.

Words: 1

Cycles: 1

Example:
```
MOVWF   TEMP_REG
```
Before Instruction
TEMP_REG = 0xFF
W = 0x4F
After Instruction
TEMP_REG = 0x4F
W = 0x4F

**NOP** **No Operation**

Syntax: [ *label* ] NOP

Operands: None

Operation: No operation

Status Affected: None

Encoding:

| 0000 | 0000 | 0000 |
|---|---|---|

Description: No operation.

Words: 1

Cycles: 1

Example:
```
NOP
```

**OPTION** **Load OPTION Register**

Syntax: [ *label* ] OPTION

Operands: None

Operation: (W) → OPTION

Status Affected: None

Encoding:

| 0000 | 0000 | 0010 |
|---|---|---|

Description: The content of the W register is loaded into the OPTION register.

Words: 1

Cycles: 1

Example
```
OPTION
```
Before Instruction
W = 0x07
After Instruction
OPTION = 0x07

**RETLW** **Return with Literal in W**

Syntax: [ *label* ] RETLW k

Operands: $0 \le k \le 255$

Operation: k → (W);
TOS → PC

Status Affected: None

Encoding:

| 1000 | kkkk | kkkk |
|---|---|---|

Description: The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.

Words: 1

Cycles: 2

Example:
```
        CALL TABLE ;W contains
                   ;table offset
                   ;value.
        •          ;W now has table
        •          ;value.
TABLE   •
        ADDWF PC   ;W = offset
        RETLW k1   ;Begin table
        RETLW k2   ;
        •
        •
        •
        RETLW kn   ; End of table
```
Before Instruction
W = 0x07
After Instruction
W = value of k8



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**RLF** **Rotate Left f through Carry**

Syntax: [ *label* ] RLF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

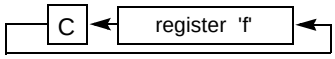
Operation: See description below

Status Affected: C

Encoding:

| 0011 | 01df | ffff |
|---|---|---|

Description: The contents of register 'f' are rotated one bit to the left through the Carry Flag (STATUS<0>). If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is stored back in register 'f'.




Words: 1

Cycles: 1

Example:
```
RLF    REG1,0
```
Before Instruction
```
REG1    =  1110 0110
C       =  0
```
After Instruction
```
REG1    =  1110 0110
W       =  1100 1100
C       =  1
```

**RRF** **Rotate Right f through Carry**

Syntax: [ *label* ] RRF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

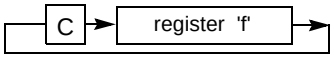
Operation: See description below

Status Affected: C

Encoding:

| 0011 | 00df | ffff |
|---|---|---|

Description: The contents of register 'f' are rotated one bit to the right through the Carry Flag (STATUS<0>). If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.




Words: 1

Cycles: 1

Example:
```
RRF    REG1,0
```
Before Instruction
```
REG1    =  1110 0110
C       =  0
```
After Instruction
```
REG1    =  1110 0110
W       =  0111 0011
C       =  0
```

**SLEEP** **Enter SLEEP Mode**

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT;
0 → WDT prescaler; if assigned
1 → $\overline{TO}$;
0 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

| 0000 | 0000 | 0011 |
|---|---|---|

Description: Time-out status bit ($\overline{TO}$) is set. The power-down status bit ($\overline{PD}$) is cleared. The WDT and its prescaler are cleared.
The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP for more details.

Words: 1

Cycles: 1

Example:
```
SLEEP
```

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**SUBWF** **Subtract W from f**

Syntax: [*label*] SUBWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f) – (W) → (dest)

Status Affected: C, DC, Z

Encoding:

| 0000 | 10df | ffff |
|---|---|---|

Description: Subtract (2's complement method) the W register from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example 1: `SUBWF REG1, 1`

Before Instruction
REG1 = 3
W = 2
C = ?
After Instruction
REG1 = 1
W = 2
C = 1 ; result is positive

Example 2:
Before Instruction
REG1 = 2
W = 2
C = ?
After Instruction
REG1 = 0
W = 2
C = 1 ; result is zero

Example 3:
Before Instruction
REG1 = 1
W = 2
C = ?
After Instruction
REG1 = 0xFF
W = 2
C = 0 ; result is negative

**SWAPF** **Swap Nibbles in f**

Syntax: [ *label* ] SWAPF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f<3:0>) → (dest<7:4>);
(f<7:4>) → (dest<3:0>)

Status Affected: None

Encoding:

| 0011 | 10df | ffff |
|---|---|---|

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.

Words: 1

Cycles: 1

Example `SWAPF REG1, 0`

Before Instruction
REG1 = 0xA5
After Instruction
REG1 = 0xA5
W = 0x5A

**TRIS** **Load TRIS Register**

Syntax: [ *label* ] TRIS f

Operands: f = 5, 6 or 7

Operation: (W) → TRIS register f

Status Affected: None

Encoding:

| 0000 | 0000 | 0fff |
|---|---|---|

Description: TRIS register 'f' (f = 5, 6, or 7) is loaded with the contents of the W register.

Words: 1

Cycles: 1

Example `TRIS PORTB`

Before Instruction
W = 0xA5
After Instruction
TRISB = 0xA5



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**XORLW** **Exclusive OR literal with W**

Syntax: [*label*] XORLW k

Operands: $0 \le k \le 255$

Operation: (W) .XOR. k → (W)

Status Affected: Z

Encoding:

| 1111 | kkkk | kkkk |
|---|---|---|

Description: The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example: XORLW 0xAF

Before Instruction
W = 0xB5
After Instruction
W = 0x1A

**XORWF** **Exclusive OR W with f**

Syntax: [ *label* ] XORWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (W) .XOR. (f) → (dest)

Status Affected: Z

Encoding:

| 0001 | 10df | ffff |
|---|---|---|

Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example XORWF REG,1

Before Instruction
REG = 0xAF
W = 0xB5
After Instruction
REG = 0x1A
W = 0xB5

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## 11.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
  - MPASM™ Assembler
  - MPLAB C17 and MPLAB C18 C Compilers
  - MPLINK™ Object Linker/ MPLIB™ Object Librarian
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB ICE 2000 In-Circuit Emulator
  - ICEPIC™ In-Circuit Emulator
- In-Circuit Debugger
  - MPLAB ICD
- Device Programmers
  - PRO MATE® II Universal Device Programmer
  - PICSTART® Plus Entry-Level Development Programmer
- Low Cost Demonstration Boards
  - PICDEM™ 1 Demonstration Board
  - PICDEM 2 Demonstration Board
  - PICDEM 3 Demonstration Board
  - PICDEM 17 Demonstration Board
  - KEELOQ® Demonstration Board

### 11.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8-bit microcontroller market. The MPLAB IDE is a Windows®-based application that contains:

- An interface to debugging tools
  - simulator
  - programmer (sold separately)
  - emulator (sold separately)
  - in-circuit debugger (sold separately)
- A full-featured editor
- A project manager
- Customizable toolbar and key mapping
- A status bar
- On-line help

The MPLAB IDE allows you to:

- Edit your source files (either assembly or ‘C’)
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
  - source files
  - absolute listing file
  - machine code

The ability to use MPLAB IDE with multiple debugging tools allows users to easily switch from the cost-effective simulator to a full-featured emulator with minimal retraining.

### 11.2 MPASM Assembler

The MPASM assembler is a full-featured universal macro assembler for all PIC MCUs.

The MPASM assembler has a command line interface and a Windows shell. It can be used as a stand-alone application on a Windows 3.x or greater system, or it can be used through MPLAB IDE. The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, an absolute LST file that contains source lines and generated machine code, and a COD file for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects.
- User-defined macros to streamline assembly code.
- Conditional assembly for multi-purpose source files.
- Directives that allow complete control over the assembly process.

### 11.3 MPLAB C17 and MPLAB C18 C Compilers

The MPLAB C17 and MPLAB C18 Code Development Systems are complete ANSI ‘C’ compilers for Microchip’s PIC17CXXX and PIC18CXXX family of microcontrollers, respectively. These compilers provide powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compilers provide symbol information that is compatible with the MPLAB IDE memory display.



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## 11.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK object linker combines relocatable objects created by the MPASM assembler and the MPLAB C17 and MPLAB C18 C compilers. It can also link relocatable objects from pre-compiled libraries, using directives from a linker script.

The MPLIB object librarian is a librarian for pre-compiled code to be used with the MPLINK object linker. When a routine from a library is called from another source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications. The MPLIB object librarian manages the creation and modification of library files.

The MPLINK object linker features include:

- Integration with MPASM assembler and MPLAB C17 and MPLAB C18 C compilers.
- Allows all memory areas to be defined as sections to provide link-time flexibility.

The MPLIB object librarian features include:

- Easier linking because single libraries can be included instead of many smaller files.
- Helps keep code maintainable by grouping related modules together.
- Allows libraries to be created and modules to be added, listed, replaced, deleted or extracted.

## 11.5 MPLAB SIM Software Simulator

The MPLAB SIM software simulator allows code development in a PC-hosted environment by simulating the PIC series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user-defined key press, to any of the pins. The execution can be performed in single step, execute until break, or trace mode.

The MPLAB SIM simulator fully supports symbolic debugging using the MPLAB C17 and the MPLAB C18 C compilers and the MPASM assembler. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent multi-project software development tool.

## 11.6 MPLAB ICE High Performance Universal In-Circuit Emulator with MPLAB IDE

The MPLAB ICE universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PIC microcontrollers (MCUs). Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment (IDE), which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PIC microcontrollers.

The MPLAB ICE in-circuit emulator system has been designed as a real-time emulation system, with advanced features that are generally found on more expensive development tools. The PC platform and Microsoft® Windows environment were chosen to best make these features available to you, the end user.

## 11.7 ICEPIC In-Circuit Emulator

The ICEPIC low cost, in-circuit emulator is a solution for the Microchip Technology PIC16C5X, PIC16C6X, PIC16C7X and PIC16CXXX families of 8-bit One-Time-Programmable (OTP) microcontrollers. The modular system can support different subsets of PIC16C5X or PIC16CXXX products through the use of interchangeable personality modules, or daughter boards. The emulator is capable of emulating without target application circuitry being present.

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## 11.8 MPLAB ICD In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD, is a powerful, low cost, run-time development tool. This tool is based on the FLASH PIC MCUs and can be used to develop for this and other PIC microcontrollers. The MPLAB ICD utilizes the in-circuit debugging capability built into the FLASH devices. This feature, along with Microchip's In-Circuit Serial Programming™ protocol, offers cost-effective in-circuit FLASH debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by watching variables, single-stepping and setting break points. Running at full speed enables testing hardware in real-time.

## 11.9 PRO MATE II Universal Device Programmer

The PRO MATE II universal device programmer is a full-featured programmer, capable of operating in Stand-alone mode, as well as PC-hosted mode. The PRO MATE II device programmer is CE compliant.

The PRO MATE II device programmer has programmable $V_{DD}$ and $V_{PP}$ supplies, which allow it to verify programmed memory at $V_{DD}$ min and $V_{DD}$ max for maximum reliability. It has an LCD display for instructions and error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In Stand-alone mode, the PRO MATE II device programmer can read, verify, or program PIC devices. It can also set code protection in this mode.

## 11.10 PICSTART Plus Entry Level Development Programmer

The PICSTART Plus development programmer is an easy-to-use, low cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient.

The PICSTART Plus development programmer supports all PIC devices with up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus development programmer is CE compliant.

## 11.11 PICDEM 1 Low Cost PIC MCU Demonstration Board

The PICDEM 1 demonstration board is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The user can program the sample microcontrollers provided with the PICDEM 1 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The user can also connect the PICDEM 1 demonstration board to the MPLAB ICE in-circuit emulator and download the firmware to the emulator for testing. A prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push button switches and eight LEDs connected to PORTB.

## 11.12 PICDEM 2 Low Cost PIC16CXX Demonstration Board

The PICDEM 2 demonstration board is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM 2 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The MPLAB ICE in-circuit emulator may also be used with the PICDEM 2 demonstration board to test firmware. A prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push button switches, a potentiometer for simulated analog input, a serial EEPROM to demonstrate usage of the $I^2C$™ bus and separate headers for connection to an LCD module and a keypad.



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## 11.13 PICDEM 3 Low Cost PIC16CXXX Demonstration Board

The PICDEM 3 demonstration board is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with an LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM 3 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer with an adapter socket, and easily test firmware. The MPLAB ICE in-circuit emulator may also be used with the PICDEM 3 demonstration board to test firmware. A prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM 3 demonstration board is a LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM 3 demonstration board provides an additional RS-232 interface and Windows software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals.

## 11.14 PICDEM 17 Demonstration Board

The PICDEM 17 demonstration board is an evaluation board that demonstrates the capabilities of several Microchip microcontrollers, including PIC17C752, PIC17C756A, PIC17C762 and PIC17C766. All necessary hardware is included to run basic demo programs, which are supplied on a 3.5-inch disk. A programmed sample is included and the user may erase it and program it with the other sample programs using the PRO MATE II device programmer, or the PICSTART Plus development programmer, and easily debug and test the sample code. In addition, the PICDEM 17 demonstration board supports downloading of programs to and executing out of external FLASH memory on board. The PICDEM 17 demonstration board is also usable with the MPLAB ICE in-circuit emulator, or the PICMASTER emulator and all of the sample programs can be run and modified using either emulator. Additionally, a generous prototype area is available for user hardware.

## 11.15 KEELOQ Evaluation and Programming Tools

KEELOQ evaluation and programming tools support Microchip's HCS Secure Data Products. The HCS evaluation kit includes a LCD display to show changing codes, a decoder to decode transmissions and a programming interface to program test transmitters.

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**TABLE 11-1: DEVELOPMENT TOOLS FROM MICROCHIP**

| | | PIC12CXXX | PIC14000 | PIC16C5X | PIC16C6X | PIC16CXXX | PIC16F62X | PIC16C7X | PIC16C7XX | PIC16C8X | PIC16F8XX | PIC16C9XX | PIC17C4X | PIC17C7XX | PIC18CXX2 | PIC18FXXX | 24CXX/ 25CXX/ 93CXX | HCSXXX | MCRFXXX | MCP2510 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Software Tools | MPLAB® Integrated Development Environment | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |
| | MPLAB® C17 C Compiler | | | ✓ | | | | | | | | | ✓ | ✓ | | | | | | |
| | MPLAB® C18 C Compiler | | | ✓ | | | | | | | | | | | ✓ | ✓ | | | | |
| | MPASM™ Assembler/ MPLINK™ Object Linker | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | |
| Emulators | MPLAB® ICE In-Circuit Emulator | ✓ | ✓ | ✓ | ✓ | ✓ | ✓** | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |
| | ICEPIC™ In-Circuit Emulator | ✓ | | ✓ | ✓ | ✓ | | ✓ | ✓ | ✓ | | ✓ | | | | | | | | |
| Debugger | MPLAB® ICD In-Circuit Debugger | | | | ✓* | | | ✓* | | | ✓ | | | | | ✓ | | | | |
| Programmers | PICSTART® Plus Entry Level Development Programmer | ✓ | ✓ | ✓ | ✓ | ✓ | ✓** | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | | | |
| | PRO MATE® II Universal Device Programmer | ✓ | ✓ | ✓ | ✓ | ✓ | ✓** | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | | ✓ | | |
| Demo Boards and Eval Kits | PICDEM™ 1 Demonstration Board | | | ✓ | | ✓ | | ✓† | | ✓ | | | ✓ | | | | | | | |
| | PICDEM™ 2 Demonstration Board | | | | ✓† | | | ✓† | | | | | | | ✓ | ✓ | | | | |
| | PICDEM™ 3 Demonstration Board | | | | | | | | | | | ✓ | | | | | | | | |
| | PICDEM™ 14A Demonstration Board | | ✓ | | | | | | | | | | | | | | | | | |
| | PICDEM™ 17 Demonstration Board | | | | | | | | | | | | | ✓ | | | | | | |
| | KEELOQ® Evaluation Kit | | | | | | | | | | | | | | | | ✓ | | | |
| | KEELOQ® Transponder Kit | | | | | | | | | | | | | | | | ✓ | | | |
| | microID™ Programmer's Kit | | | | | | | | | | | | | | | | | ✓ | | |
| | 125 kHz microID™ Developer's Kit | | | | | | | | | | | | | | | | | | ✓ | |
| | 125 kHz Anticollision microID™ Developer's Kit | | | | | | | | | | | | | | | | | | ✓ | |
| | 13.56 MHz Anticollision microID™ Developer's Kit | | | | | | | | | | | | | | | | | | ✓ | |
| | MCP2510 CAN Developer's Kit | | | | | | | | | | | | | | | | | | | ✓ |

* Contact the Microchip Technology Inc. web site at www.microchip.com for information on how to use the MPLAB® ICD In-Circuit Debugger (DV164001) with PIC16C62, 63, 64, 65, 72, 73, 74, 76, 77.

** Contact Microchip Technology Inc. for availability date.

† Development tool is available on select devices.



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**NOTES:**

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## 12.0 ELECTRICAL CHARACTERISTICS - PIC16C54A

**Absolute Maximum Ratings(†)**

Ambient Temperature under bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... 0V to +7.5V

Voltage on $\overline{MCLR}$ with respect to $V_{SS}$(1) ..... 0V to +14V

Voltage on all other pins with respect to $V_{SS}$ ..... –0.6V to ($V_{DD}$ + 0.6V)

Total power dissipation(2) ..... 800 mW

Max. current out of $V_{SS}$ pin ..... 150 mA

Max. current into $V_{DD}$ pin ..... 100 mA

Max. current into an input pin (T0CKI only) ..... ±500 µA

Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{DD}$) ..... ±20 mA

Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{DD}$) ..... ±20 mA

Max. output current sunk by any I/O pin ..... 25 mA

Max. output current sourced by any I/O pin ..... 20 mA

Max. output current sourced by a single I/O port (PORTA, B or C) ..... 40 mA

Max. output current sunk by a single I/O port (PORTA, B or C) ..... 50 mA

**Note 1:** Voltage spikes below $V_{SS}$ at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50 to 100 Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to $V_{SS}$.

**2:** Power Dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.



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## 12.1 DC Characteristics: PIC16C54/55/56/57-RC, XT, 10, HS, LP (Commercial)

| PIC16C54/55/56/57-RC, XT, 10, HS, LP (Commercial) | | | Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic/Device** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D001 | VDD | **Supply Voltage** | | | | | |
| | | PIC16C5X-RC | 3.0 | — | 6.25 | V | |
| | | PIC16C5X-XT | 3.0 | — | 6.25 | V | |
| | | PIC16C5X-10 | 4.5 | — | 5.5 | V | |
| | | PIC16C5X-HS | 4.5 | — | 5.5 | V | |
| | | PIC16C5X-LP | 2.5 | — | 6.25 | V | |
| D002 | VDR | **RAM Data Retention Voltage(1)** | | 1.5* | — | V | Device in SLEEP Mode |
| D003 | VPOR | **VDD Start Voltage** to ensure Power-on Reset | | VSS | — | V | See Section 5.1 for details on Power-on Reset |
| D004 | SVDD | **VDD Rise Rate** to ensure Power-on Reset | 0.05* | — | — | V/ms | See Section 5.1 for details on Power-on Reset |
| D010 | IDD | **Supply Current(2)** | | | | | |
| | | PIC16C5X-RC(3) | — | 1.8 | 3.3 | mA | FOSC = 4 MHz, VDD = 5.5V |
| | | PIC16C5X-XT | — | 1.8 | 3.3 | mA | FOSC = 4 MHz, VDD = 5.5V |
| | | PIC16C5X-10 | — | 4.8 | 10 | mA | FOSC = 10 MHz, VDD = 5.5V |
| | | PIC16C5X-HS | — | 4.8 | 10 | mA | FOSC = 10 MHz, VDD = 5.5V |
| | | PIC16C5X-HS | — | 9.0 | 20 | mA | FOSC = 20 MHz, VDD = 5.5V |
| | | PIC16C5X-LP | — | 15 | 32 | µA | FOSC = 32 kHz, VDD = 3.0V, WDT disabled |
| D020 | IPD | **Power-down Current(2)** | — | 4.0 | 12 | µA | VDD = 3.0V, WDT enabled |
| | | | — | 0.6 | 9 | µA | VDD = 3.0V, WDT disabled |

* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

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## 12.2 DC Characteristics: PIC16C54/55/56/57-RCI, XTI, 10I, HSI, LPI (Industrial)

| PIC16C54/55/56/57-RCI, XTI, 10I, HSI, LPI (Industrial) | | | Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +85°C for industrial | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic/Device** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D001 | VDD | **Supply Voltage** | | | | | |
| | | PIC16C5X-RCI | 3.0 | — | 6.25 | V | |
| | | PIC16C5X-XTI | 3.0 | — | 6.25 | V | |
| | | PIC16C5X-10I | 4.5 | — | 5.5 | V | |
| | | PIC16C5X-HSI | 4.5 | — | 5.5 | V | |
| | | PIC16C5X-LPI | 2.5 | — | 6.25 | V | |
| D002 | VDR | **RAM Data Retention Voltage(1)** | — | 1.5* | — | V | Device in SLEEP mode |
| D003 | VPOR | **VDD Start Voltage** to ensure Power-on Reset | — | VSS | — | V | See Section 5.1 for details on Power-on Reset |
| D004 | SVDD | **VDD Rise Rate** to ensure Power-on Reset | 0.05* | — | — | V/ms | See Section 5.1 for details on Power-on Reset |
| D010 | IDD | **Supply Current(2)** | | | | | |
| | | PIC16C5X-RCI(3) | — | 1.8 | 3.3 | mA | FOSC = 4 MHz, VDD = 5.5V |
| | | PIC16C5X-XTI | — | 1.8 | 3.3 | mA | FOSC = 4 MHz, VDD = 5.5V |
| | | PIC16C5X-10I | — | 4.8 | 10 | mA | FOSC = 10 MHz, VDD = 5.5V |
| | | PIC16C5X-HSI | — | 4.8 | 10 | mA | FOSC = 10 MHz, VDD = 5.5V |
| | | PIC16C5X-HSI | — | 9.0 | 20 | mA | FOSC = 20 MHz, VDD = 5.5V |
| | | PIC16C5X-LPI | — | 15 | 40 | µA | FOSC = 32 kHz, VDD = 3.0V, WDT disabled |
| D020 | IPD | **Power-down Current(2)** | — | 4.0 | 14 | µA | VDD = 3.0V, WDT enabled |
| | | | — | 0.6 | 12 | µA | VDD = 3.0V, WDT disabled |

* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.



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## 12.3 DC Characteristics: PIC16C54/55/56/57-RCE, XTE, 10E, HSE, LPE (Extended)

| PIC16C54/55/56/57-RCE, XTE, 10E, HSE, LPE (Extended) | | | Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C for extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic/Device** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D001 | VDD | **Supply Voltage** | | | | | |
| | | PIC16C5X-RCE | 3.25 | — | 6.0 | V | |
| | | PIC16C5X-XTE | 3.25 | — | 6.0 | V | |
| | | PIC16C5X-10E | 4.5 | — | 5.5 | V | |
| | | PIC16C5X-HSE | 4.5 | — | 5.5 | V | |
| | | PIC16C5X-LPE | 2.5 | — | 6.0 | V | |
| D002 | VDR | **RAM Data Retention Voltage(1)** | — | 1.5* | — | V | Device in SLEEP mode |
| D003 | VPOR | **VDD Start Voltage** to ensure Power-on Reset | — | VSS | — | V | See Section 5.1 for details on Power-on Reset |
| D004 | SVDD | **VDD Rise Rate** to ensure Power-on Reset | 0.05* | — | — | V/ms | See Section 5.1 for details on Power-on Reset |
| D010 | IDD | **Supply Current(2)** | | | | | |
| | | PIC16C5X-RCE(3) | — | 1.8 | 3.3 | mA | FOSC = 4 MHz, VDD = 5.5V |
| | | PIC16C5X-XTE | — | 1.8 | 3.3 | mA | FOSC = 4 MHz, VDD = 5.5V |
| | | PIC16C5X-10E | — | 4.8 | 10 | mA | FOSC = 10 MHz, VDD = 5.5V |
| | | PIC16C5X-HSE | — | 4.8 | 10 | mA | FOSC = 10 MHz, VDD = 5.5V |
| | | PIC16C5X-HSE | — | 9.0 | 20 | mA | FOSC = 16 MHz, VDD = 5.5V |
| | | PIC16C5X-LPE | — | 19 | 55 | µA | FOSC = 32 kHz, VDD = 3.25V, WDT disabled |
| D020 | IPD | **Power-down Current(2)** | — | 5.0 | 22 | µA | VDD = 3.25V, WDT enabled |
| | | | — | 0.8 | 18 | µA | VDD = 3.25V, WDT disabled |

* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

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## 12.4 DC Characteristics: PIC16C54/55/56/57-RC, XT, 10, HS, LP (Commercial) PIC16C54/55/56/57-RCI, XTI, 10I, HSI, LPI (Industrial)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic/Device** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D030 | VIL | **Input Low Voltage** | | | | | |
| | | I/O ports | VSS | — | 0.2 VDD | V | Pin at hi-impedance |
| | | MCLR (Schmitt Trigger) | VSS | — | 0.15 VDD | V | |
| | | T0CKI (Schmitt Trigger) | VSS | — | 0.15 VDD | V | |
| | | OSC1 (Schmitt Trigger) | VSS | — | 0.15 VDD | V | PIC16C5X-RC only(3) |
| | | OSC1 (Schmitt Trigger) | VSS | — | 0.3 VDD | V | PIC16C5X-XT, 10, HS, LP |
| D040 | VIH | **Input High Voltage** | | | | | |
| | | I/O ports | 0.45 VDD | — | VDD | V | For all VDD(4) |
| | | I/O ports | 2.0 | — | VDD | V | 4.0V < VDD ≤ 5.5V(4) |
| | | I/O ports | 0.36 VDD | — | VDD | V | VDD > 5.5V |
| | | MCLR (Schmitt Trigger) | 0.85 VDD | — | VDD | V | |
| | | T0CKI (Schmitt Trigger) | 0.85 VDD | — | VDD | V | |
| | | OSC1 (Schmitt Trigger) | 0.85 VDD | — | VDD | V | PIC16C5X-RC only(3) |
| | | OSC1 (Schmitt Trigger) | 0.7 VDD | — | VDD | V | PIC16C5X-XT, 10, HS, LP |
| D050 | VHYS | **Hysteresis of Schmitt Trigger inputs** | 0.15 VDD* | — | — | V | |
| D060 | IIL | **Input Leakage Current(1,2)** | | | | | **For VDD ≤ 5.5V:** |
| | | I/O ports | –1 | 0.5 | +1 | µA | VSS ≤ VPIN ≤ VDD, pin at hi-impedance |
| | | MCLR | –5 | — | — | µA | VPIN = VSS + 0.25V |
| | | MCLR | — | 0.5 | +5 | µA | VPIN = VDD |
| | | T0CKI | –3 | 0.5 | +3 | µA | VSS ≤ VPIN ≤ VDD |
| | | OSC1 | –3 | 0.5 | +3 | µA | VSS ≤ VPIN ≤ VDD, PIC16C5X-XT, 10, HS, LP |
| D080 | VOL | **Output Low Voltage** | | | | | |
| | | I/O ports | — | — | 0.6 | V | IOL = 8.7 mA, VDD = 4.5V |
| | | OSC2/CLKOUT | — | — | 0.6 | V | IOL = 1.6 mA, VDD = 4.5V, PIC16C5X-RC |
| D090 | VOH | **Output High Voltage(2)** | | | | | |
| | | I/O ports | VDD – 0.7 | — | — | V | IOH = –5.4 mA, VDD = 4.5V |
| | | OSC2/CLKOUT | VDD – 0.7 | — | — | V | IOH = –1.0 mA, VDD = 4.5V, PIC16C5X-RC |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

**2:** Negative current is defined as coming out of the pin.

**3:** For PIC16C5X-RC devices, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

**4:** The user may use the better of the two specifications.



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## 12.5 DC Characteristics: PIC16C54/55/56/57-RCE, XTE, 10E, HSE, LPE (Extended)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature –40°C ≤ TA ≤ +125°C for extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D030 | VIL | **Input Low Voltage** | | | | | |
| | | I/O ports | Vss | — | 0.15 VDD | V | Pin at hi-impedance |
| | | MCLR (Schmitt Trigger) | Vss | — | 0.15 VDD | V | |
| | | T0CKI (Schmitt Trigger) | Vss | — | 0.15 VDD | V | |
| | | OSC1 (Schmitt Trigger) | Vss | — | 0.15 VDD | V | PIC16C5X-RC only(3) |
| | | OSC1 (Schmitt Trigger) | Vss | — | 0.3 VDD | V | PIC16C5X-XT, 10, HS, LP |
| D040 | VIH | **Input High Voltage** | | | | | |
| | | I/O ports | 0.45 VDD | — | VDD | V | For all VDD(4) |
| | | I/O ports | 2.0 | — | VDD | V | 4.0V < VDD ≤ 5.5V(4) |
| | | I/O ports | 0.36 VDD | — | VDD | V | VDD > 5.5 V |
| | | MCLR (Schmitt Trigger) | 0.85 VDD | — | VDD | V | |
| | | T0CKI (Schmitt Trigger) | 0.85 VDD | — | VDD | V | |
| | | OSC1 (Schmitt Trigger) | 0.85 VDD | — | VDD | V | PIC16C5X-RC only(3) |
| | | OSC1 (Schmitt Trigger) | 0.7 VDD | — | VDD | V | PIC16C5X-XT, 10, HS, LP |
| D050 | VHYS | **Hysteresis of Schmitt Trigger inputs** | 0.15 VDD* | — | — | V | |
| D060 | IIL | **Input Leakage Current (1,2)** | | | | | **For VDD ≤ 5.5 V:** |
| | | I/O ports | –1 | 0.5 | +1 | µA | VSS ≤ VPIN ≤ VDD, pin at hi-impedance |
| | | MCLR | –5 | — | — | µA | VPIN = VSS + 0.25V |
| | | MCLR | — | 0.5 | +5 | µA | VPIN = VDD |
| | | T0CKI | –3 | 0.5 | +3 | µA | VSS ≤ VPIN ≤ VDD |
| | | OSC1 | –3 | 0.5 | +3 | µA | VSS ≤ VPIN ≤ VDD, PIC16C5X-XT, 10, HS, LP |
| D080 | VOL | **Output Low Voltage** | | | | | |
| | | I/O ports | — | — | 0.6 | V | IOL = 8.7 mA, VDD = 4.5V |
| | | OSC2/CLKOUT | — | — | 0.6 | V | IOL = 1.6 mA, VDD = 4.5V, PIC16C5X-RC |
| D090 | VOH | **Output High Voltage(2)** | | | | | |
| | | I/O ports | VDD – 0.7 | — | — | V | IOH = –5.4 mA, VDD = 4.5V |
| | | OSC2/CLKOUT | VDD – 0.7 | — | — | V | IOH = –1.0 mA, VDD = 4.5V, PIC16C5X-RC |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** The leakage current on the $\overline{\text{MCLR}}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

**2:** Negative current is defined as coming out of the pin.

**3:** For PIC16C5X-RC devices, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

**4:** The user may use the better of the two specifications.

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## 12.6 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

| | |
|---|---|
| T | |
| F Frequency | T Time |

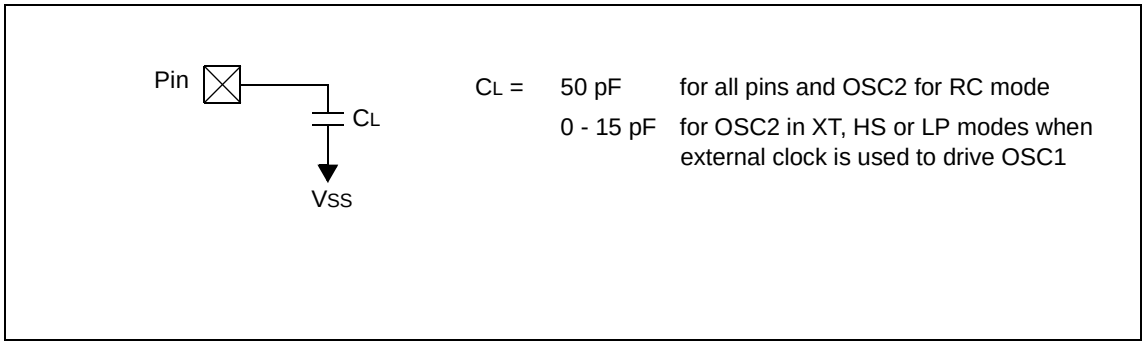
Lowercase letters (pp) and their meanings:

| | |
|---|---|
| pp | |
| 2 to | mc $\overline{\text{MCLR}}$ |
| ck CLKOUT | osc oscillator |
| cy cycle time | os OSC1 |
| drt device reset timer | t0 T0CKI |
| io I/O port | wdt watchdog timer |

Uppercase letters and their meanings:

| | |
|---|---|
| S | |
| F Fall | P Period |
| H High | R Rise |
| I Invalid (Hi-impedance) | V Valid |
| L Low | Z Hi-impedance |

**FIGURE 12-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16C54/55/56/57**



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## 12.7 Timing Diagrams and Specifications

**FIGURE 12-2: EXTERNAL CLOCK TIMING - PIC16C54/55/56/57**

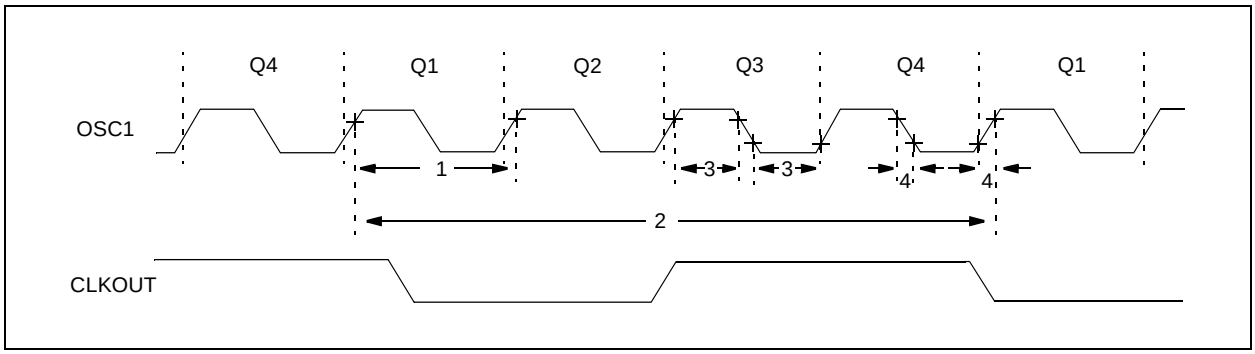


**TABLE 12-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54/55/56/57**

| AC Characteristics | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–40°C ≤ TA ≤ +125°C for extended | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| 1A | FOSC | External CLKIN Frequency(1) | DC | — | 4.0 | MHz | XT OSC mode |
| | | | DC | — | 10 | MHz | 10 MHz mode |
| | | | DC | — | 20 | MHz | HS OSC mode (Comm/Ind) |
| | | | DC | — | 16 | MHz | HS OSC mode (Ext) |
| | | | DC | — | 40 | kHz | LP OSC mode |
| | | Oscillator Frequency(1) | DC | — | 4.0 | MHz | RC OSC mode |
| | | | 0.1 | — | 4.0 | MHz | XT OSC mode |
| | | | 4.0 | — | 10 | MHz | 10 MHz mode |
| | | | 4.0 | — | 20 | MHz | HS OSC mode (Comm/Ind) |
| | | | 4.0 | — | 16 | MHz | HS OSC mode (Ext) |
| | | | DC | — | 40 | kHz | LP OSC mode |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

**2:** Instruction cycle period (TCY) equals four times the input oscillator time base period.

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**TABLE 12-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54/55/56/57**

| AC Characteristics | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–40°C ≤ TA ≤ +125°C for extended | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| 1 | TOSC | External CLKIN Period(1) | 250 | — | — | ns | XT OSC mode |
| | | | 100 | — | — | ns | 10 MHz mode |
| | | | 50 | — | — | ns | HS OSC mode (Comm/Ind) |
| | | | 62.5 | — | — | ns | HS OSC mode (Ext) |
| | | | 25 | — | — | µs | LP OSC mode |
| | | Oscillator Period(1) | 250 | — | — | ns | RC OSC mode |
| | | | 250 | — | 10,000 | ns | XT OSC mode |
| | | | 100 | — | 250 | ns | 10 MHz mode |
| | | | 50 | — | 250 | ns | HS OSC mode (Comm/Ind) |
| | | | 62.5 | — | 250 | ns | HS OSC mode (Ext) |
| | | | 25 | — | — | µs | LP OSC mode |
| 2 | Tcy | Instruction Cycle Time(2) | — | 4/FOSC | — | — | |
| 3 | TosL, TosH | Clock in (OSC1) Low or High Time | 85* | — | — | ns | XT oscillator |
| | | | 20* | — | — | ns | HS oscillator |
| | | | 2.0* | — | — | µs | LP oscillator |
| 4 | TosR, TosF | Clock in (OSC1) Rise or Fall Time | — | — | 25* | ns | XT oscillator |
| | | | — | — | 25* | ns | HS oscillator |
| | | | — | — | 50* | ns | LP oscillator |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

**2:** Instruction cycle period (TCY) equals four times the input oscillator time base period.



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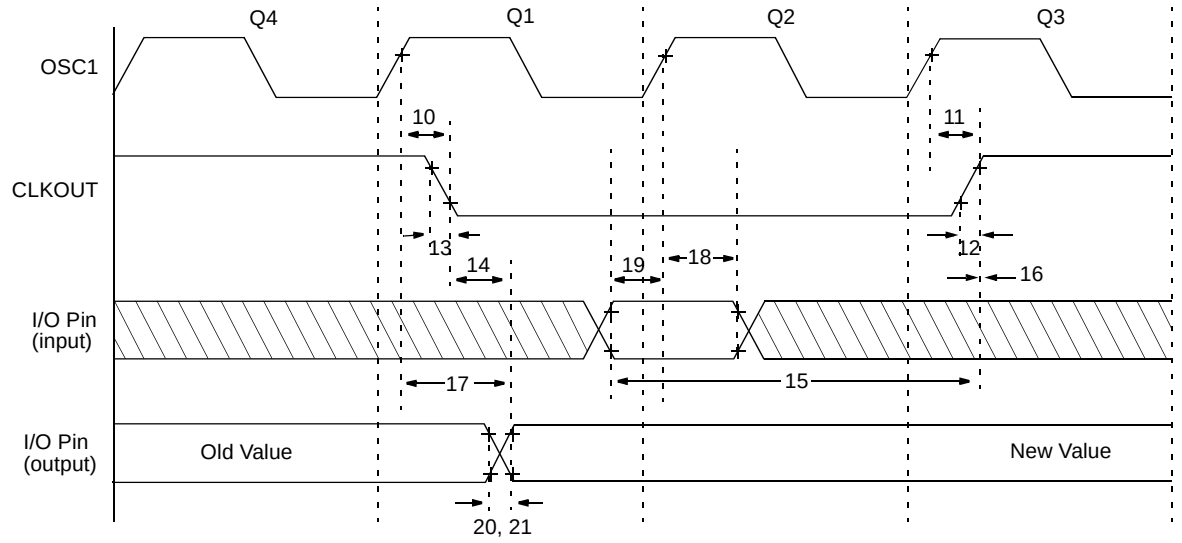
**FIGURE 12-3: CLKOUT AND I/O TIMING - PIC16C54/55/56/57**




**Note:** Please refer to Figure 12-1 for load conditions.

**TABLE 12-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C54/55/56/57**

| **AC Characteristics** | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–40°C ≤ TA ≤ +125°C for extended | | | | | |
|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** |
| 10 | TosH2ckL | OSC1↑ to CLKOUT↓(1) | — | 15 | 30** | ns |
| 11 | TosH2ckH | OSC1↑ to CLKOUT↑(1) | — | 15 | 30** | ns |
| 12 | TckR | CLKOUT rise time(1) | — | 5.0 | 15** | ns |
| 13 | TckF | CLKOUT fall time(1) | — | 5.0 | 15** | ns |
| 14 | TckL2ioV | CLKOUT↓ to Port out valid(1) | — | — | 40** | ns |
| 15 | TioV2ckH | Port in valid before CLKOUT↑(1) | 0.25 TCY+30* | — | — | ns |
| 16 | TckH2ioI | Port in hold after CLKOUT↑(1) | 0* | — | — | ns |
| 17 | TosH2ioV | OSC1↑ (Q1 cycle) to Port out valid(2) | — | — | 100* | ns |
| 18 | TosH2ioI | OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time) | TBD | — | — | ns |
| 19 | TioV2osH | Port input valid to OSC1↑ (I/O in setup time) | TBD | — | — | ns |
| 20 | TioR | Port output rise time(2) | — | 10 | 25** | ns |
| 21 | TioF | Port output fall time(2) | — | 10 | 25** | ns |

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Measurements are taken in RC Mode where CLKOUT output is 4 x Tosc.

**2:** Please refer to Figure 12-1 for load conditions.

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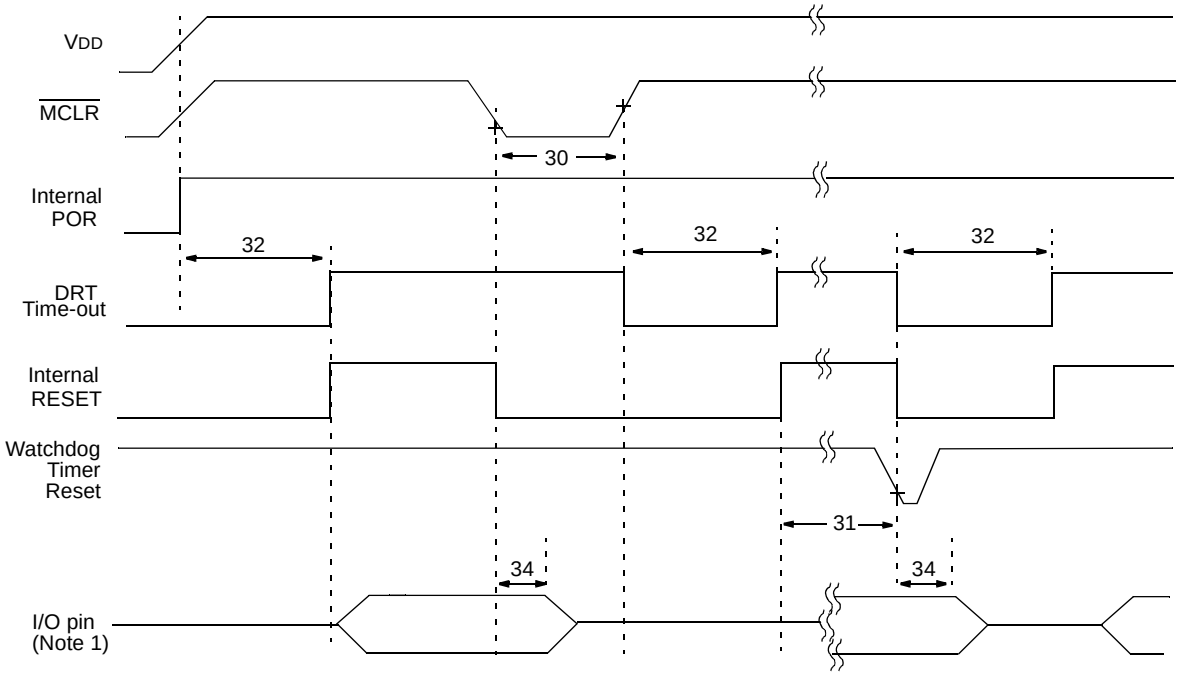
**FIGURE 12-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C54/55/56/57**




**Note 1:** Please refer to Figure 12-1 for load conditions.

**TABLE 12-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C54/55/56/57**

| **AC Characteristics** | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–40°C ≤ TA ≤ +125°C for extended | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| 30 | TmcL | $\overline{\text{MCLR}}$ Pulse Width (low) | 100* | — | — | ns | VDD = 5.0V |
| 31 | Twdt | Watchdog Timer Time-out Period (No Prescaler) | 9.0* | 18* | 30* | ms | VDD = 5.0V (Comm) |
| 32 | TDRT | Device Reset Timer Period | 9.0* | 18* | 30* | ms | VDD = 5.0V (Comm) |
| 34 | Tioz | I/O Hi-impedance from $\overline{\text{MCLR}}$ Low | — | — | 100* | ns | |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.



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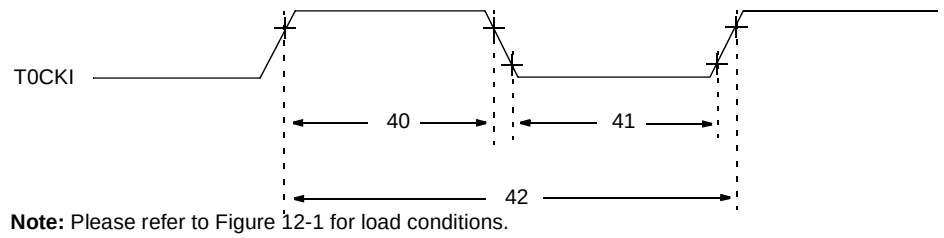
**FIGURE 12-5: TIMER0 CLOCK TIMINGS - PIC16C54/55/56/57**




**Note:** Please refer to Figure 12-1 for load conditions.

**TABLE 12-4: TIMER0 CLOCK REQUIREMENTS - PIC16C54/55/56/57**

| **AC Characteristics** | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–40°C ≤ TA ≤ +125°C for extended | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| 40 | Tt0H | T0CKI High Pulse Width<br>- No Prescaler | 0.5 TCY + 20* | — | — | ns | |
| | | - With Prescaler | 10* | — | — | ns | |
| 41 | Tt0L | T0CKI Low Pulse Width<br>- No Prescaler | 0.5 TCY + 20* | — | — | ns | |
| | | - With Prescaler | 10* | — | — | ns | |
| 42 | Tt0P | T0CKI Period | 20 or $\frac{T_{CY} + 40}{N}$* | — | — | ns | Whichever is greater.<br>N = Prescale Value (1, 2, 4,..., 256) |

* These parameters are characterized but not tested.

† Data in the Typical (“Typ”) column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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## 13.0 ELECTRICAL CHARACTERISTICS - PIC16CR54A

### Absolute Maximum Ratings(†)

Ambient Temperature under bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... 0 to +7.5V

Voltage on $\overline{MCLR}$ with respect to $V_{SS}$(1) ..... 0 to +14V

Voltage on all other pins with respect to $V_{SS}$ ..... –0.6V to ($V_{DD}$ + 0.6V)

Total power dissipation(2) ..... 800 mW

Max. current out of $V_{SS}$ pin ..... 150 mA

Max. current into $V_{DD}$ pin ..... 50 mA

Max. current into an input pin (T0CKI only) ..... ±500 µA

Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{DD}$) ..... ±20 mA

Output clamp current, $I_{OK}$ ($V_0$ < 0 or $V_0$ > $V_{DD}$) ..... ±20 mA

Max. output current sunk by any I/O pin ..... 25 mA

Max. output current sourced by any I/O pin ..... 20 mA

Max. output current sourced by a single I/O port (PORTA or B) ..... 40 mA

Max. output current sunk by a single I/O port (PORTA or B) ..... 50 mA

**Note 1:** Voltage spikes below Vss at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA may cause latch-up. Thus, a series resistor of 50 to 100 Ω should be used when applying a low level to the $\overline{MCLR}$ pin rather than pulling this pin directly to Vss.

**2:** Power Dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.



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## 13.1 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

| **PIC16LCR54A-04**<br>**PIC16LCR54A-04I**<br>(Commercial, Industrial) | | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial | | | | |
|---|---|---|---|---|---|---|---|
| **PIC16CR54A-04, 10, 20**<br>**PIC16CR54A-04I, 10I, 20I**<br>(Commercial, Industrial) | | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial | | | | |
| **Param No.** | **Symbol** | **Characteristic/Device** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| | VDD | **Supply Voltage** | | | | | |
| D001 | | PIC16LCR54A | 2.0 | — | 6.25 | V | |
| D001<br>D001A | | PIC16CR54A | 2.5<br>4.5 | —<br>— | 6.25<br>5.5 | V<br>V | RC and XT modes<br>HS mode |
| D002 | VDR | **RAM Data Retention Voltage(1)** | — | 1.5* | — | V | Device in SLEEP mode |
| D003 | VPOR | **VDD Start Voltage** to ensure Power-on Reset | — | VSS | — | V | See Section 5.1 for details on Power-on Reset |
| D004 | SVDD | **VDD Rise Rate** to ensure Power-on Reset | 0.05* | — | — | V/ms | See Section 5.1 for details on Power-on Reset |
| | IDD | **Supply Current(2)** | | | | | |
| D005 | | PICLCR54A | —<br>— | 10<br>— | 20<br>70 | µA<br>µA | Fosc = 32 kHz, VDD = 2.0V<br>Fosc = 32 kHz, VDD = 6.0V |
| D005A | | PIC16CR54A | | | | | **RC(3) and XT modes:** |
| | | | —<br>—<br>— | 2.0<br>0.8<br>90 | 3.6<br>1.8<br>350 | mA<br>mA<br>µA | FOSC = 4.0 MHz, VDD = 6.0V<br>FOSC = 4.0 MHz, VDD = 3.0V<br>FOSC = 200 kHz, VDD = 2.5V |
| | | | | | | | **HS mode:** |
| | | | —<br>— | 4.8<br>9.0 | 10<br>20 | mA<br>mA | FOSC = 10 MHz, VDD = 5.5V<br>FOSC = 20 MHz, VDD = 5.5V |

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

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## 13.1 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **PIC16LCR54A-04**<br>**PIC16LCR54A-04I**<br>(Commercial, Industrial) | | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial | | | | |
| **PIC16CR54A-04, 10, 20**<br>**PIC16CR54A-04I, 10I, 20I**<br>(Commercial, Industrial) | | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial | | | | |
| **Param No.** | **Symbol** | **Characteristic/Device** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| | IPD | **Power-down Current(2)** | | | | | |
| D006 | | PIC16LCR54A-Commercial | — | 1.0 | 6.0 | µA | VDD = 2.5V, WDT disabled |
| | | | — | 2.0 | 8.0* | µA | VDD = 4.0V, WDT disabled |
| | | | — | 3.0 | 15 | µA | VDD = 6.0V, WDT disabled |
| | | | — | 5.0 | 25 | µA | VDD = 6.0V, WDT enabled |
| D006A | | PIC16CR54A-Commercial | — | 1.0 | 6.0 | µA | VDD = 2.5V, WDT disabled |
| | | | — | 2.0 | 8.0* | µA | VDD = 4.0V, WDT disabled |
| | | | — | 3.0 | 15 | µA | VDD = 6.0V, WDT disabled |
| | | | — | 5.0 | 25 | µA | VDD = 6.0V, WDT enabled |
| D007 | | PIC16LCR54A-Industrial | — | 1.0 | 8.0 | µA | VDD = 2.5V, WDT disabled |
| | | | — | 2.0 | 10* | µA | VDD = 4.0V, WDT disabled |
| | | | — | 3.0 | 20* | µA | VDD = 4.0V, WDT enabled |
| | | | — | 3.0 | 18 | µA | VDD = 6.0V, WDT disabled |
| | | | — | 5.0 | 45 | µA | VDD = 6.0V, WDT enabled |
| D007A | | PIC16CR54A-Industrial | — | 1.0 | 8.0 | µA | VDD = 2.5V, WDT disabled |
| | | | — | 2.0 | 10* | µA | VDD = 4.0V, WDT disabled |
| | | | — | 3.0 | 20* | µA | VDD = 4.0V, WDT enabled |
| | | | — | 3.0 | 18 | µA | VDD = 6.0V, WDT disabled |
| | | | — | 5.0 | 45 | µA | VDD = 6.0V, WDT enabled |

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.



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## 13.2 DC Characteristics: PIC16CR54A-04E, 10E, 20E (Extended)

| PIC16CR54A-04E, 10E, 20E (Extended) | | | Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C for extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D001 | VDD | **Supply Voltage**<br>RC, XT and LP modes<br>HS mode | <br>3.25<br>4.5 | <br>—<br>— | <br>6.0<br>5.5 | <br>V<br>V | |
| D002 | VDR | **RAM Data Retention Voltage**(1) | — | 1.5* | — | V | Device in SLEEP mode |
| D003 | VPOR | **VDD Start Voltage** to ensure Power-on Reset | — | VSS | — | V | See Section 5.1 for details on Power-on Reset |
| D004 | SVDD | **VDD Rise Rate** to ensure Power-on Reset | 0.05* | — | — | V/ms | See Section 5.1 for details on Power-on Reset |
| D010 | IDD | **Supply Current**(2)<br>RC(3) and XT modes<br>HS mode<br>HS mode | <br>—<br>—<br>— | <br>1.8<br>4.8<br>9.0 | <br>3.3<br>10<br>20 | <br>mA<br>mA<br>mA | <br>FOSC = 4.0 MHz, VDD = 5.5V<br>FOSC = 10 MHz, VDD = 5.5V<br>FOSC = 16 MHz, VDD = 5.5V |
| D020 | IPD | **Power-down Current**(2) | —<br>— | 5.0<br>0.8 | 22<br>18 | µA<br>µA | VDD = 3.25V, WDT enabled<br>VDD = 3.25V, WDT disabled |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.The power-down current in SLEEP mode does not depend on the oscillator type.

**3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

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## 13.3 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D030 | VIL | **Input Low Voltage** | | | | | |
| | | I/O ports | VSS | — | 0.2 VDD | V | Pin at hi-impedance |
| | | MCLR (Schmitt Trigger) | VSS | — | 0.15 VDD | V | |
| | | T0CKI (Schmitt Trigger) | VSS | — | 0.15 VDD | V | |
| | | OSC1 (Schmitt Trigger) | VSS | — | 0.15 VDD | V | RC mode only(3) |
| | | OSC1 | VSS | — | 0.15 VDD | V | XT, HS and LP modes |
| D040 | VIH | **Input High Voltage** | | | | | |
| | | I/O ports | 2.0 | — | VDD | V | VDD = 3.0V to 5.5V(4) |
| | | I/O ports | 0.6 VDD | — | VDD | V | Full VDD range(4) |
| | | MCLR (Schmitt Trigger) | 0.85 VDD | — | VDD | V | |
| | | T0CKI (Schmitt Trigger) | 0.85 VDD | — | VDD | V | |
| | | OSC1 (Schmitt Trigger) | 0.85 VDD | — | VDD | V | RC mode only(3) |
| | | OSC1 | 0.85 VDD | — | VDD | V | XT, HS and LP modes |
| D050 | VHYS | **Hysteresis of Schmitt Trigger inputs** | 0.15 VDD* | — | — | V | |
| D060 | IIL | **Input Leakage Current(1,2)** | | | | | **For VDD ≤ 5.5V:** |
| | | I/O ports | –1.0 | — | +1.0 | µA | VSS ≤ VPIN ≤ VDD, pin at hi-impedance |
| | | MCLR | –5.0 | — | — | µA | VPIN = VSS + 0.25V |
| | | MCLR | — | 0.5 | +5.0 | µA | VPIN = VDD |
| | | T0CKI | –3.0 | 0.5 | +3.0 | µA | VSS ≤ VPIN ≤ VDD |
| | | OSC1 | –3.0 | 0.5 | +3.0 | µA | VSS ≤ VPIN ≤ VDD, XT, HS and LP modes |
| D080 | VOL | **Output Low Voltage** | | | | | |
| | | I/O ports | — | — | 0.5 | V | IOL = 10 mA, VDD = 6.0V |
| | | OSC2/CLKOUT | — | — | 0.5 | V | IOL = 1.9 mA, VDD = 6.0V, RC mode only |
| D090 | VOH | **Output High Voltage(2)** | | | | | |
| | | I/O ports | VDD – 0.5 | — | — | V | IOH = –4.0 mA, VDD = 6.0V |
| | | OSC2/CLKOUT | VDD – 0.5 | — | — | V | IOH = –0.8 mA, VDD = 6.0V, RC mode only |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** The leakage current on the $\overline{\text{MCLR}}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

**2:** Negative current is defined as coming out of the pin.

**3:** For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

**4:** The user may use the better of the two specifications.



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## 13.4 DC Characteristics: PIC16CR54A-04E, 10E, 20E (Extended)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature –40°C ≤ TA ≤ +125°C for extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D030 | VIL | **Input Low Voltage** | | | | | |
| | | I/O ports | Vss | — | 0.15 VDD | V | Pin at hi-impedance |
| | | MCLR (Schmitt Trigger) | Vss | — | 0.15 VDD | V | |
| | | T0CKI (Schmitt Trigger) | Vss | — | 0.15 VDD | V | |
| | | OSC1 (Schmitt Trigger) | Vss | — | 0.15 VDD | V | RC mode only(3) |
| | | OSC1 | Vss | — | 0.3 VDD | V | XT, HS and LP modes |
| D040 | VIH | **Input High Voltage** | | | | | |
| | | I/O ports | 0.45 VDD | — | VDD | V | For all VDD(4) |
| | | I/O ports | 2.0 | — | VDD | V | 4.0V < VDD ≤ 5.5V(4) |
| | | I/O ports | 0.36 VDD | — | VDD | V | VDD > 5.5V |
| | | MCLR (Schmitt Trigger) | 0.85 VDD | — | VDD | V | |
| | | T0CKI (Schmitt Trigger) | 0.85 VDD | — | VDD | V | |
| | | OSC1 (Schmitt Trigger) | 0.85 VDD | — | VDD | V | RC mode only(3) |
| | | OSC1 | 0.7 VDD | — | VDD | V | XT, HS and LP modes |
| D050 | VHYS | **Hysteresis of Schmitt Trigger inputs** | 0.15 VDD* | — | — | V | |
| D060 | IIL | **Input Leakage Current(1,2)** | | | | | **For VDD ≤ 5.5V:** |
| | | I/O ports | –1.0 | 0.5 | +1.0 | µA | VSS ≤ VPIN ≤ VDD, pin at hi-impedance |
| | | MCLR | –5.0 | — | — | µA | VPIN = VSS + 0.25V |
| | | MCLR | — | 0.5 | +5.0 | µA | VPIN = VDD |
| | | T0CKI | –3.0 | 0.5 | +3.0 | µA | VSS ≤ VPIN ≤ VDD |
| | | OSC1 | –3.0 | 0.5 | +3.0 | µA | VSS ≤ VPIN ≤ VDD, XT, HS and LP modes |
| D080 | VOL | **Output Low Voltage** | | | | | |
| | | I/O ports | — | — | 0.6 | V | IOL = 8.7 mA, VDD = 4.5V |
| | | OSC2/CLKOUT | — | — | 0.6 | V | IOL = 1.6 mA, VDD = 4.5V, RC mode only |
| D090 | VOH | **Output High Voltage(2)** | | | | | |
| | | I/O ports | VDD – 0.7 | — | — | V | IOH = –5.4 mA, VDD = 4.5V |
| | | OSC2/CLKOUT | VDD – 0.7 | — | — | V | IOH = –1.0 mA, VDD = 4.5V, RC mode only |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

**2:** Negative current is defined as coming out of the pin.

**3:** For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

**4:** The user may use the better of the two specifications.

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## 13.5 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

| | |
|---|---|
| T | |
| F Frequency | T Time |

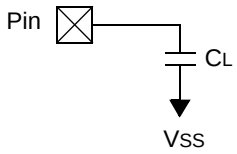
Lowercase letters (pp) and their meanings:

| | |
|---|---|
| pp | |
| 2 to | mc $\overline{\text{MCLR}}$ |
| ck CLKOUT | osc oscillator |
| cy cycle time | os OSC1 |
| drt device reset timer | t0 T0CKI |
| io I/O port | wdt watchdog timer |

Uppercase letters and their meanings:

| | |
|---|---|
| S | |
| F Fall | P Period |
| H High | R Rise |
| I Invalid (Hi-impedance) | V Valid |
| L Low | Z Hi-impedance |

**FIGURE 13-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16CR54A**




$C_L$ = 50 pF for all pins and OSC2 for RC modes

0 -15 pF for OSC2 in XT, HS or LP modes when external clock is used to drive OSC1



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## 13.6 Timing Diagrams and Specifications

**FIGURE 13-2: EXTERNAL CLOCK TIMING - PIC16CR54A**

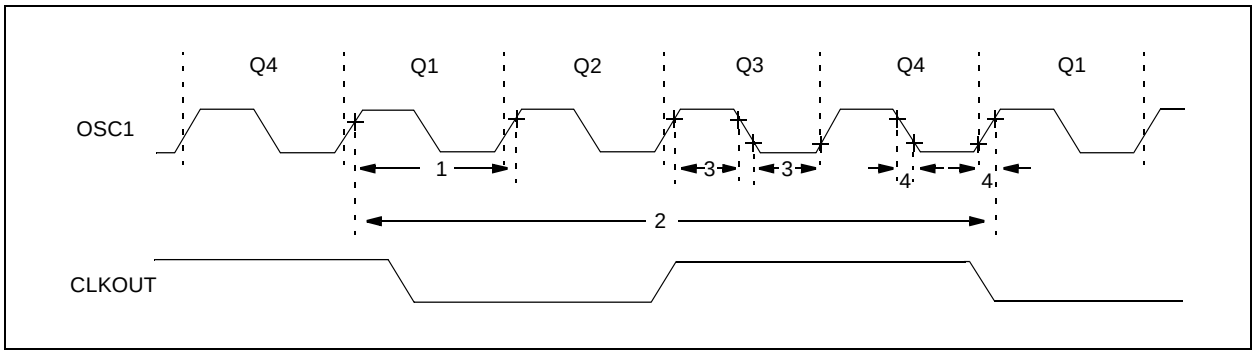


**TABLE 13-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16CR54A**

| AC Characteristics | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–40°C ≤ TA ≤ +125°C for extended | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| | FOSC | External CLKIN Frequency(1) | DC | — | 4.0 | MHz | XT OSC mode |
| | | | DC | — | 4.0 | MHz | HS OSC mode (04) |
| | | | DC | — | 10 | MHz | HS OSC mode (10) |
| | | | DC | — | 20 | MHz | HS OSC mode (20) |
| | | | DC | — | 200 | kHz | LP OSC mode |
| | | Oscillator Frequency(1) | DC | — | 4.0 | MHz | RC OSC mode |
| | | | 0.1 | — | 4.0 | MHz | XT OSC mode |
| | | | 4.0 | — | 4.0 | MHz | HS OSC mode (04) |
| | | | 4.0 | — | 10 | MHz | HS OSC mode (10) |
| | | | 4.0 | — | 20 | MHz | HS OSC mode (20) |
| | | | 5.0 | — | 200 | kHz | LP OSC mode |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

**2:** Instruction cycle period (TCY) equals four times the input oscillator time base period.

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**TABLE 13-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16CR54A**

| AC Characteristics | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–40°C ≤ TA ≤ +125°C for extended | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| 1 | TOSC | External CLKIN Period(1) | 250 | — | — | ns | XT OSC mode |
| | | | 250 | — | — | ns | HS OSC mode (04) |
| | | | 100 | — | — | ns | HS OSC mode (10) |
| | | | 50 | — | — | ns | HS OSC mode (20) |
| | | | 5.0 | — | — | µs | LP OSC mode |
| | | Oscillator Period(1) | 250 | — | — | ns | RC OSC mode |
| | | | 250 | — | 10,000 | ns | XT OSC mode |
| | | | 250 | — | 250 | ns | HS OSC mode (04) |
| | | | 100 | — | 250 | ns | HS OSC mode (10) |
| | | | 50 | — | 250 | ns | HS OSC mode (20) |
| | | | 5.0 | — | 200 | µs | LP OSC mode |
| 2 | Tcy | Instruction Cycle Time(2) | — | 4/FOSC | — | — | |
| 3 | TosL, TosH | Clock in (OSC1) Low or High Time | 50* | — | — | ns | XT oscillator |
| | | | 20* | — | — | ns | HS oscillator |
| | | | 2.0* | — | — | µs | LP oscillator |
| 4 | TosR, TosF | Clock in (OSC1) Rise or Fall Time | — | — | 25* | ns | XT oscillator |
| | | | — | — | 25* | ns | HS oscillator |
| | | | — | — | 50* | ns | LP oscillator |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

**2:** Instruction cycle period (TCY) equals four times the input oscillator time base period.



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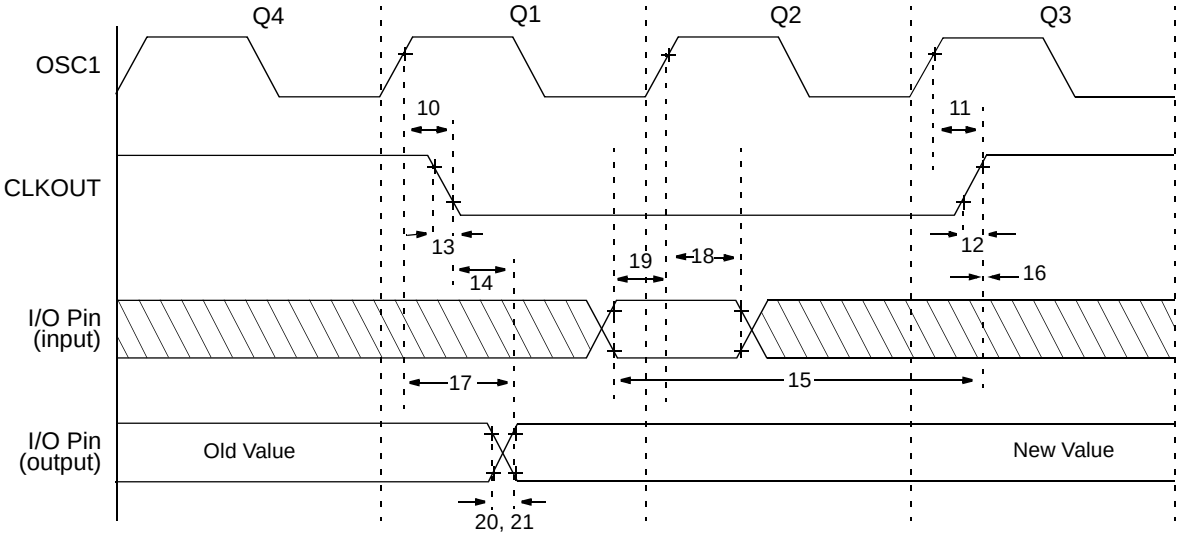
**FIGURE 13-3: CLKOUT AND I/O TIMING - PIC16CR54A**




**Note:** Please refer to Figure 13.1 for load conditions.

**TABLE 13-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16CR54A**

| AC Characteristics | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–40°C ≤ TA ≤ +125°C for extended | | | | | |
|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** |
| 10 | TosH2ckL | OSC1↑ to CLKOUT↓(1) | — | 15 | 30** | ns |
| 11 | TosH2ckH | OSC1↑ to CLKOUT↑(1) | — | 15 | 30** | ns |
| 12 | TckR | CLKOUT rise time(1) | — | 5.0 | 15** | ns |
| 13 | TckF | CLKOUT fall time(1) | — | 5.0 | 15** | ns |
| 14 | TckL2ioV | CLKOUT↓ to Port out valid(1) | — | — | 40** | ns |
| 15 | TioV2ckH | Port in valid before CLKOUT↑(1) | 0.25 TCY+30* | — | — | ns |
| 16 | TckH2ioI | Port in hold after CLKOUT↑(1) | 0* | — | — | ns |
| 17 | TosH2ioV | OSC1↑ (Q1 cycle) to Port out valid(2) | — | — | 100* | ns |
| 18 | TosH2ioI | OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time) | TBD | — | — | ns |
| 19 | TioV2osH | Port input valid to OSC1↑ (I/O in setup time) | TBD | — | — | ns |
| 20 | TioR | Port output rise time(2) | — | 10 | 25** | ns |
| 21 | TioF | Port output fall time(2) | — | 10 | 25** | ns |

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

**2:** Please refer to Figure 13.1 for load conditions.

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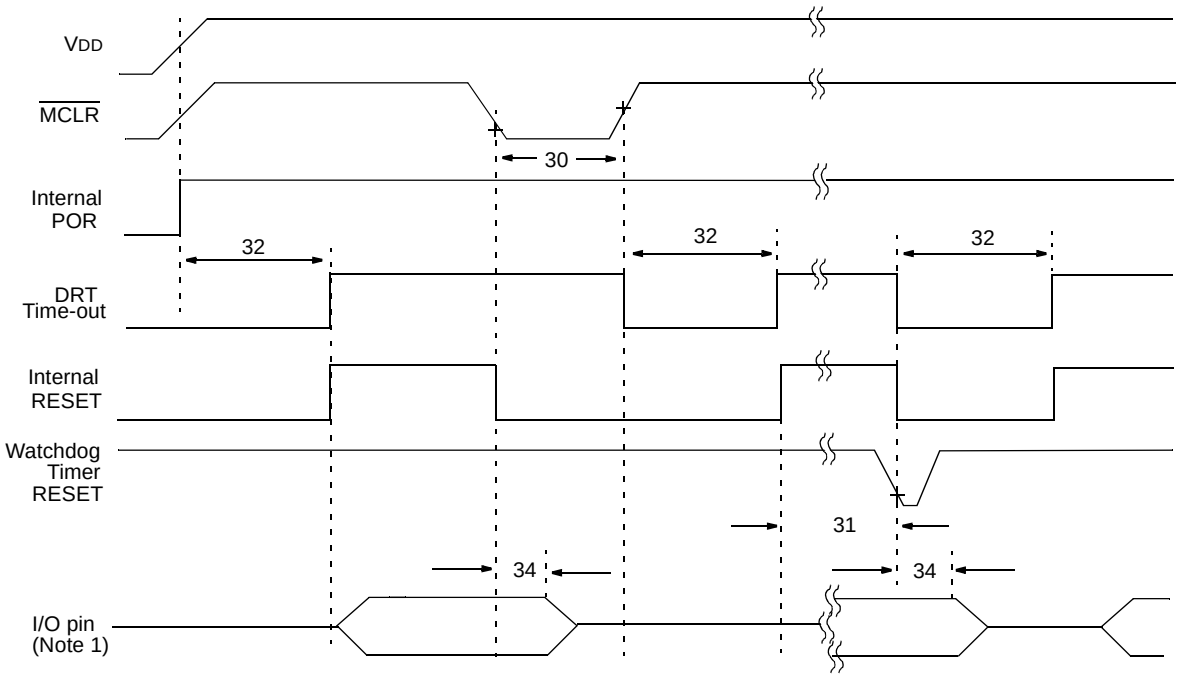
**FIGURE 13-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16CR54A**




**Note 1:** Please refer to Figure 13.1 for load conditions.

**TABLE 13-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16CR54A**

| **AC Characteristics** | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–40°C ≤ TA ≤ +125°C for extended | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| 30 | TmcL | $\overline{\text{MCLR}}$ Pulse Width (low) | 1.0* | — | — | µs | VDD = 5.0V |
| 31 | Twdt | Watchdog Timer Time-out Period (No Prescaler) | 7.0* | 18* | 40* | ms | VDD = 5.0V (Comm) |
| 32 | TDRT | Device Reset Timer Period | 7.0* | 18* | 30* | ms | VDD = 5.0V (Comm) |
| 34 | Tioz | I/O Hi-impedance from $\overline{\text{MCLR}}$ Low | — | — | 1.0* | µs | |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.



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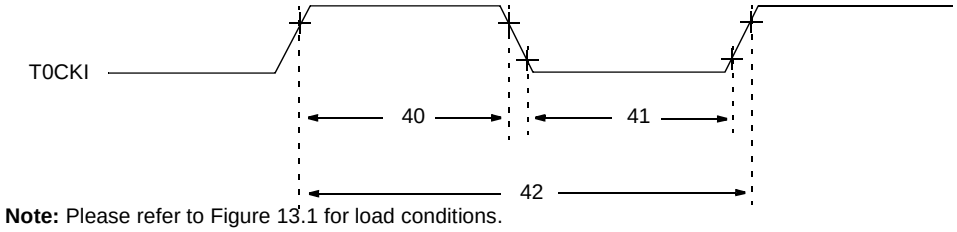
**FIGURE 13-5: TIMER0 CLOCK TIMINGS - PIC16CR54A**




**Note:** Please refer to Figure 13.1 for load conditions.

**TABLE 13-4: TIMER0 CLOCK REQUIREMENTS - PIC16CR54A**

| AC Characteristics | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–40°C ≤ TA ≤ +125°C for extended |
|---|---|

| Param No. | Symbol | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 40 | Tt0H | T0CKI High Pulse Width | | | | | |
| | | - No Prescaler | 0.5 TCY + 20* | — | — | ns | |
| | | - With Prescaler | 10* | — | — | ns | |
| 41 | Tt0L | T0CKI Low Pulse Width | | | | | |
| | | - No Prescaler | 0.5 TCY + 20* | — | — | ns | |
| | | - With Prescaler | 10* | — | — | ns | |
| 42 | Tt0P | T0CKI Period | 20 or $\frac{T_{CY} + 40}{N}$* | — | — | ns | Whichever is greater.<br>N = Prescale Value (1, 2, 4,..., 256) |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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## 14.0 DEVICE CHARACTERIZATION - PIC16C54A

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean – 3σ) respectively, where σ is a standard deviation, over the whole temperature range.

**FIGURE 14-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE**

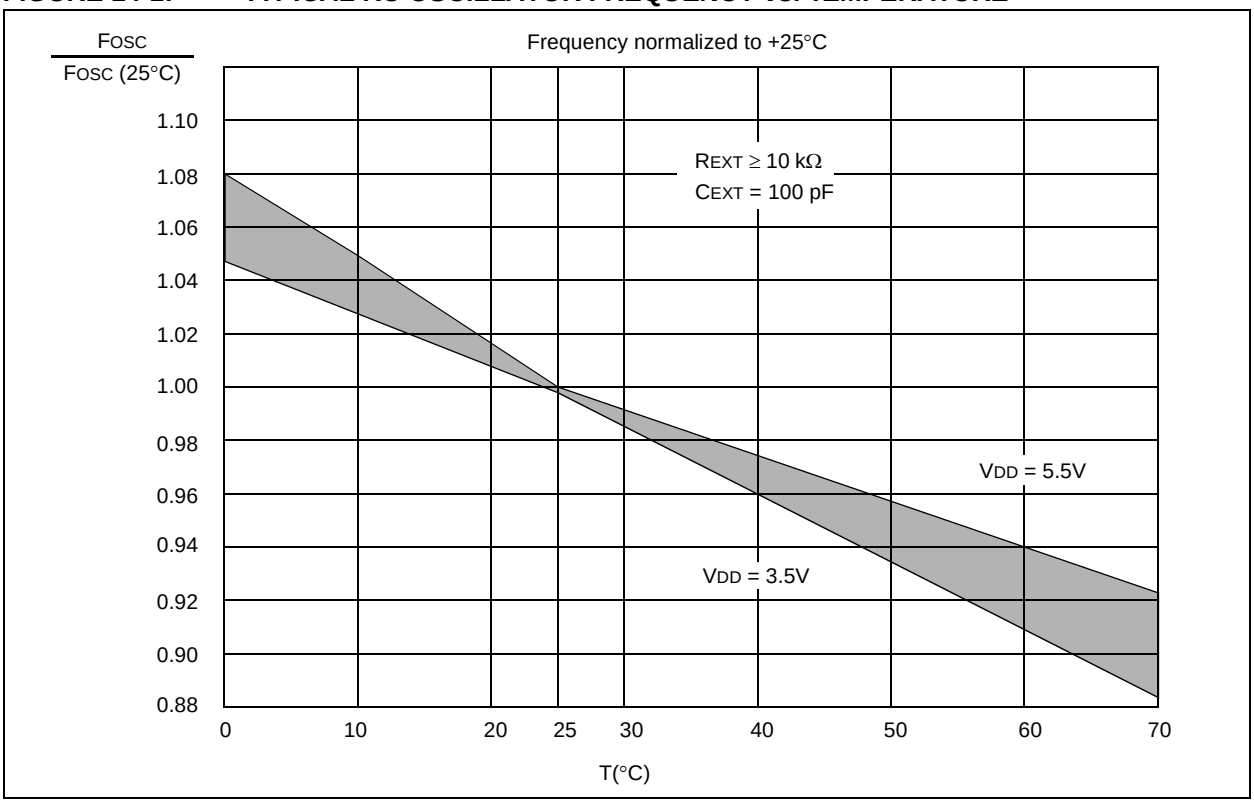


**TABLE 14-1: RC OSCILLATOR FREQUENCIES**

| CEXT | REXT | Average FOSC @ 5 V, 25°C | |
|---|---|---|---|
| 20 pF | 3.3K | 5 MHz | ± 27% |
| | 5K | 3.8 MHz | ± 21% |
| | 10K | 2.2 MHz | ± 21% |
| | 100K | 262 kHz | ± 31% |
| 100 pF | 3.3K | 1.6 MHz | ± 13% |
| | 5K | 1.2 MHz | ± 13% |
| | 10K | 684 kHz | ± 18% |
| | 100K | 71 kHz | ± 25% |
| 300 pF | 3.3K | 660 kHz | ± 10% |
| | 5.0K | 484 kHz | ± 14% |
| | 10K | 267 kHz | ± 15% |
| | 100K | 29 kHz | ± 19% |

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ±3 standard deviations from the average value for VDD = 5V.



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**FIGURE 14-2: TYPICAL RC OSC FREQUENCY vs. VDD, CEXT = 20 PF**

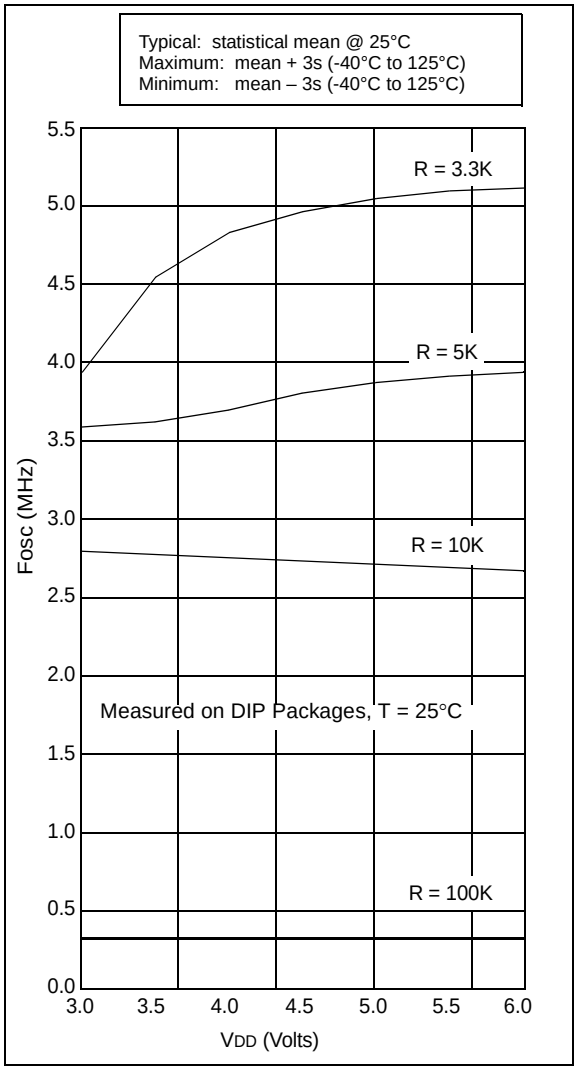


**FIGURE 14-3: TYPICAL RC OSC FREQUENCY vs. VDD, CEXT = 100 PF**

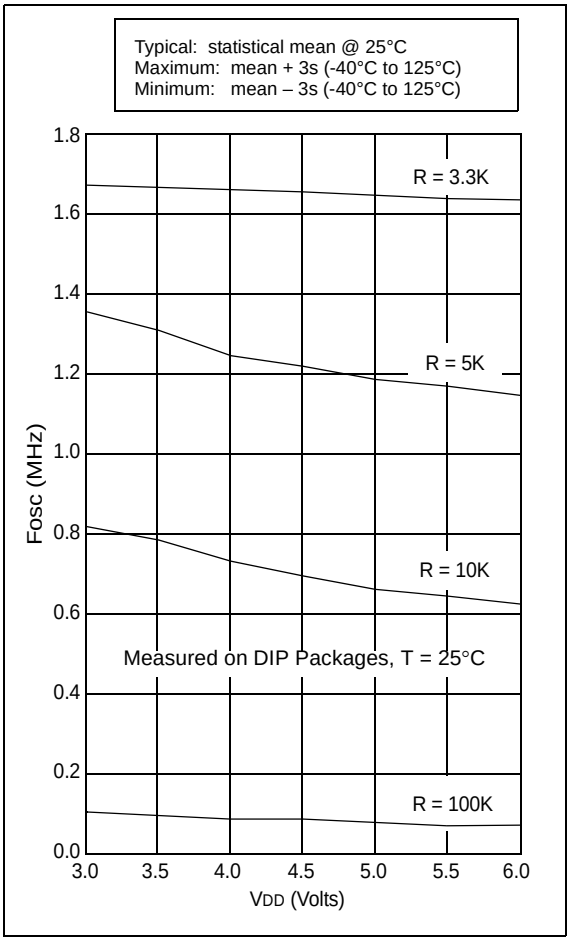


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**FIGURE 14-4: TYPICAL RC OSC FREQUENCY vs. VDD, CEXT = 300 PF**

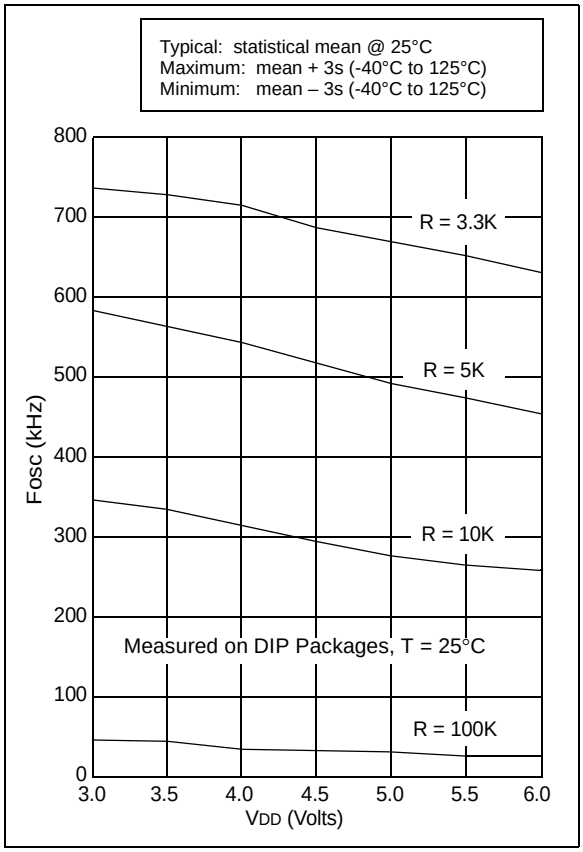


**FIGURE 14-5: TYPICAL IPD vs. VDD, WATCHDOG DISABLED**

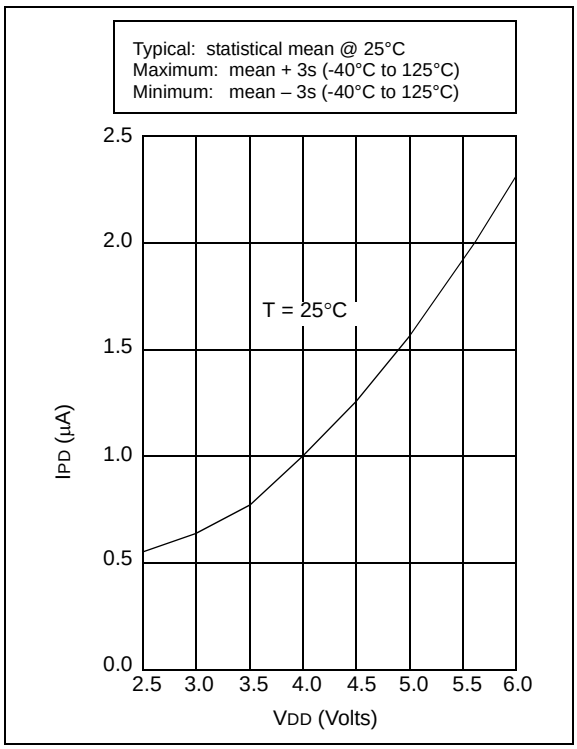




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**FIGURE 14-6: MAXIMUM IPD vs. VDD, WATCHDOG DISABLED**

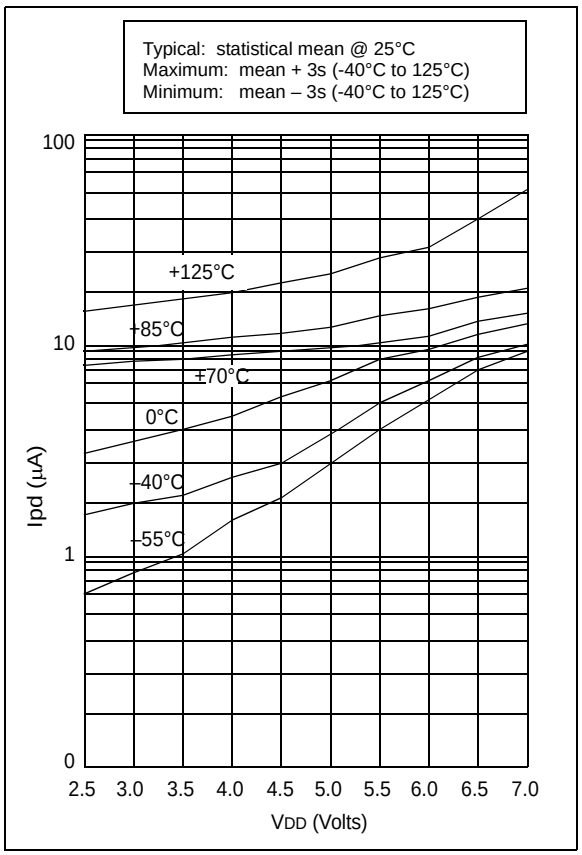



**FIGURE 14-7: TYPICAL IPD vs. VDD, WATCHDOG ENABLED**

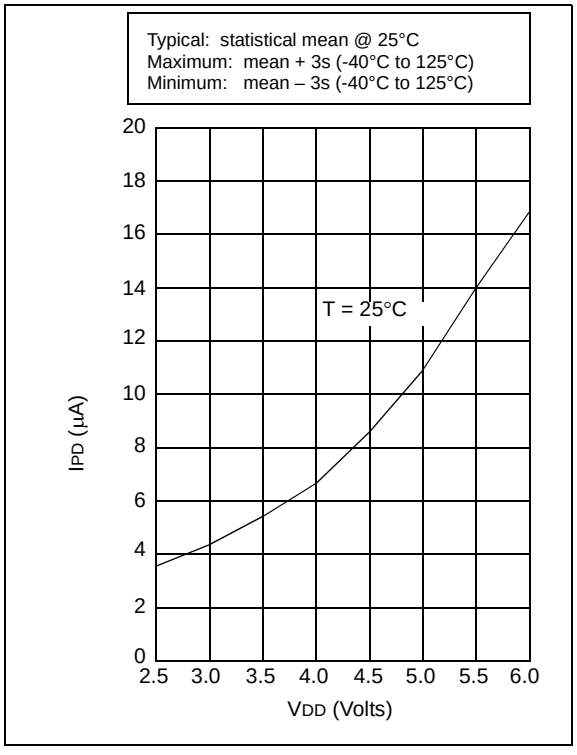
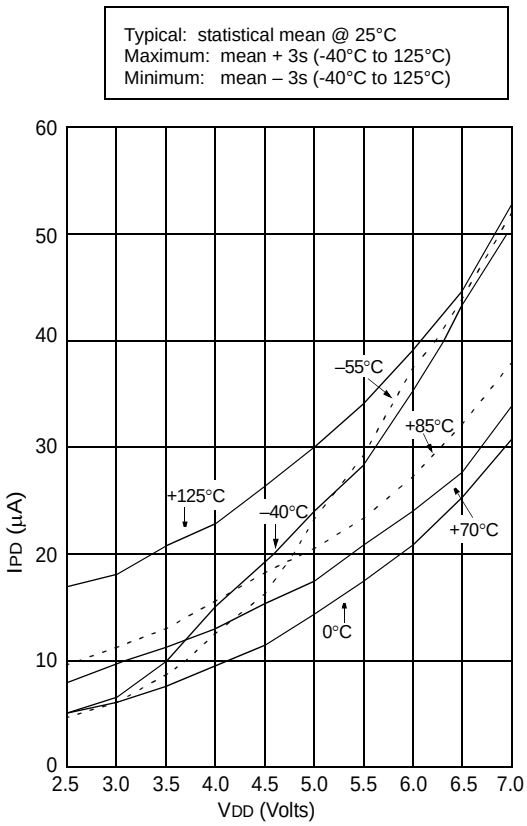



**FIGURE 14-8: MAXIMUM IPD vs. VDD, WATCHDOG ENABLED**




IPD, with WDT enabled, has two components:
The leakage current, which increases with higher temperature, and the operating current of the WDT logic, which increases with lower temperature. At –40°C, the latter dominates explaining the apparently anomalous behavior.

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**FIGURE 14-9: VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS vs. VDD**

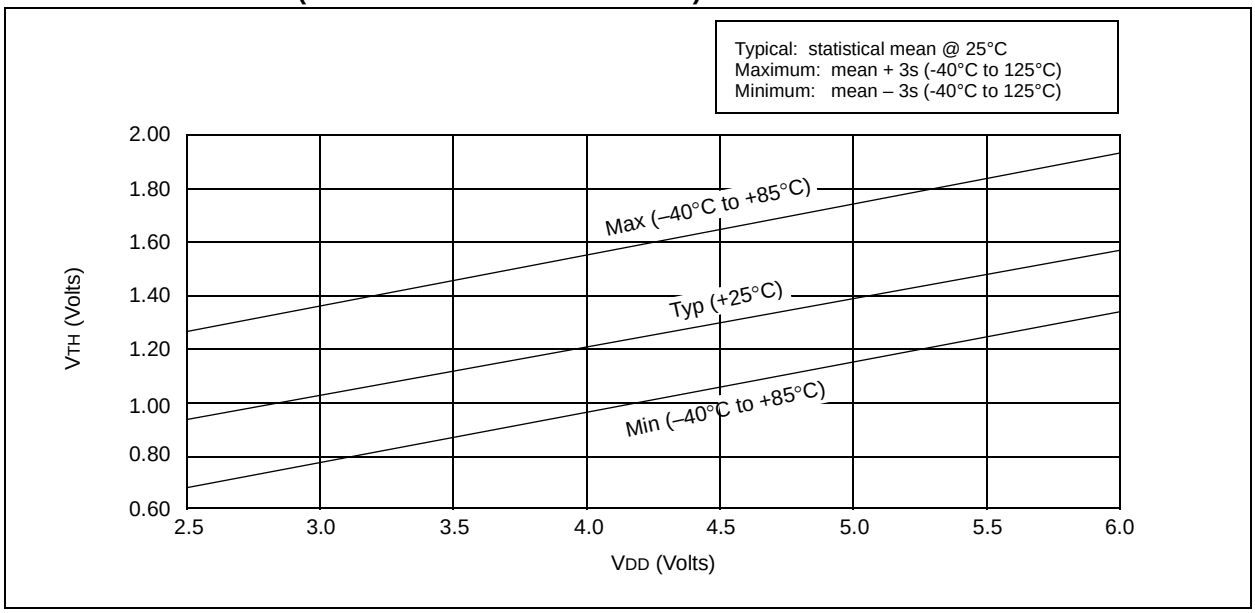
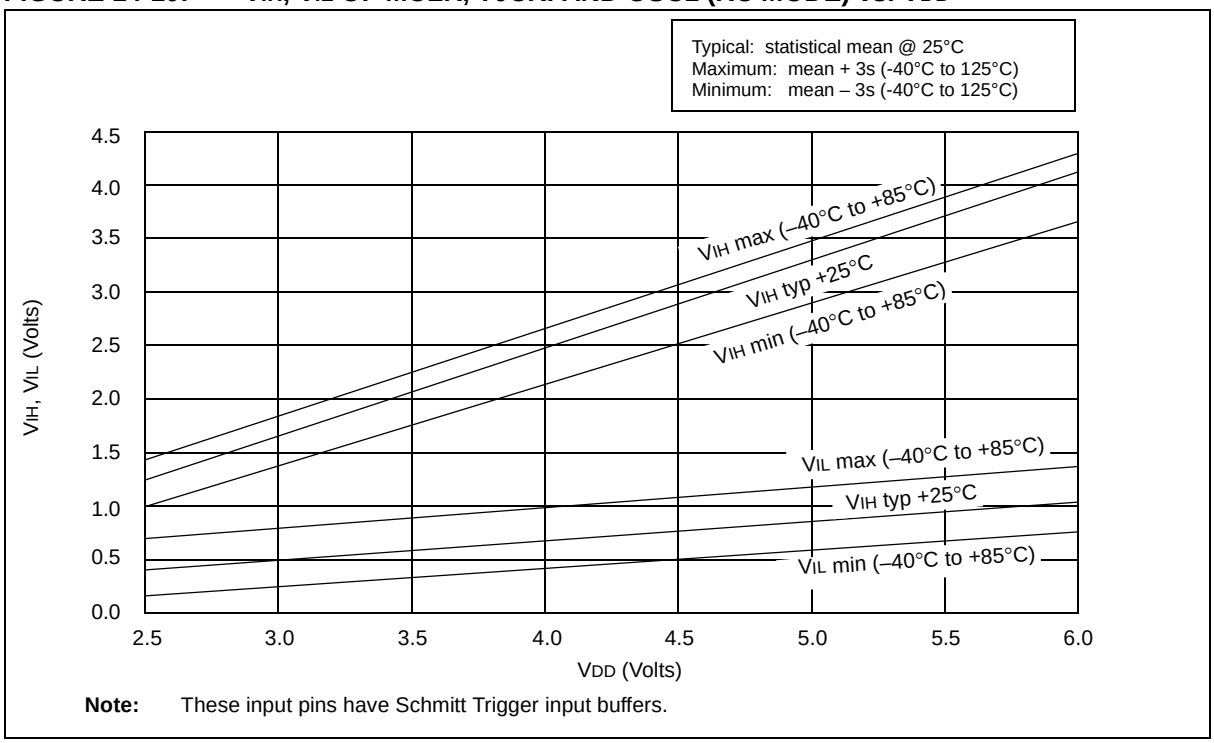



**FIGURE 14-10: VIH, VIL OF $\overline{\text{MCLR}}$, T0CKI AND OSC1 (RC MODE) vs. VDD**




**Note:** These input pins have Schmitt Trigger input buffers.



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**FIGURE 14-11: $V_{TH}$ (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (XT, HS, AND LP MODES) vs. $V_{DD}$**

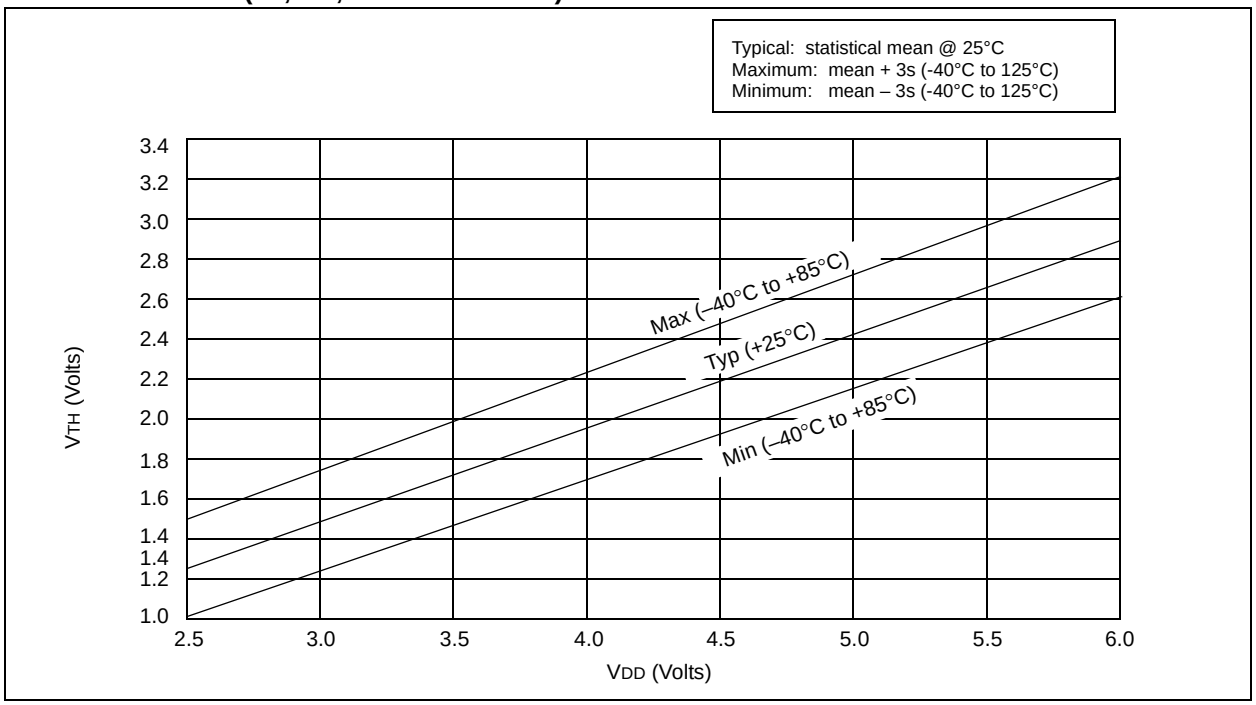


**FIGURE 14-12: TYPICAL IDD VS. FREQUENCY (EXTERNAL CLOCK, 25°C)**

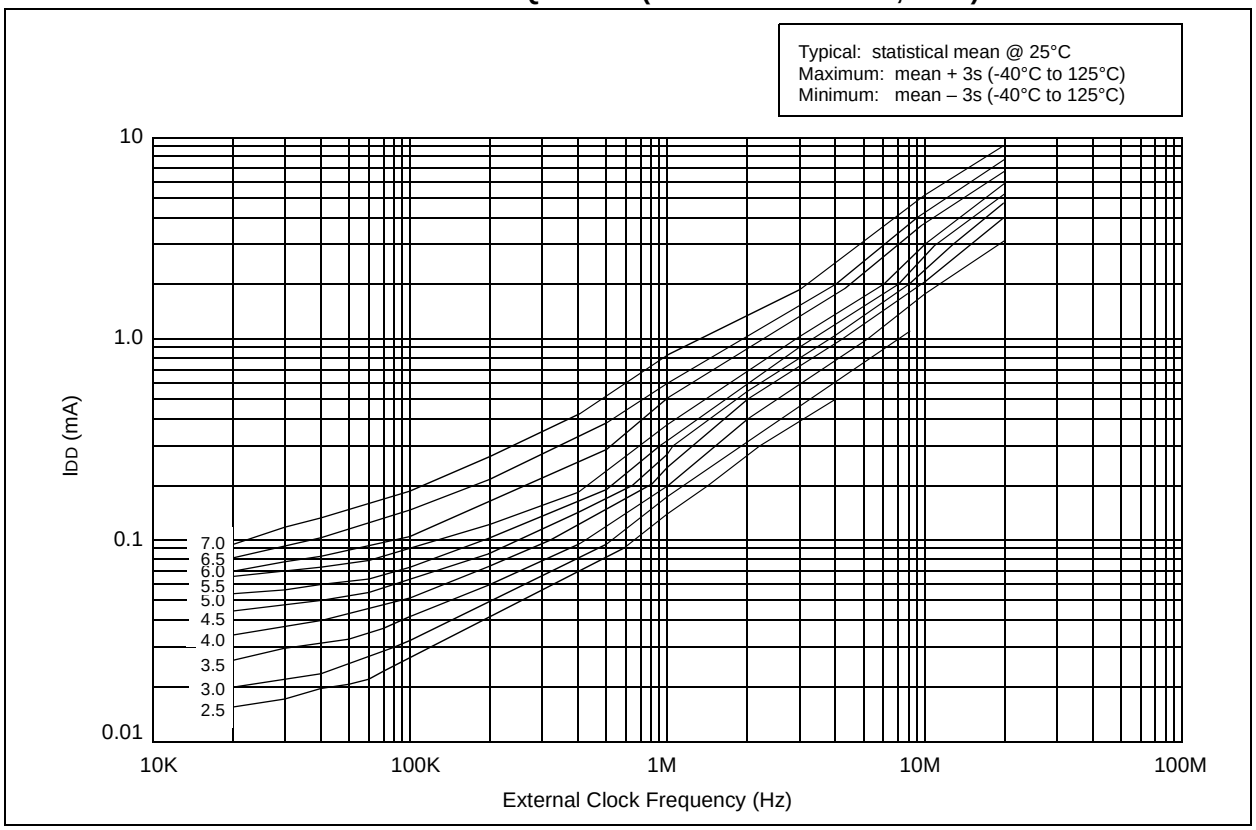


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**FIGURE 14-13: MAXIMUM IDD VS. FREQUENCY (EXTERNAL CLOCK, –40°C TO +85°C)**

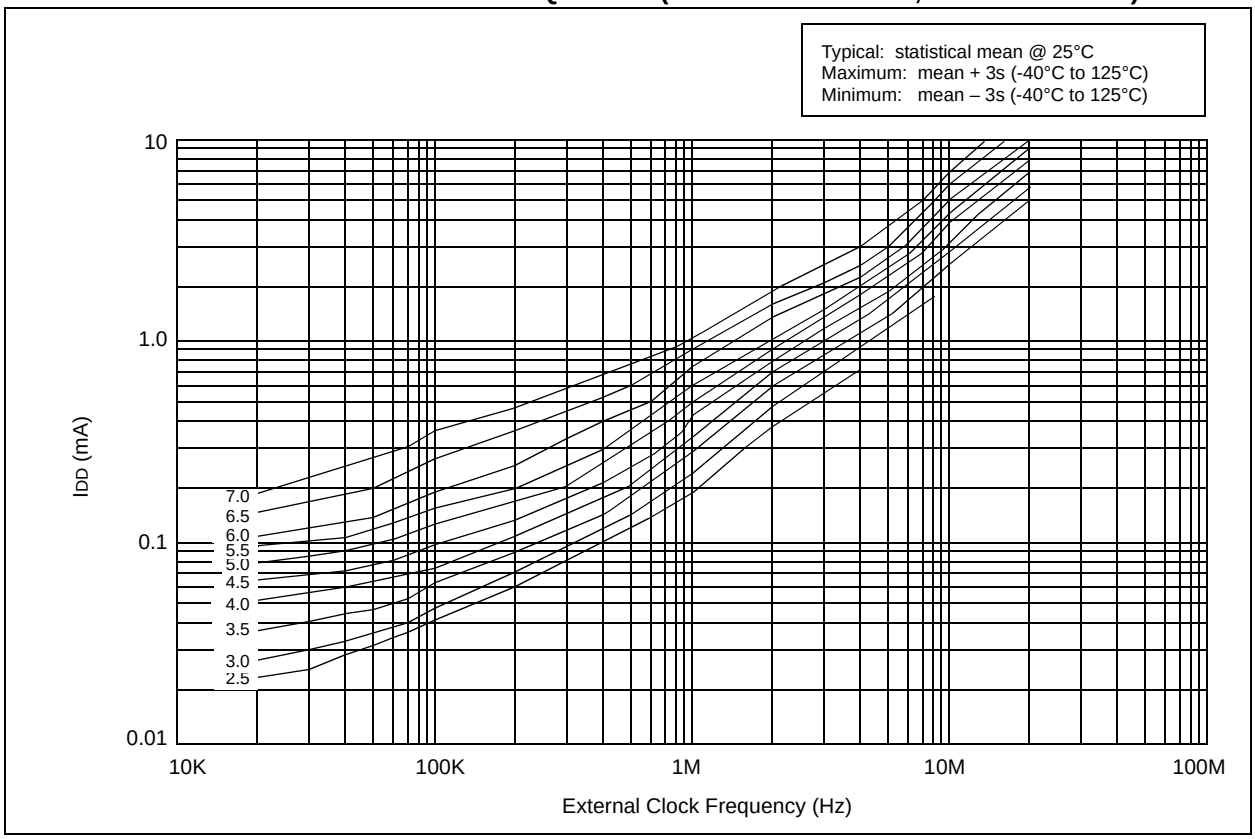


**FIGURE 14-14: MAXIMUM IDD vs. FREQUENCY (EXTERNAL CLOCK –55°C TO +125°C)**

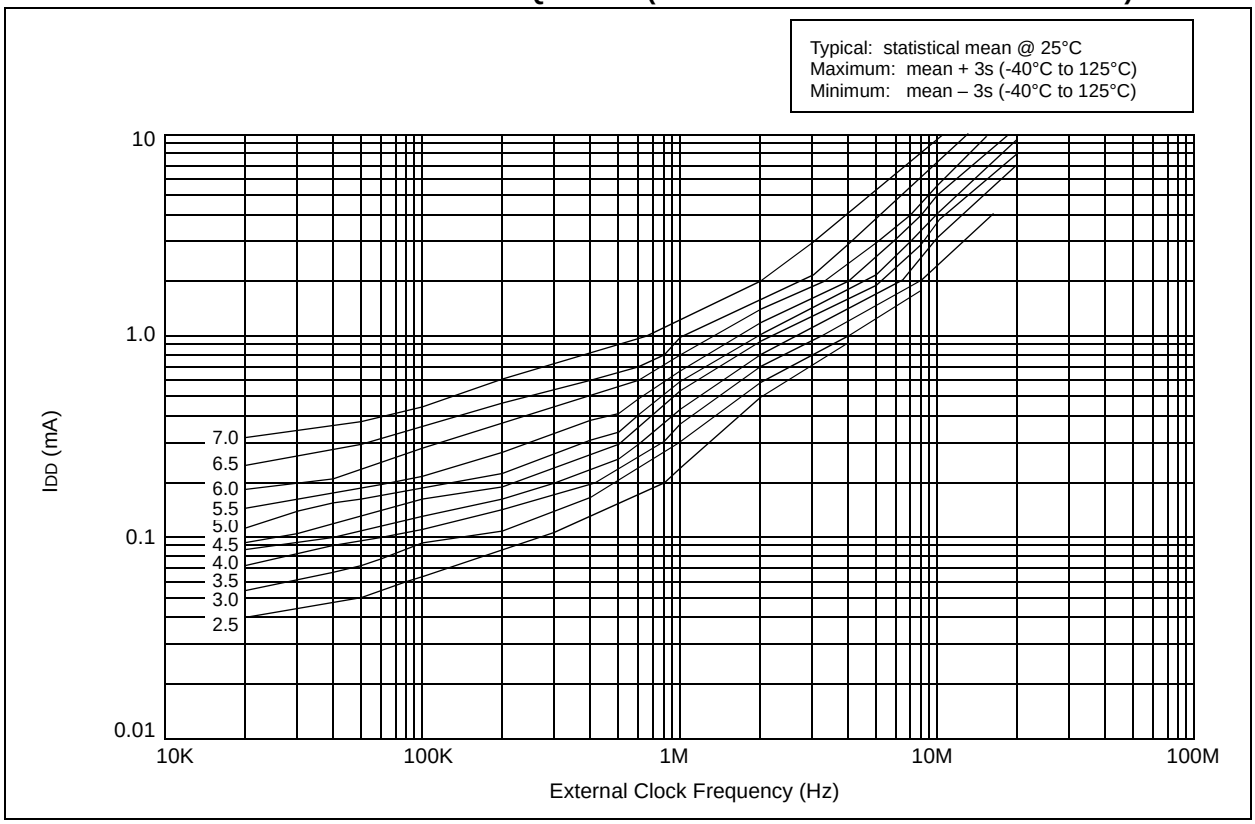




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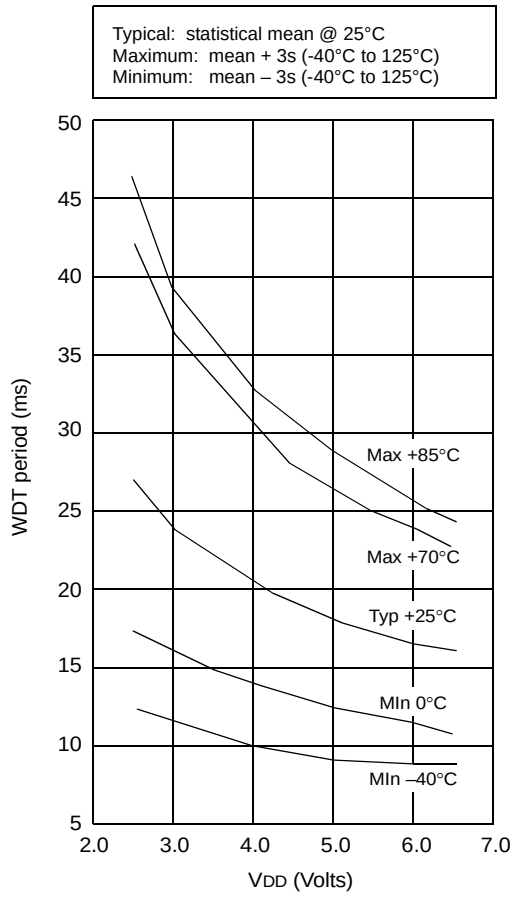
**FIGURE 14-15: WDT TIMER TIME-OUT PERIOD vs. $V_{DD}$ (1)**




**Note 1:** Prescaler set to 1:1.

**FIGURE 14-16: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR vs. $V_{DD}$**

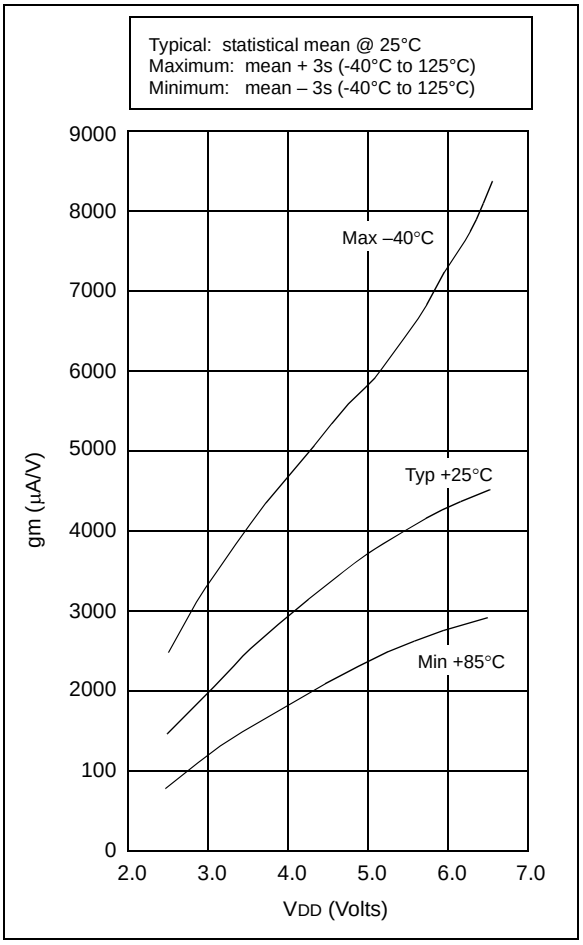



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**FIGURE 14-17: TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. VDD**

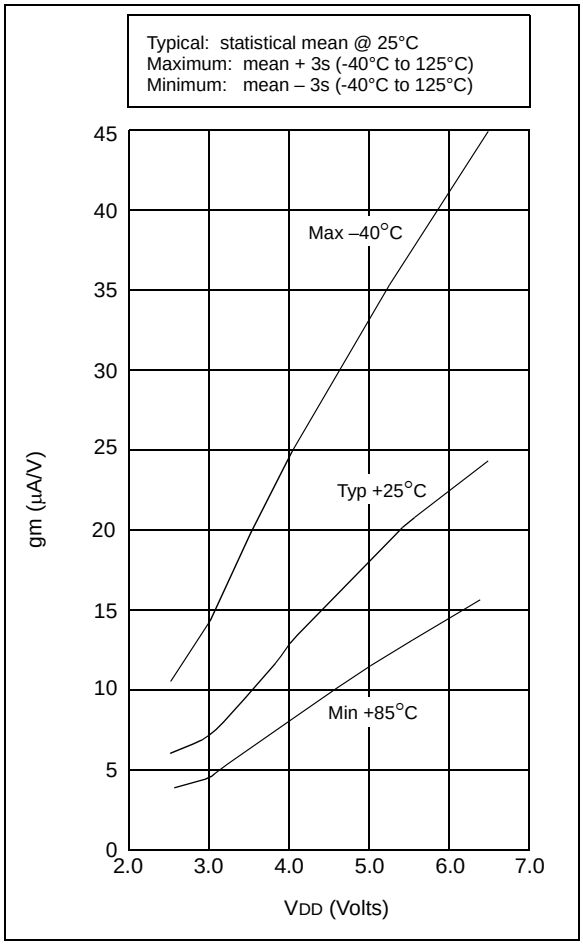


**FIGURE 14-18: TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD**

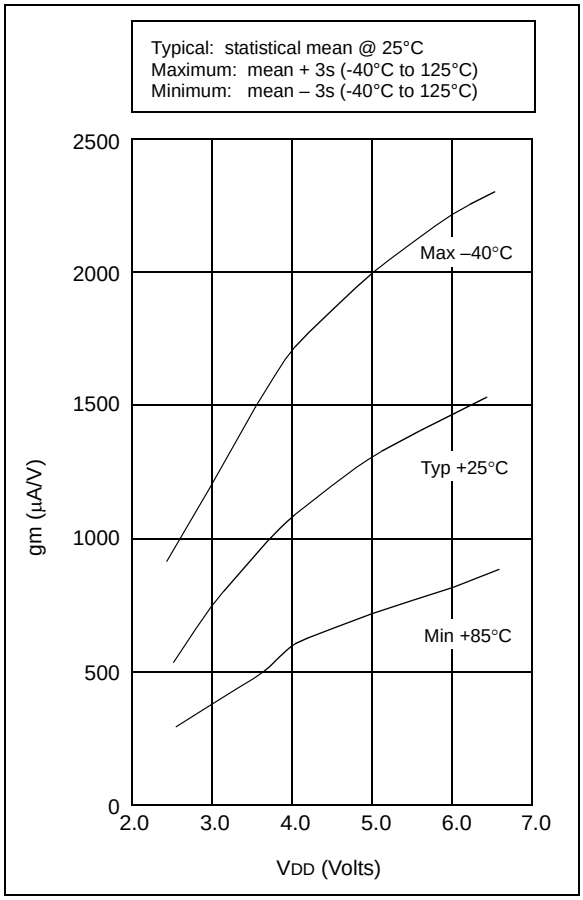




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**FIGURE 14-19: PORTA, B AND C $I_{OH}$ vs. $V_{OH}$, $V_{DD}$ = 3 V**

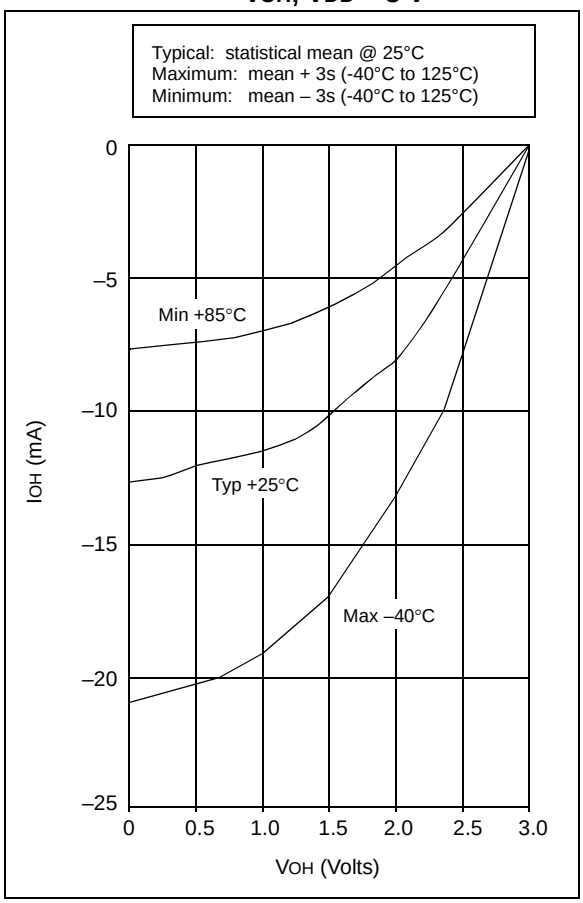


**FIGURE 14-20: PORTA, B AND C $I_{OH}$ vs. $V_{OH}$, $V_{DD}$ = 5 V**

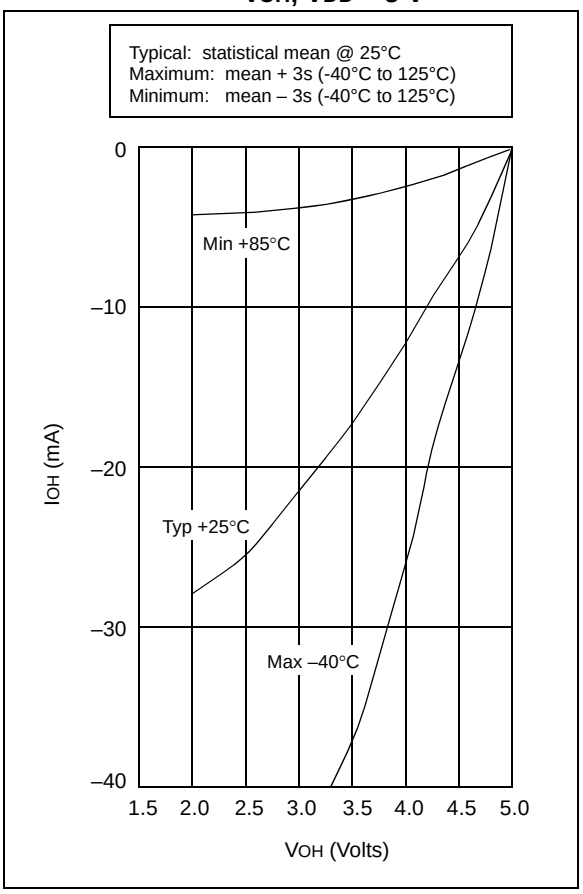


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**FIGURE 14-21: PORTA, B AND C IOL vs. VOL, VDD = 3 V**

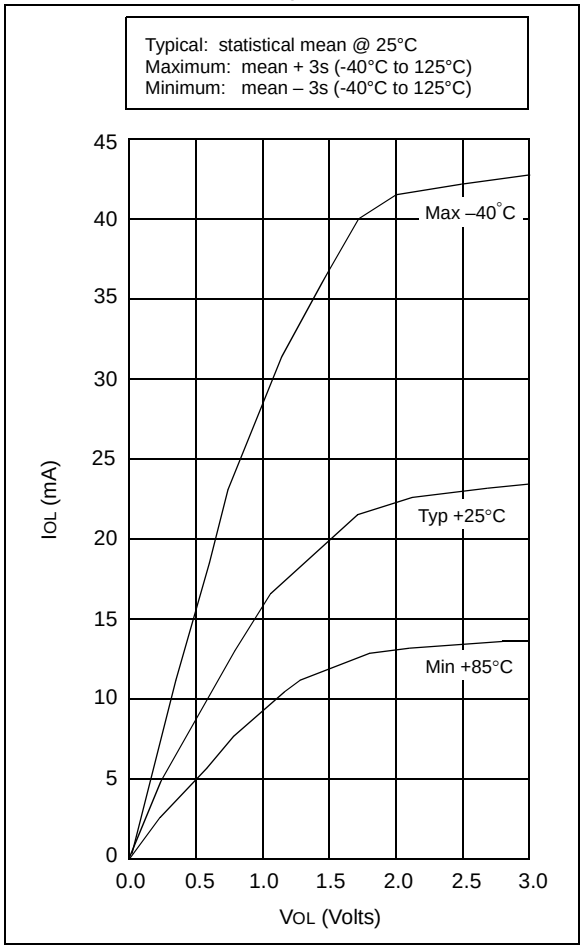


**FIGURE 14-22: PORTA, B AND C IOL vs. VOL, VDD = 5 V**

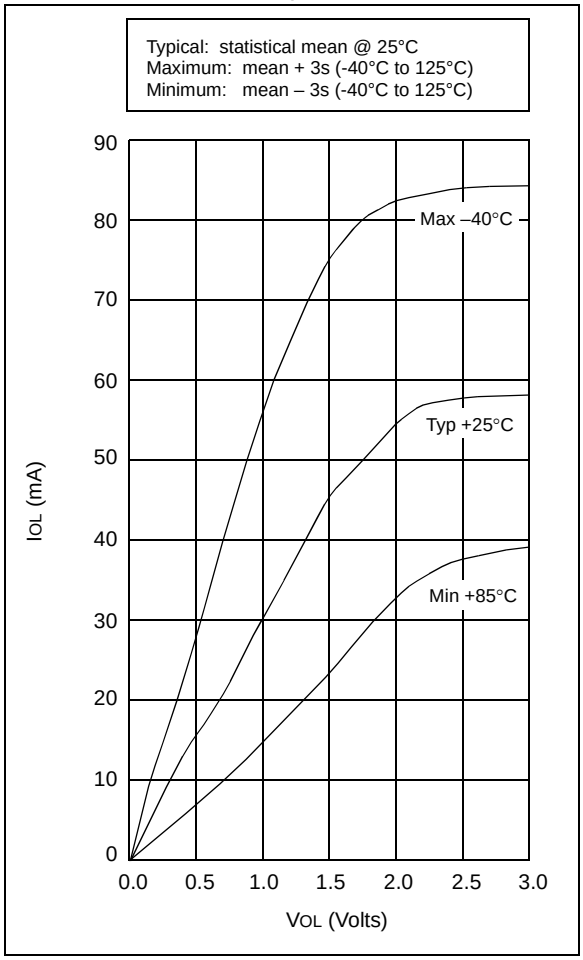




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**TABLE 14-2: INPUT CAPACITANCE FOR PIC16C54/56**

| Pin | Typical Capacitance (pF) | |
|---|---|---|
| | 18L PDIP | 18L SOIC |
| RA port | 5.0 | 4.3 |
| RB port | 5.0 | 4.3 |
| $\overline{MCLR}$ | 17.0 | 17.0 |
| OSC1 | 4.0 | 3.5 |
| OSC2/CLKOUT | 4.3 | 3.5 |
| T0CKI | 3.2 | 2.8 |

All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

**TABLE 14-3: INPUT CAPACITANCE FOR PIC16C55/57**

| Pin | Typical Capacitance (pF) | |
|---|---|---|
| | 28L PDIP (600 mil) | 28L SOIC |
| RA port | 5.2 | 4.8 |
| RB port | 5.6 | 4.7 |
| RC port | 5.0 | 4.1 |
| $\overline{MCLR}$ | 17.0 | 17.0 |
| OSC1 | 6.6 | 3.5 |
| OSC2/CLKOUT | 4.6 | 3.5 |
| T0CKI | 4.5 | 3.5 |

All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

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## 15.0 ELECTRICAL CHARACTERISTICS - PIC16C54A

Absolute Maximum Ratings(†)

Ambient temperature under bias ..... –55°C to +125°C

Storage temperature ..... –65°C to +150°C

Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... 0 to +7.5V

Voltage on $\overline{MCLR}$ with respect to $V_{SS}$ ..... 0 to +14V

Voltage on all other pins with respect to $V_{SS}$ ..... –0.6V to ($V_{DD}$ + 0.6V)

Total power dissipation(1) ..... 800 mW

Max. current out of $V_{SS}$ pin ..... 150 mA

Max. current into $V_{DD}$ pin ..... 100 mA

Max. current into an input pin (T0CKI only) ..... ±500 µA

Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{DD}$) ..... ±20 mA

Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{DD}$) ..... ±20 mA

Max. output current sunk by any I/O pin ..... 25 mA

Max. output current sourced by any I/O pin ..... 20 mA

Max. output current sourced by a single I/O port (PORTA or B) ..... 50 mA

Max. output current sunk by a single I/O port (PORTA or B) ..... 50 mA

**Note 1:** Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.



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## 15.1 DC Characteristics: PIC16C54A-04, 10, 20 (Commercial)
## PIC16C54A-04I, 10I, 20I (Industrial)
## PIC16LC54A-04 (Commercial)
## PIC16LC54A-04I (Industrial)

| | |
|---|---|
| **PIC16LC54A-04**<br>**PIC16LC54A-04I**<br>(Commercial, Industrial) | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial |
| **PIC16C54A-04, 10, 20**<br>**PIC16C54A-04I, 10I, 20I**<br>(Commercial, Industrial) | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial |

| Param No. | Symbol | Characteristic/Device | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | VDD | **Supply Voltage** | | | | | |
| D001 | | PIC16LC54A | 3.0<br>2.5 | —<br>— | 6.25<br>6.25 | V<br>V | XT and RC modes<br>LP mode |
| D001A | | PIC16C54A | 3.0<br>4.5 | —<br>— | 6.25<br>5.5 | V<br>V | RC, XT and LP modes<br>HS mode |
| D002 | VDR | **RAM Data Retention Voltage(1)** | — | 1.5* | — | V | Device in SLEEP mode |
| D003 | VPOR | **VDD Start Voltage** to ensure Power-on Reset | — | Vss | — | V | See Section 5.1 for details on Power-on Reset |
| D004 | SVDD | **VDD Rise Rate** to ensure Power-on Reset | 0.05* | — | — | V/ms | See Section 5.1 for details on Power-on Reset |
| D005 | IDD | **Supply Current(2)** | | | | | |
| | | PIC16LC5X | —<br><br>—<br><br>— | 0.5<br><br>11<br><br>11 | 2.5<br><br>27<br><br>35 | mA<br><br>µA<br><br>µA | FOSC = 4.0 MHz, VDD = 5.5V, RC(3) and XT modes<br>FOSC = 32 kHz, VDD = 2.5V, WDT disabled, LP mode, Commercial<br>FOSC = 32 kHz, VDD = 2.5V, WDT disabled, LP mode, Industrial |
| D005A | | PIC16C5X | —<br><br>—<br>—<br>—<br><br>— | 1.8<br><br>2.4<br>4.5<br>14<br><br>17 | 2.4<br><br>8.0<br>16<br>29<br><br>37 | mA<br><br>mA<br>mA<br>µA<br><br>µA | FOSC = 4.0 MHz, VDD = 5.5V, RC(3) and XT modes<br>FOSC = 10 MHz, VDD = 5.5V, HS mode<br>FOSC = 20 MHz, VDD = 5.5V, HS mode<br>FOSC = 32 kHz, VDD = 3.0V, WDT disabled, LP mode, Commercial<br>FOSC = 32 kHz, VDD = 3.0V, WDT disabled, LP mode, Industrial |

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

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## 15.1 DC Characteristics: PIC16C54A-04, 10, 20 (Commercial)
## PIC16C54A-04I, 10I, 20I (Industrial)
## PIC16LC54A-04 (Commercial)
## PIC16LC54A-04I (Industrial)

| | |
|---|---|
| **PIC16LC54A-04**<br>**PIC16LC54A-04I**<br>(Commercial, Industrial) | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial |
| **PIC16C54A-04, 10, 20**<br>**PIC16C54A-04I, 10I, 20I**<br>(Commercial, Industrial) | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial |

| Param No. | Symbol | Characteristic/Device | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | IPD | **Power-down Current(2)** | | | | | |
| D006 | | PIC16LC5X | — | 2.5 | 12 | µA | VDD = 2.5V, WDT enabled, Commercial |
| | | | — | 0.25 | 4.0 | µA | VDD = 2.5V, WDT disabled, Commercial |
| | | | — | 2.5 | 14 | µA | VDD = 2.5V, WDT enabled, Industrial |
| | | | — | 0.25 | 5.0 | µA | VDD = 2.5V, WDT disabled, Industrial |
| D006A | | PIC16C5X | — | 4.0 | 12 | µA | VDD = 3.0V, WDT enabled, Commercial |
| | | | — | 0.25 | 4.0 | µA | VDD = 3.0V, WDT disabled, Commercial |
| | | | — | 5.0 | 14 | µA | VDD = 3.0V, WDT enabled, Industrial |
| | | | — | 0.3 | 5.0 | µA | VDD = 3.0V, WDT disabled, Industrial |

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.



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## 15.2 DC Characteristics: PIC16C54A-04E, 10E, 20E (Extended) PIC16LC54A-04E (Extended)

| **PIC16LC54A-04E** (Extended) | | | **Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ TA ≤ +125°C for extended | | | | |
|---|---|---|---|---|---|---|---|
| **PIC16C54A-04E, 10E, 20E** (Extended) | | | **Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ TA ≤ +125°C for extended | | | | |
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| | VDD | **Supply Voltage** | | | | | |
| D001 | | PIC16LC54A | 3.0<br>2.5 | —<br>— | 6.25<br>6.25 | V<br>V | XT and RC modes<br>LP mode |
| D001A | | PIC16C54A | 3.5<br>4.5 | —<br>— | 5.5<br>5.5 | V<br>V | RC and XT modes<br>HS mode |
| D002 | VDR | **RAM Data Retention Voltage(1)** | — | 1.5* | — | V | Device in SLEEP mode |
| D003 | VPOR | **VDD Start Voltage** to ensure Power-on Reset | — | Vss | — | V | See Section 5.1 for details on Power-on Reset |
| D004 | SVDD | **VDD Rise Rate** to ensure Power-on Reset | 0.05* | — | — | V/ms | See Section 5.1 for details on Power-on Reset |
| | IDD | **Supply Current(2)** | | | | | |
| D010 | | PIC16LC54A | —<br><br>—<br><br>—<br><br>— | 0.5<br><br>11<br><br>11<br><br>11 | 25<br><br>27<br><br>35<br><br>37 | mA<br><br>µA<br><br>µA<br><br>µA | FOSC = 4.0 MHz, VDD = 5.5V, RC(3) and XT modes<br>FOSC = 32 kHz, VDD = 2.5V, LP mode, Commercial<br>FOSC = 32 kHz, VDD = 2.5V, LP mode, Industrial<br>FOSC = 32 kHz, VDD = 2.5V, LP mode, Extended |
| D010A | | PIC16C54A | —<br><br>—<br><br>— | 1.8<br><br>4.8<br><br>9.0 | 3.3<br><br>10<br><br>20 | mA<br><br>mA<br><br>mA | FOSC = 4.0 MHz, VDD = 5.5V, RC(3) and XT modes<br>FOSC = 10 MHz, VDD = 5.5V, HS mode<br>FOSC = 20 MHz, VDD = 5.5V, HS mode |

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

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## 15.2 DC Characteristics: PIC16C54A-04E, 10E, 20E (Extended) PIC16LC54A-04E (Extended)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **PIC16LC54A-04E** (Extended) | | | **Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ TA ≤ +125°C for extended | | | | |
| **PIC16C54A-04E, 10E, 20E** (Extended) | | | **Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ TA ≤ +125°C for extended | | | | |
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| | IPD | **Power-down Current(2)** | | | | | |
| D020 | | PIC16LC54A | — | 2.5 | 15 | µA | VDD = 2.5V, WDT enabled, Extended |
| | | | — | 0.25 | 7.0 | µA | VDD = 2.5V, WDT disabled, Extended |
| D020A | | PIC16C54A | — | 5.0 | 22 | µA | VDD = 3.5V, WDT enabled |
| | | | — | 0.8 | 18* | µA | VDD = 3.5V, WDT disabled |

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.



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## 15.3 DC Characteristics: PIC16LV54A-02 (Commercial) PIC16LV54A-02I (Industrial)

| PIC16LV54A-02<br>PIC16LV54A-02I<br>(Commercial, Industrial) | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–20°C ≤ TA ≤ +85°C for industrial | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D001 | VDD | **Supply Voltage**<br>RC and XT modes | 2.0 | — | 3.8 | V | |
| D002 | VDR | **RAM Data Retention Voltage(1)** | — | 1.5* | — | V | Device in SLEEP mode |
| D003 | VPOR | **VDD Start Voltage** to ensure Power-on Reset | — | Vss | — | V | See Section 5.1 for details on Power-on Reset |
| D004 | SVDD | **VDD Rise Rate** to ensure Power-on Reset | 0.05* | — | — | V/ms | See Section 5.1 for details on Power-on Reset |
| D010 | IDD | **Supply Current(2)**<br>RC(3) and XT modes<br>LP mode, Commercial<br>LP mode, Industrial | <br>—<br>—<br>— | <br>0.5<br>11<br>14 | <br>—<br>27<br>35 | <br>mA<br>µA<br>µA | <br>FOSC = 2.0 MHz, VDD = 3.0V<br>FOSC = 32 kHz, VDD = 2.5V WDT disabled<br>FOSC = 32 kHz, VDD = 2.5V WDT disabled |
| D020 | IPD | **Power-down Current(2,4)**<br>Commercial<br>Commercial<br>Industrial<br>Industrial | <br>—<br>—<br>—<br>— | <br>2.5<br>0.25<br>3.5<br>0.3 | <br>12<br>4.0<br>14<br>5.0 | <br>µA<br>µA<br>µA<br>µA | <br>VDD = 2.5V, WDT enabled<br>VDD = 2.5V, WDT disabled<br>VDD = 2.5V, WDT enabled<br>VDD = 2.5V, WDT disabled |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

**4:** The oscillator start-up time can be as much as 8 seconds for XT and LP oscillator selection on wake-up from SLEEP mode or during initial power-up.

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## 15.4 DC Characteristics: PIC16C54A-04, 10, 20, PIC16LC54A-04, PIC16LV54A-02 (Commercial) PIC16C54A-04I, 10I, 20I, PIC16LC54A-04I, PIC16LV54A-02I (Industrial) PIC16C54A-04E, 10E, 20E, PIC16LC54A-04E (Extended)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–20°C ≤ TA ≤ +85°C for industrial-PIC16LV54A-02I<br>–40°C ≤ TA ≤ +125°C for extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D030 | VIL | **Input Low Voltage** | | | | | |
| | | I/O ports | VSS | — | 0.2 VDD | V | Pin at hi-impedance |
| | | MCLR (Schmitt Trigger) | VSS | — | 0.15 VDD | V | |
| | | T0CKI (Schmitt Trigger) | VSS | — | 0.15 VDD | V | |
| | | OSC1 (Schmitt Trigger) | VSS | — | 0.15 VDD | V | RC mode only(3) |
| | | OSC1 | VSS | — | 0.3 VDD | | XT, HS and LP modes |
| D040 | VIH | **Input High Voltage** | | | | | |
| | | I/O ports | 0.2 VDD + 1 | — | VDD | V | For all VDD(4) |
| | | I/O ports | 2.0 | — | VDD | V | 4.0V < VDD ≤ 5.5V(4) |
| | | MCLR (Schmitt Trigger) | 0.85 VDD | — | VDD | V | |
| | | T0CKI (Schmitt Trigger) | 0.85 VDD | — | VDD | V | |
| | | OSC1 (Schmitt Trigger) | 0.85 VDD | — | VDD | V | RC mode only(3) |
| | | OSC1 | 0.7 VDD | — | VDD | V | XT, HS and LP modes |
| D050 | VHYS | **Hysteresis of Schmitt Trigger inputs** | 0.15 VDD* | — | — | V | |
| D060 | IIL | **Input Leakage Current(1,2)** | | | | | **For VDD ≤ 5.5V:** |
| | | I/O ports | -1.0 | 0.5 | +1.0 | µA | VSS ≤ VPIN ≤ VDD, pin at hi-impedance |
| | | MCLR | -5.0 | — | +5.0 | µA | VPIN = VSS +0.25V |
| | | MCLR | — | 0.5 | +3.0 | µA | VPIN = VDD |
| | | T0CKI | -3.0 | 0.5 | +3.0 | µA | VSS ≤ VPIN ≤ VDD |
| | | OSC1 | -3.0 | 0.5 | — | µA | VSS ≤ VPIN ≤ VDD, XT, HS and LP modes |
| D080 | VOL | **Output Low Voltage** | | | | | |
| | | I/O ports | — | — | 0.6 | V | IOL = 8.7 mA, VDD = 4.5V |
| | | OSC2/CLKOUT | — | — | 0.6 | V | IOL = 1.6 mA, VDD = 4.5V, RC mode only |
| | VOH | **Output High Voltage(2)** | | | | | |
| | | I/O ports | VDD - 0.7 | — | — | V | IOH = -5.4 mA, VDD = 4.5V |
| | | OSC2/CLKOUT | VDD - 0.7 | — | — | V | IOH = -1.0 mA, VDD = 4.5V, RC mode only |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

**2:** Negative current is defined as coming out of the pin.

**3:** For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.



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## 15.5 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

| | |
|---|---|
| T | |
| F Frequency | T Time |

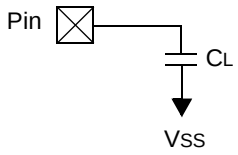
Lowercase letters (pp) and their meanings:

| | |
|---|---|
| pp | |
| 2 to | mc $\overline{\text{MCLR}}$ |
| ck CLKOUT | osc oscillator |
| cy cycle time | os OSC1 |
| drt device reset timer | t0 T0CKI |
| io I/O port | wdt watchdog timer |

Uppercase letters and their meanings:

| | |
|---|---|
| S | |
| F Fall | P Period |
| H High | R Rise |
| I Invalid (Hi-impedance) | V Valid |
| L Low | Z Hi-impedance |

**FIGURE 15-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16C54A**




$C_L$ = 50 pF for all pins and OSC2 for RC modes

0 -15 pF for OSC2 in XT, HS or LP modes when external clock is used to drive OSC1

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## 15.6 Timing Diagrams and Specifications

**FIGURE 15-2: EXTERNAL CLOCK TIMING - PIC16C54A**

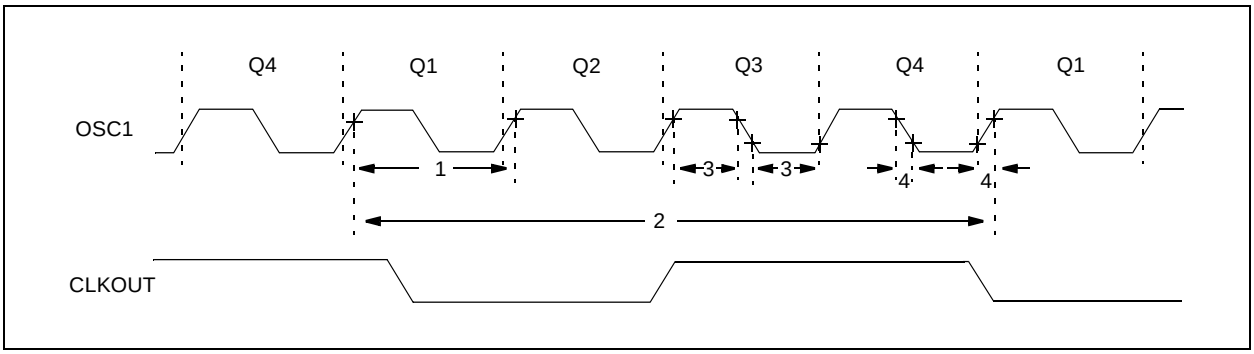


**TABLE 15-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54A**

| AC Characteristics | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–20°C ≤ TA ≤ +85°C for industrial - PIC16LV54A-02I<br>–40°C ≤ TA ≤ +125°C for extended | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| | FOSC | External CLKIN Frequency(1) | DC | — | 4.0 | MHz | XT osc mode |
| | | | DC | — | 2.0 | MHz | XT osc mode (PIC16LV54A) |
| | | | DC | — | 4.0 | MHz | HS osc mode (04) |
| | | | DC | — | 10 | MHz | HS osc mode (10) |
| | | | DC | — | 20 | MHz | HS osc mode (20) |
| | | | DC | — | 200 | kHz | LP osc mode |
| | | Oscillator Frequency(1) | DC | — | 4.0 | MHz | RC osc mode |
| | | | DC | — | 2.0 | MHz | RC osc mode (PIC16LV54A) |
| | | | 0.1 | — | 4.0 | MHz | XT osc mode |
| | | | 0.1 | — | 2.0 | MHz | XT osc mode (PIC16LV54A) |
| | | | 4.0 | — | 4.0 | MHz | HS osc mode (04) |
| | | | 4.0 | — | 10 | MHz | HS osc mode (10) |
| | | | 4.0 | — | 20 | MHz | HS osc mode (20) |
| | | | 5.0 | — | 200 | kHz | LP osc mode |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

**2:** Instruction cycle period (TCY) equals four times the input oscillator time base period.



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**TABLE 15-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54A**

| AC Characteristics | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–20°C ≤ TA ≤ +85°C for industrial - PIC16LV54A-02I<br>–40°C ≤ TA ≤ +125°C for extended | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| 1 | TOSC | External CLKIN Period(1) | 250 | — | — | ns | XT OSC mode |
| | | | 500 | — | — | ns | XT OSC mode (PIC16LV54A) |
| | | | 250 | — | — | ns | HS OSC mode (04) |
| | | | 100 | — | — | ns | HS OSC mode (10) |
| | | | 50 | — | — | ns | HS OSC mode (20) |
| | | | 5.0 | — | — | µs | LP OSC mode |
| | | Oscillator Period(1) | 250 | — | — | ns | RC OSC mode |
| | | | 500 | — | — | ns | RC OSC mode (PIC16LV54A) |
| | | | 250 | — | 10,000 | ns | XT OSC mode |
| | | | 500 | — | — | ns | XT OSC mode (PIC16LV54A) |
| | | | 250 | — | 250 | ns | HS OSC mode (04) |
| | | | 100 | — | 250 | ns | HS OSC mode (10) |
| | | | 50 | — | 250 | ns | HS OSC mode (20) |
| | | | 5.0 | — | 200 | µs | LP OSC mode |
| 2 | Tcy | Instruction Cycle Time(2) | — | 4/FOSC | — | — | |
| 3 | TosL, TosH | Clock in (OSC1) Low or High Time | 85* | — | — | ns | XT oscillator |
| | | | 20* | — | — | ns | HS oscillator |
| | | | 2.0* | — | — | µs | LP oscillator |
| 4 | TosR, TosF | Clock in (OSC1) Rise or Fall Time | — | — | 25* | ns | XT oscillator |
| | | | — | — | 25* | ns | HS oscillator |
| | | | — | — | 50* | ns | LP oscillator |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

**2:** Instruction cycle period (TCY) equals four times the input oscillator time base period.

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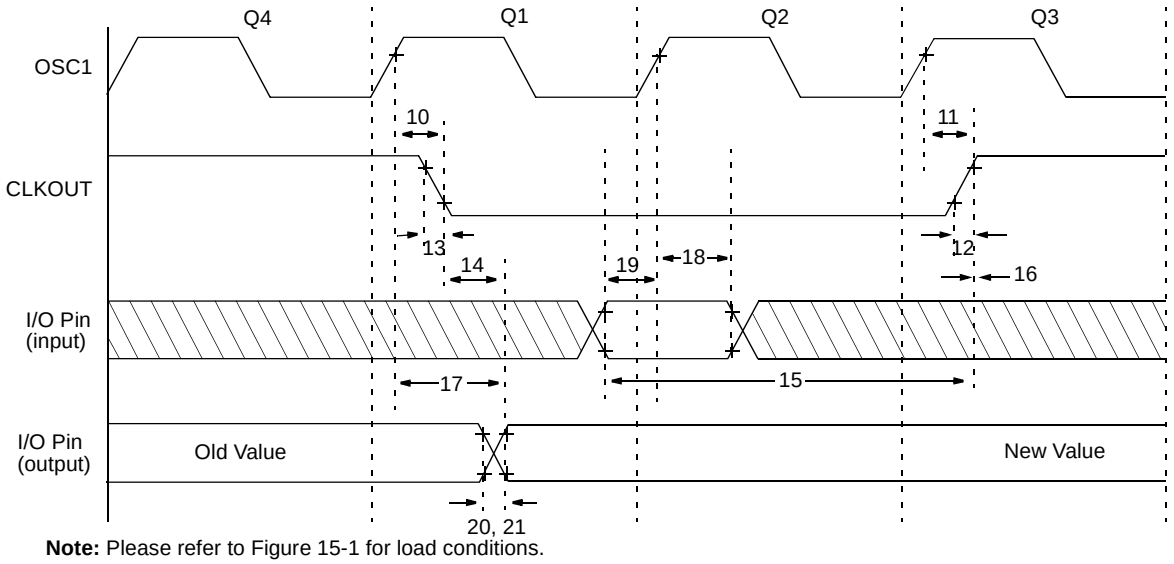
**FIGURE 15-3: CLKOUT AND I/O TIMING - PIC16C54A**




**Note:** Please refer to Figure 15-1 for load conditions.

**TABLE 15-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C54A**

| AC Characteristics | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–20°C ≤ TA ≤ +85°C for industrial - PIC16LV54A-02I<br>–40°C ≤ TA ≤ +125°C for extended | | | | | |
|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** |
| 10 | TosH2ckL | OSC1↑ to CLKOUT↓(1) | — | 15 | 30** | ns |
| 11 | TosH2ckH | OSC1↑ to CLKOUT↑(1) | — | 15 | 30** | ns |
| 12 | TckR | CLKOUT rise time(1) | — | 5.0 | 15** | ns |
| 13 | TckF | CLKOUT fall time(1) | — | 5.0 | 15** | ns |
| 14 | TckL2ioV | CLKOUT↓ to Port out valid(1) | — | — | 40** | ns |
| 15 | TioV2ckH | Port in valid before CLKOUT↑(1) | 0.25 TCY+30* | — | — | ns |
| 16 | TckH2ioI | Port in hold after CLKOUT↑(1) | 0* | — | — | ns |
| 17 | TosH2ioV | OSC1↑ (Q1 cycle) to Port out valid(2) | — | — | 100* | ns |
| 18 | TosH2ioI | OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time) | TBD | — | — | ns |
| 19 | TioV2osH | Port input valid to OSC1↑ (I/O in setup time) | TBD | — | — | ns |
| 20 | TioR | Port output rise time(2) | — | 10 | 25** | ns |
| 21 | TioF | Port output fall time(2) | — | 10 | 25** | ns |

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

**2:** Please refer to Figure 15-1 for load conditions.



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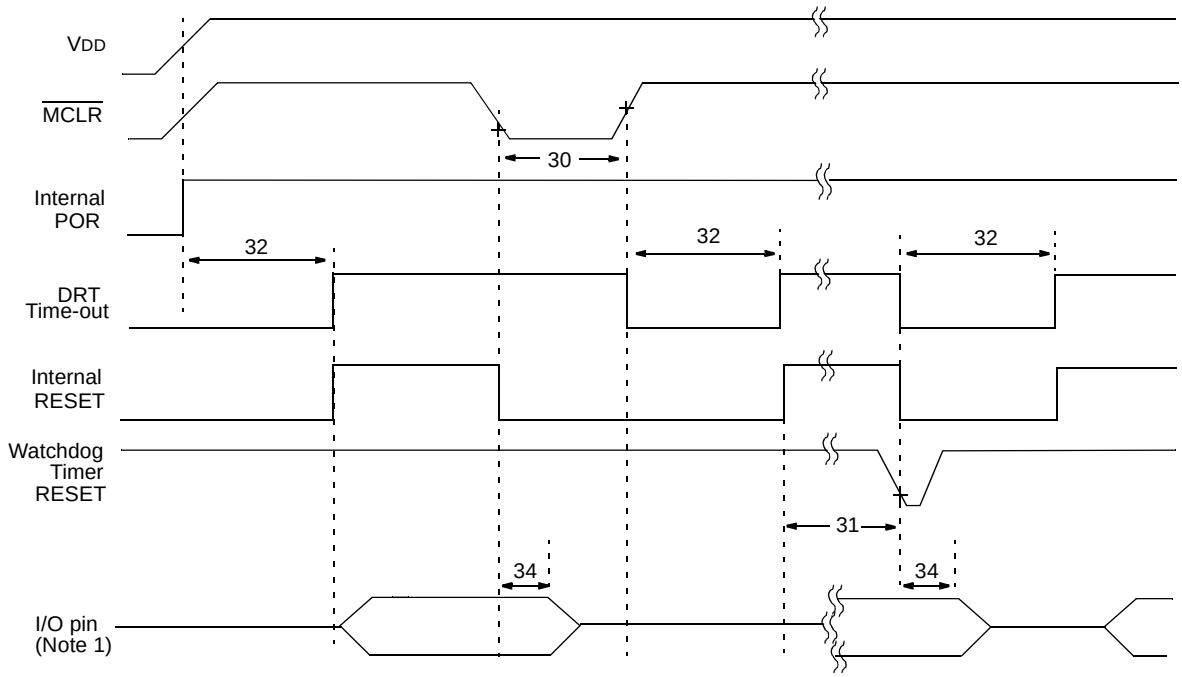
**FIGURE 15-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C54A**




**Note 1:** Please refer to Figure 15-1 for load conditions.

**TABLE 15-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C54A**

| AC Characteristics | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–20°C ≤ TA ≤ +85°C for industrial - PIC16LV54A-02I<br>–40°C ≤ TA ≤ +125°C for extended | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| 30 | TmcL | $\overline{MCLR}$ Pulse Width (low) | 100*<br>1 | —<br>— | —<br>— | ns<br>µs | VDD = 5.0V<br>VDD = 5.0V (PIC16LV54A only) |
| 31 | Twdt | Watchdog Timer Time-out Period (No Prescaler) | 9.0* | 18* | 30* | ms | VDD = 5.0V (Comm) |
| 32 | TDRT | Device Reset Timer Period | 9.0* | 18* | 30* | ms | VDD = 5.0V (Comm) |
| 34 | Tioz | I/O Hi-impedance from $\overline{MCLR}$ Low | —<br>— | —<br>— | 100*<br>1µs | ns<br>— | <br>(PIC16LV54A only) |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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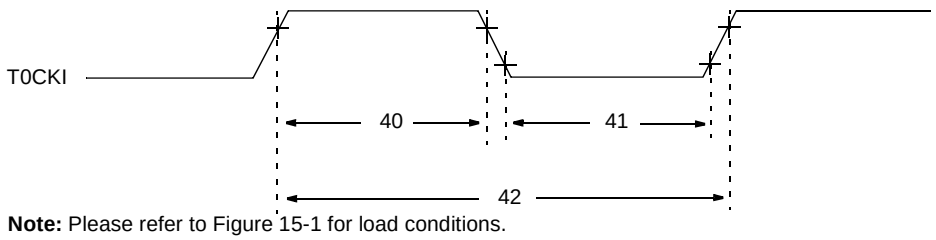
**FIGURE 15-5: TIMER0 CLOCK TIMINGS - PIC16C54A**




**Note:** Please refer to Figure 15-1 for load conditions.

**TABLE 15-4: TIMER0 CLOCK REQUIREMENTS - PIC16C54A**

| AC Characteristics | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–20°C ≤ TA ≤ +85°C for industrial - PIC16LV54A-02I<br>–40°C ≤ TA ≤ +125°C for extended |
|---|---|

| Param No. | Symbol | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 40 | Tt0H | T0CKI High Pulse Width | | | | | |
| | | - No Prescaler | 0.5 TCY + 20* | — | — | ns | |
| | | - With Prescaler | 10* | — | — | ns | |
| 41 | Tt0L | T0CKI Low Pulse Width | | | | | |
| | | - No Prescaler | 0.5 TCY + 20* | — | — | ns | |
| | | - With Prescaler | 10* | — | — | ns | |
| 42 | Tt0P | T0CKI Period | 20 or $\frac{T_{CY} + 40}{N}$* | — | — | ns | Whichever is greater.<br>N = Prescale Value (1, 2, 4,..., 256) |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.



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**NOTES:**

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## 16.0 DEVICE CHARACTERIZATION - PIC16C54A

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean – 3σ) respectively, where σ is a standard deviation, over the whole temperature range.

**FIGURE 16-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE**

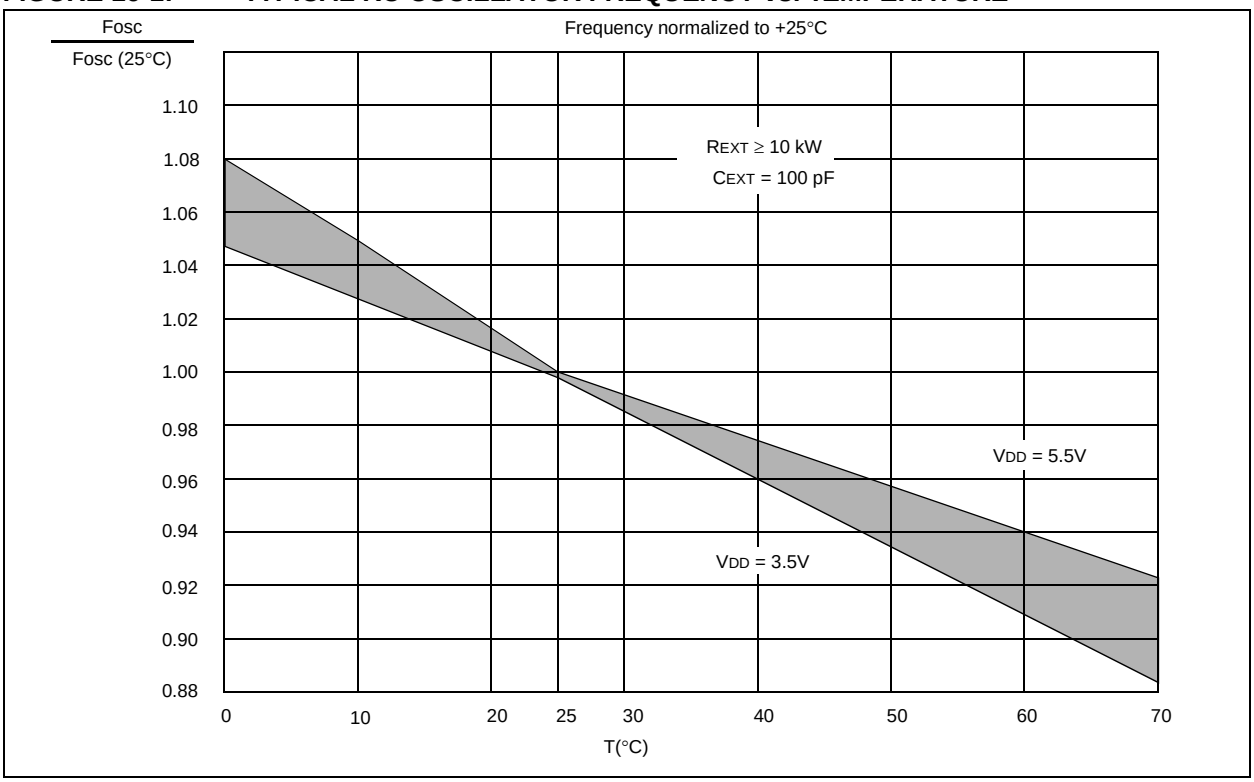


**TABLE 16-1: RC OSCILLATOR FREQUENCIES**

| CEXT | REXT | Average Fosc @ 5 V, 25°C | |
|---|---|---|---|
| 20 pF | 3.3K | 5 MHz | ± 27% |
| | 5K | 3.8 MHz | ± 21% |
| | 10K | 2.2 MHz | ± 21% |
| | 100K | 262 kHz | ± 31% |
| 100 pF | 3.3K | 1.6 MHz | ± 13% |
| | 5K | 1.2 MHz | ± 13% |
| | 10K | 684 kHz | ± 18% |
| | 100K | 71 kHz | ± 25% |
| 300 pF | 3.3K | 660 kHz | ± 10% |
| | 5.0K | 484 kHz | ± 14% |
| | 10K | 267 kHz | ± 15% |
| | 100K | 29 kHz | ± 19% |

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ±3 standard deviation from average value for VDD = 5V.



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**FIGURE 16-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 20 pF, 25°C**

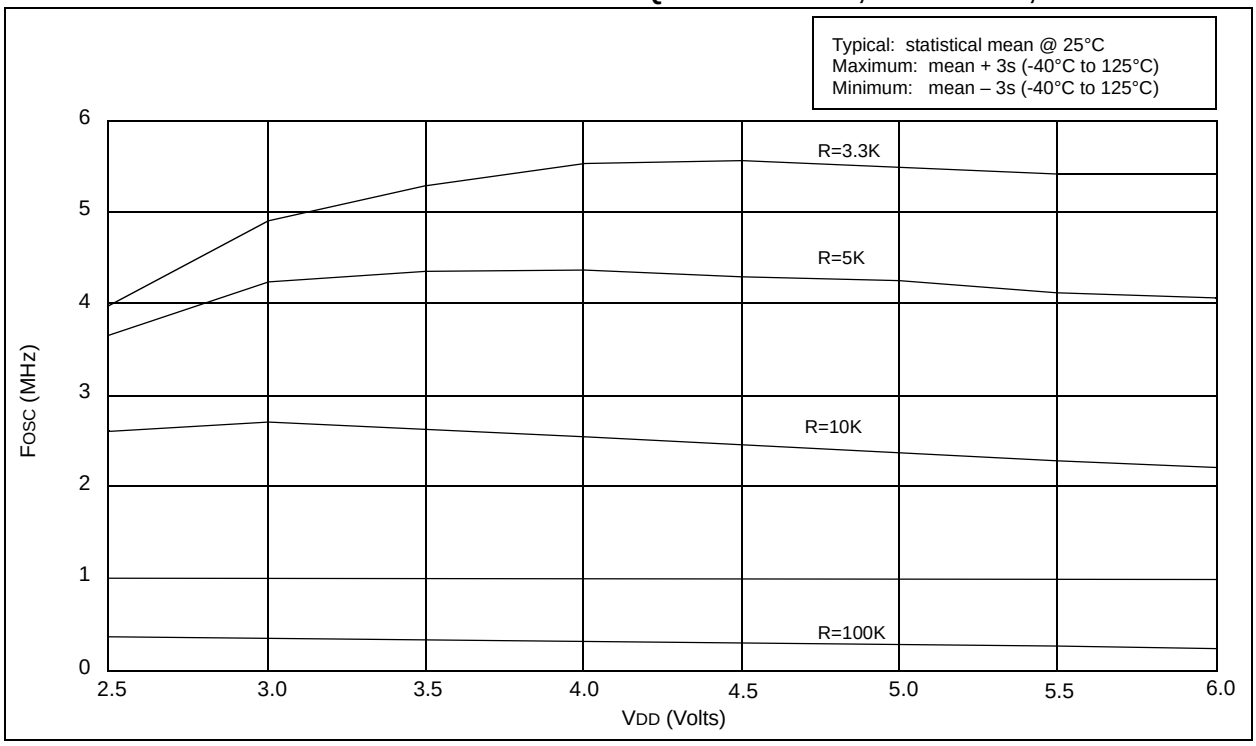


**FIGURE 16-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 100 pF, 25°C**

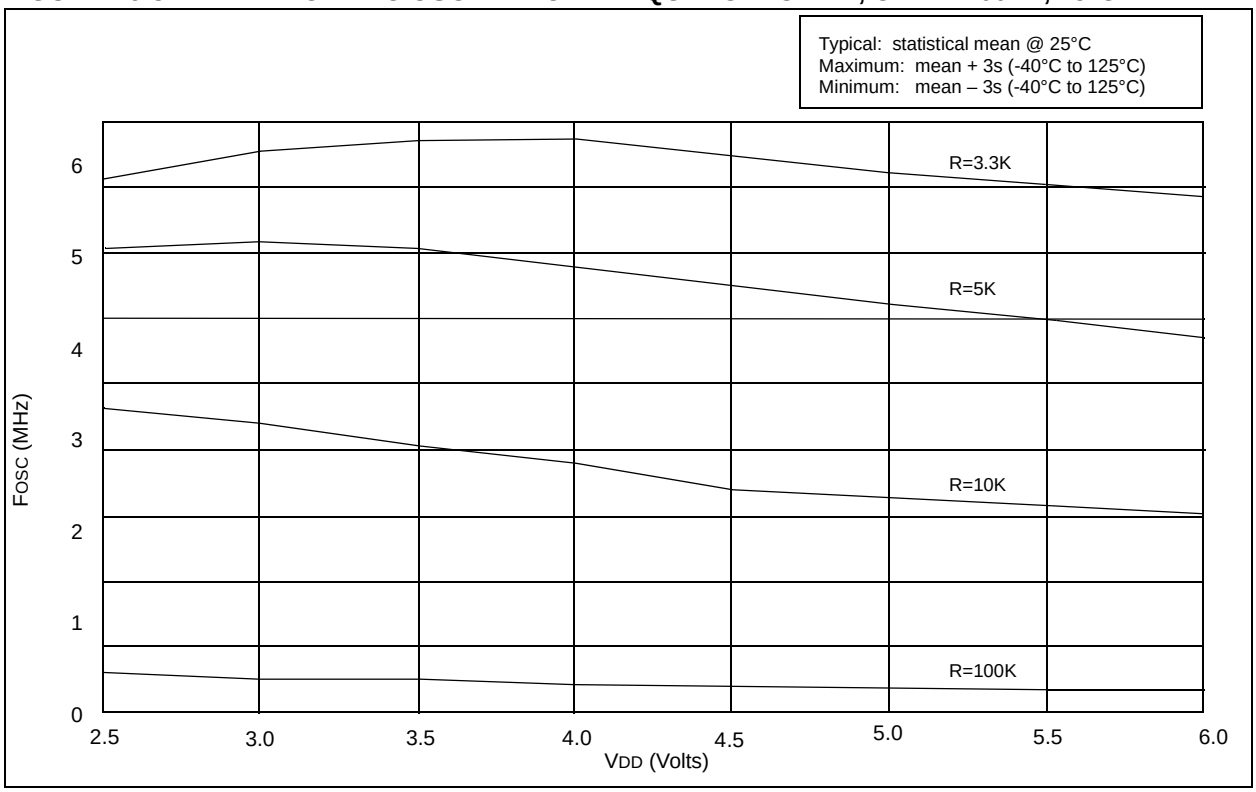


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**FIGURE 16-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 300 pF, 25°C**

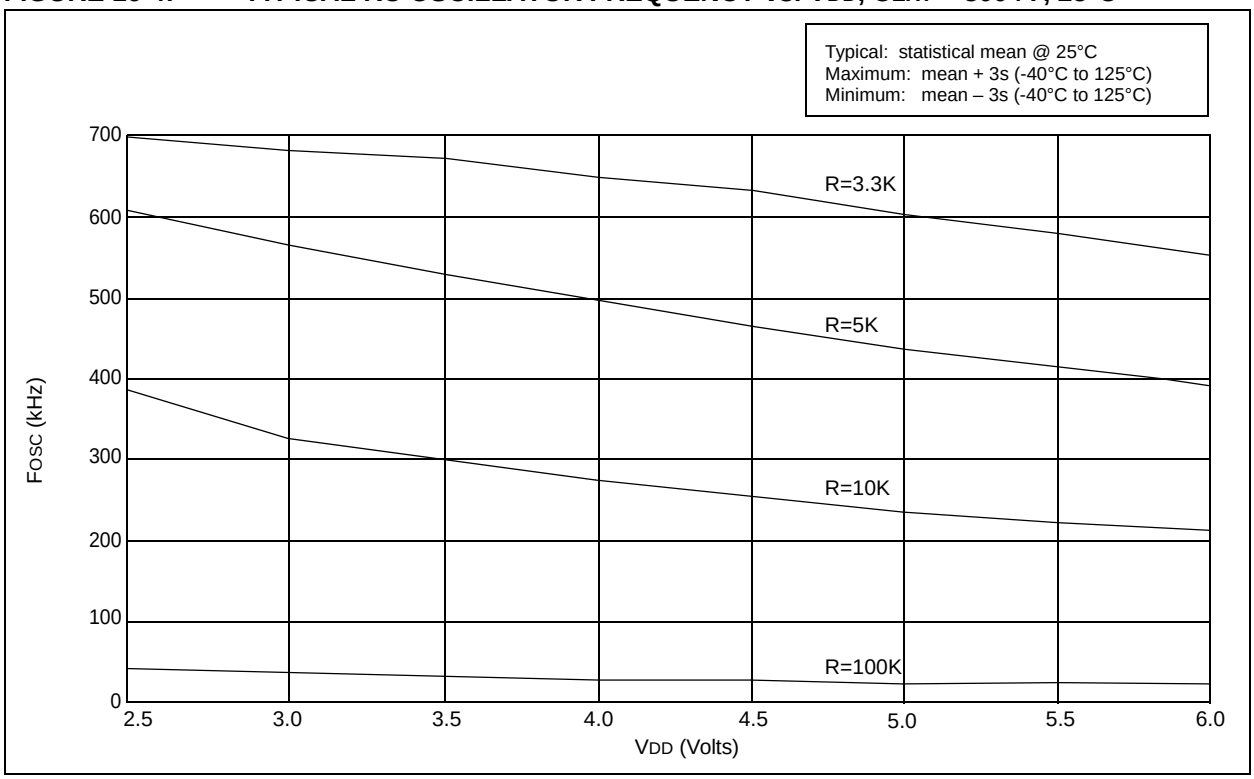




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**FIGURE 16-5: TYPICAL IPD VS. VDD, WATCHDOG DISABLED (25°C)**

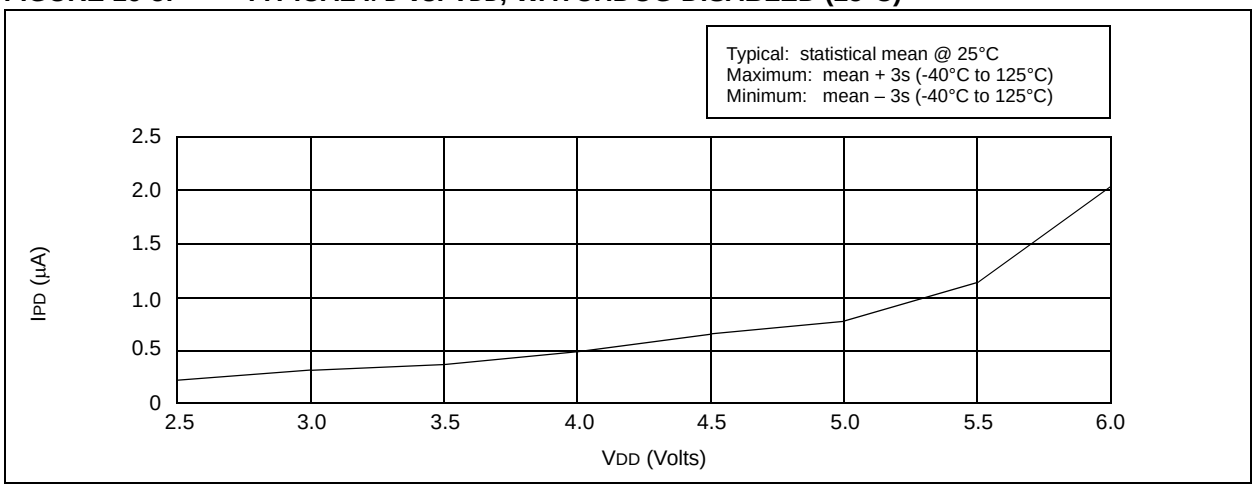


**FIGURE 16-6: TYPICAL IPD VS. VDD, WATCHDOG ENABLED (25°C)**

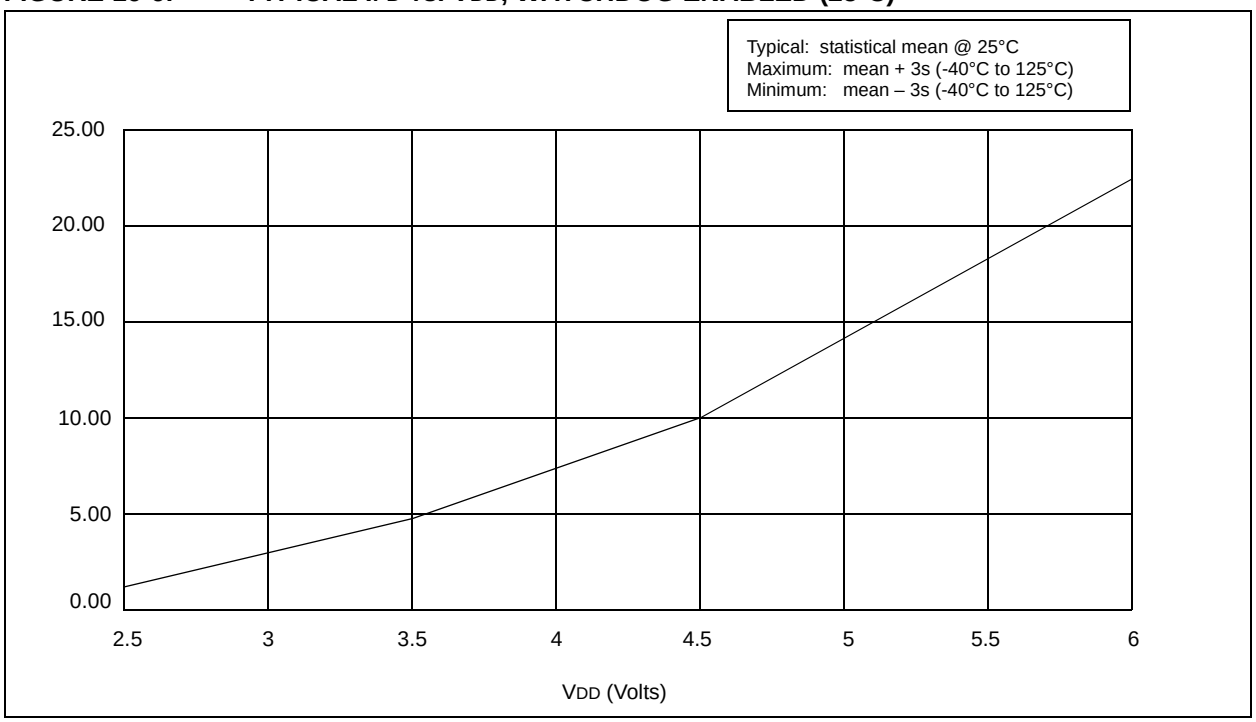


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**FIGURE 16-7: VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS - VDD**

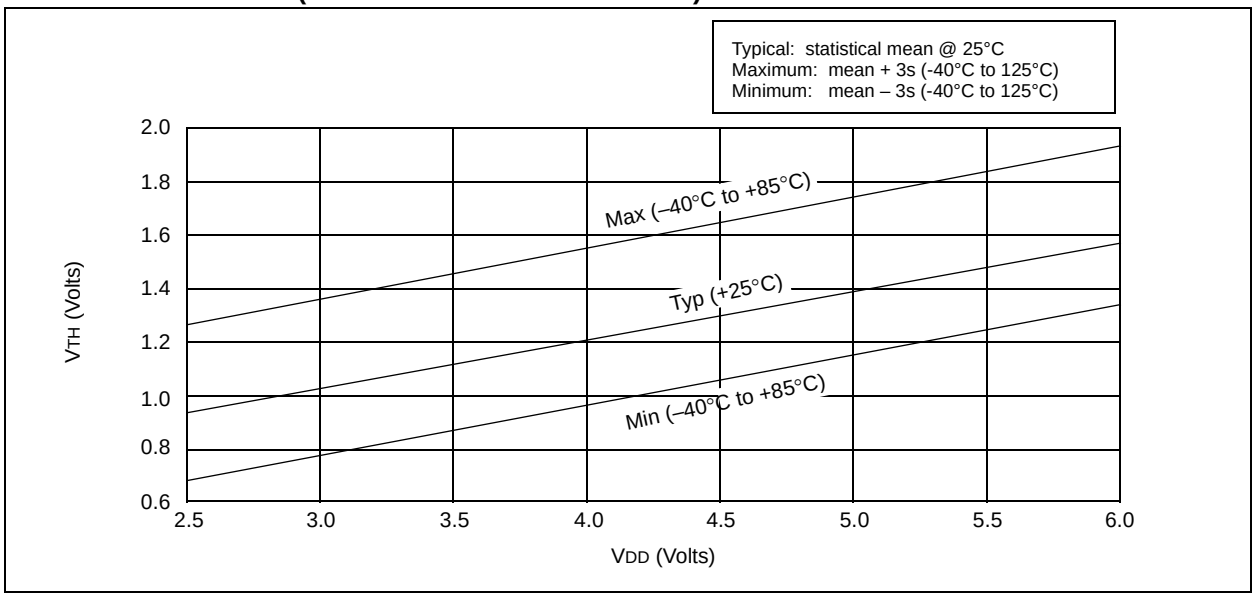


**FIGURE 16-8: VTH (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT, HS, AND LP MODES) vs. VDD**

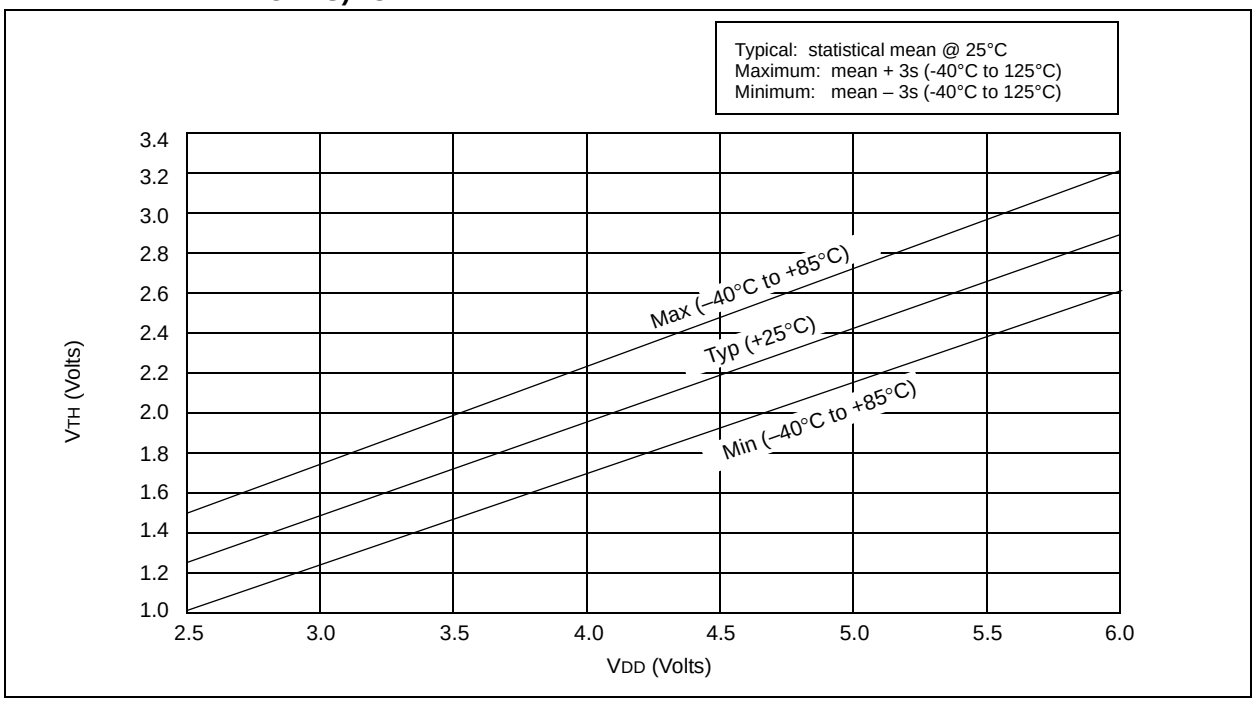




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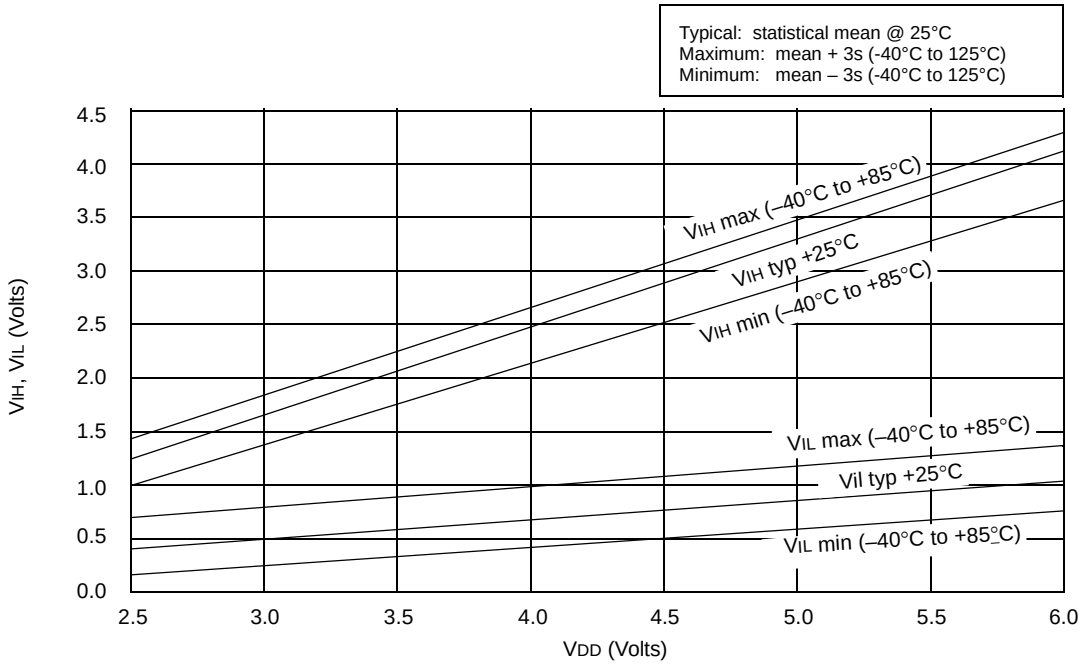
**FIGURE 16-9: VIH, VIL OF $\overline{\text{MCLR}}$, T0CKI AND OSC1 (IN RC MODE) vs. VDD**




**Note:** These input pins have Schmitt Trigger input buffers.

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**FIGURE 16-10: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 20 pF, 25°C)**

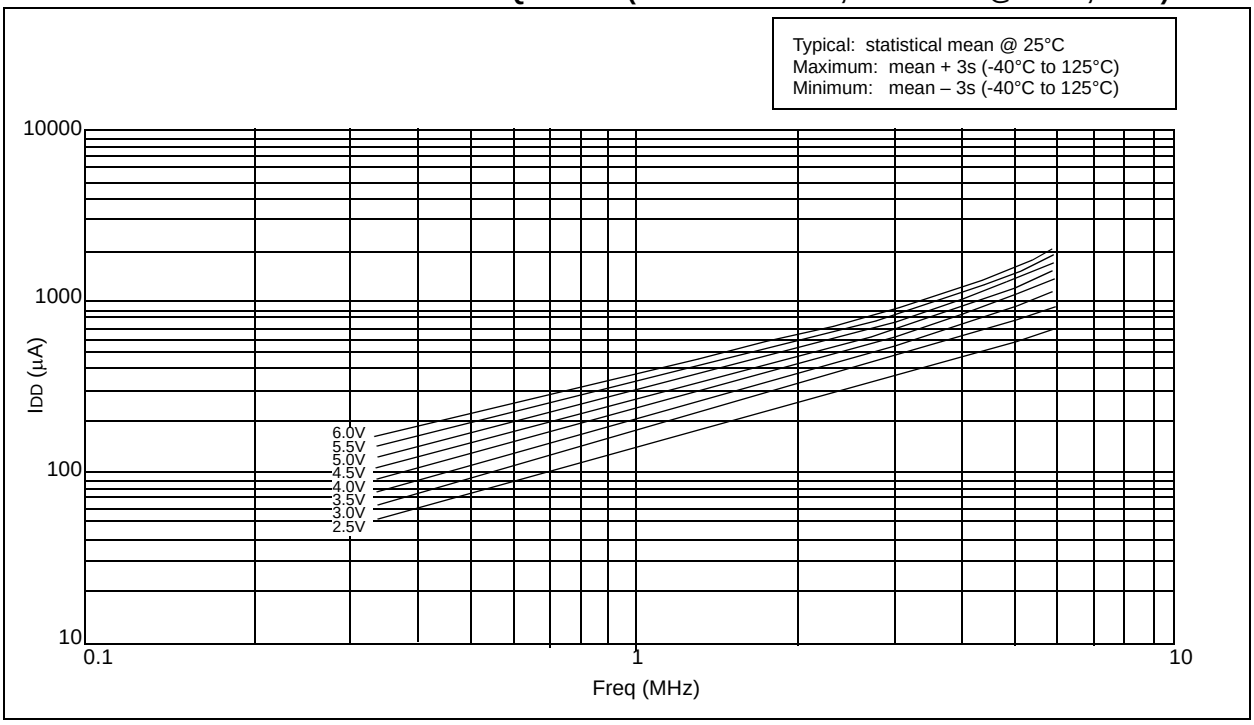


**FIGURE 16-11: MAXIMUM IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 20 pF, –40°C to +85°C)**

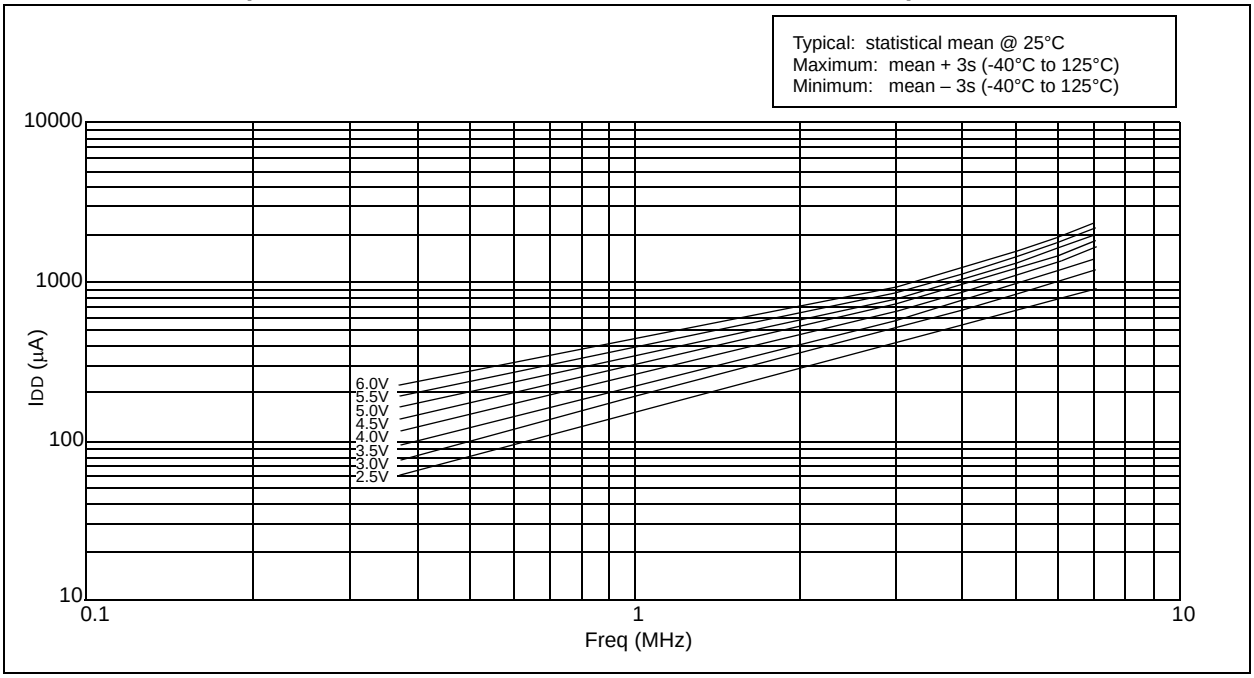




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**FIGURE 16-12: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 100 pF, 25°C)**

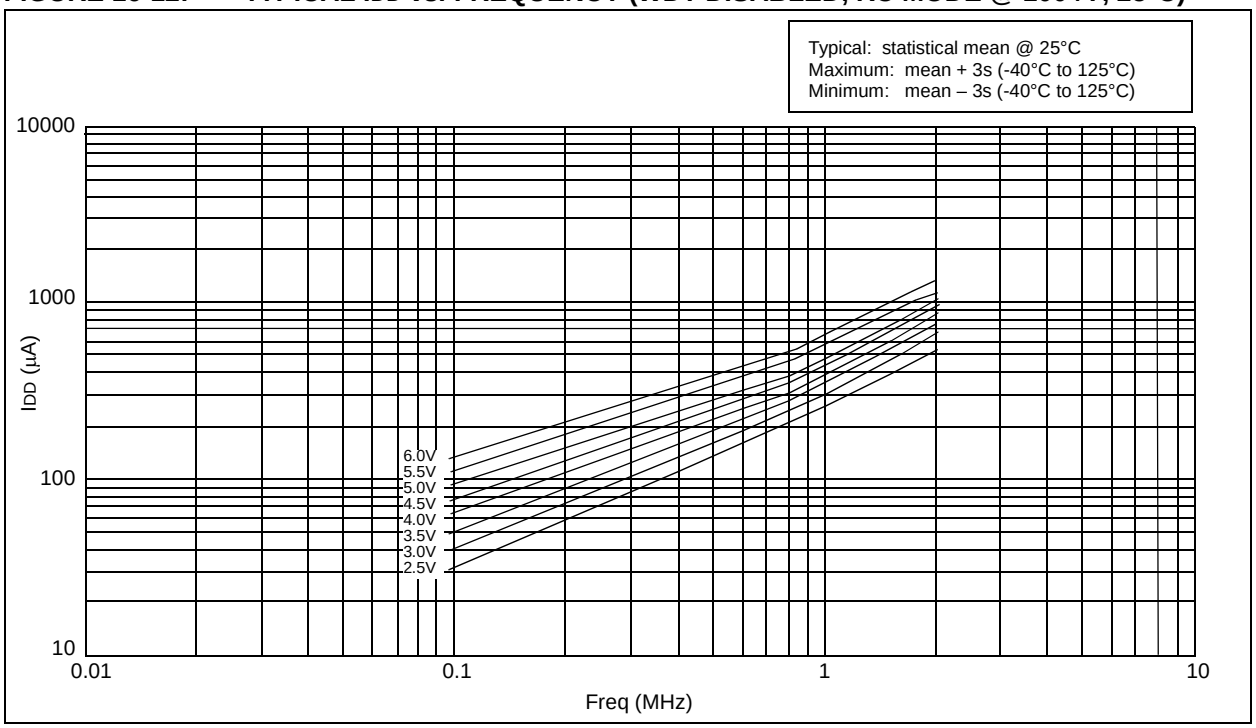


**FIGURE 16-13: MAXIMUM IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 100 pF, –40°C to +85°C)**

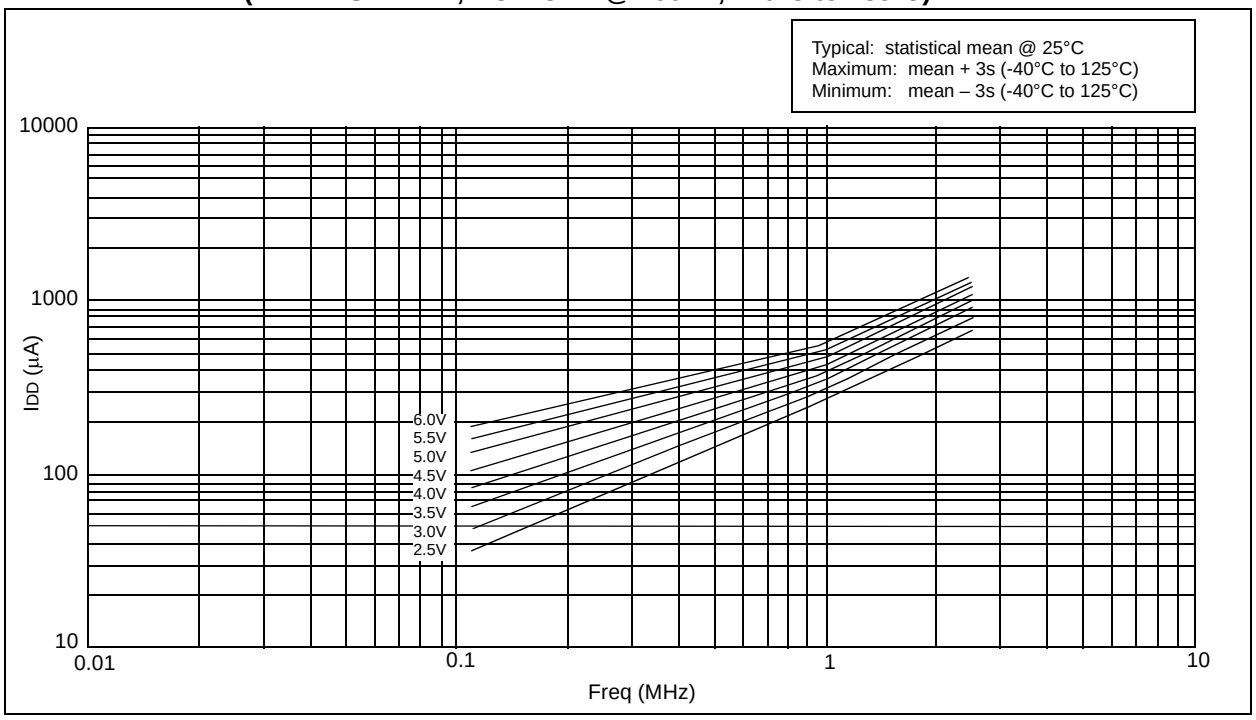


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**FIGURE 16-14: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 300 pF, 25°C)**

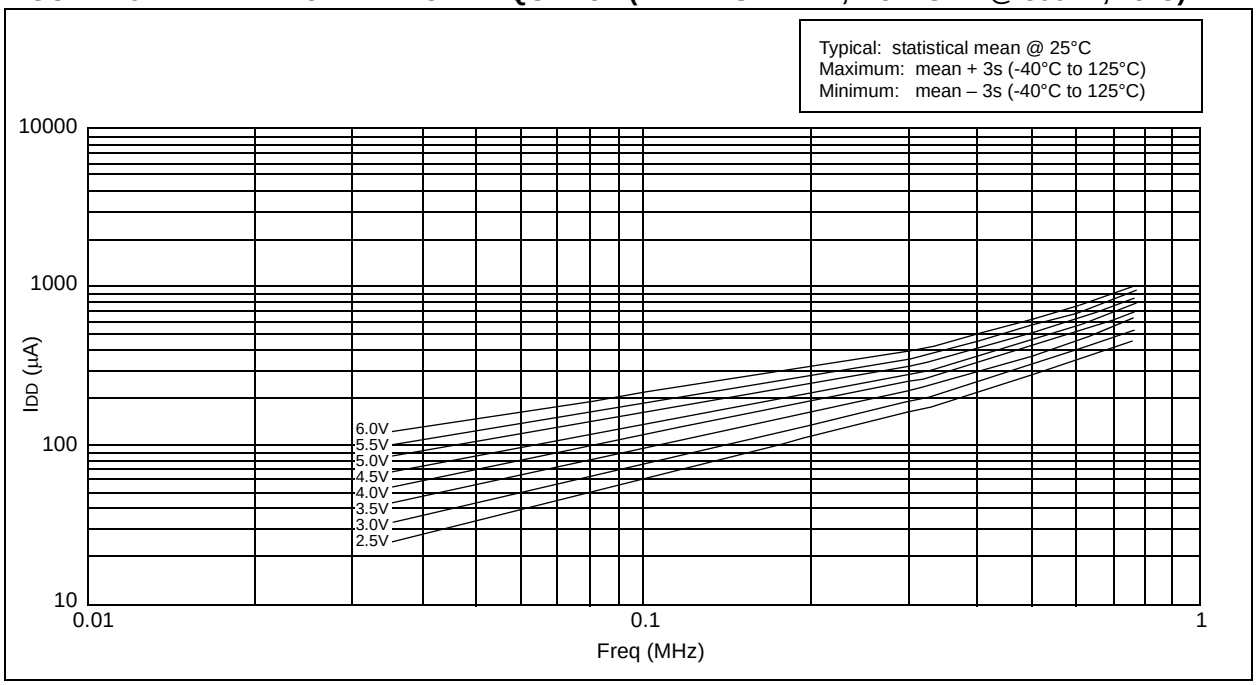


**FIGURE 16-15: MAXIMUM IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 300 pF, –40°C to +85°C)**

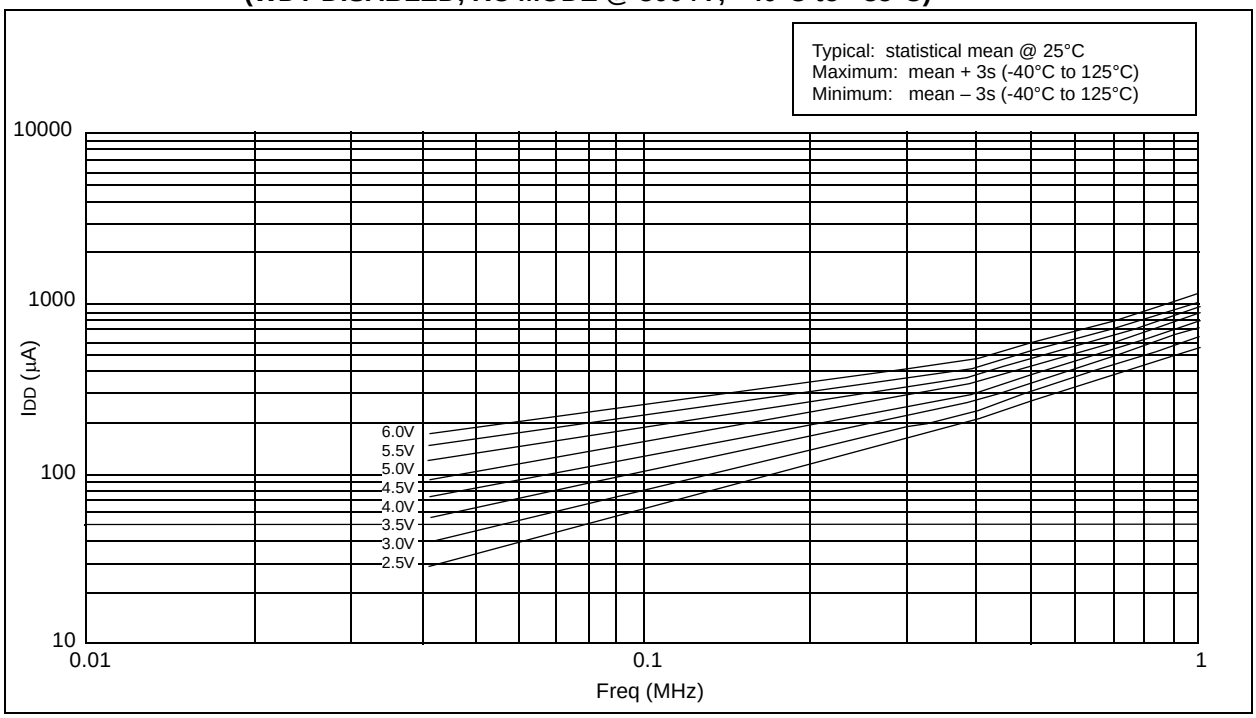




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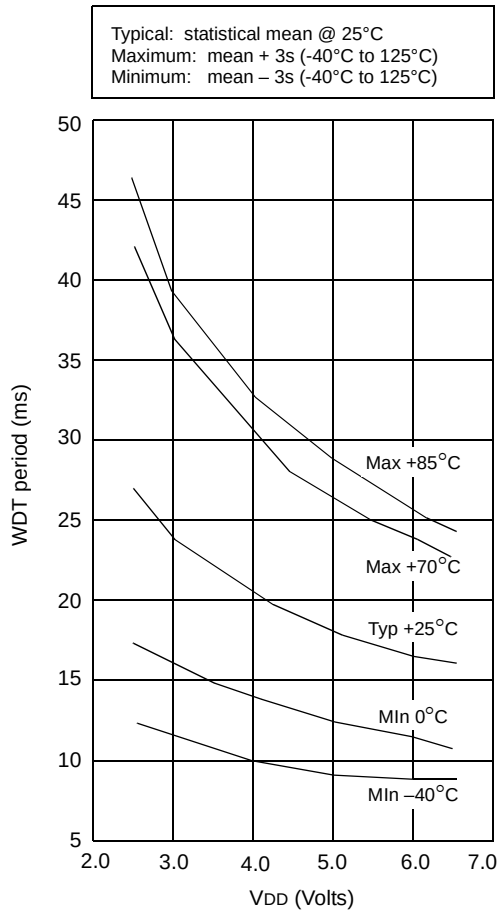
**FIGURE 16-16: WDT TIMER TIME-OUT PERIOD vs. $V_{DD}$ (1)**




**Note 1:** Prescaler set to 1:1.

**FIGURE 16-17: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR vs. $V_{DD}$**

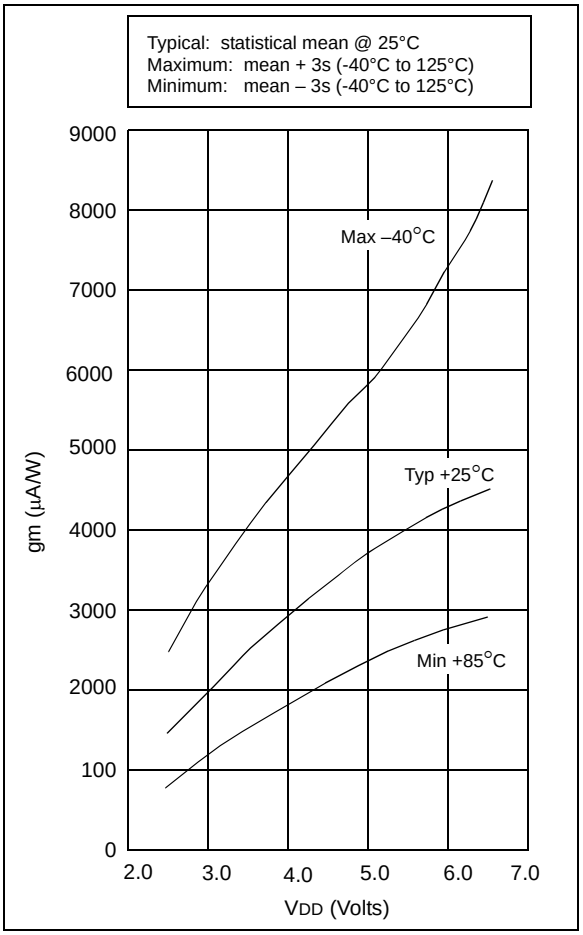



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**FIGURE 16-18: TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. VDD**

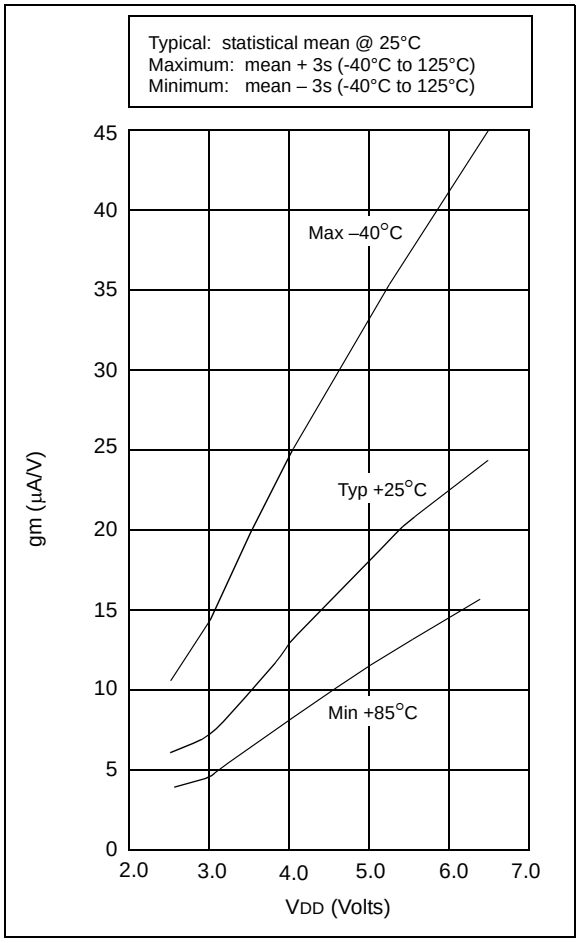


**FIGURE 16-19: TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD**

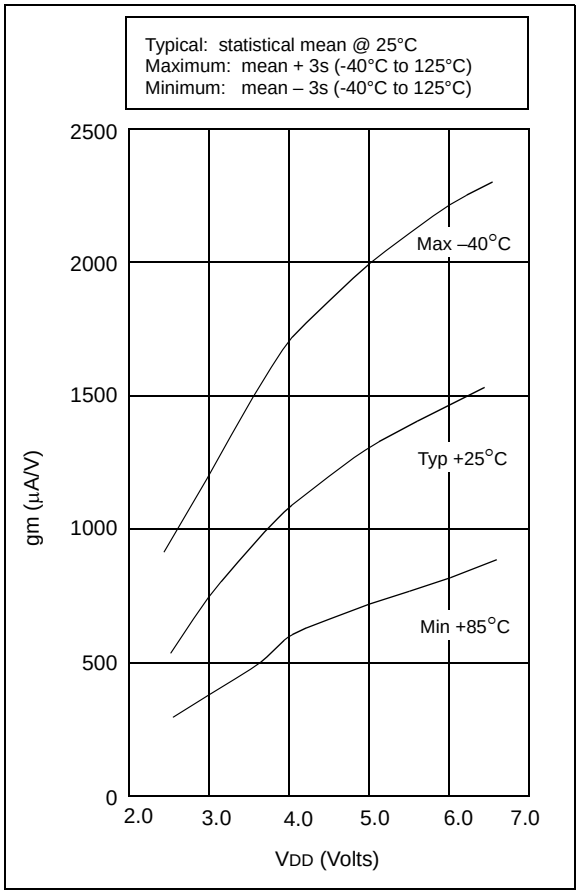




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**FIGURE 16-20: PORTA, B AND C $I_{OH}$ vs. $V_{OH}$, $V_{DD}$ = 3V**

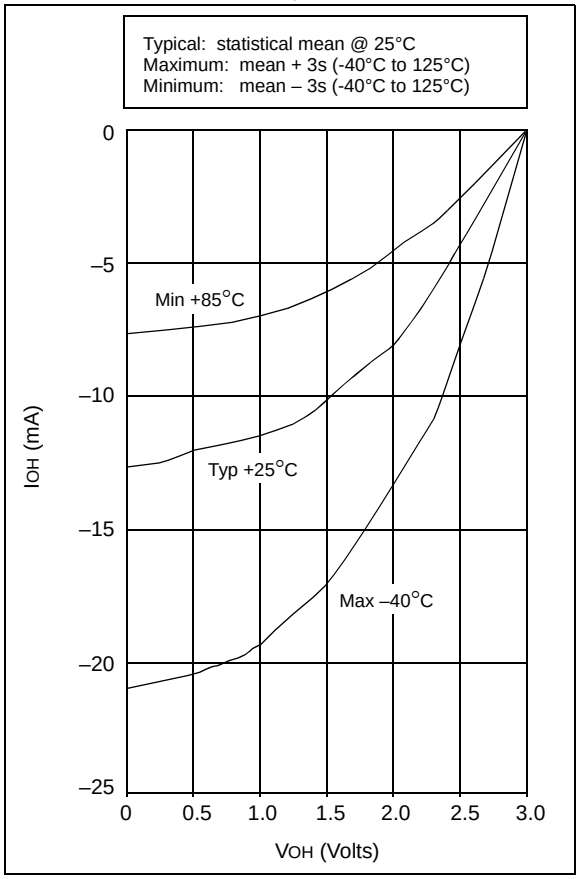


**FIGURE 16-21: PORTA, B AND C $I_{OH}$ vs. $V_{OH}$, $V_{DD}$ = 5V**

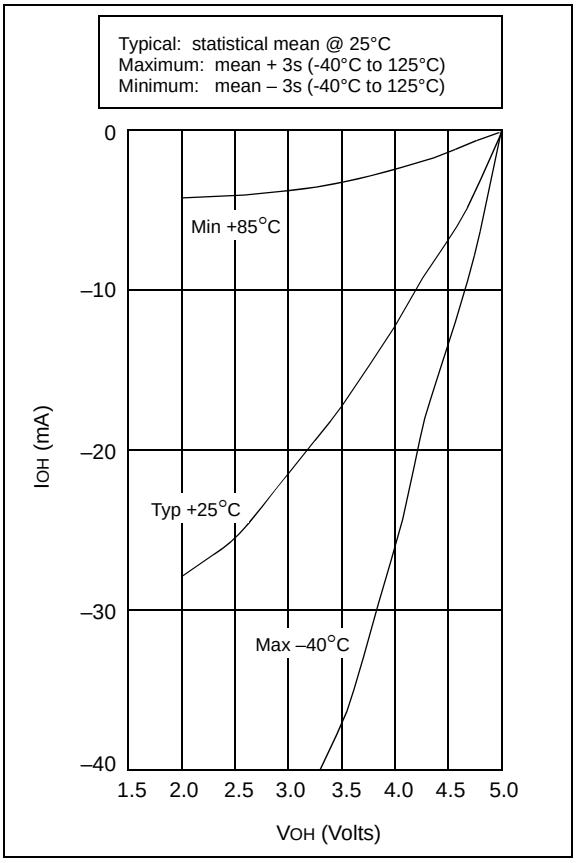


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**FIGURE 16-22: PORTA, B AND C IOL vs. VOL, VDD = 3V**

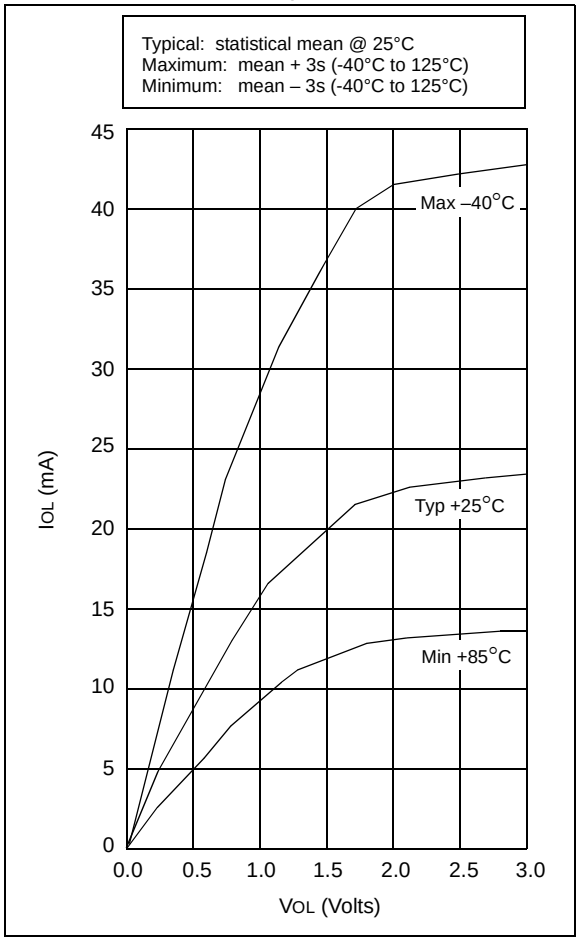


**FIGURE 16-23: PORTA, B AND C IOL vs. VOL, VDD = 5V**

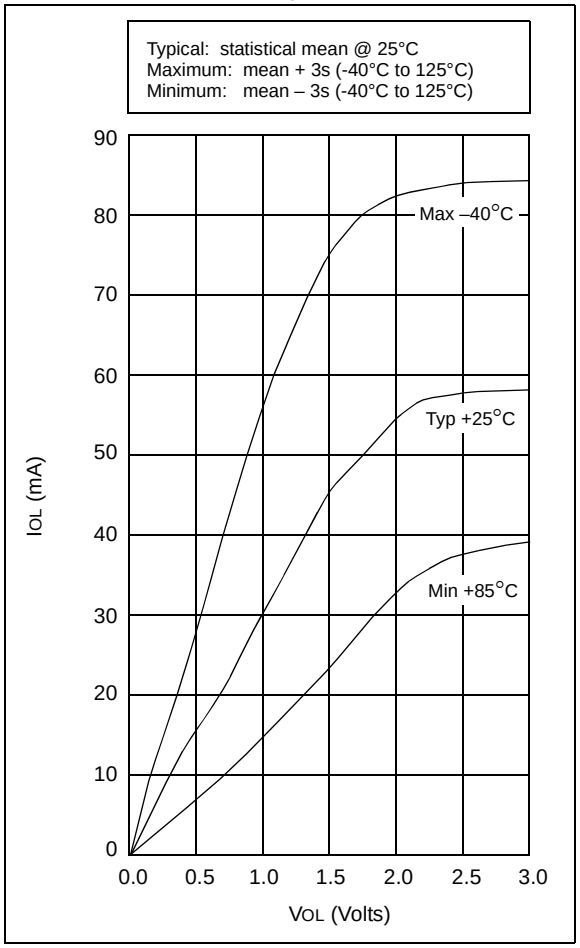


**TABLE 16-2: INPUT CAPACITANCE FOR PIC16C54A/C58A**

| Pin | Typical Capacitance (pF) | |
|---|---|---|
| | 18L PDIP | 18L SOIC |
| RA port | 5.0 | 4.3 |
| RB port | 5.0 | 4.3 |
| $\overline{MCLR}$ | 17.0 | 17.0 |
| OSC1 | 4.0 | 3.5 |
| OSC2/CLKOUT | 4.3 | 3.5 |
| T0CKI | 3.2 | 2.8 |

All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.



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**NOTES:**

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## 17.0 ELECTRICAL CHARACTERISTICS - PIC16LC54A

**Absolute Maximum Ratings(†)**

Ambient temperature under bias ..... –55°C to +125°C
Storage temperature ..... –65°C to +150°C
Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... 0 to +7.5V
Voltage on $\overline{MCLR}$ with respect to $V_{SS}$ ..... 0 to +14V
Voltage on all other pins with respect to $V_{SS}$ ..... –0.6V to ($V_{DD}$ + 0.6V)
Total power dissipation(1) ..... 800 mW
Max. current out of $V_{SS}$ pin ..... 150 mA
Max. current into $V_{DD}$ pin ..... 100 mA
Max. current into an input pin (T0CKI only) ..... ±500 µA
Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{DD}$) ..... ±20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{DD}$) ..... ±20 mA
Max. output current sunk by any I/O pin ..... 25 mA
Max. output current sourced by any I/O pin ..... 20 mA
Max. output current sourced by a single I/O (Port A, B or C) ..... 50 mA
Max. output current sunk by a single I/O (Port A, B or C) ..... 50 mA

**Note 1:** Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.



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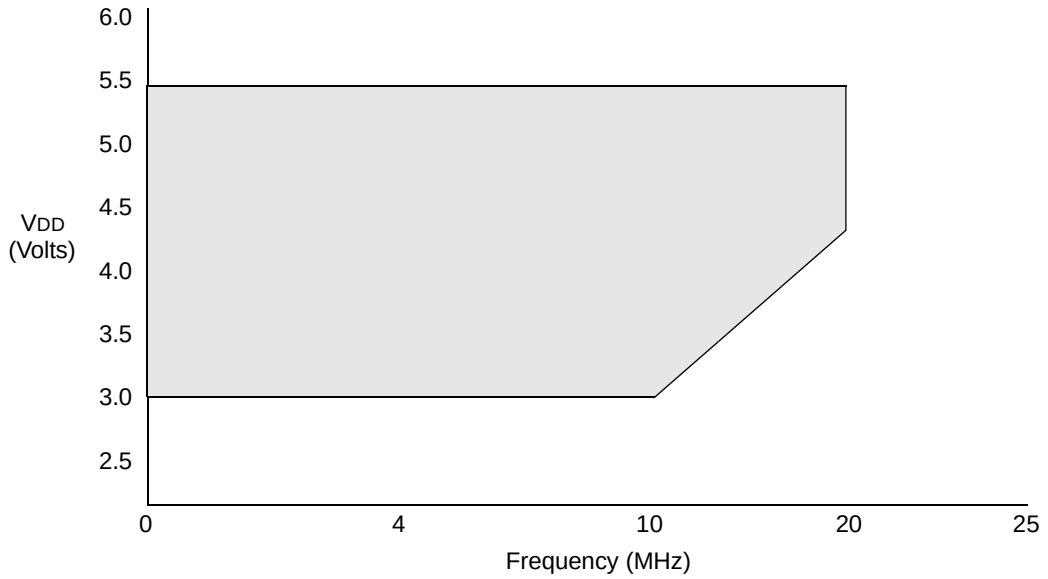
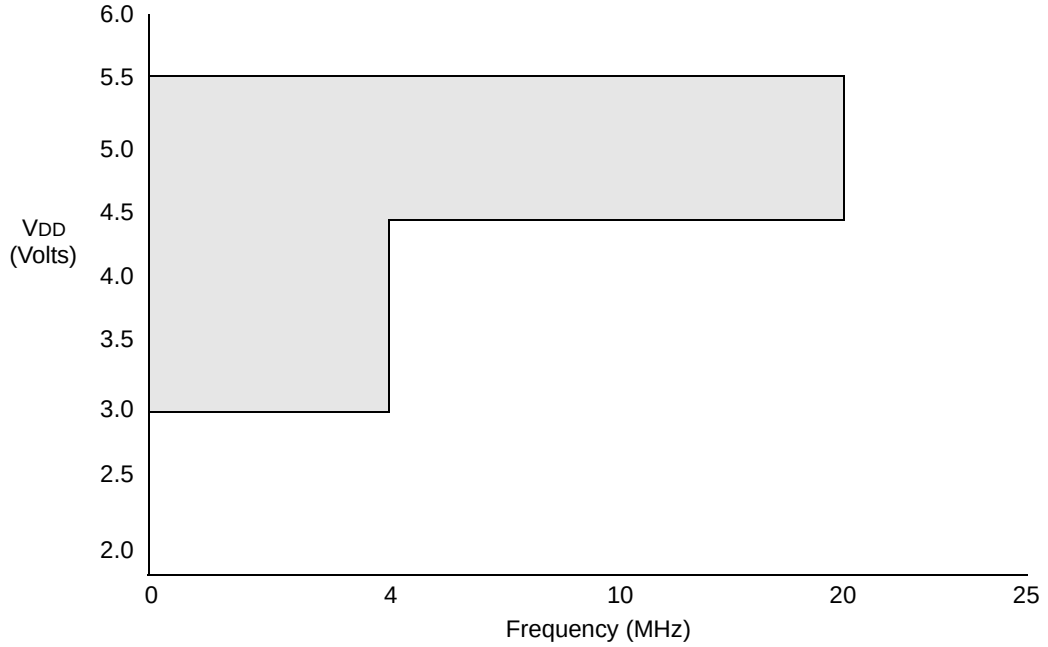
**FIGURE 17-1: PIC16C54C/55A/56A/57C/58B-04, 20 VOLTAGE-FREQUENCY GRAPH, $0°C \leq T_A \leq +70°C$ (COMMERCIAL TEMPS)**




**Note 1:** The shaded region indicates the permissible combinations of voltage and frequency.

**2:** The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

**FIGURE 17-2: PIC16C54C/55A/56A/57C/58B-04, 20 VOLTAGE-FREQUENCY GRAPH, $-40°C \leq T_A < 0°C$, $+70°C < T_A \leq +125°C$ (OUTSIDE OF COMMERCIAL TEMPS)**




**Note 1:** The shaded region indicates the permissible combinations of voltage and frequency.

**2:** The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

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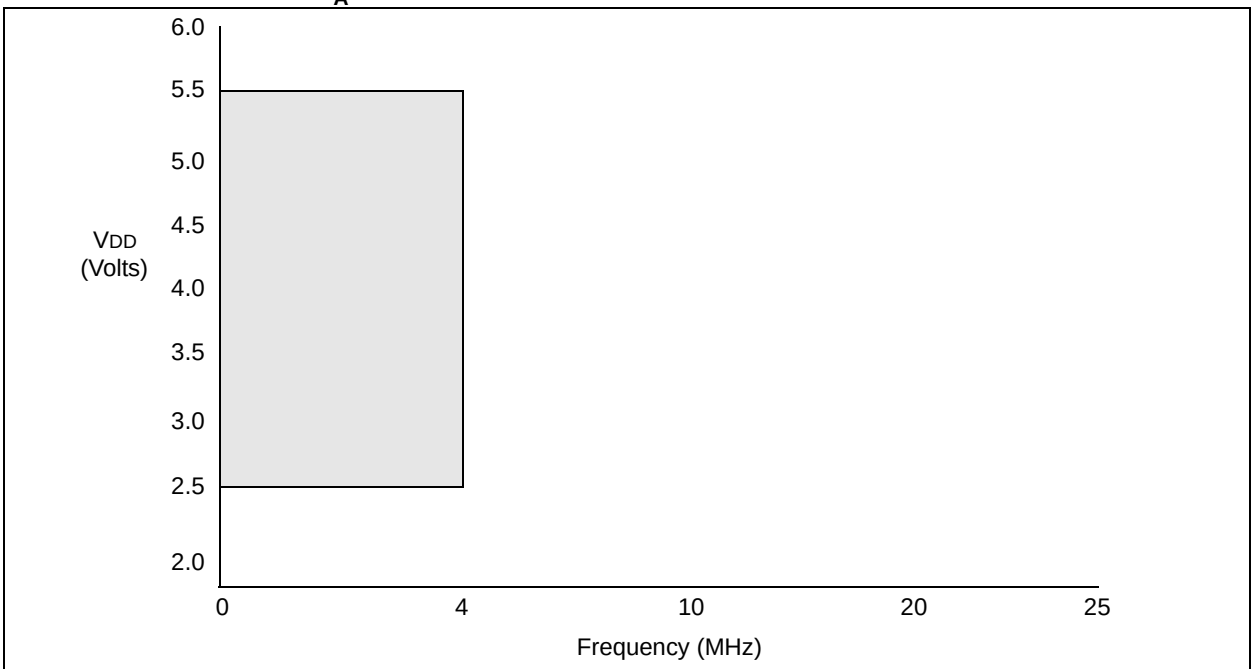
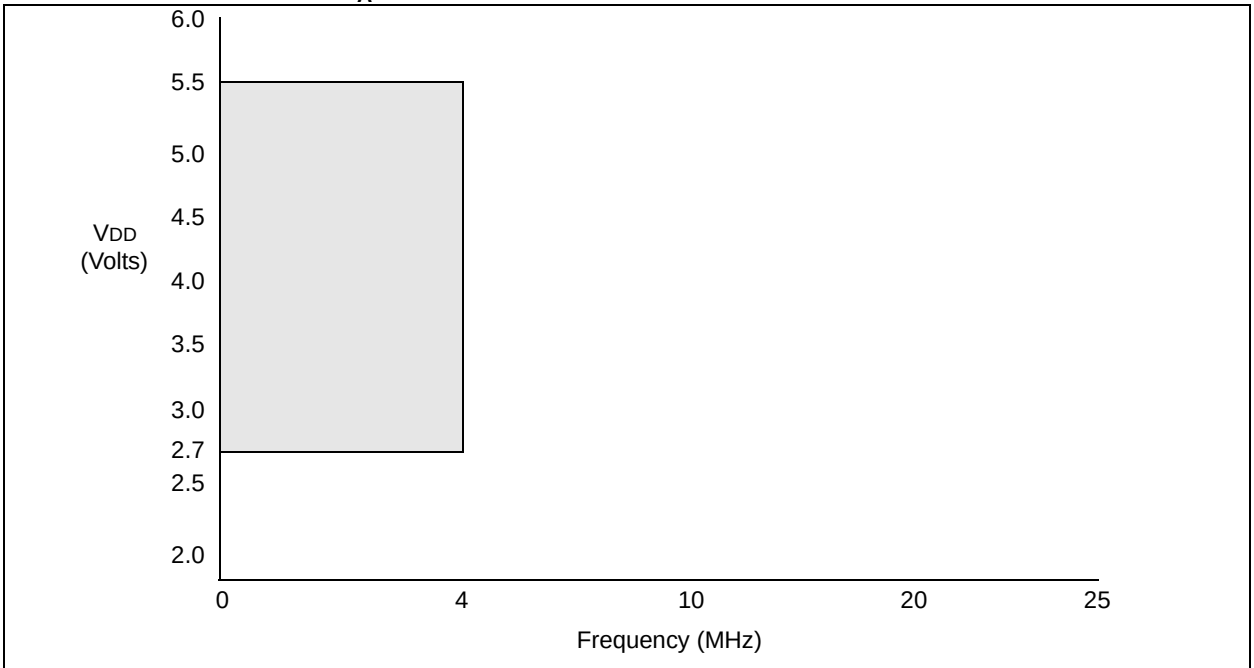
**FIGURE 17-3: PIC16LC54C/55A/56A/57C/58B VOLTAGE-FREQUENCY GRAPH, $0°C \leq T_A \leq +85°C$**




**Note 1:** The shaded region indicates the permissible combinations of voltage and frequency.

**2:** The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

**FIGURE 17-4: PIC16LC54C/55A/56A/57C/58B VOLTAGE-FREQUENCY GRAPH, $-40°C \leq T_A \leq 0°C$**




**Note 1:** The shaded region indicates the permissible combinations of voltage and frequency.

**2:** The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.



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## 17.1 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial)
## PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial)
## PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial)
## PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **PIC16LC5X**<br>**PIC16LCR5X**<br>(Commercial, Industrial) | | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial | | | | |
| **PIC16C5X**<br>**PIC16CR5X**<br>(Commercial, Industrial) | | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial | | | | |
| **Param No.** | **Symbol** | **Characteristic/Device** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| | VDD | **Supply Voltage** | | | | | |
| D001 | | PIC16LC5X | 2.5<br>2.7<br>2.5 | —<br>—<br>— | 5.5<br>5.5<br>5.5 | V<br>V<br>V | –40°C ≤ TA ≤ + 85°C, 16LCR5X<br>–40°C ≤ TA ≤ 0°C, 16LC5X<br>0°C ≤ TA ≤ + 85°C 16LC5X |
| D001A | | PIC16C5X | 3.0<br>4.5 | —<br>— | 5.5<br>5.5 | V<br>V | RC, XT, LP and HS mode<br>from 0 - 10 MHz<br>from 10 - 20 MHz |
| D002 | VDR | **RAM Data Retention Voltage(1)** | — | 1.5* | — | V | Device in SLEEP mode |
| D003 | VPOR | **VDD Start Voltage** to ensure Power-on Reset | — | VSS | — | V | See Section 5.1 for details on Power-on Reset |
| D004 | SVDD | **VDD Rise Rate** to ensure Power-on Reset | 0.05* | — | — | V/ms | See Section 5.1 for details on Power-on Reset |

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

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## 17.1 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial) PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial) PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial) PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **PIC16LC5X**<br>**PIC16LCR5X**<br>(Commercial, Industrial) | | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial | | | | |
| **PIC16C5X**<br>**PIC16CR5X**<br>(Commercial, Industrial) | | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial | | | | |
| **Param No.** | **Symbol** | **Characteristic/Device** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| | IDD | **Supply Current(2,3)** | | | | | |
| D010 | | PIC16LC5X | — | 0.5 | 2.4 | mA | FOSC = 4.0 MHz, VDD = 5.5V, XT and RC modes |
| | | | — | 11 | 27 | µA | FOSC = 32 kHz, VDD = 2.5V, LP mode, Commercial |
| | | | — | 14 | 35 | µA | FOSC = 32 kHz, VDD = 2.5V, LP mode, Industrial |
| D010A | | PIC16C5X | — | 1.8 | 2.4 | mA | FOSC = 4 MHz, VDD = 5.5V, XT and RC modes |
| | | | — | 2.6 | 3.6* | mA | |
| | | | — | 4.5 | 16 | mA | FOSC = 10 MHz, VDD = 3.0V, HS mode |
| | | | — | 14 | 32 | µA | FOSC = 20 MHz, VDD = 5.5V, HS mode |
| | | | — | 17 | 40 | µA | FOSC = 32 kHz, VDD = 3.0V, LP mode, Commercial |
| | | | | | | | FOSC = 32 kHz, VDD = 3.0V, LP mode, Industrial |

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.



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## 17.1 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial) PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial) PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial) PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **PIC16LC5X**<br>**PIC16LCR5X**<br>(Commercial, Industrial) | | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial | | | | |
| **PIC16C5X**<br>**PIC16CR5X**<br>(Commercial, Industrial) | | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial | | | | |
| **Param No.** | **Symbol** | **Characteristic/Device** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| | IPD | **Power-down Current(2)** | | | | | |
| D020 | | PIC16LC5X | — | 0.25 | 2 | µA | VDD = 2.5V, WDT disabled, Commercial |
| | | | — | 0.25 | 3 | µA | VDD = 2.5V, WDT disabled, Industrial |
| | | | — | 1 | 5 | µA | VDD = 2.5V, WDT enabled, Commercial |
| | | | — | 1.25 | 8 | µA | VDD = 2.5V, WDT enabled, Industrial |
| D020A | | PIC16C5X | — | 0.25 | 4.0 | µA | VDD = 3.0V, WDT disabled, Commercial |
| | | | — | 0.25 | 5.0 | µA | VDD = 3.0V, WDT disabled, Industrial |
| | | | — | 1.8 | 7.0* | µA | VDD = 5.5V, WDT disabled, Commercial |
| | | | — | 2.0 | 8.0* | µA | VDD = 5.5V, WDT disabled, Industrial |
| | | | — | 4 | 12* | µA | VDD = 3.0V, WDT enabled, Commercial |
| | | | — | 4 | 14* | µA | VDD = 3.0V, WDT enabled, Industrial |
| | | | — | 9.8 | 27* | µA | VDD = 5.5V, WDT enabled, Commercial |
| | | | — | 12 | 30* | µA | VDD = 5.5V, WDT enabled, Industrial |

Legend: Rows with standard voltage device data only are shaded for improved readability.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

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## 17.2 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04E, 20E (Extended) PIC16CR54C/CR56A/CR57C/CR58B-04E, 20E (Extended)

| PIC16C54C/C55A/C56A/C57C/C58B-04E, 20E<br>PIC16CR54C/CR56A/CR57C/CR58B-04E, 20E<br>(Extended) | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature –40°C ≤ TA ≤ +125°C for extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D001 | VDD | **Supply Voltage** | | | | | RC, XT, LP, and HS mode |
| | | | 3.0 | — | 5.5 | V | from 0 - 10 MHz |
| | | | 4.5 | — | 5.5 | V | from 10 - 20 MHz |
| D002 | VDR | **RAM Data Retention Voltage(1)** | — | 1.5* | — | V | Device in SLEEP mode |
| D003 | VPOR | **VDD start voltage** to ensure Power-on Reset | — | Vss | — | V | See Section 5.1 for details on Power-on Reset |
| D004 | SVDD | **VDD rise rate** to ensure Power-on Reset | 0.05* | — | — | V/ms | See Section 5.1 for details on Power-on Reset |
| D010 | IDD | **Supply Current(2)** | | | | | |
| | | XT and RC(3) modes | — | 1.8 | 3.3 | mA | FOSC = 4.0 MHz, VDD = 5.5V |
| | | HS mode | — | 9.0 | 20 | mA | FOSC = 20 MHz, VDD = 5.5V |
| D020 | IPD | **Power-down Current(2)** | — | 0.3 | 17 | µA | VDD = 3.0V, WDT disabled |
| | | | — | 10 | 50* | µA | VDD = 4.5V, WDT disabled |
| | | | — | 12 | 60* | µA | VDD = 5.5V, WDT disabled |
| | | | — | 4.8 | 31* | µA | VDD = 3.0V, WDT enabled |
| | | | — | 18 | 68* | µA | VDD = 4.5V, WDT enabled |
| | | | — | 26 | 90* | µA | VDD = 5.5V, WDT enabled |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only, and are not tested.

**Note 1:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.

**3:** Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.



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## 17.3 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial, Extended) PIC16LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial) PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial, Extended) PIC16LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–40°C ≤ TA ≤ +125°C for extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D030 | VIL | **Input Low Voltage** | | | | | |
| | | I/O Ports | VSS | — | 0.8 V | V | 4.5V <VDD ≤ 5.5V |
| | | I/O Ports | VSS | — | 0.15 VDD | V | Otherwise |
| | | MCLR (Schmitt Trigger) | VSS | — | 0.15 VDD | V | |
| | | T0CKI (Schmitt Trigger) | VSS | — | 0.15 VDD | V | |
| | | OSC1 (Schmitt Trigger) | VSS | — | 0.15 VDD | V | RC mode only(3) |
| | | OSC1 | VSS | — | 0.3 VDD | V | XT, HS and LP modes |
| D040 | VIH | **Input High Voltage** | | | | | |
| | | I/O ports | 2.0 | — | VDD | V | 4.5V < VDD ≤ 5.5V |
| | | I/O ports | 0.25 VDD+0.8 | — | VDD | V | Otherwise |
| | | MCLR (Schmitt Trigger) | 0.85 VDD | — | VDD | V | |
| | | T0CKI (Schmitt Trigger) | 0.85 VDD | — | VDD | V | |
| | | OSC1 (Schmitt Trigger) | 0.85 VDD | — | VDD | V | RC mode only(3) |
| | | OSC1 | 0.7 VDD | — | VDD | V | XT, HS and LP modes |
| D050 | VHYS | **Hysteresis of Schmitt Trigger inputs** | 0.15 VDD* | — | — | V | |
| D060 | IIL | **Input Leakage Current(1,2)** | | | | | **For VDD ≤ 5.5V:** |
| | | I/O ports | -1.0 | 0.5 | +1.0 | µA | VSS ≤ VPIN ≤ VDD, pin at hi-impedance |
| | | MCLR | -5.0 | — | +5.0 | µA | VPIN = VSS +0.25V |
| | | MCLR | | 0.5 | +3.0 | µA | VPIN = VDD |
| | | T0CKI | -3.0 | 0.5 | +3.0 | µA | VSS ≤ VPIN ≤ VDD |
| | | OSC1 | -3.0 | 0.5 | — | µA | VSS ≤ VPIN ≤ VDD, XT, HS and LP modes |
| D080 | VOL | **Output Low Voltage** | | | | | |
| | | I/O ports | — | — | 0.6 | V | IOL = 8.7 mA, VDD = 4.5V |
| | | OSC2/CLKOUT | — | — | 0.6 | V | IOL = 1.6 mA, VDD = 4.5V, RC mode only |
| D090 | VOH | **Output High Voltage(2)** | | | | | |
| | | I/O ports | VDD - 0.7 | — | — | V | IOH = -5.4 mA, VDD = 4.5V |
| | | OSC2/CLKOUT | VDD - 0.7 | — | — | V | IOH = -1.0 mA, VDD = 4.5V, RC mode only |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

**2:** Negative current is defined as coming out of the pin.

**3:** For the RC mode, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

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## 17.4 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

| | |
|---|---|
| T | |
| F Frequency | T Time |

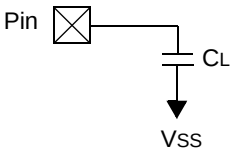
Lowercase letters (pp) and their meanings:

| | |
|---|---|
| pp | |
| 2 to | mc $\overline{\text{MCLR}}$ |
| ck CLKOUT | osc oscillator |
| cy cycle time | os OSC1 |
| drt device reset timer | t0 T0CKI |
| io I/O port | wdt watchdog timer |

Uppercase letters and their meanings:

| | |
|---|---|
| S | |
| F Fall | P Period |
| H High | R Rise |
| I Invalid (Hi-impedance) | V Valid |
| L Low | Z Hi-impedance |

**FIGURE 17-5: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16C54C/CR54C/C55A/C56A/CR56A/C57C/CR57C/C58B/CR58B-04, 20**




$C_L$ = 50 pF for all pins and OSC2 for RC mode

0 -15 pF for OSC2 in XT, HS or LP modes when external clock is used to drive OSC1



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## 17.5 Timing Diagrams and Specifications

**FIGURE 17-6: EXTERNAL CLOCK TIMING - PIC16C5X, PIC16CR5X**

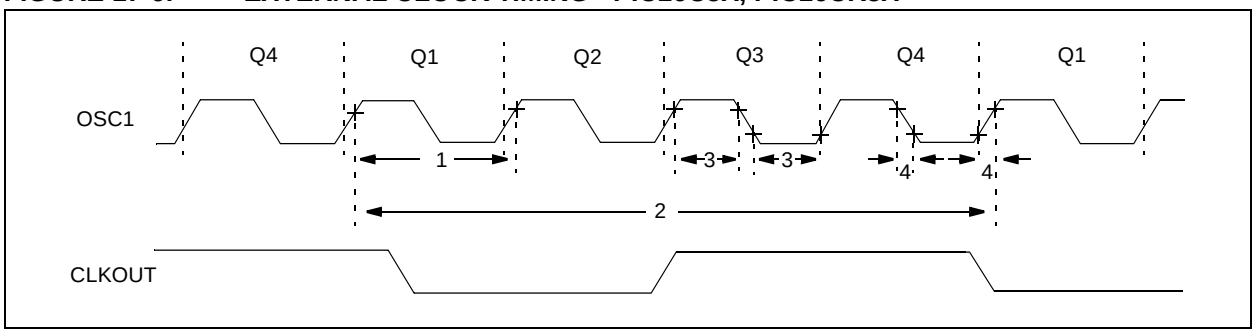


**TABLE 17-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X**

| AC Characteristics | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–40°C ≤ TA ≤ +125°C for extended | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| | FOSC | External CLKIN Frequency(1) | DC | — | 4.0 | MHz | XT OSC mode |
| | | | DC | — | 4.0 | MHz | HS OSC mode (04) |
| | | | DC | — | 20 | MHz | HS OSC mode (20) |
| | | | DC | — | 200 | kHz | LP OSC mode |
| | | Oscillator Frequency(1) | DC | — | 4.0 | MHz | RC OSC mode |
| | | | 0.45 | — | 4.0 | MHz | XT OSC mode |
| | | | 4.0 | — | 4.0 | MHz | HS OSC mode (04) |
| | | | 4.0 | — | 20 | MHz | HS OSC mode (20) |
| | | | 5.0 | — | 200 | kHz | LP OSC mode |
| 1 | TOSC | External CLKIN Period(1) | 250 | — | — | ns | XT OSC mode |
| | | | 250 | — | — | ns | HS OSC mode (04) |
| | | | 50 | — | — | ns | HS OSC mode (20) |
| | | | 5.0 | — | — | µs | LP OSC mode |
| | | Oscillator Period(1) | 250 | — | — | ns | RC OSC mode |
| | | | 250 | — | 2,200 | ns | XT OSC mode |
| | | | 250 | — | 250 | ns | HS OSC mode (04) |
| | | | 50 | — | 250 | ns | HS OSC mode (20) |
| | | | 5.0 | — | 200 | µs | LP OSC mode |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

**2:** Instruction cycle period (TCY) equals four times the input oscillator time base period.

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**TABLE 17-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X**

| AC Characteristics | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–40°C ≤ TA ≤ +125°C for extended | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| 2 | Tcy | Instruction Cycle Time(2) | — | 4/FOSC | — | — | |
| 3 | TosL, TosH | Clock in (OSC1) Low or High Time | 50* | — | — | ns | XT oscillator |
| | | | 20* | — | — | ns | HS oscillator |
| | | | 2.0* | — | — | µs | LP oscillator |
| 4 | TosR, TosF | Clock in (OSC1) Rise or Fall Time | — | — | 25* | ns | XT oscillator |
| | | | — | — | 25* | ns | HS oscillator |
| | | | — | — | 50* | ns | LP oscillator |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

**2:** Instruction cycle period (TCY) equals four times the input oscillator time base period.



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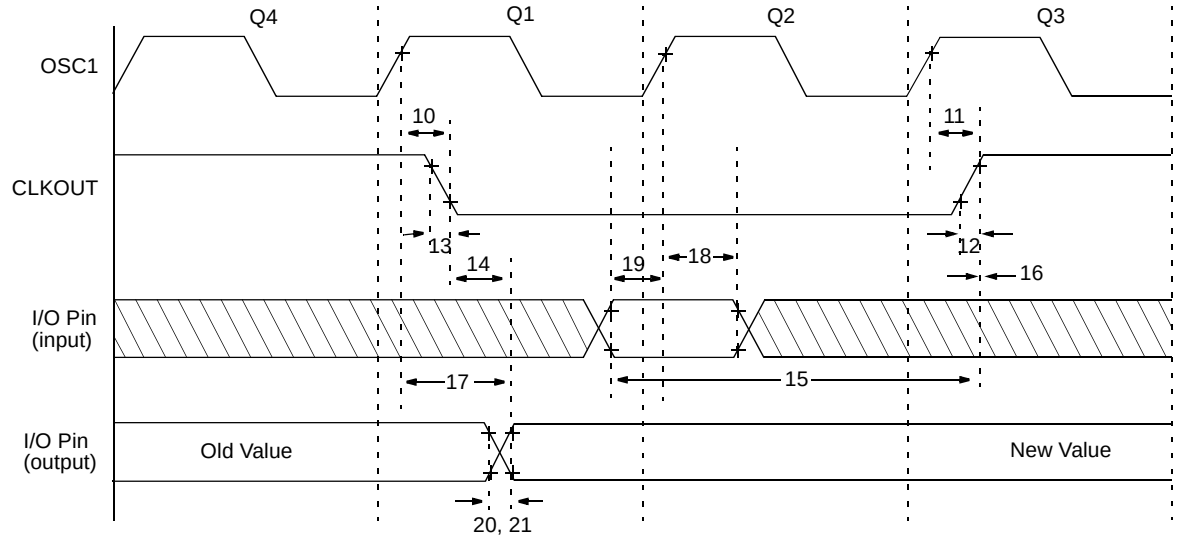
**FIGURE 17-7: CLKOUT AND I/O TIMING - PIC16C5X, PIC16CR5X**




**Note:** Refer to Figure 17-5 for load conditions.

**TABLE 17-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X**

| **AC Characteristics** | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–40°C ≤ TA ≤ +125°C for extended | | | | | |
|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** |
| 10 | TosH2ckL | OSC1↑ to CLKOUT↓(1) | — | 15 | 30** | ns |
| 11 | TosH2ckH | OSC1↑ to CLKOUT↑(1) | — | 15 | 30** | ns |
| 12 | TckR | CLKOUT rise time(1) | — | 5.0 | 15** | ns |
| 13 | TckF | CLKOUT fall time(1) | — | 5.0 | 15** | ns |
| 14 | TckL2ioV | CLKOUT↓ to Port out valid(1) | — | — | 40** | ns |
| 15 | TioV2ckH | Port in valid before CLKOUT↑(1) | 0.25 TCY+30* | — | — | ns |
| 16 | TckH2ioI | Port in hold after CLKOUT↑(1) | 0* | — | — | ns |
| 17 | TosH2ioV | OSC1↑ (Q1 cycle) to Port out valid(2) | — | — | 100* | ns |
| 18 | TosH2ioI | OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time) | TBD | — | — | ns |
| 19 | TioV2osH | Port input valid to OSC1↑ (I/O in setup time) | TBD | — | — | ns |
| 20 | TioR | Port output rise time(2) | — | 10 | 25** | ns |
| 21 | TioF | Port output fall time(2) | — | 10 | 25** | ns |

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

**2:** Refer to Figure 17-5 for load conditions.

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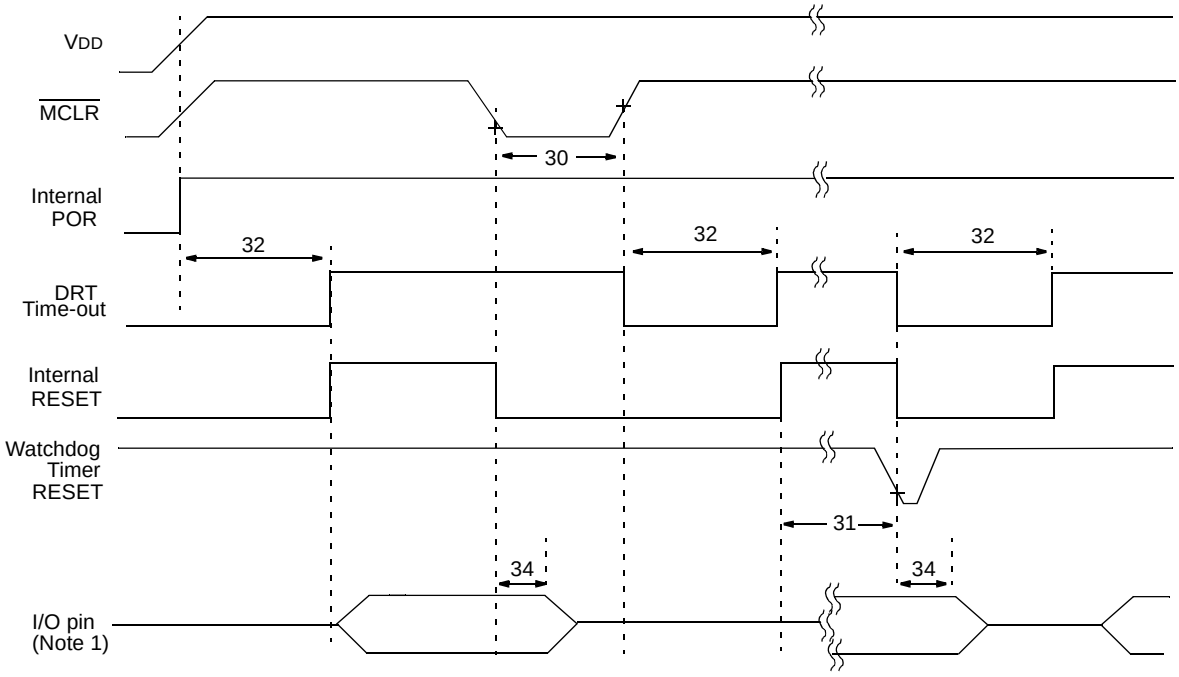
**FIGURE 17-8: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C5X, PIC16CR5X**




**Note 1:** Please refer to Figure 17-5 for load conditions.

**TABLE 17-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C5X, PIC16CR5X**

| **AC Characteristics** | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–40°C ≤ TA ≤ +125°C for extended | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| 30 | TmcL | $\overline{\text{MCLR}}$ Pulse Width (low) | 1000* | — | — | ns | VDD = 5.0V |
| 31 | Twdt | Watchdog Timer Time-out Period (No Prescaler) | 9.0* | 18* | 30* | ms | VDD = 5.0V (Comm) |
| 32 | TDRT | Device Reset Timer Period | 9.0* | 18* | 30* | ms | VDD = 5.0V (Comm) |
| 34 | Tioz | I/O Hi-impedance from $\overline{\text{MCLR}}$ Low | 100* | 300* | 1000* | ns | |

* These parameters are characterized but not tested.

† Data in the Typical (“Typ”) column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.



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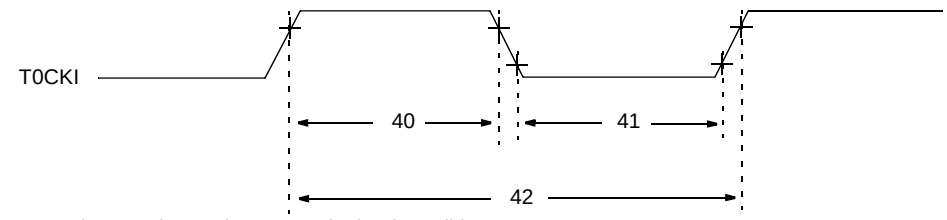
**FIGURE 17-9: TIMER0 CLOCK TIMINGS - PIC16C5X, PIC16CR5X**




**Note:** Please refer to Figure 17-5 for load conditions.

**TABLE 17-4: TIMER0 CLOCK REQUIREMENTS - PIC16C5X, PIC16CR5X**

| AC Characteristics | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial<br>–40°C ≤ TA ≤ +85°C for industrial<br>–40°C ≤ TA ≤ +125°C for extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| 40 | Tt0H | T0CKI High Pulse Width<br>- No Prescaler | 0.5 TCY + 20* | — | — | ns | |
| | | - With Prescaler | 10* | — | — | ns | |
| 41 | Tt0L | T0CKI Low Pulse Width<br>- No Prescaler | 0.5 TCY + 20* | — | — | ns | |
| | | - With Prescaler | 10* | — | — | ns | |
| 42 | Tt0P | T0CKI Period | 20 or $\frac{T_{CY} + 40}{N}$* | — | — | ns | Whichever is greater.<br>N = Prescale Value (1, 2, 4,..., 256) |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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## 18.0 DEVICE CHARACTERIZATION - PIC16LC54A

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean – 3σ) respectively, where σ is a standard deviation, over the whole temperature range.

**FIGURE 18-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE**

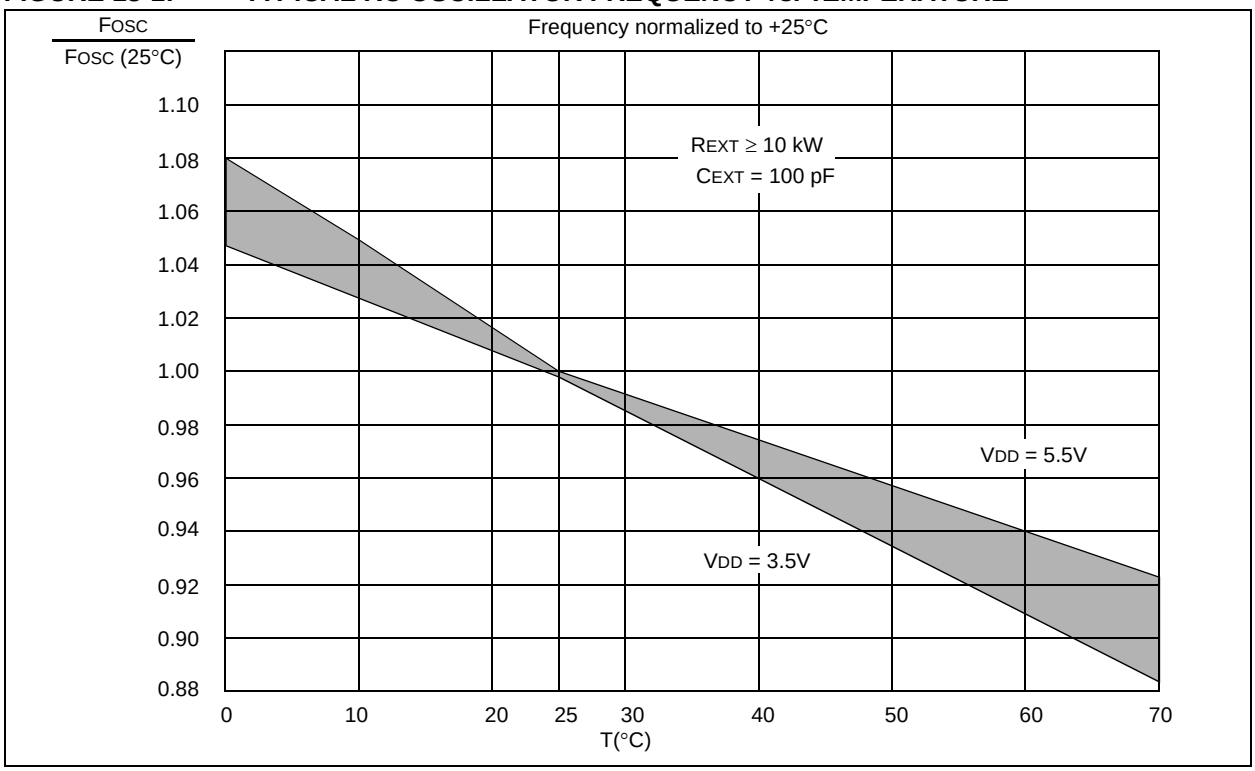


**TABLE 18-1: RC OSCILLATOR FREQUENCIES**

| CEXT | REXT | Average Fosc @ 5V, 25°C | |
|---|---|---|---|
| 20 pF | 3.3K | 5 MHz | ± 27% |
| | 5K | 3.8 MHz | ± 21% |
| | 10K | 2.2 MHz | ± 21% |
| | 100K | 262 kHz | ± 31% |
| 100 pF | 3.3K | 1.63 MHz | ± 13% |
| | 5K | 1.2 MHz | ± 13% |
| | 10K | 684 kHz | ± 18% |
| | 100K | 71 kHz | ± 25% |
| 300 pF | 3.3K | 660 kHz | ± 10% |
| | 5.0K | 484 kHz | ± 14% |
| | 10K | 267 kHz | ± 15% |
| | 100K | 29 kHz | ± 19% |

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ±3 standard deviation from average value for VDD = 5V.



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**FIGURE 18-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 20 pF, 25°C**

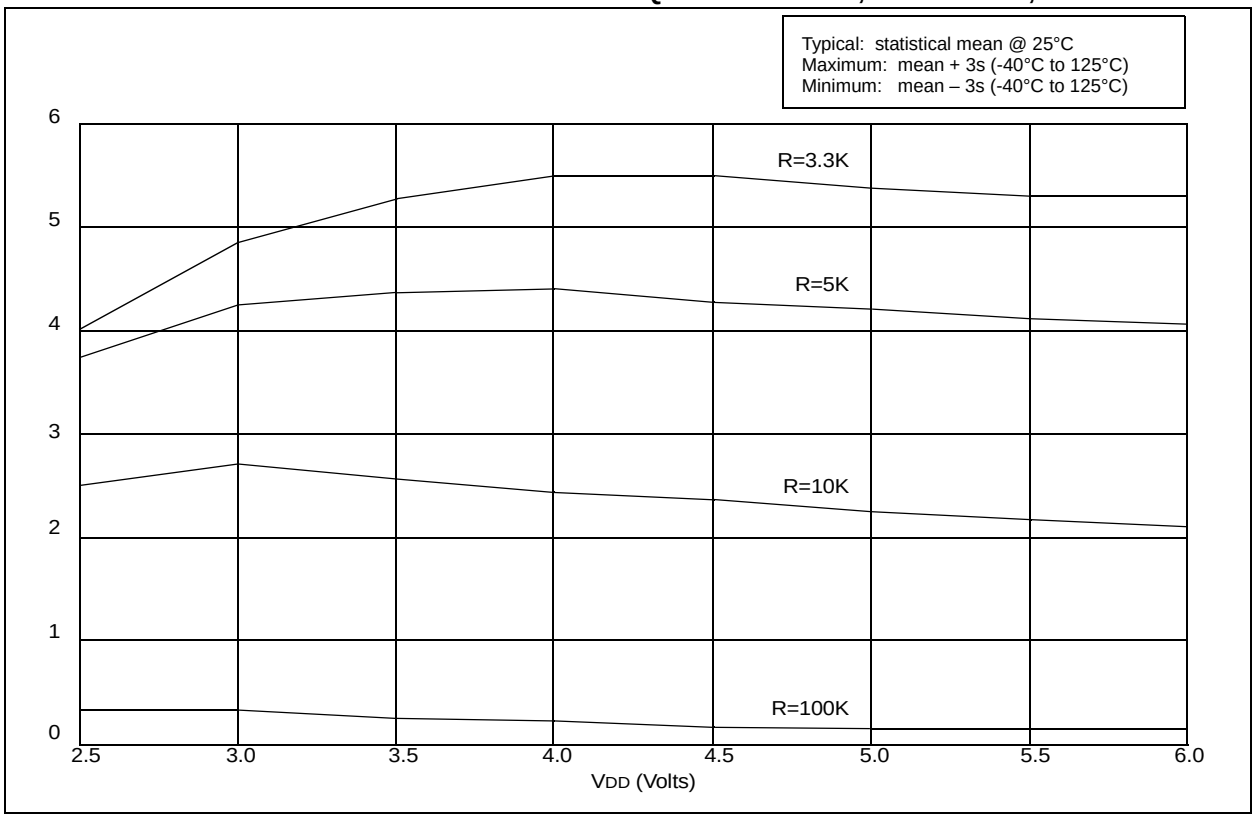


**FIGURE 18-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 100 pF, 25°C**

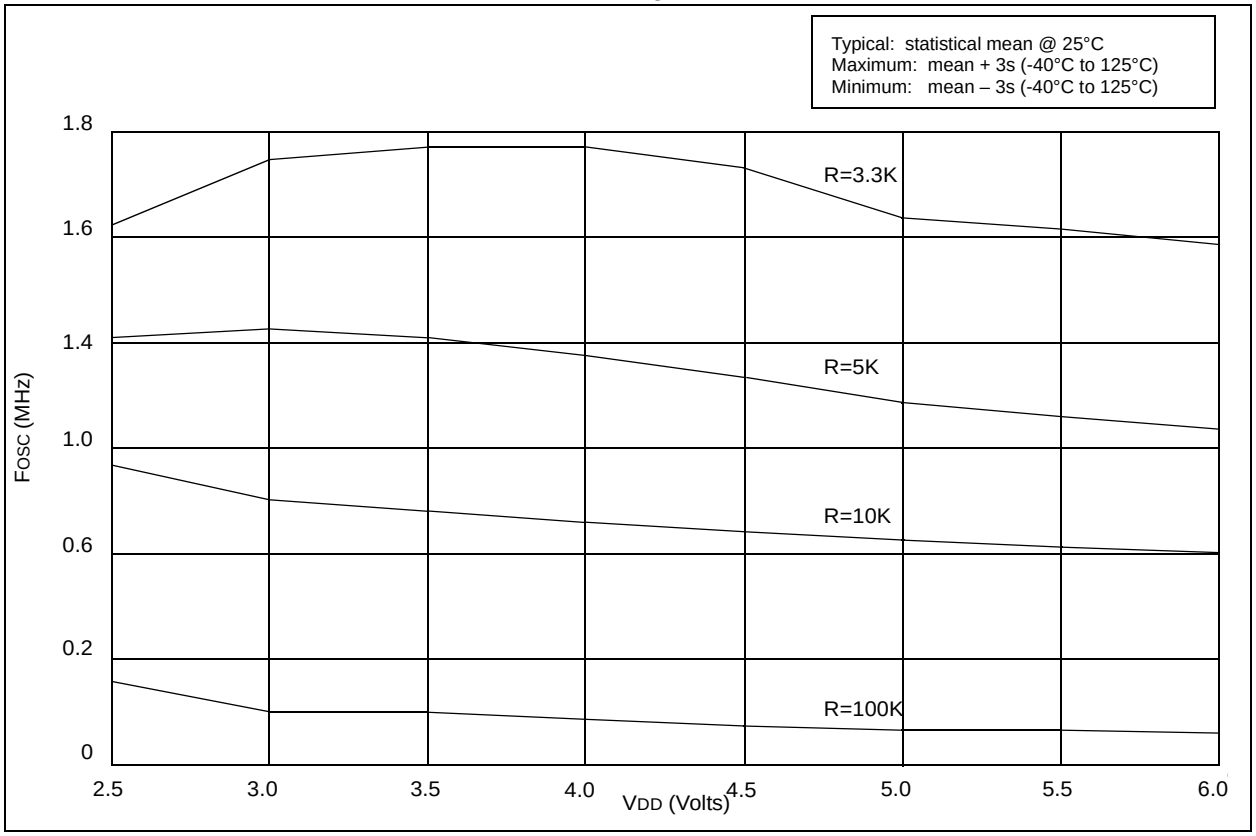


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**FIGURE 18-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 300 pF, 25°C**

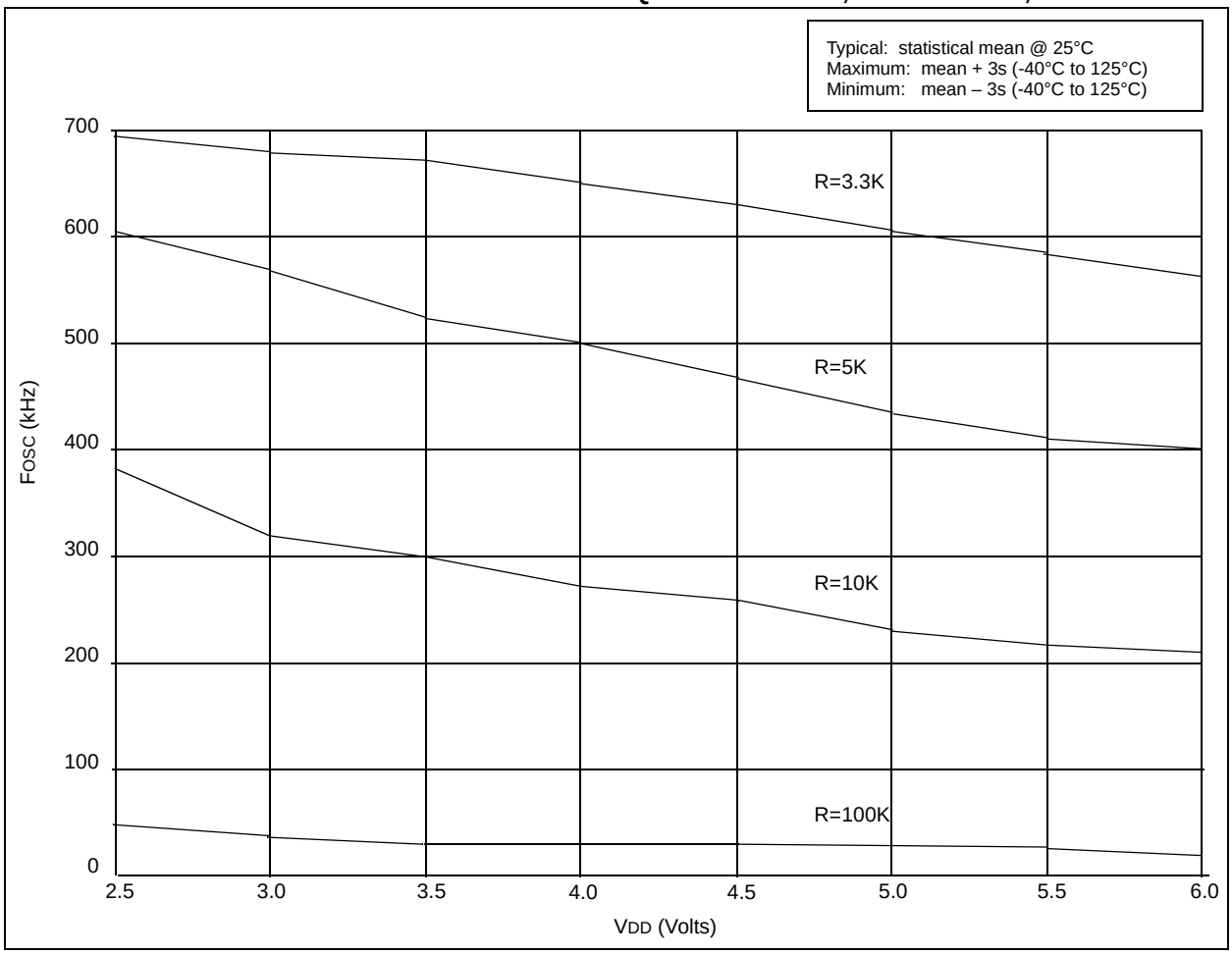


**FIGURE 18-5: TYPICAL IPD vs. VDD, WATCHDOG DISABLED (25°C)**

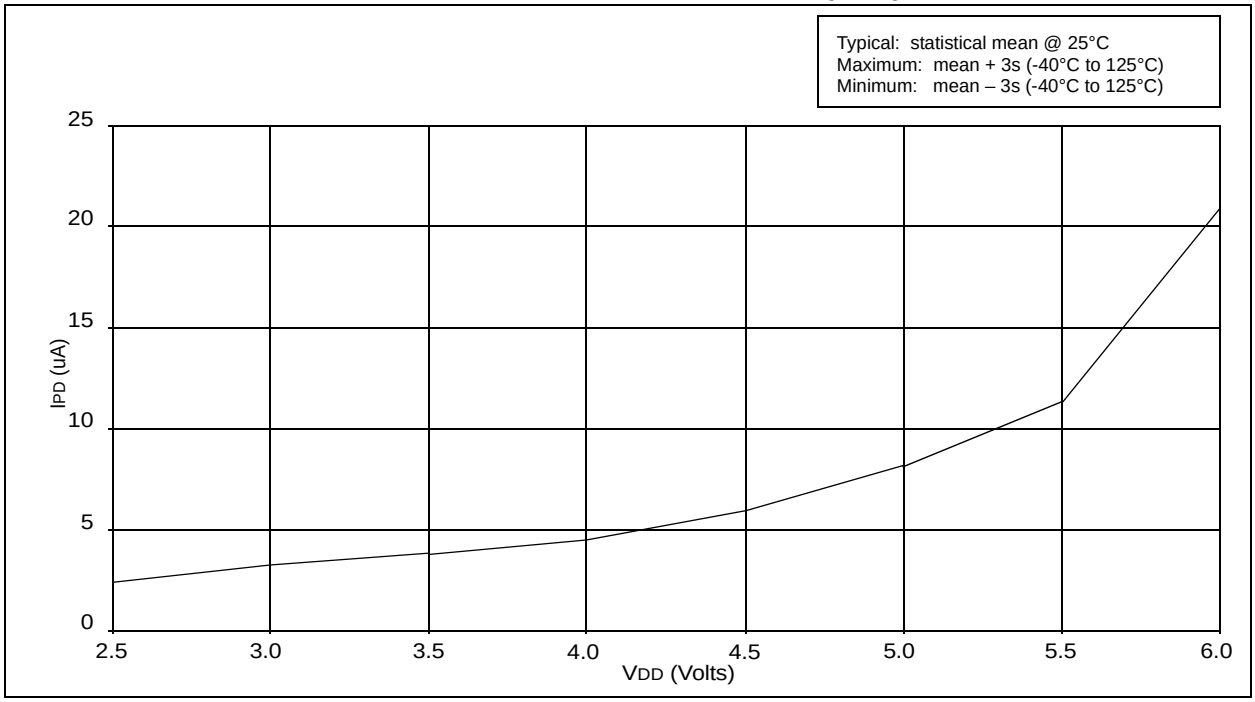




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**FIGURE 18-6: TYPICAL IPD vs. VDD, WATCHDOG ENABLED (25°C)**

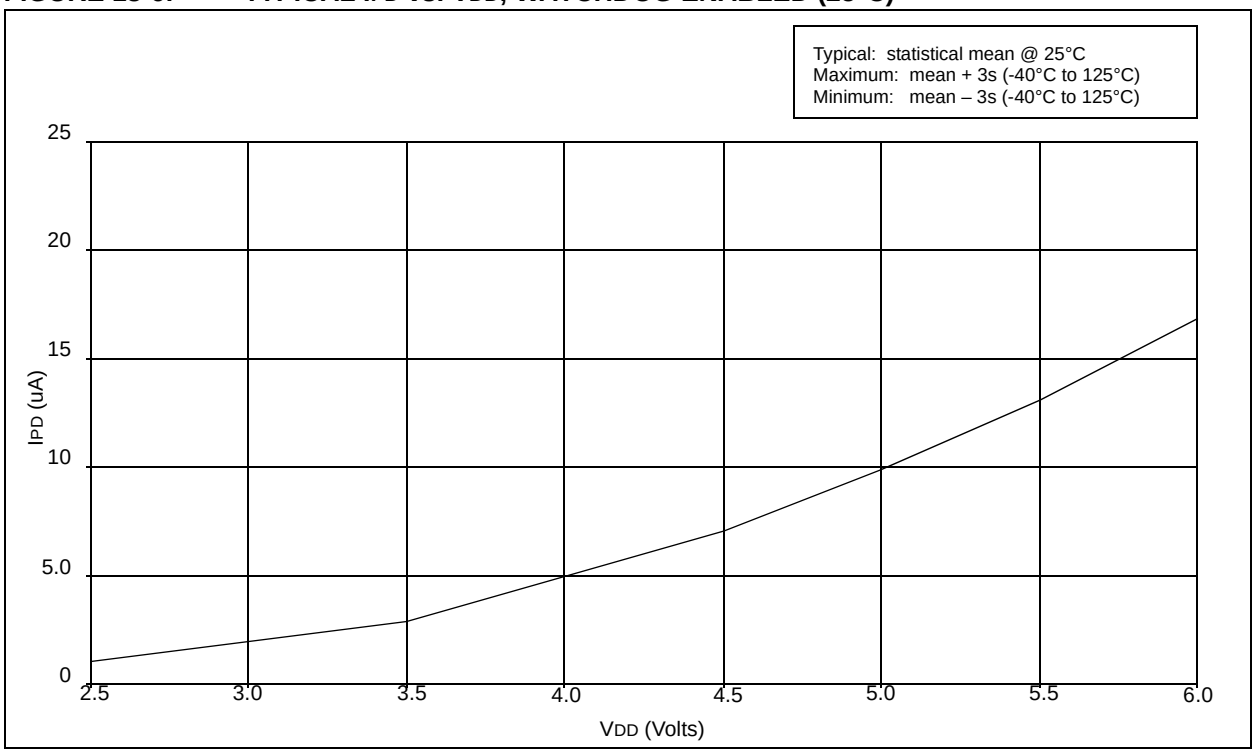


**FIGURE 18-7: TYPICAL IPD vs. VDD, WATCHDOG ENABLED (–40°C, 85°C)**

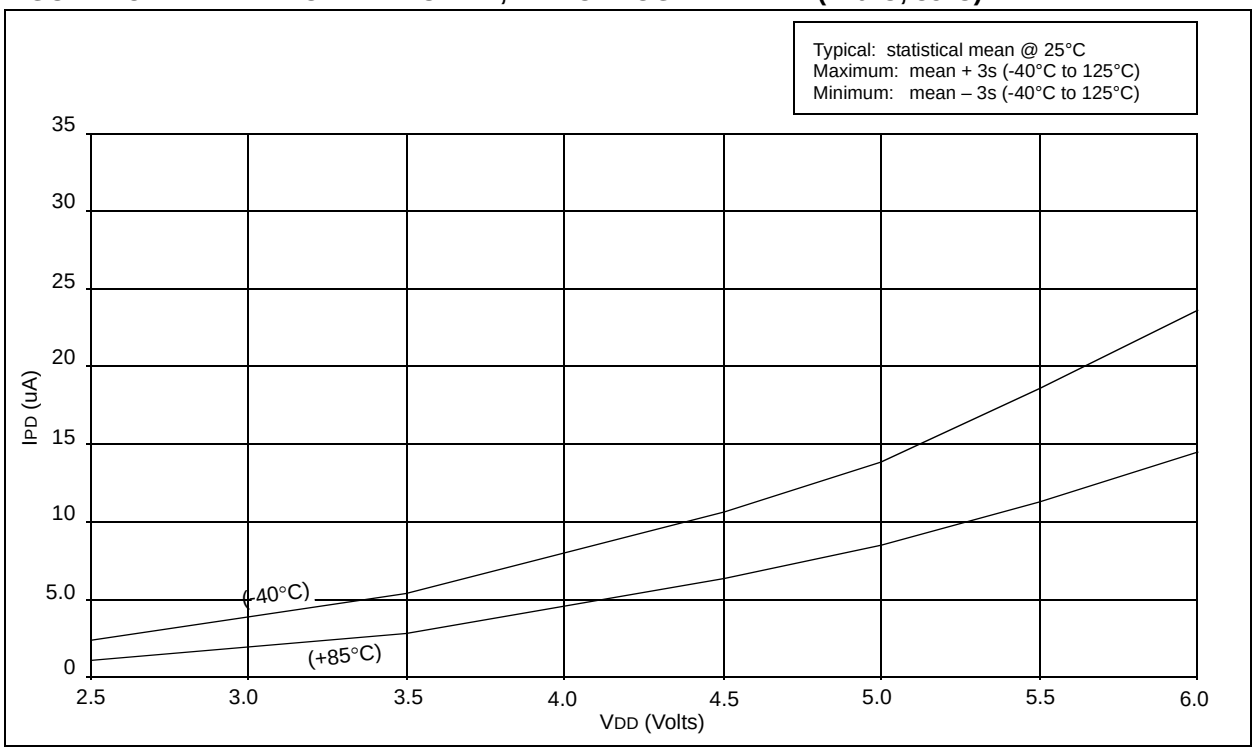


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**FIGURE 18-8: VTH (INPUT THRESHOLD TRIP POINT VOLTAGE) OF I/O PINS vs. VDD**

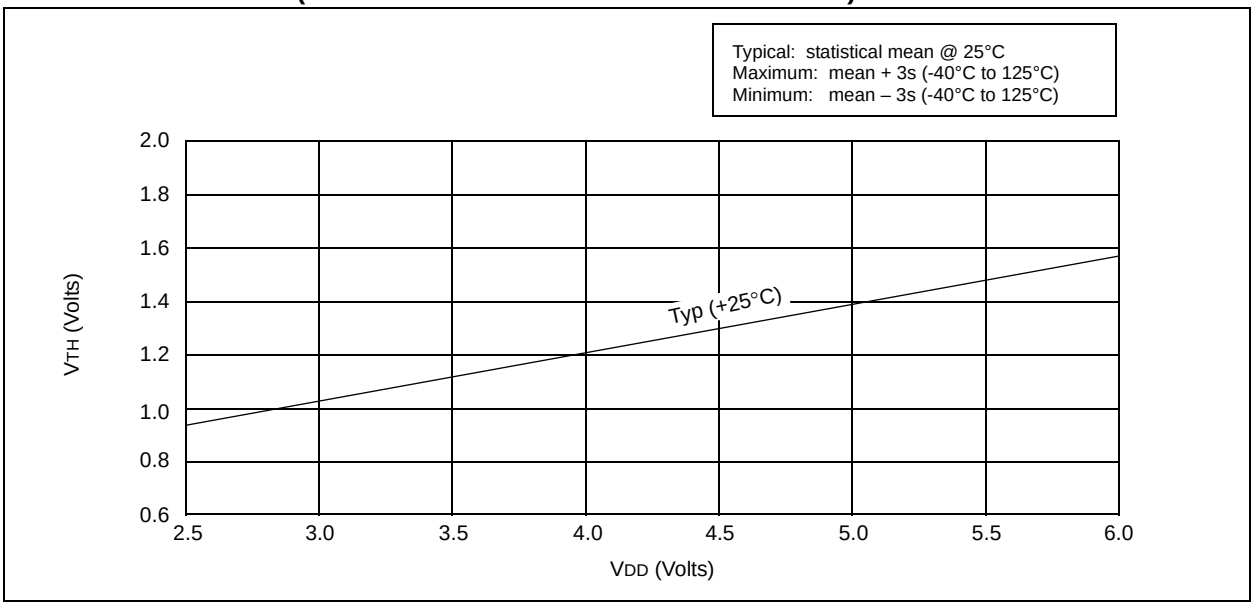
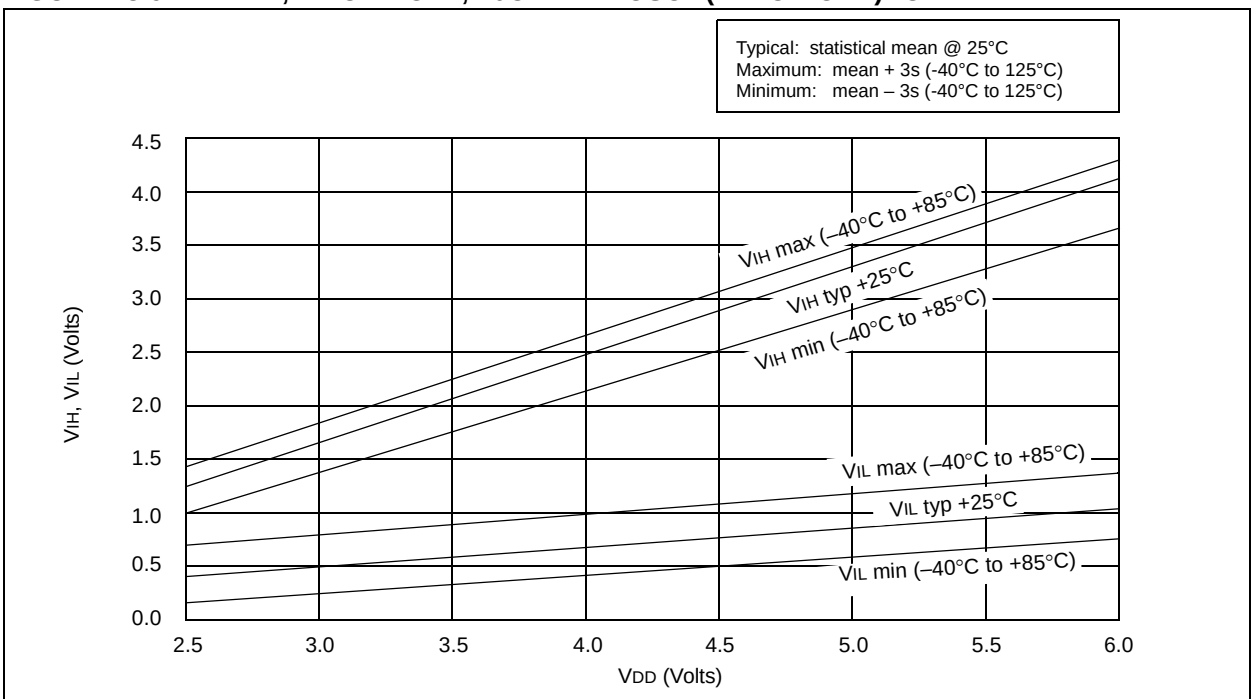



**FIGURE 18-9: VIH, VIL OF $\overline{\text{MCLR}}$, T0CKI AND OSC1 (IN RC MODE) vs. VDD**




**Note:** These input pins have Schmitt Trigger input buffers.



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**FIGURE 18-10: VTH (INPUT THRESHOLD TRIP POINT VOLTAGE) OF OSC1 INPUT (IN XT, HS AND LP MODES) vs. VDD**

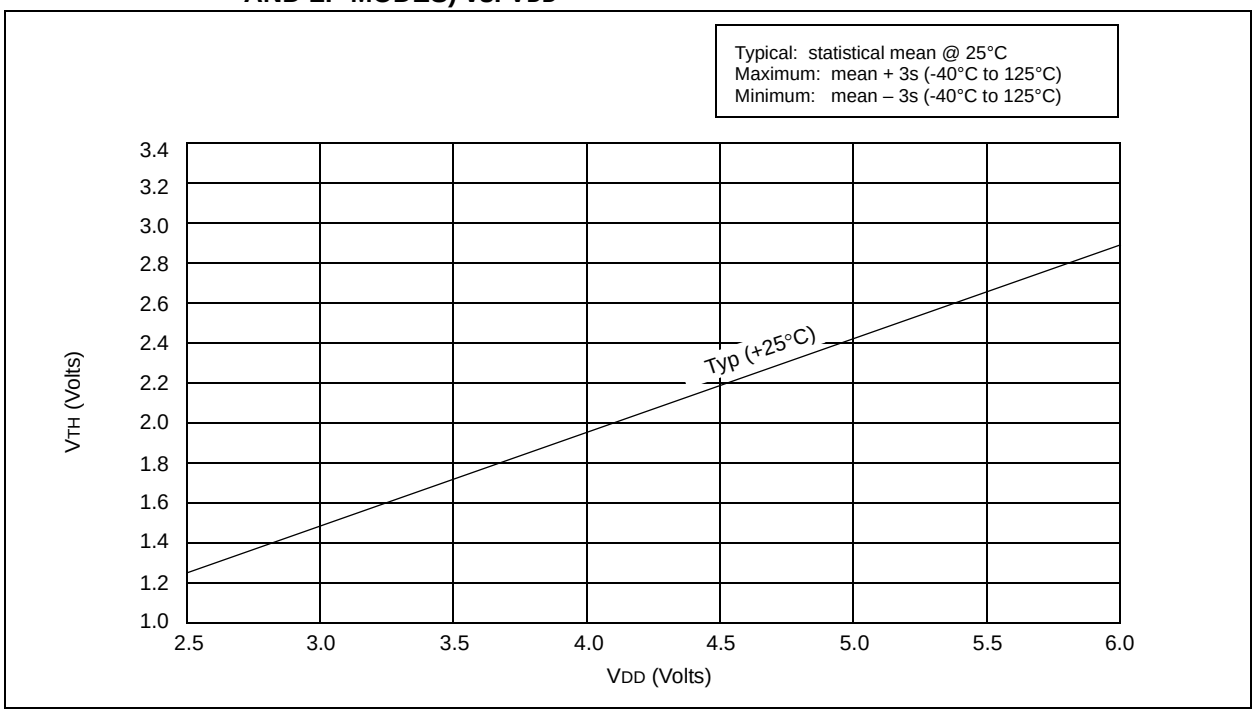


**FIGURE 18-11: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 20 pF, 25°C)**

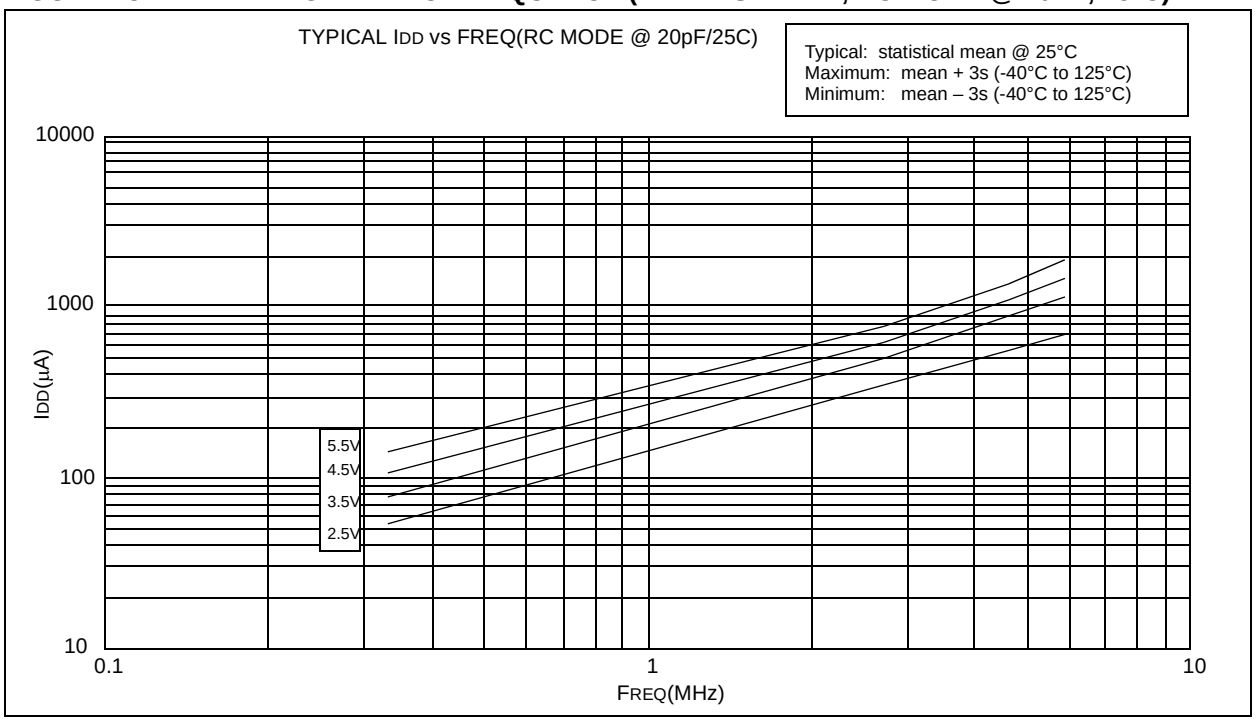


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**FIGURE 18-12: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 100 pF, 25°C)**

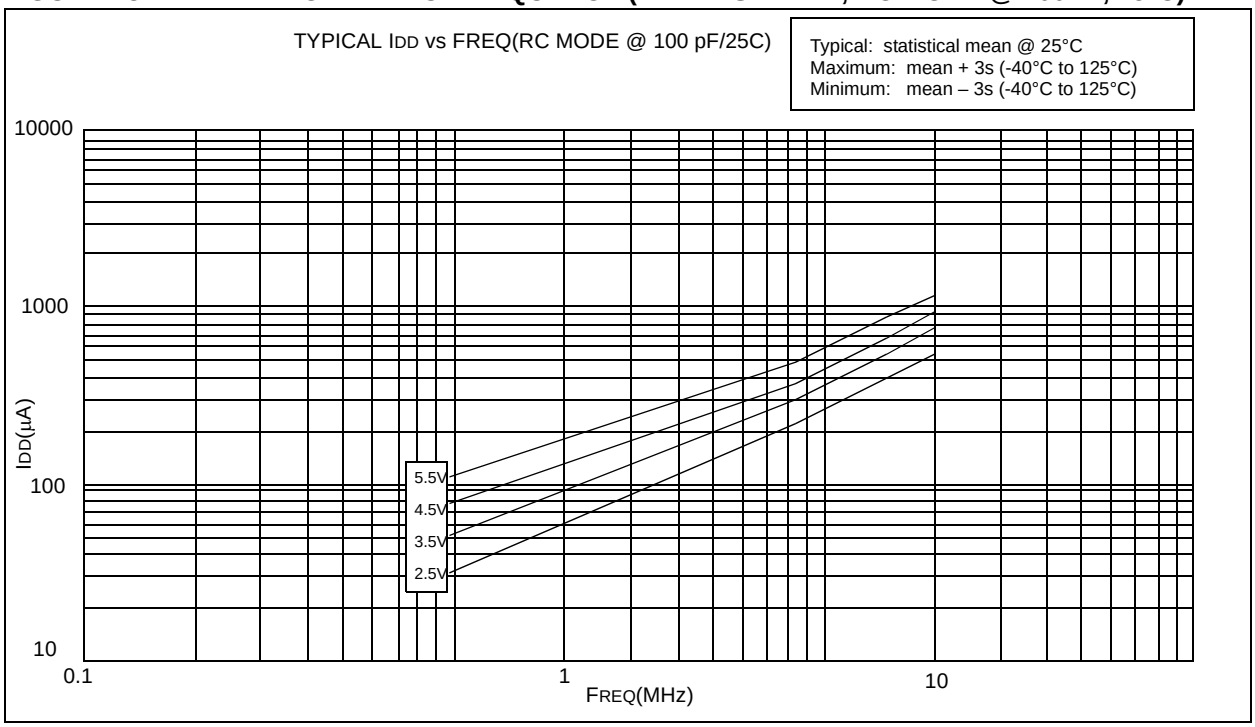


**FIGURE 18-13: TYPICAL IDD vs. FREQUENCY (WDT DISABLED, RC MODE @ 300 pF, 25°C)**

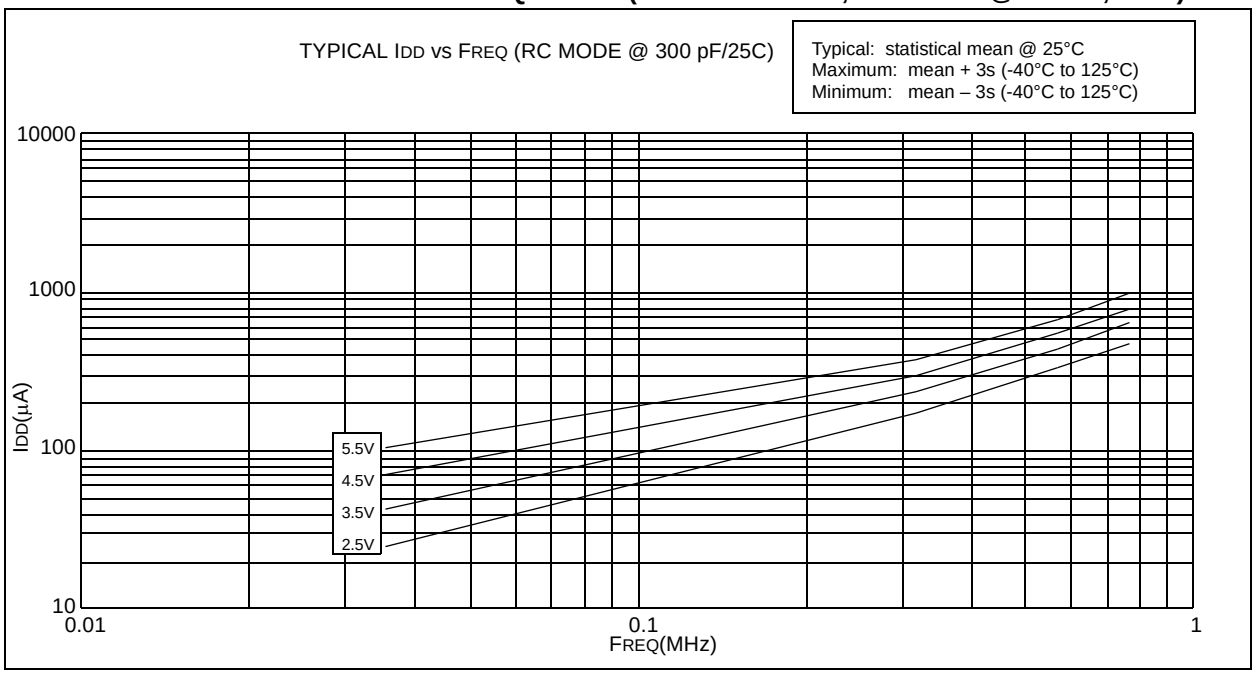




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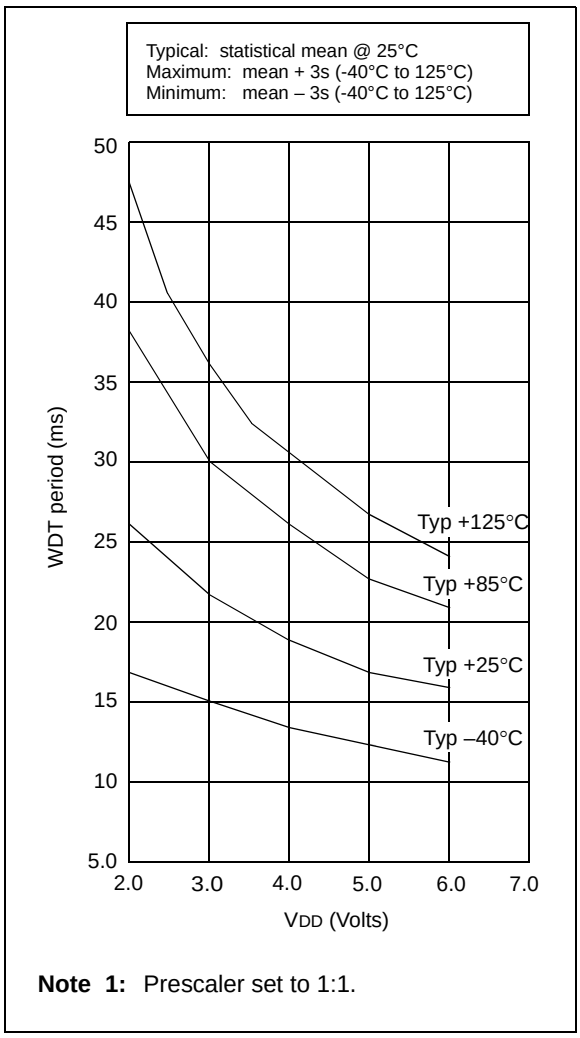
**FIGURE 18-14: WDT TIMER TIME-OUT PERIOD vs. $V_{DD}$(1)**




**Note 1:** Prescaler set to 1:1.

**FIGURE 18-15: PORTA, B AND C $I_{OH}$ vs. $V_{OH}$, $V_{DD}$ = 3 V**

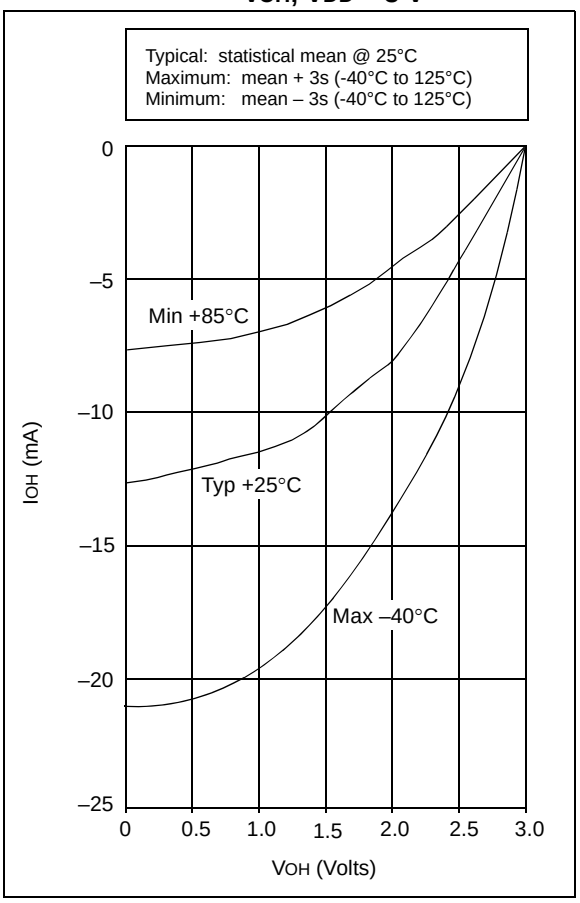



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**FIGURE 18-16: PORTA, B AND C $I_{OH}$ vs. $V_{OH}$, $V_{DD}$ = 5 V**

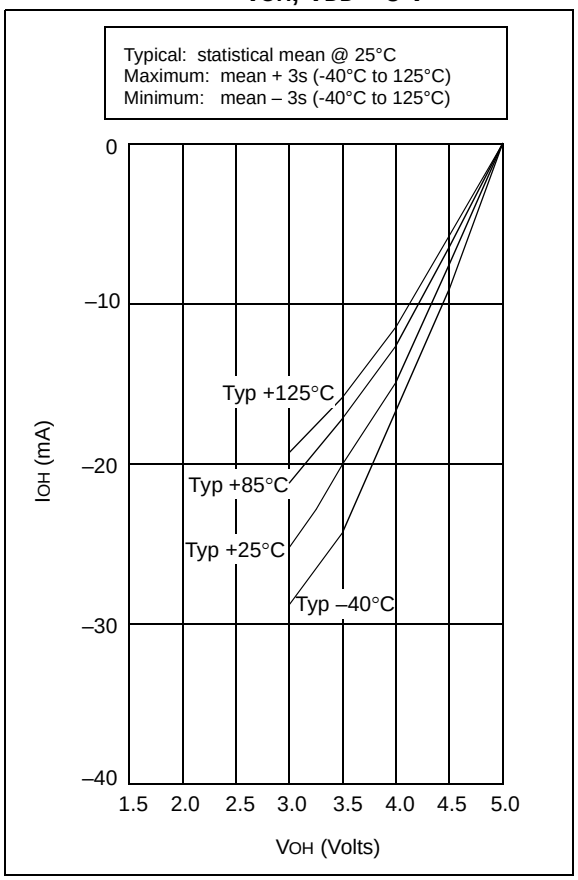


**FIGURE 18-17: PORTA, B AND C $I_{OL}$ vs. $V_{OL}$, $V_{DD}$ = 3 V**

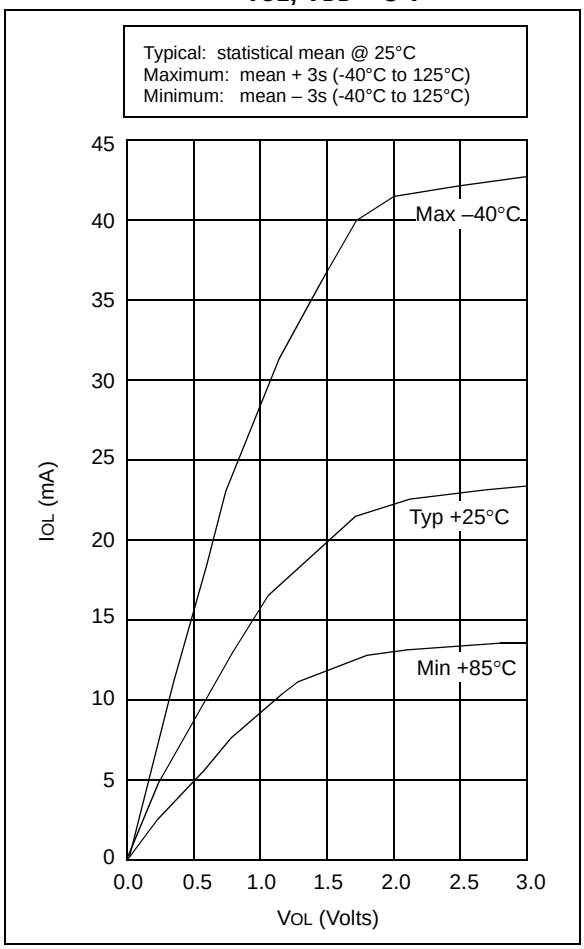




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**FIGURE 18-18: PORTA, B AND C $I_{OL}$ vs. $V_{OL}$, $V_{DD}$ = 5 V**

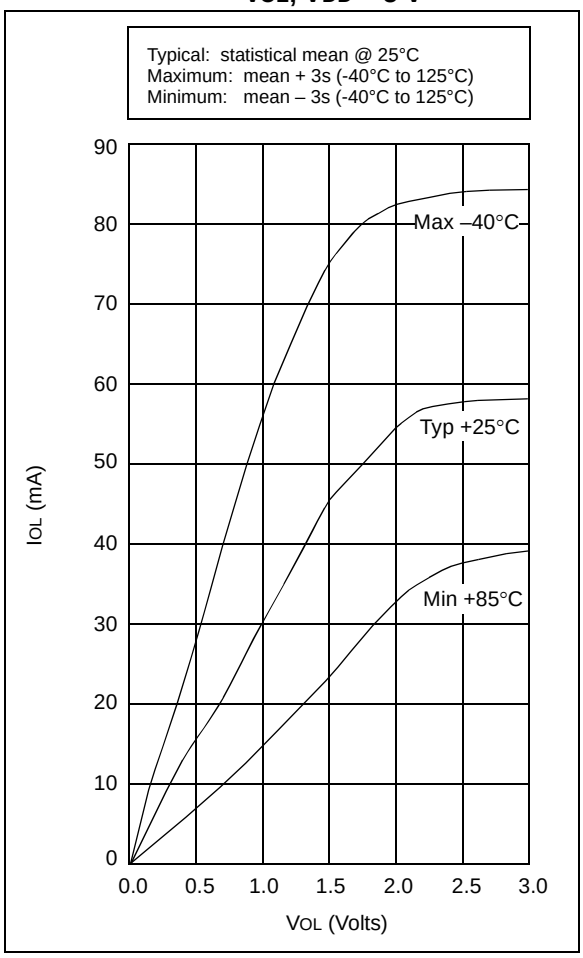


**TABLE 18-2: INPUT CAPACITANCE**

| Pin | Typical Capacitance (pF) | |
|---|---|---|
| | 18L PDIP | 18L SOIC |
| RA port | 5.0 | 4.3 |
| RB port | 5.0 | 4.3 |
| $\overline{MCLR}$ | 17.0 | 17.0 |
| OSC1 | 4.0 | 3.5 |
| OSC2/CLKOUT | 4.3 | 3.5 |
| T0CKI | 3.2 | 2.8 |

All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

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## 19.0 ELECTRICAL CHARACTERISTICS - PIC16LC54C 40MHz

**Absolute Maximum Ratings(†)**

Ambient temperature under bias ..... –55°C to +125°C
Storage temperature ..... –65°C to +150°C
Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... 0 to +7.5V
Voltage on $\overline{MCLR}$ with respect to $V_{SS}$ ..... 0 to +14V
Voltage on all other pins with respect to $V_{SS}$ ..... –0.6V to ($V_{DD}$ + 0.6V)
Total power dissipation(1) ..... 800 mW
Max. current out of $V_{SS}$ pin ..... 150 mA
Max. current into $V_{DD}$ pin ..... 100 mA
Max. current into an input pin (T0CKI only) ..... ±500 µA
Input clamp current, $I_{IK}$ ($V_I$ < 0 or $V_I$ > $V_{DD}$) ..... ±20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{DD}$) ..... ±20 mA
Max. output current sunk by any I/O pin ..... 25 mA
Max. output current sourced by any I/O pin ..... 20 mA
Max. output current sourced by a single I/O (Port A, B or C) ..... 50 mA
Max. output current sunk by a single I/O (Port A, B or C) ..... 50 mA

**Note 1:** Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.



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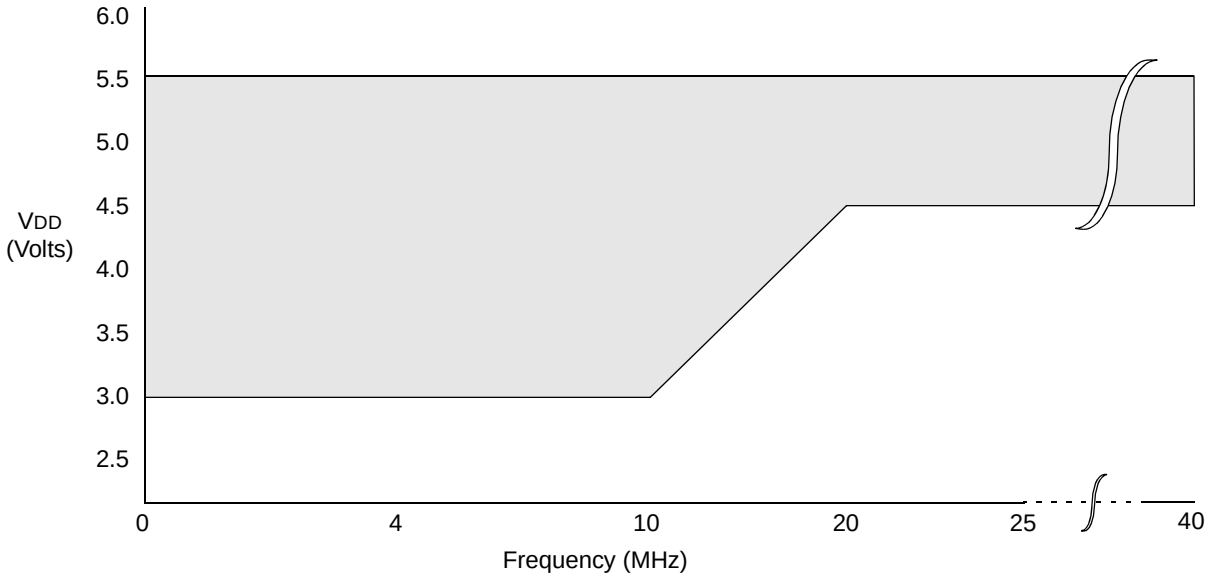
**FIGURE 19-1: PIC16C54C/C55A/C56A/C57C/C58B-40 VOLTAGE-FREQUENCY GRAPH, $0°C \leq T_A \leq +70°C$**




**Note 1:** The shaded region indicates the permissible combinations of voltage and frequency.

**2:** The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

**3:** Operation between 20 to 40 MHz requires the following:

- VDD between 4.5V. and 5.5V
- OSC1 externally driven
- OSC2 not connected
- HS mode
- Commercial temperatures

Devices qualified for 40 MHz operation have -40 designation (ex: PIC16C54C-40/P).

**4:** For operation between DC and 20 MHz, see Section 17.1.

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## 19.1 DC Characteristics:PIC16C54C/C55A/C56A/C57C/C58B-40 (Commercial)(1)

| PIC16C54C/C55A/C56A/C57C/C58B-40 (Commercial) | | | Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C for commercial | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D001 | VDD | **Supply Voltage** | 4.5 | — | 5.5 | V | HS mode from 20 - 40 MHz |
| D002 | VDR | **RAM Data Retention Voltage(2)** | — | 1.5* | — | V | Device in SLEEP mode |
| D003 | VPOR | **VDD Start Voltage** to ensure Power-on Reset | — | Vss | — | V | See Section 5.1 for details on Power-on Reset |
| D004 | SVDD | **VDD Rise Rate** to ensure Power-on Reset | 0.05* | — | — | V/ms | See Section 5.1 for details on Power-on Reset |
| D010 | IDD | **Supply Current(3)** | —<br>— | 5.2<br>6.8 | 12.3<br>16 | mA<br>mA | FOSC = 40 MHz, VDD = 4.5V, HS mode<br>FOSC = 40 MHz, VDD = 5.5V, HS mode |
| D020 | IPD | **Power-down Current(3)** | —<br>— | 1.8<br>9.8 | 7.0<br>27* | µA<br>µA | VDD = 5.5V, WDT disabled, Commercial<br>VDD = 5.5V, WDT enabled, Commercial |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** Device operation between 20 MHz to 40 MHz requires the following: VDD between 4.5V to 5.5V, OSC1 pin externally driven, OSC2 pin not connected, HS oscillator mode and commercial temperatures. For operation between DC and 20 MHz, See Section 19.1.

**2:** This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

**3:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode. The power-down current in SLEEP mode does not depend on the oscillator type.



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## 19.2 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-40 (Commercial)(1)

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| D030 | VIL | **Input Low Voltage** | | | | | |
| | | I/O Ports | VSS | — | 0.8 | V | 4.5V <VDD ≤ 5.5V |
| | | MCLR (Schmitt Trigger) | VSS | — | 0.15 VDD | V | |
| | | T0CKI (Schmitt Trigger) | VSS | — | 0.15 VDD | V | |
| | | OSC1 | VSS | — | 0.2 VDD | V | HS, 20 MHz ≤ FOSC ≤ 40 MHz |
| D040 | VIH | **Input High Voltage** | | | | | |
| | | I/O ports | 2.0 | — | VDD | V | 4.5V < VDD ≤ 5.5V |
| | | MCLR (Schmitt Trigger) | 0.85 VDD | — | VDD | V | |
| | | T0CKI (Schmitt Trigger) | 0.85 VDD | — | VDD | V | |
| | | OSC1 | 0.8 VDD | — | VDD | V | HS, 20 MHz ≤ FOSC ≤ 40 MHz |
| D050 | VHYS | **Hysteresis of Schmitt Trigger inputs** | 0.15 VDD* | — | — | V | |
| D060 | IIL | **Input Leakage Current(2,3)** | | | | | **For VDD ≤ 5.5V:** |
| | | I/O ports | -1.0 | 0.5 | +1.0 | µA | VSS ≤ VPIN ≤ VDD, pin at hi-impedance |
| | | MCLR | -5.0 | — | +5.0 | µA | VPIN = VSS +0.25V |
| | | MCLR | — | 0.5 | +3.0 | µA | VPIN = VDD |
| | | T0CKI | -3.0 | 0.5 | +3.0 | µA | VSS ≤ VPIN ≤ VDD |
| | | OSC1 | -3.0 | 0.5 | — | µA | VSS ≤ VPIN ≤ VDD, HS |
| D080 | VOL | **Output Low Voltage** | | | | | |
| | | I/O ports | — | — | 0.6 | V | IOL = 8.7 mA, VDD = 4.5V |
| D090 | VOH | **Output High Voltage(3)** | | | | | |
| | | I/O ports | VDD - 0.7 | — | — | V | IOH = -5.4 mA, VDD = 4.5V |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

**Note 1:** Device operation between 20 MHz to 40 MHz requires the following: VDD between 4.5V to 5.5V, OSC1 pin externally driven, OSC2 pin not connected and HS oscillator mode and commercial temperatures. For operation between DC and 20 MHz, See Section 17.3.

**2:** The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

**3:** Negative current is defined as coming out of the pin.

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## 19.3 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS
2. TppS

| | |
|---|---|
| T | |
| F Frequency | T Time |

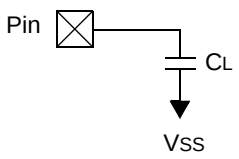
Lowercase letters (pp) and their meanings:

| | |
|---|---|
| pp | |
| 2 to | mc $\overline{\text{MCLR}}$ |
| ck CLKOUT | osc oscillator |
| cy cycle time | os OSC1 |
| drt device reset timer | t0 T0CKI |
| io I/O port | wdt watchdog timer |

Uppercase letters and their meanings:

| | |
|---|---|
| S | |
| F Fall | P Period |
| H High | R Rise |
| I Invalid (Hi-impedance) | V Valid |
| L Low | Z Hi-impedance |

**FIGURE 19-2: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS - PIC16C54C/C55A/C56A/C57C/C58B-40**




$C_L$ = 50 pF for all pins except OSC2
0 pF for OSC2 in HS mode for operation between 20 MHz to 40 MHz



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## 19.4 Timing Diagrams and Specifications

**FIGURE 19-3: EXTERNAL CLOCK TIMING - PIC16C5X-40**

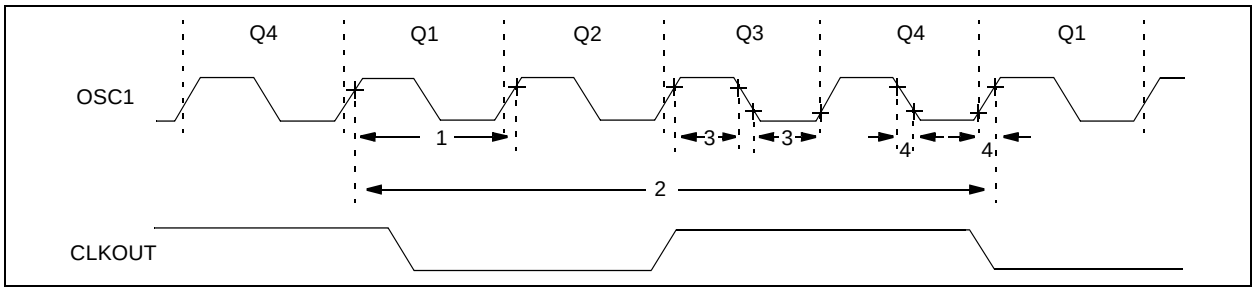


**TABLE 19-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X-40**

| AC Characteristics | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| | FOSC | External CLKIN Frequency(1) | 20 | — | 40 | MHz | HS OSC mode |
| 1 | TOSC | External CLKIN Period(1) | 25 | — | — | ns | HS OSC mode |
| 2 | Tcy | Instruction Cycle Time(2) | — | 4/FOSC | — | — | |
| 3 | TosL, TosH | Clock in (OSC1) Low or High Time | 6.0* | — | — | ns | HS oscillator |
| 4 | TosR, TosF | Clock in (OSC1) Rise or Fall Time | — | — | 6.5* | ns | HS oscillator |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

**2:** Instruction cycle period (TCY) equals four times the input oscillator time base period.

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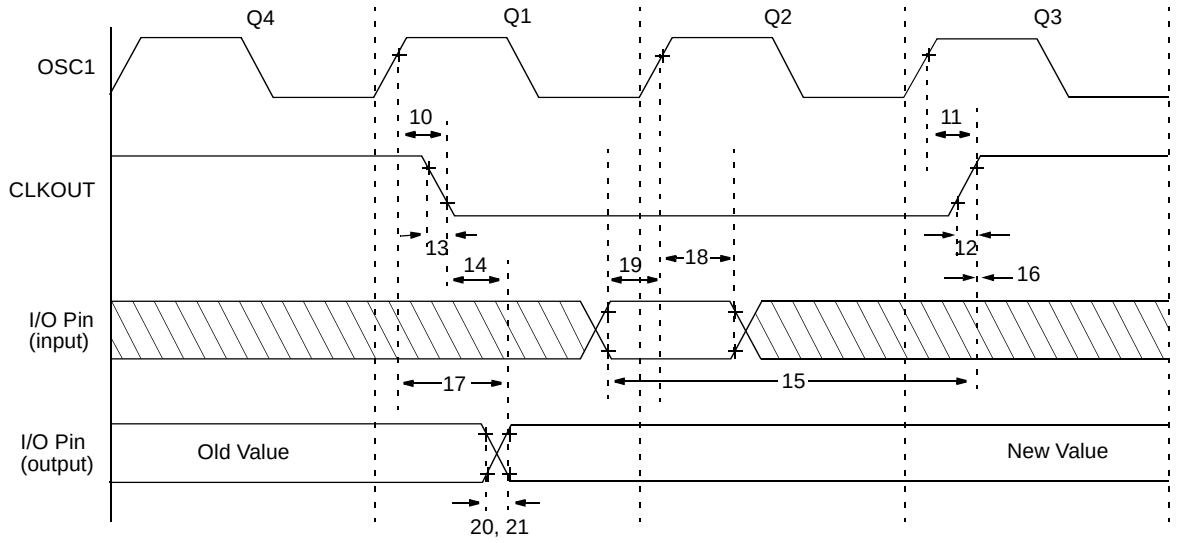
**FIGURE 19-4: CLKOUT AND I/O TIMING - PIC16C5X-40**




**Note:** Refer to Figure 19-2 for load conditions.

**TABLE 19-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C5X-40**

| **AC Characteristics** | | **Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C for commercial | | | | |
|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** |
| 10 | TosH2ckL | OSC1↑ to CLKOUT↓(1,2) | — | 15 | 30** | ns |
| 11 | TosH2ckH | OSC1↑ to CLKOUT↑(1,2) | — | 15 | 30** | ns |
| 12 | TckR | CLKOUT rise time(1,2) | — | 5.0 | 15** | ns |
| 13 | TckF | CLKOUT fall time(1,2) | — | 5.0 | 15** | ns |
| 14 | TckL2ioV | CLKOUT↓ to Port out valid(1,2) | — | — | 40** | ns |
| 15 | TioV2ckH | Port in valid before CLKOUT↑(1,2) | 0.25 TCY+30* | — | — | ns |
| 16 | TckH2ioI | Port in hold after CLKOUT↑(1,2) | 0* | — | — | ns |
| 17 | TosH2ioV | OSC1↑ (Q1 cycle) to Port out valid(2) | — | — | 100 | ns |
| 18 | TosH2ioI | OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time) | TBD | — | — | ns |
| 19 | TioV2osH | Port input valid to OSC1↑ (I/O in setup time) | TBD | — | — | ns |
| 20 | TioR | Port output rise time(2) | — | 10 | 25** | ns |
| 21 | TioF | Port output fall time(2) | — | 10 | 25** | ns |

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

**2:** Refer to Figure 19-2 for load conditions.



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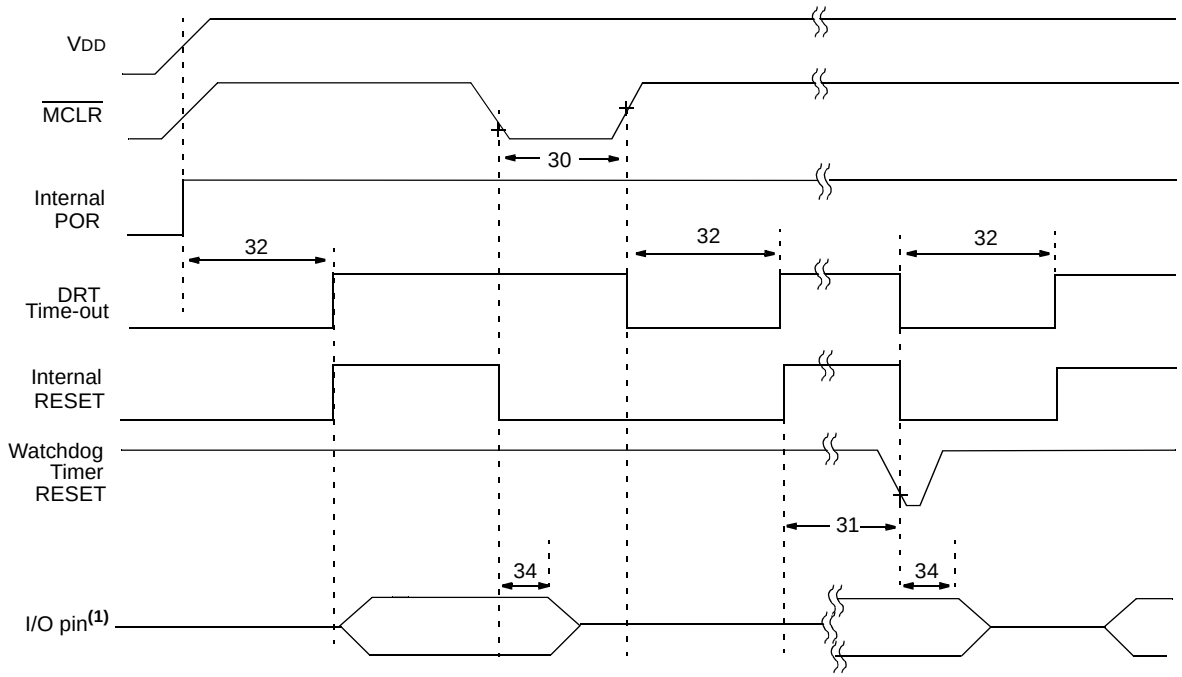
**FIGURE 19-5: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C5X-40**




**Note 1:** Please refer to Figure 19-2 for load conditions.

**TABLE 19-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C5X-40**

| AC Characteristics | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature 0°C ≤ TA ≤ +70°C (commercial)<br>Operating Voltage VDD range is described in Section 19.1. | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| 30 | TmcL | $\overline{\text{MCLR}}$ Pulse Width (low) | 1000* | — | — | ns | VDD = 5.0V |
| 31 | Twdt | Watchdog Timer Time-out Period (No Prescaler) | 9.0* | 18* | 30* | ms | VDD = 5.0V (Comm) |
| 32 | TDRT | Device Reset Timer Period | 9.0* | 18* | 30* | ms | VDD = 5.0V (Comm) |
| 34 | Tioz | I/O Hi-impedance from $\overline{\text{MCLR}}$ Low | 100* | 300* | 1000* | ns | |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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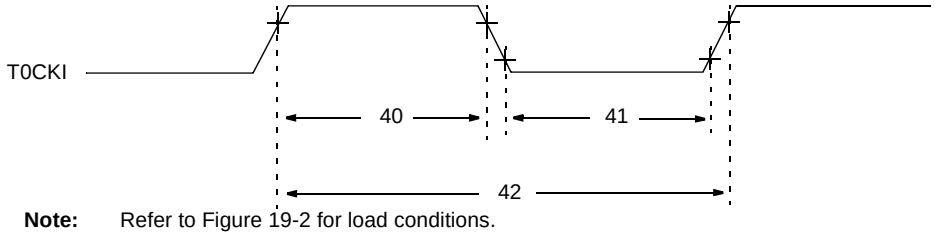
**FIGURE 19-6: TIMER0 CLOCK TIMINGS - PIC16C5X-40**




**Note:** Refer to Figure 19-2 for load conditions.

**TABLE 19-4: TIMER0 CLOCK REQUIREMENTS PIC16C5X-40**

| **AC Characteristics** | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature 0°C ≤ TA ≤ +70°C for commercial | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ†** | **Max** | **Units** | **Conditions** |
| 40 | Tt0H | T0CKI High Pulse Width<br>- No Prescaler | 0.5 TCY + 20* | — | — | ns | |
| | | - With Prescaler | 10* | — | — | ns | |
| 41 | Tt0L | T0CKI Low Pulse Width<br>- No Prescaler | 0.5 TCY + 20* | — | — | ns | |
| | | - With Prescaler | 10* | — | — | ns | |
| 42 | Tt0P | T0CKI Period | 20 or $\frac{T_{CY} + 40}{N}$* | — | — | ns | Whichever is greater.<br>N = Prescale Value (1, 2, 4,..., 256) |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.



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**NOTES:**

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## 20.0 DEVICE CHARACTERIZATION - PIC16LC54C 40MHz

The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean – 3σ) respectively, where σ is a standard deviation, over the whole temperature range.

**FIGURE 20-1: TYPICAL IPD vs. VDD, WATCHDOG DISABLED (25°C)**

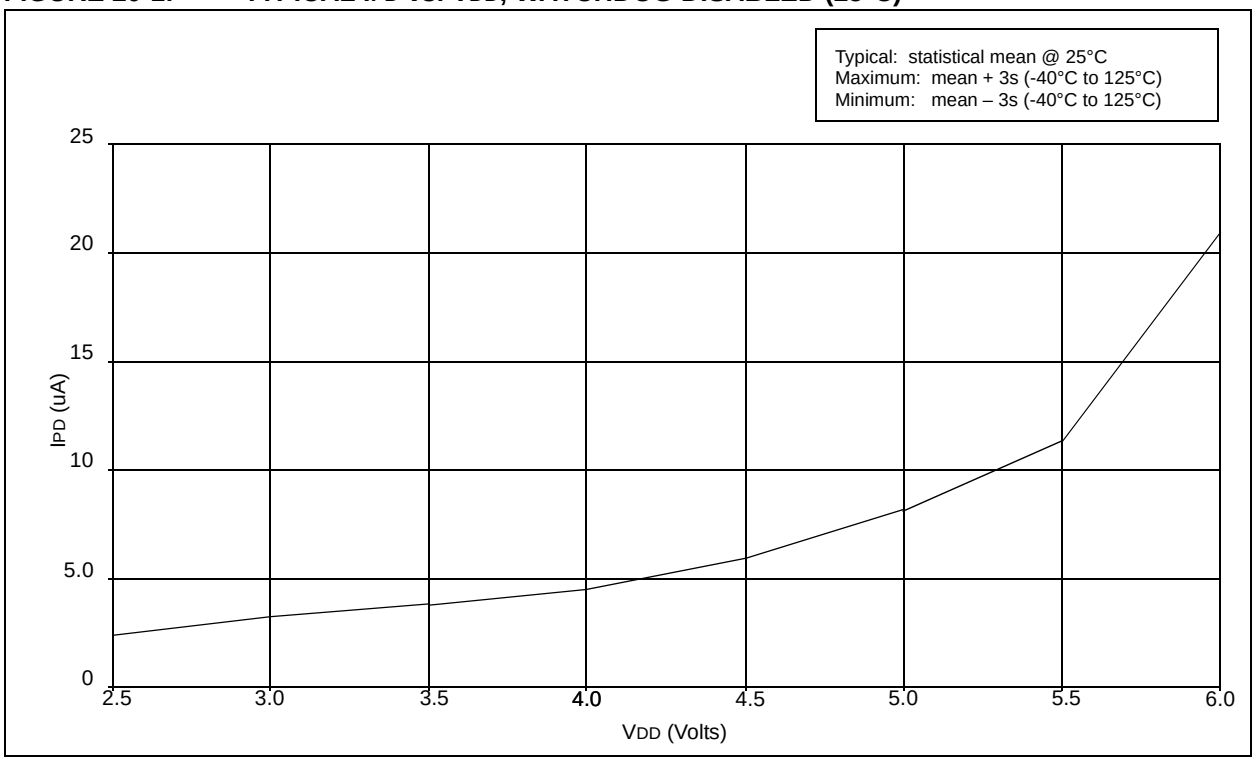




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**FIGURE 20-2: TYPICAL IPD vs. VDD, WATCHDOG ENABLED (25°C)**

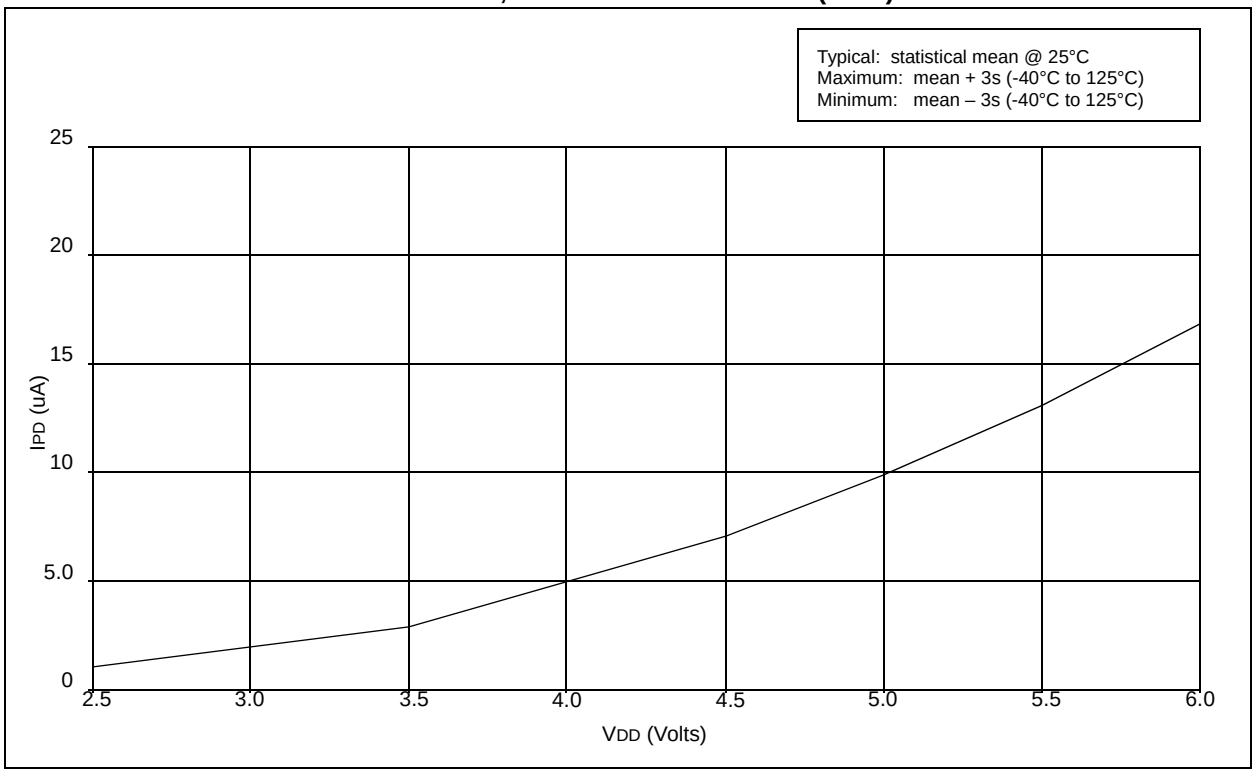


**FIGURE 20-3: TYPICAL IPD vs. VDD, WATCHDOG ENABLED (–40°C, 85°C)**

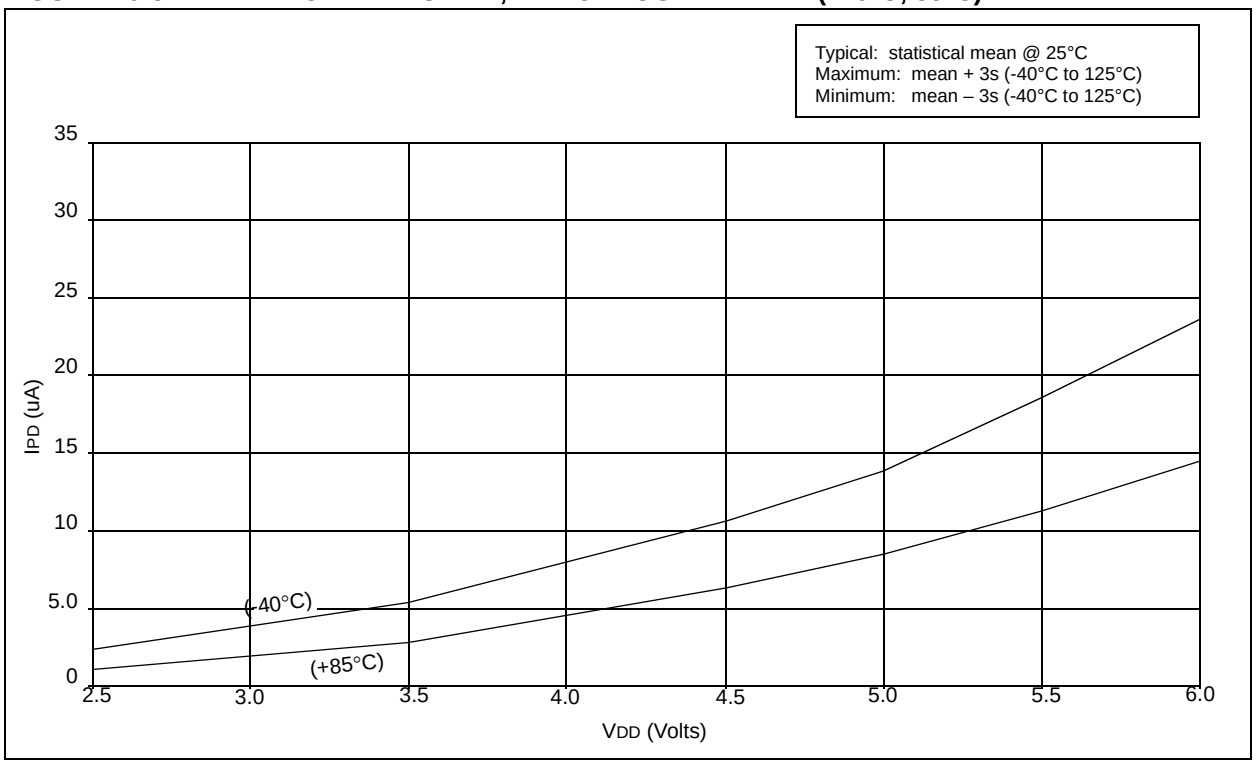


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**FIGURE 20-4: VTH (INPUT THRESHOLD TRIP POINT VOLTAGE) OF I/O PINS vs. VDD**

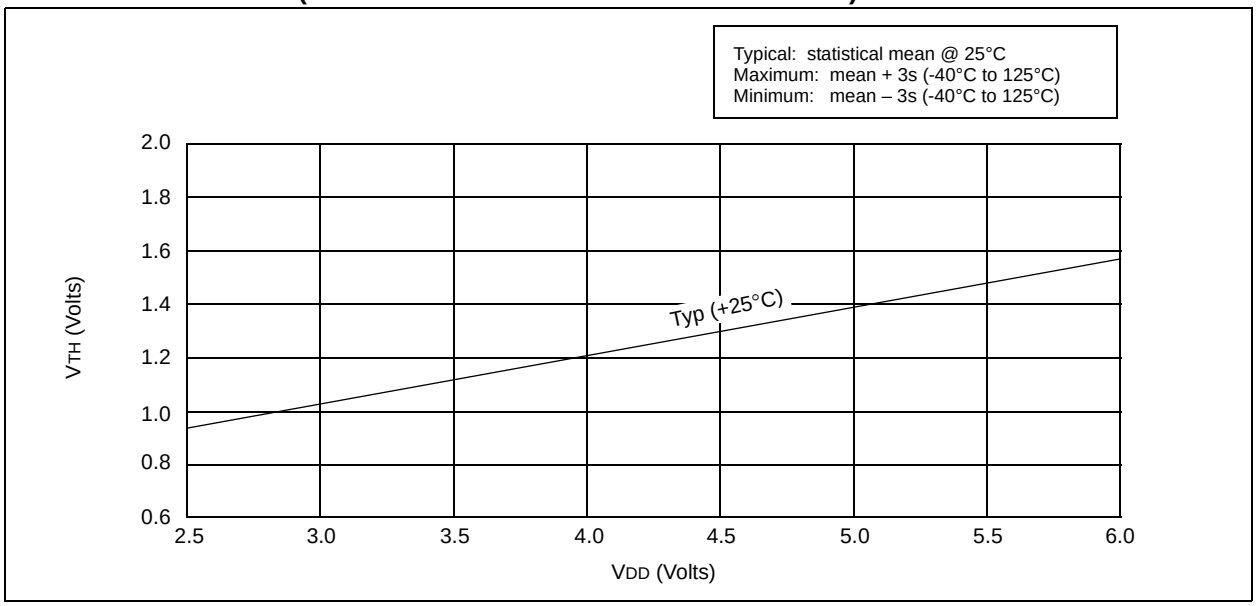


**FIGURE 20-5: VTH (INPUT THRESHOLD TRIP POINT VOLTAGE) OF OSC1 INPUT (HS MODE) vs. VDD**

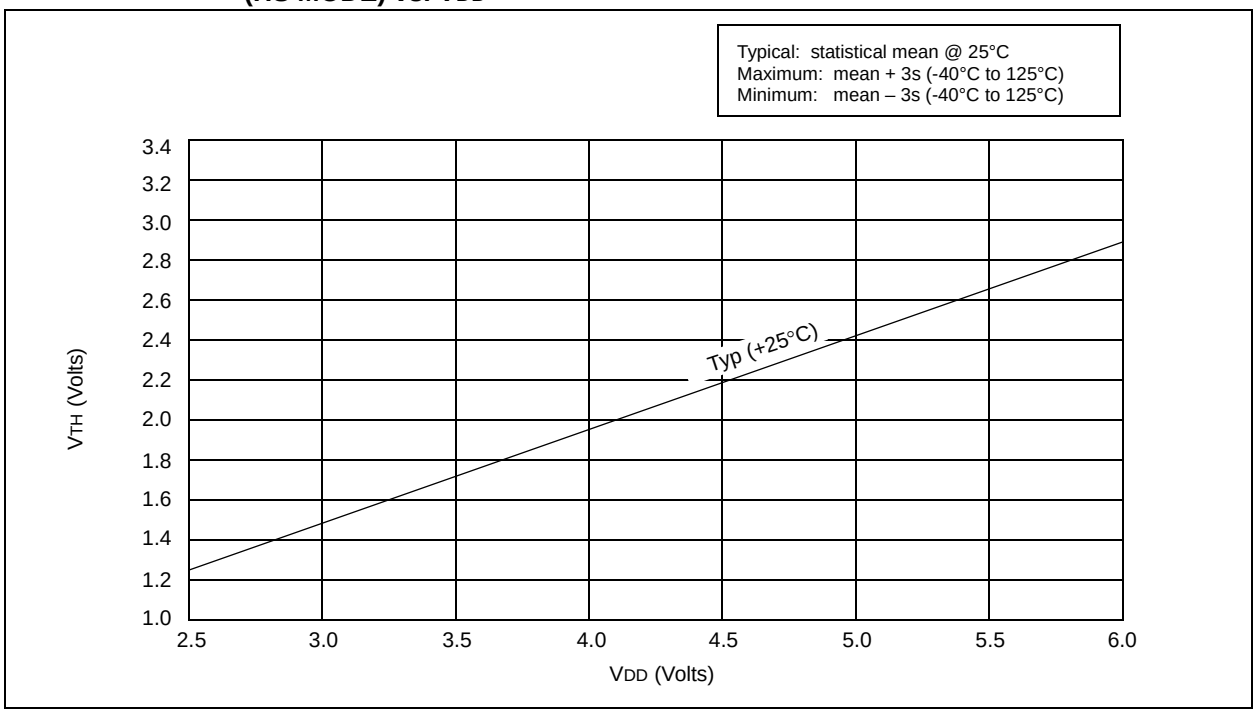




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**FIGURE 20-6: TYPICAL IDD vs. VDD (40 MHZ, WDT DISABLED, HS MODE, 70°C)**

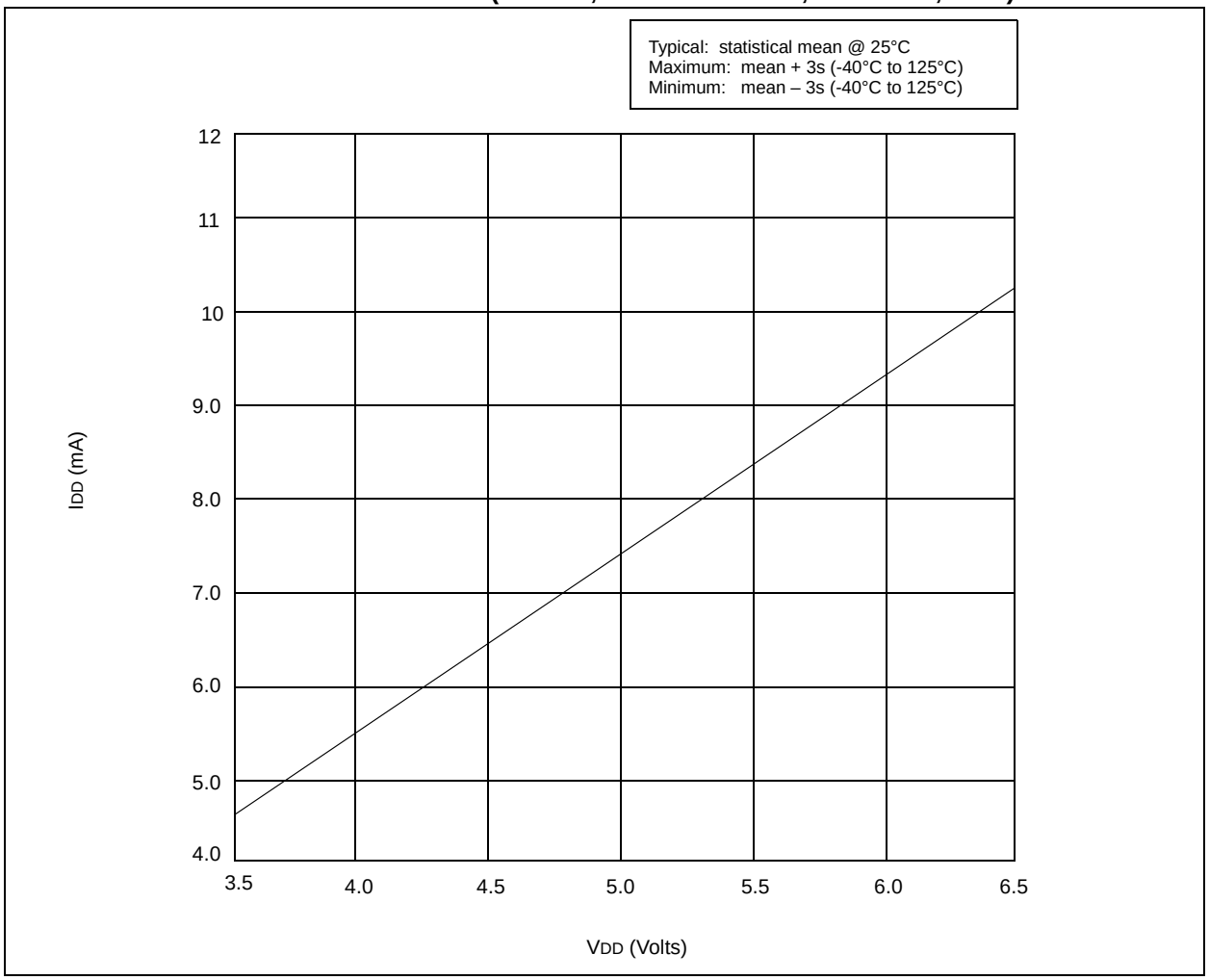


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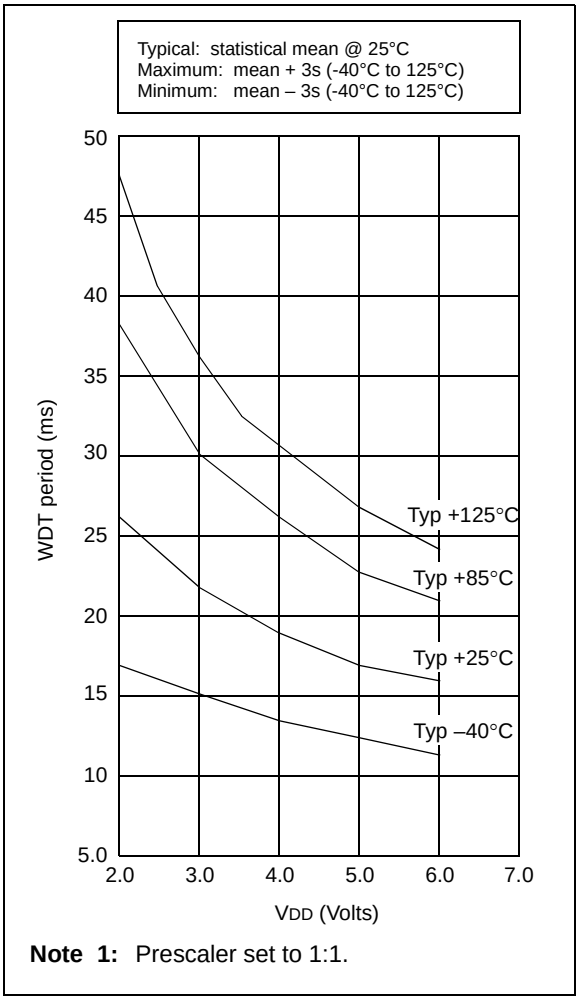
**FIGURE 20-7: WDT TIMER TIME-OUT PERIOD vs. VDD(1)**




**Note 1:** Prescaler set to 1:1.

**FIGURE 20-8: IOH vs. VOH, VDD = 5 V**

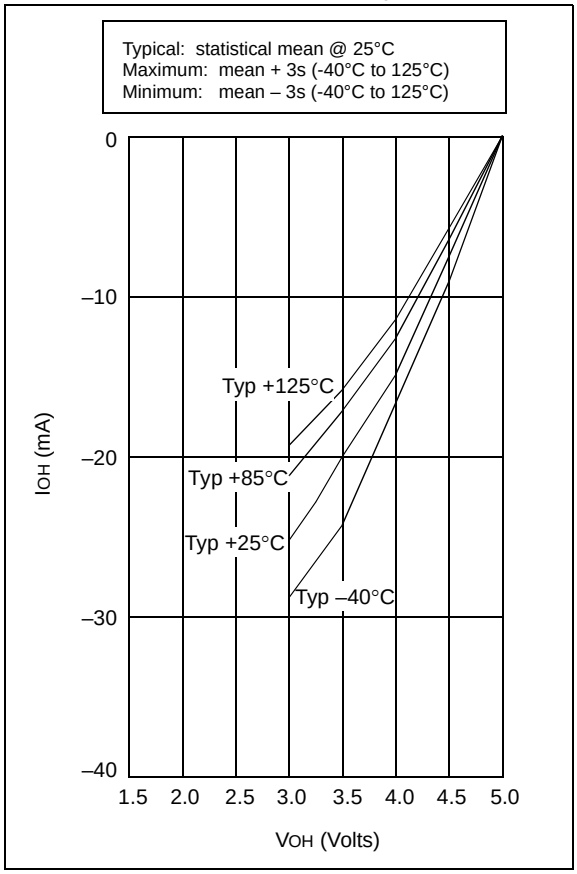



**TABLE 20-1: INPUT CAPACITANCE**

| Pin | Typical Capacitance (pF) | |
|---|---|---|
| | 18L PDIP | 18L SOIC |
| RA port | 5.0 | 4.3 |
| RB port | 5.0 | 4.3 |
| $\overline{MCLR}$ | 17.0 | 17.0 |
| OSC1 | 4.0 | 3.5 |
| OSC2/CLKOUT | 4.3 | 3.5 |
| T0CKI | 3.2 | 2.8 |

All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.



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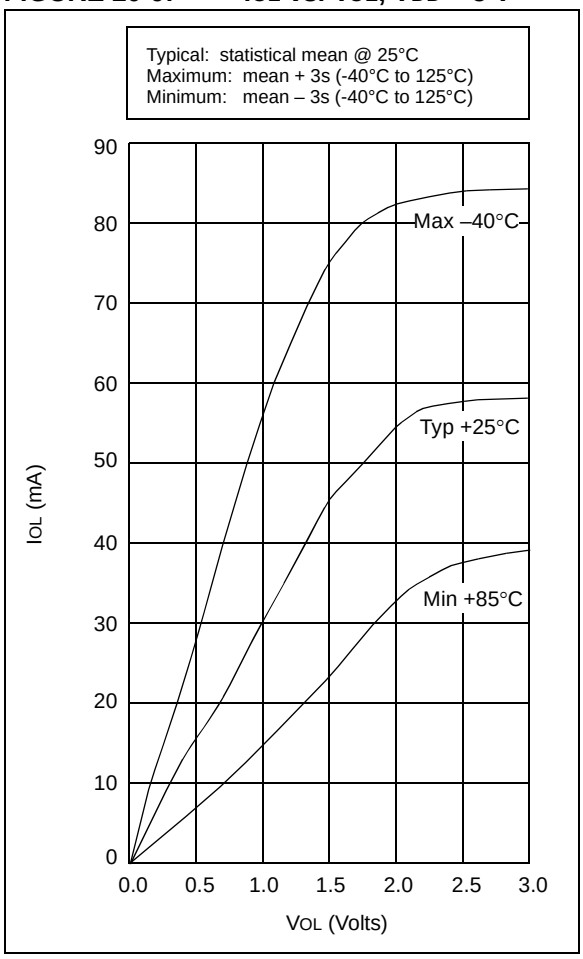
**FIGURE 20-9: IOL vs. VOL, VDD = 5 V**

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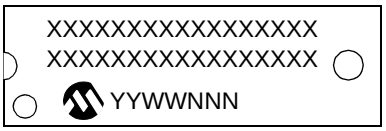
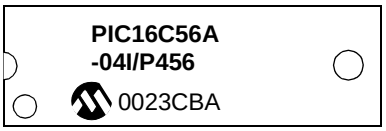
## 21.0 PACKAGING INFORMATION

### 21.1 Package Marketing Information

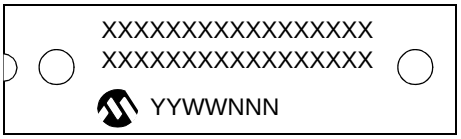
18-Lead PDIP



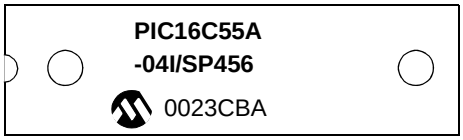

Example



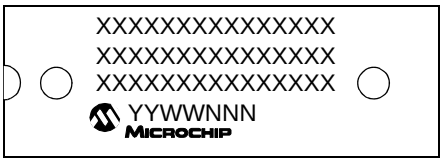

28-Lead Skinny PDIP (.300")



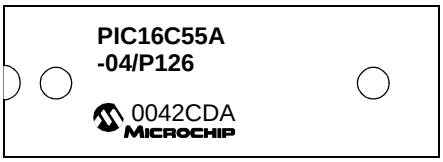

Example




28-Lead PDIP (.600")



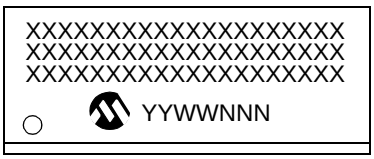

Example




18-Lead SOIC

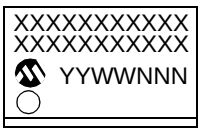
Example

28-Lead SOIC




Example

20-Lead SSOP




Example

28-Lead SSOP

Example

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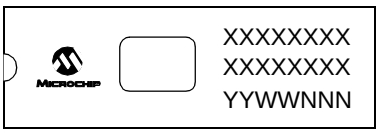
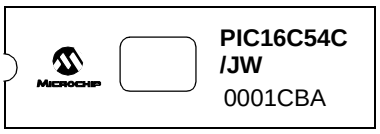
## Package Marking Information (Cont'd)

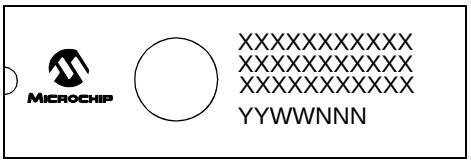
18-Lead CERDIP Windowed



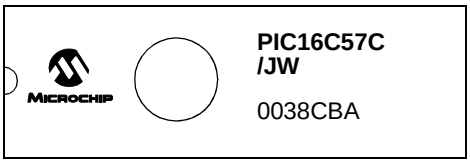

Example




28-Lead CERDIP Windowed




Example




| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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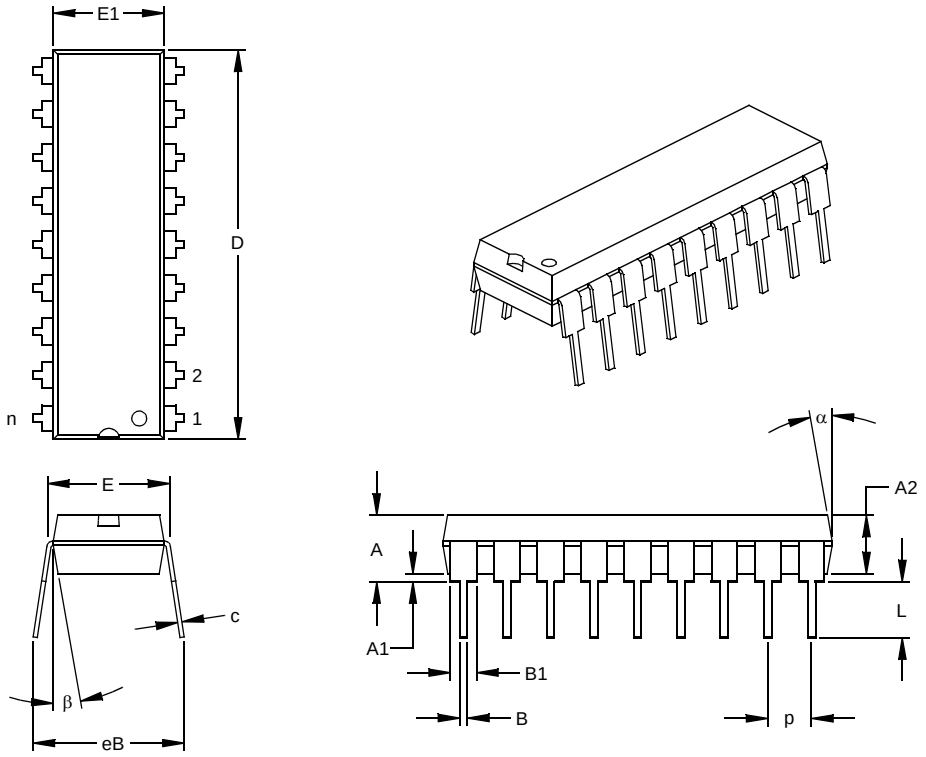
### 18-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 18 | | | 18 | |
| Pitch | p | | .100 | | | 2.54 | |
| Top to Seating Plane | A | .140 | .155 | .170 | 3.56 | 3.94 | 4.32 |
| Molded Package Thickness | A2 | .115 | .130 | .145 | 2.92 | 3.30 | 3.68 |
| Base to Seating Plane | A1 | .015 | | | 0.38 | | |
| Shoulder to Shoulder Width | E | .300 | .313 | .325 | 7.62 | 7.94 | 8.26 |
| Molded Package Width | E1 | .240 | .250 | .260 | 6.10 | 6.35 | 6.60 |
| Overall Length | D | .890 | .898 | .905 | 22.61 | 22.80 | 22.99 |
| Tip to Seating Plane | L | .125 | .130 | .135 | 3.18 | 3.30 | 3.43 |
| Lead Thickness | c | .008 | .012 | .015 | 0.20 | 0.29 | 0.38 |
| Upper Lead Width | B1 | .045 | .058 | .070 | 1.14 | 1.46 | 1.78 |
| Lower Lead Width | B | .014 | .018 | .022 | 0.36 | 0.46 | 0.56 |
| Overall Row Spacing § | eB | .310 | .370 | .430 | 7.87 | 9.40 | 10.92 |
| Mold Draft Angle Top | α | 5 | 10 | 15 | 5 | 10 | 15 |
| Mold Draft Angle Bottom | β | 5 | 10 | 15 | 5 | 10 | 15 |

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-007



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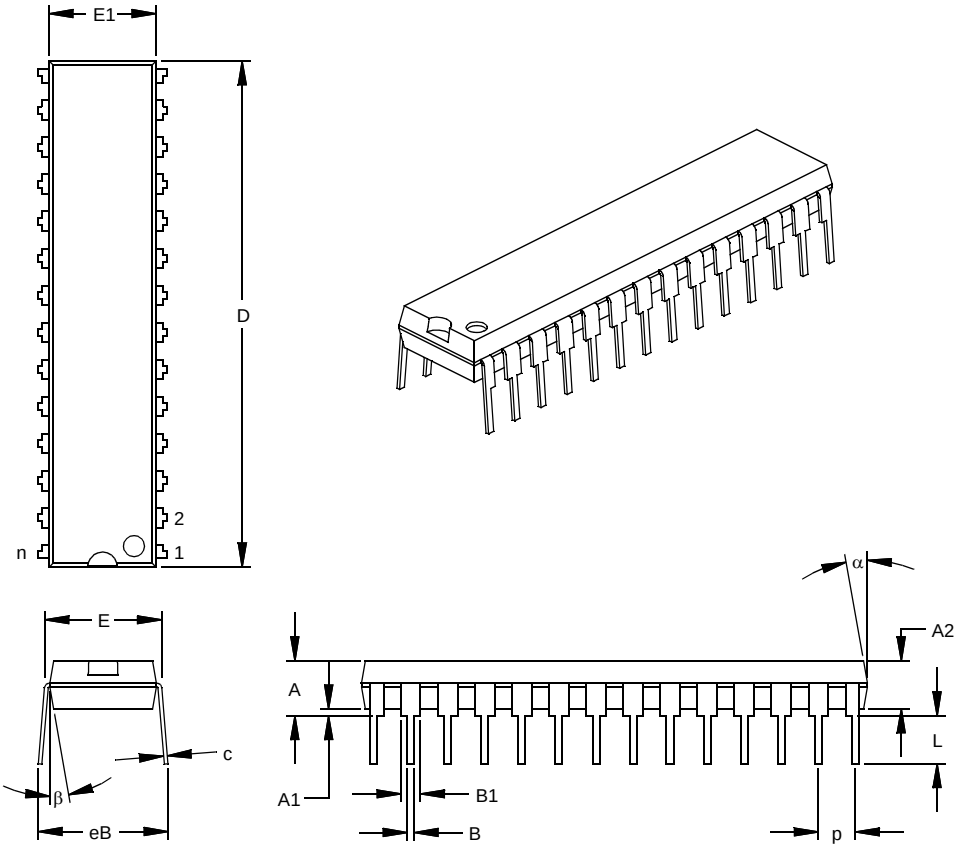
### 28-Lead Skinny Plastic Dual In-line (SP) – 300 mil (PDIP)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 28 | | | 28 | |
| Pitch | p | | .100 | | | 2.54 | |
| Top to Seating Plane | A | .140 | .150 | .160 | 3.56 | 3.81 | 4.06 |
| Molded Package Thickness | A2 | .125 | .130 | .135 | 3.18 | 3.30 | 3.43 |
| Base to Seating Plane | A1 | .015 | | | 0.38 | | |
| Shoulder to Shoulder Width | E | .300 | .310 | .325 | 7.62 | 7.87 | 8.26 |
| Molded Package Width | E1 | .275 | .285 | .295 | 6.99 | 7.24 | 7.49 |
| Overall Length | D | 1.345 | 1.365 | 1.385 | 34.16 | 34.67 | 35.18 |
| Tip to Seating Plane | L | .125 | .130 | .135 | 3.18 | 3.30 | 3.43 |
| Lead Thickness | c | .008 | .012 | .015 | 0.20 | 0.29 | 0.38 |
| Upper Lead Width | B1 | .040 | .053 | .065 | 1.02 | 1.33 | 1.65 |
| Lower Lead Width | B | .016 | .019 | .022 | 0.41 | 0.48 | 0.56 |
| Overall Row Spacing § | eB | .320 | .350 | .430 | 8.13 | 8.89 | 10.92 |
| Mold Draft Angle Top | α | 5 | 10 | 15 | 5 | 10 | 15 |
| Mold Draft Angle Bottom | β | 5 | 10 | 15 | 5 | 10 | 15 |

* Controlling Parameter
§ Significant Characteristic
Notes:
Dimension D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MO-095
Drawing No. C04-070

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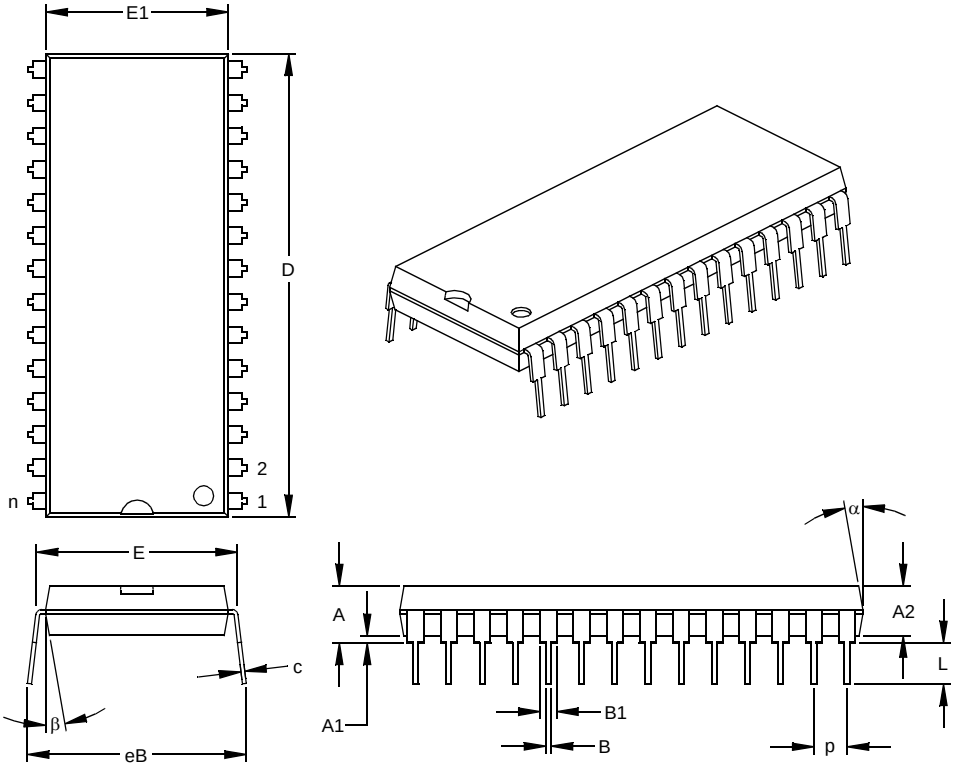
### 28-Lead Plastic Dual In-line (P) – 600 mil (PDIP)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 28 | | | 28 | |
| Pitch | p | | .100 | | | 2.54 | |
| Top to Seating Plane | A | .160 | .175 | .190 | 4.06 | 4.45 | 4.83 |
| Molded Package Thickness | A2 | .140 | .150 | .160 | 3.56 | 3.81 | 4.06 |
| Base to Seating Plane | A1 | .015 | | | 0.38 | | |
| Shoulder to Shoulder Width | E | .595 | .600 | .625 | 15.11 | 15.24 | 15.88 |
| Molded Package Width | E1 | .505 | .545 | .560 | 12.83 | 13.84 | 14.22 |
| Overall Length | D | 1.395 | 1.430 | 1.465 | 35.43 | 36.32 | 37.21 |
| Tip to Seating Plane | L | .120 | .130 | .135 | 3.05 | 3.30 | 3.43 |
| Lead Thickness | c | .008 | .012 | .015 | 0.20 | 0.29 | 0.38 |
| Upper Lead Width | B1 | .030 | .050 | .070 | 0.76 | 1.27 | 1.78 |
| Lower Lead Width | B | .014 | .018 | .022 | 0.36 | 0.46 | 0.56 |
| Overall Row Spacing § | eB | .620 | .650 | .680 | 15.75 | 16.51 | 17.27 |
| Mold Draft Angle Top | α | 5 | 10 | 15 | 5 | 10 | 15 |
| Mold Draft Angle Bottom | β | 5 | 10 | 15 | 5 | 10 | 15 |

* Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MO-011
Drawing No. C04-079



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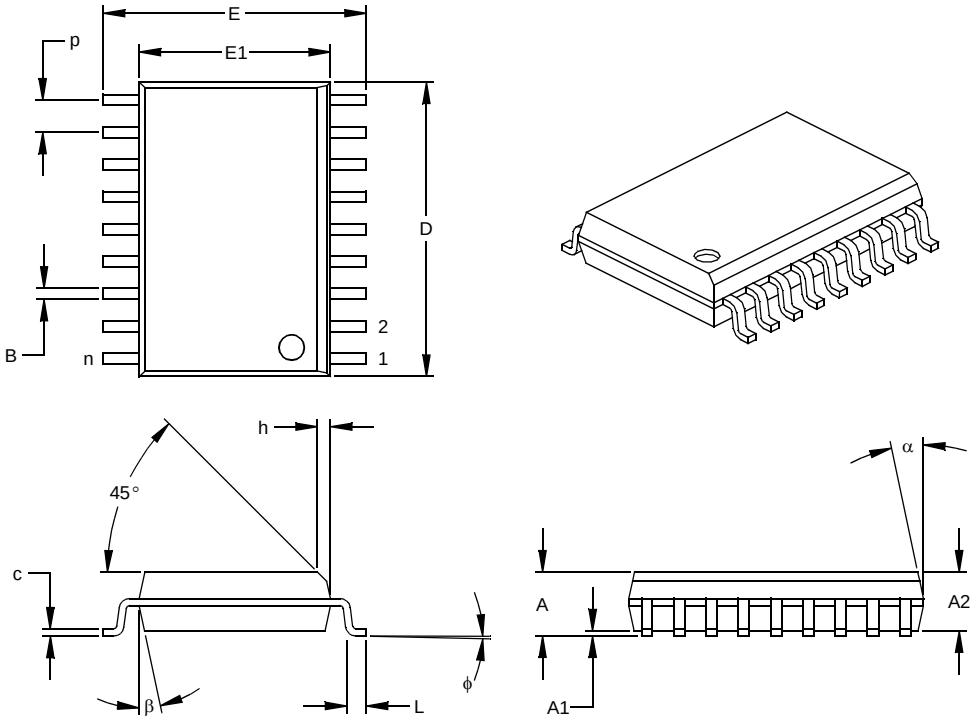
### 18-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 18 | | | 18 | |
| Pitch | p | | .050 | | | 1.27 | |
| Overall Height | A | .093 | .099 | .104 | 2.36 | 2.50 | 2.64 |
| Molded Package Thickness | A2 | .088 | .091 | .094 | 2.24 | 2.31 | 2.39 |
| Standoff § | A1 | .004 | .008 | .012 | 0.10 | 0.20 | 0.30 |
| Overall Width | E | .394 | .407 | .420 | 10.01 | 10.34 | 10.67 |
| Molded Package Width | E1 | .291 | .295 | .299 | 7.39 | 7.49 | 7.59 |
| Overall Length | D | .446 | .454 | .462 | 11.33 | 11.53 | 11.73 |
| Chamfer Distance | h | .010 | .020 | .029 | 0.25 | 0.50 | 0.74 |
| Foot Length | L | .016 | .033 | .050 | 0.41 | 0.84 | 1.27 |
| Foot Angle | ϕ | 0 | 4 | 8 | 0 | 4 | 8 |
| Lead Thickness | c | .009 | .011 | .012 | 0.23 | 0.27 | 0.30 |
| Lead Width | B | .014 | .017 | .020 | 0.36 | 0.42 | 0.51 |
| Mold Draft Angle Top | α | 0 | 12 | 15 | 0 | 12 | 15 |
| Mold Draft Angle Bottom | β | 0 | 12 | 15 | 0 | 12 | 15 |

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-013
Drawing No. C04-051

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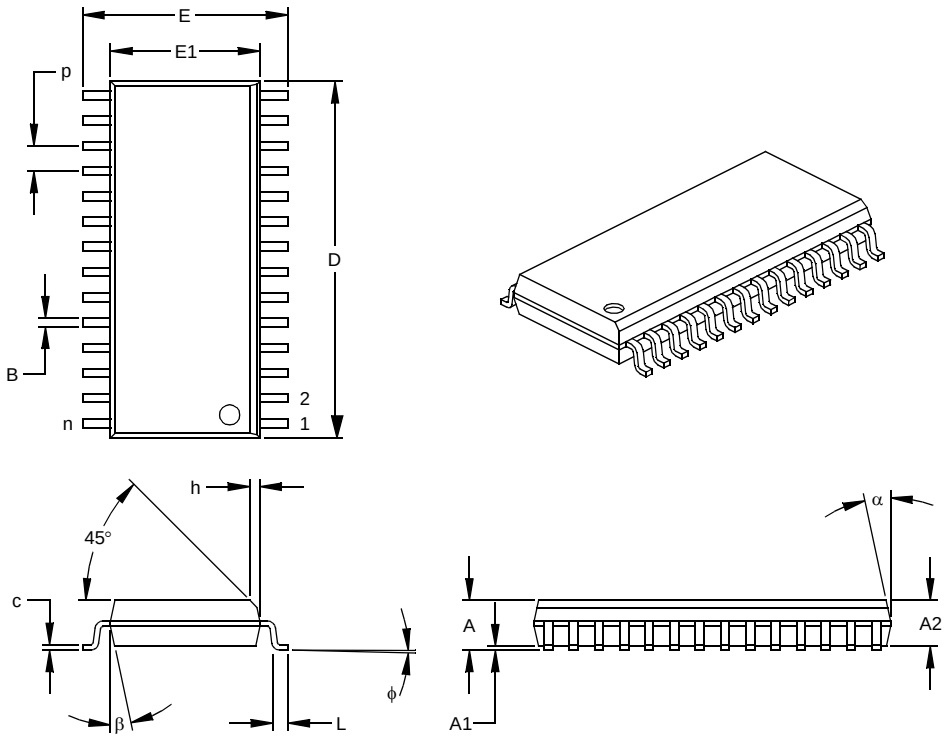
### 28-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 28 | | | 28 | |
| Pitch | p | | .050 | | | 1.27 | |
| Overall Height | A | .093 | .099 | .104 | 2.36 | 2.50 | 2.64 |
| Molded Package Thickness | A2 | .088 | .091 | .094 | 2.24 | 2.31 | 2.39 |
| Standoff § | A1 | .004 | .008 | .012 | 0.10 | 0.20 | 0.30 |
| Overall Width | E | .394 | .407 | .420 | 10.01 | 10.34 | 10.67 |
| Molded Package Width | E1 | .288 | .295 | .299 | 7.32 | 7.49 | 7.59 |
| Overall Length | D | .695 | .704 | .712 | 17.65 | 17.87 | 18.08 |
| Chamfer Distance | h | .010 | .020 | .029 | 0.25 | 0.50 | 0.74 |
| Foot Length | L | .016 | .033 | .050 | 0.41 | 0.84 | 1.27 |
| Foot Angle Top | ϕ | 0 | 4 | 8 | 0 | 4 | 8 |
| Lead Thickness | c | .009 | .011 | .013 | 0.23 | 0.28 | 0.33 |
| Lead Width | B | .014 | .017 | .020 | 0.36 | 0.42 | 0.51 |
| Mold Draft Angle Top | α | 0 | 12 | 15 | 0 | 12 | 15 |
| Mold Draft Angle Bottom | β | 0 | 12 | 15 | 0 | 12 | 15 |

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-013
Drawing No. C04-052



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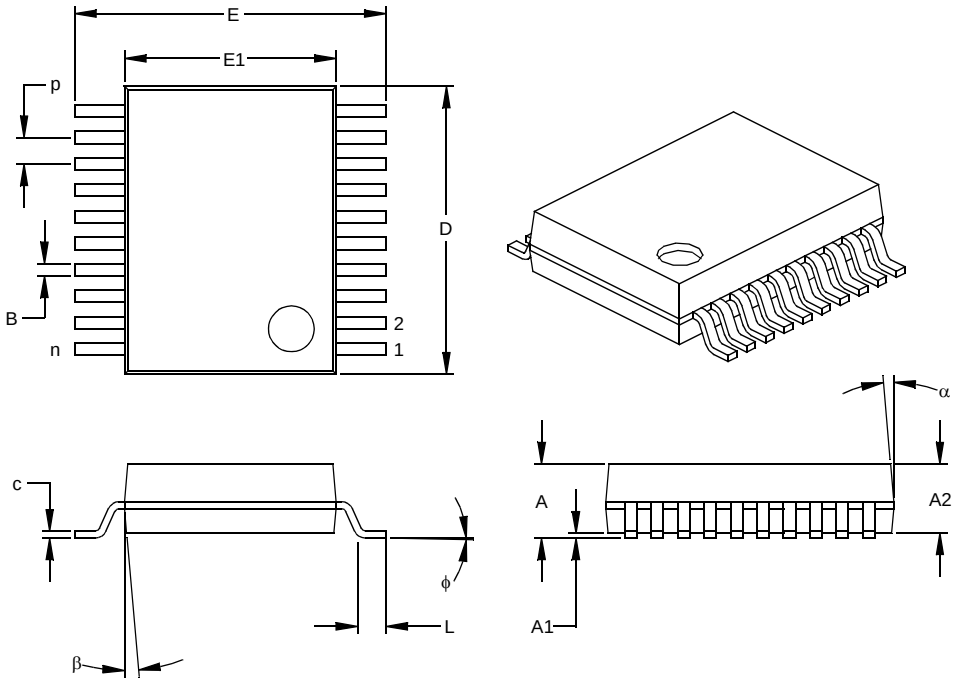
### 20-Lead Plastic Shrink Small Outline (SS) – 209 mil, 5.30 mm (SSOP)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 20 | | | 20 | |
| Pitch | p | | .026 | | | 0.65 | |
| Overall Height | A | .068 | .073 | .078 | 1.73 | 1.85 | 1.98 |
| Molded Package Thickness | A2 | .064 | .068 | .072 | 1.63 | 1.73 | 1.83 |
| Standoff § | A1 | .002 | .006 | .010 | 0.05 | 0.15 | 0.25 |
| Overall Width | E | .299 | .309 | .322 | 7.59 | 7.85 | 8.18 |
| Molded Package Width | E1 | .201 | .207 | .212 | 5.11 | 5.25 | 5.38 |
| Overall Length | D | .278 | .284 | .289 | 7.06 | 7.20 | 7.34 |
| Foot Length | L | .022 | .030 | .037 | 0.56 | 0.75 | 0.94 |
| Lead Thickness | c | .004 | .007 | .010 | 0.10 | 0.18 | 0.25 |
| Foot Angle | ϕ | 0 | 4 | 8 | 0.00 | 101.60 | 203.20 |
| Lead Width | B | .010 | .013 | .015 | 0.25 | 0.32 | 0.38 |
| Mold Draft Angle Top | α | 0 | 5 | 10 | 0 | 5 | 10 |
| Mold Draft Angle Bottom | β | 0 | 5 | 10 | 0 | 5 | 10 |

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MO-150
Drawing No. C04-072

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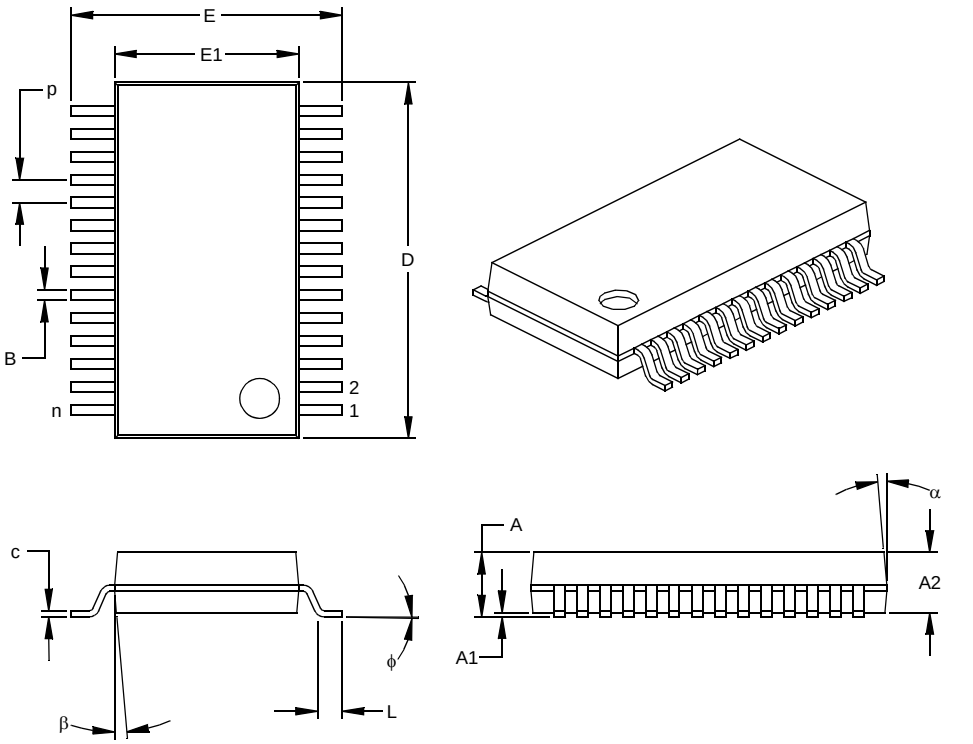
### 28-Lead Plastic Shrink Small Outline (SS) – 209 mil, 5.30 mm (SSOP)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | | MILLIMETERS* | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 28 | | | 28 | |
| Pitch | p | | .026 | | | 0.65 | |
| Overall Height | A | .068 | .073 | .078 | 1.73 | 1.85 | 1.98 |
| Molded Package Thickness | A2 | .064 | .068 | .072 | 1.63 | 1.73 | 1.83 |
| Standoff § | A1 | .002 | .006 | .010 | 0.05 | 0.15 | 0.25 |
| Overall Width | E | .299 | .309 | .319 | 7.59 | 7.85 | 8.10 |
| Molded Package Width | E1 | .201 | .207 | .212 | 5.11 | 5.25 | 5.38 |
| Overall Length | D | .396 | .402 | .407 | 10.06 | 10.20 | 10.34 |
| Foot Length | L | .022 | .030 | .037 | 0.56 | 0.75 | 0.94 |
| Lead Thickness | c | .004 | .007 | .010 | 0.10 | 0.18 | 0.25 |
| Foot Angle | ϕ | 0 | 4 | 8 | 0.00 | 101.60 | 203.20 |
| Lead Width | B | .010 | .013 | .015 | 0.25 | 0.32 | 0.38 |
| Mold Draft Angle Top | α | 0 | 5 | 10 | 0 | 5 | 10 |
| Mold Draft Angle Bottom | β | 0 | 5 | 10 | 0 | 5 | 10 |

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-150
Drawing No. C04-073



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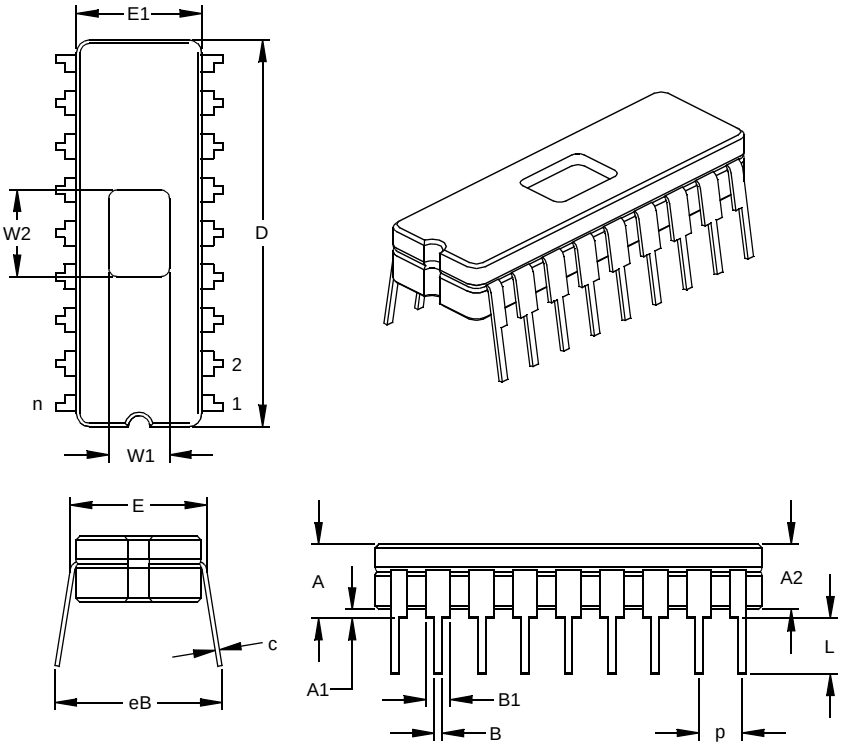
### 18-Lead Ceramic Dual In-line with Window (JW) – 300 mil (CERDIP)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 18 | | | 18 | |
| Pitch | p | | .100 | | | 2.54 | |
| Top to Seating Plane | A | .170 | .183 | .195 | 4.32 | 4.64 | 4.95 |
| Ceramic Package Height | A2 | .155 | .160 | .165 | 3.94 | 4.06 | 4.19 |
| Standoff | A1 | .015 | .023 | .030 | 0.38 | 0.57 | 0.76 |
| Shoulder to Shoulder Width | E | .300 | .313 | .325 | 7.62 | 7.94 | 8.26 |
| Ceramic Pkg. Width | E1 | .285 | .290 | .295 | 7.24 | 7.37 | 7.49 |
| Overall Length | D | .880 | .900 | .920 | 22.35 | 22.86 | 23.37 |
| Tip to Seating Plane | L | .125 | .138 | .150 | 3.18 | 3.49 | 3.81 |
| Lead Thickness | c | .008 | .010 | .012 | 0.20 | 0.25 | 0.30 |
| Upper Lead Width | B1 | .050 | .055 | .060 | 1.27 | 1.40 | 1.52 |
| Lower Lead Width | B | .016 | .019 | .021 | 0.41 | 0.47 | 0.53 |
| Overall Row Spacing § | eB | .345 | .385 | .425 | 8.76 | 9.78 | 10.80 |
| Window Width | W1 | .130 | .140 | .150 | 3.30 | 3.56 | 3.81 |
| Window Length | W2 | .190 | .200 | .210 | 4.83 | 5.08 | 5.33 |

* Controlling Parameter
§ Significant Characteristic
JEDEC Equivalent: MO-036
Drawing No. C04-010

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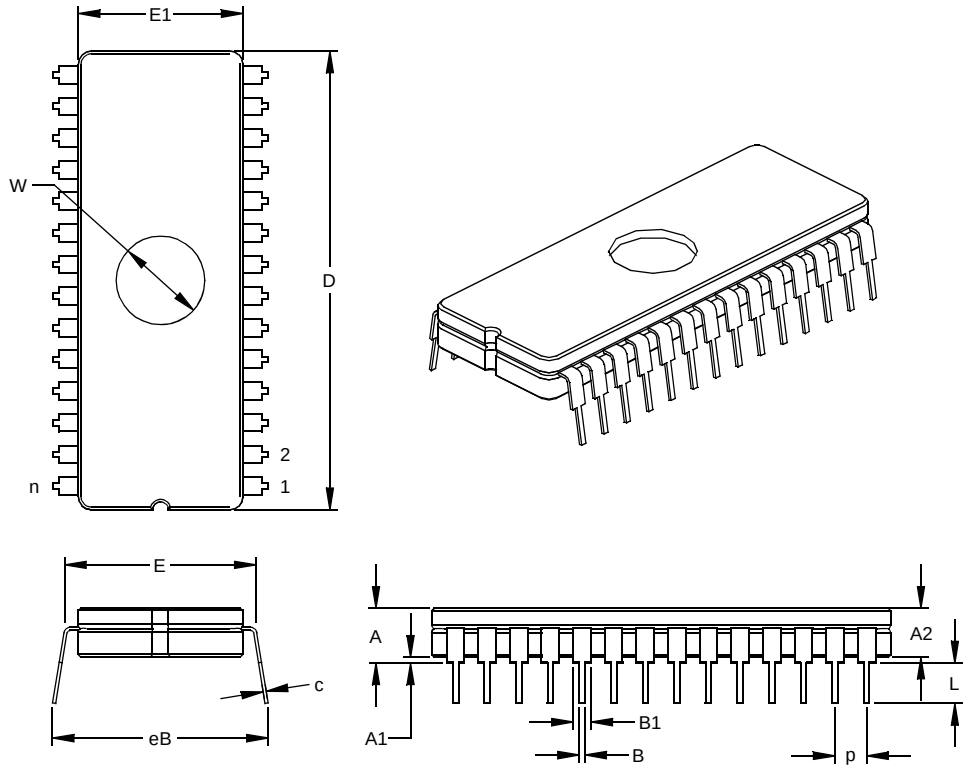
### 28-Lead Ceramic Dual In-line with Window (JW) – 600 mil (CERDIP)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 28 | | | 28 | |
| Pitch | p | | .100 | | | 2.54 | |
| Top to Seating Plane | A | .195 | .210 | .225 | 4.95 | 5.33 | 5.72 |
| Ceramic Package Height | A2 | .155 | .160 | .165 | 3.94 | 4.06 | 4.19 |
| Standoff | A1 | .015 | .038 | .060 | 0.38 | 0.95 | 1.52 |
| Shoulder to Shoulder Width | E | .595 | .600 | .625 | 15.11 | 15.24 | 15.88 |
| Ceramic Pkg. Width | E1 | .514 | .520 | .526 | 13.06 | 13.21 | 13.36 |
| Overall Length | D | 1.430 | 1.460 | 1.490 | 36.32 | 37.08 | 37.85 |
| Tip to Seating Plane | L | .125 | .138 | .150 | 3.18 | 3.49 | 3.81 |
| Lead Thickness | c | .008 | .010 | .012 | 0.20 | 0.25 | 0.30 |
| Upper Lead Width | B1 | .050 | .058 | .065 | 1.27 | 1.46 | 1.65 |
| Lower Lead Width | B | .016 | .020 | .023 | 0.41 | 0.51 | 0.58 |
| Overall Row Spacing § | eB | .610 | .660 | .710 | 15.49 | 16.76 | 18.03 |
| Window Diameter | W | .270 | .280 | .290 | 6.86 | 7.11 | 7.37 |

* Controlling Parameter
§ Significant Characteristic
JEDEC Equivalent: MO-103
Drawing No. C04-013



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## APPENDIX A: COMPATIBILITY

To convert code written for PIC16CXX to PIC16C5X, the user should take the following steps:

1. Check any `CALL`, `GOTO` or instructions that modify the PC to determine if any program memory page select operations (PA2, PA1, PA0 bits) need to be made.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any special function register page switching. Redefine data variables to reallocate them.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change RESET vector to proper value for processor used.
6. Remove any use of the `ADDLW`, `RETURN` and `SUBLW` instructions.
7. Rewrite any code segments that use interrupts.

## APPENDIX B: REVISION HISTORY

**Revision KE (January 2013)**

Added a note to each package outline drawing.

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## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | - | XX | X | /XX | XXX |
|---|---|---|---|---|---|
| Device | | Frequency Range/OSC Type | Temperature Range | Package | Pattern |

| | | |
|---|---|---|
| Device | PIC16C54 | PIC16C54T(2) |
| | PIC16C54A | PIC16C54AT(2) |
| | PIC16CR54A | PIC16CR54AT(2) |
| | PIC16C54C | PIC16C54CT(2) |
| | PIC16CR54C | PIC16CR54CT(2) |
| | PIC16C55 | PIC16C55T(2) |
| | PIC16C55A | PIC16C55AT(2) |
| | PIC16C56 | PIC16C56T(2) |
| | PIC16C56A | PIC16C56AT(2) |
| | PIC16CR56A | PIC16CR56AT(2) |
| | PIC16C57 | PIC16C57T(2) |
| | PIC16C57C | PIC16C57CT(2) |
| | PIC16CR57C | PIC16CR57CT(2) |
| | PIC16C58B | PIC16C58BT(2) |
| | PIC16CR58B | PIC16CR58BT(2) |

| | | |
|---|---|---|
| Frequency Range/ Oscillator Type | RC | Resistor Capacitor |
| | LP | Low Power Crystal |
| | XT | Standard Crystal/Resonator |
| | HS | High Speed Crystal |
| | 02 | 200 KHz (LP) or 2 MHz (XT and RC) |
| | 04 | 200 KHz (LP) or 4 MHz (XT and RC) |
| | 10 | 10 MHz (HS only) |
| | 20 | 20 MHz (HS only) |
| | 40 | 40 MHz (HS only) |
| | b(4) | No oscillator type for JW packages(3) |

*RC/LP/XT/HS are for 16C54/55/56/57 devices only
-02 is available for 16LV54A only
-04/10/20 options are available for all other devices
-40 is available for 16C54C/55A/56A/57C/58B devices only

| | | | |
|---|---|---|---|
| Temperature Range | b(4) | = | 0°C to +70°C |
| | I | = | -40°C to +85°C |
| | E | = | -40°C to +125°C |

| | | | |
|---|---|---|---|
| Package | S | = | Die in Waffle Pack |
| | JW | = | 28-pin 600 mil/18-pin 300 mil windowed CERDIP(3) |
| | P | = | 28-pin 600 mil/18-pin 300 mil PDIP |
| | SO | = | 300 mil SOIC |
| | SS | = | 209 mil SSOP |
| | SP | = | 28-pin 300 mil Skinny PDIP |

*See Section 21 for additional package information.

| | |
|---|---|
| Pattern | QTP, SQTP, ROM code (factory specified) or Special Requirements. Blank for OTP and Windowed devices. |

**Examples:**

a) PIC16C55A - 04/P 301 = Commercial Temp., PDIP package, 4 MHz, standard VDD limits, QTP pattern #301

b) PIC16LC54C - 04I/SO Industrial Temp., SOIC package, 200 kHz, extended VDD limits

c) PIC16C57 - RC/SP = RC Oscillator, commercial temp, skinny PDIP package, 4 MHz, standard VDD limits

d) PIC16C58BT -40/SS 123 = commercial temp, SSOP package in tape and reel, 4 MHz, extended VDD limits, ROM pattern #123

**Note 1:** C = normal voltage range
LC = extended

**2:** T = in tape and reel - SOIC and SSOP packages only

**3:** JW Devices are UV erasable and can be programmed to any device configuration. JW Devices meet the electrical requirements of each oscillator type, including LC devices.

**4:** b = Blank

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Printed on recycled paper.

ISBN: 9781620769355

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