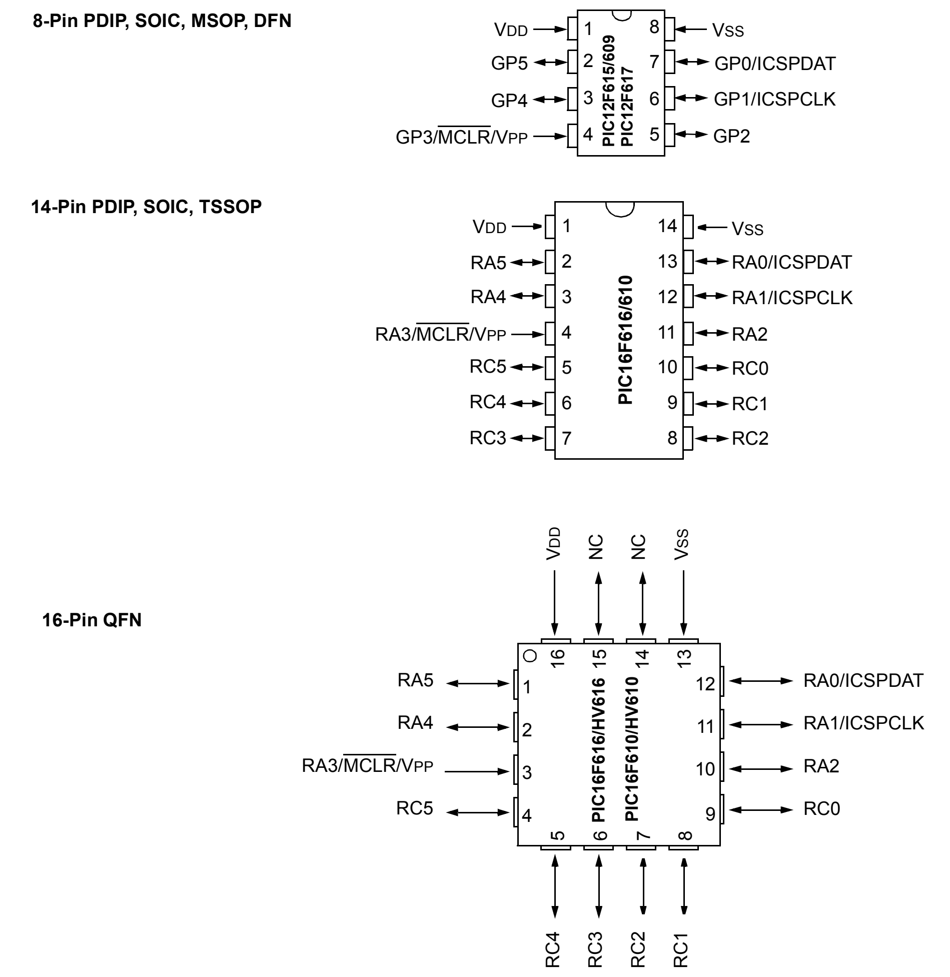
FIGURE 2-1: 8-PIN, 14-PIN, AND 16-PIN PROGRAMMING PINS DIAGRAM FOR PIC12F609/ 12F615/12F617/16F610/16F616[(1)]



Note 1: Please see specific data sheets for alternate pin functionality.

TABLE 2-1: PIN DESCRIPTIONS IN PROGRAM/VERIFY MODE: PIC12F609/12F615/12F617/ 16F610/16F616 AND PIC12HV609/12HV615/16HV610/16HV616

Pin Name	During Programming		
	Function	Pin Type	Pin Description
GP1/RA1	ICSPCLK	I	Clock input – Schmitt Trigger input
GP0/RA0	ICSPDAT	I/O	Data input/output – Schmitt Trigger input
$\overline{\text{MCLR}}$	Program/Verify mode	P[(1)]	Program Mode Select
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

Legend: I = Input, O = Output, P = Power

Note 1: In the PIC12F609/12F615/12F617/16F610/16F616 and PIC12HV609/12HV615/16HV610/16HV616, the programming high voltage is internally generated. To activate the Program/Verify mode, voltage of VIHH and a current of IIHH (see Table 7-1) needs to be applied to $\overline{\text{MCLR}}$ input.

3.0 MEMORY DESCRIPTION

3.1 Program Memory Map

The user memory space extends from 0x0000 to 0x1FFF. In Program/Verify mode, the program memory space extends from 0x0000 to 0x3FFF, with the first half (0x0000-0x1FFF) being user program memory and the second half (0x2000-0x3FFF) being configuration memory. The Program Counter (PC) will increment from 0x0000 to 0x1FFF and wrap to 0x0000. If the PC is between 0x2000 to 0x3FFF it will wrap around to 0x2000 (not to 0x0000). Once in configuration memory, the highest bit of the PC stays a '1', thus always pointing to the configuration memory. The only way to point to user program memory is to reset the part and re-enter Program/Verify mode as described in **Section 4.0 "Program/Verify Mode"**.

For all of the devices covered in this document, the configuration memory space, 0x2000 to 0x2008, is physically implemented. However, only locations 0x2000 to 0x2003, 0x2007 and 0x2008 are available. Other locations are reserved.

3.2 User ID Locations

A user may store identification information (user ID) in four designated locations. The user ID locations are mapped in 0x2000 to 0x2003. It is recommended that the user use only the seven Least Significant bits (LSbs) of each user ID location. The user ID locations read out normally, even after code protection is enabled. It is recommended that ID locations are written as '`xx xxxx xbbb bbbb`' where '`bbb bbbb`' is the user ID information.

The 14 bits may be programmed, but only the 7 LSbs are read and displayed by MPLAB® IDE.

3.3 Calibration Word

For all of the devices covered in this document, the 4/8 MHz Internal Oscillator (INTOSC) module is factory calibrated. This value is stored in the Calibration Word (0x2008). See the applicable device data sheet for more information.

The Calibration Word does not necessarily participate in the erase operation unless a specific procedure is executed. Therefore, the device can be erased without affecting the Calibration Word. This simplifies the erase procedure since these values do not need to be read and restored after the device is erased.

FIGURE 3-1: PIC12F615/HV615, PIC12F609/HV609, PIC16F610/HV610 PROGRAM MEMORY MAPPING

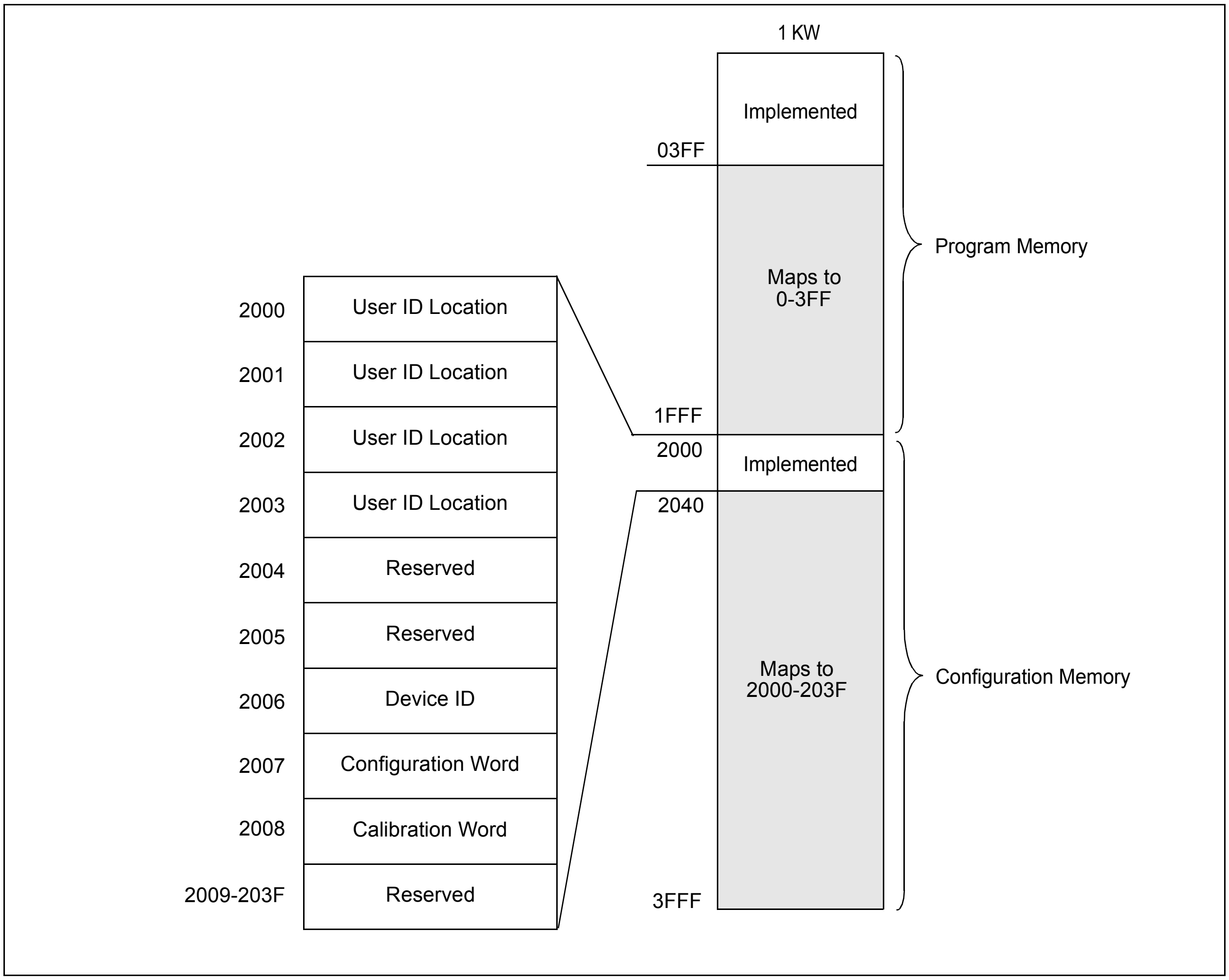
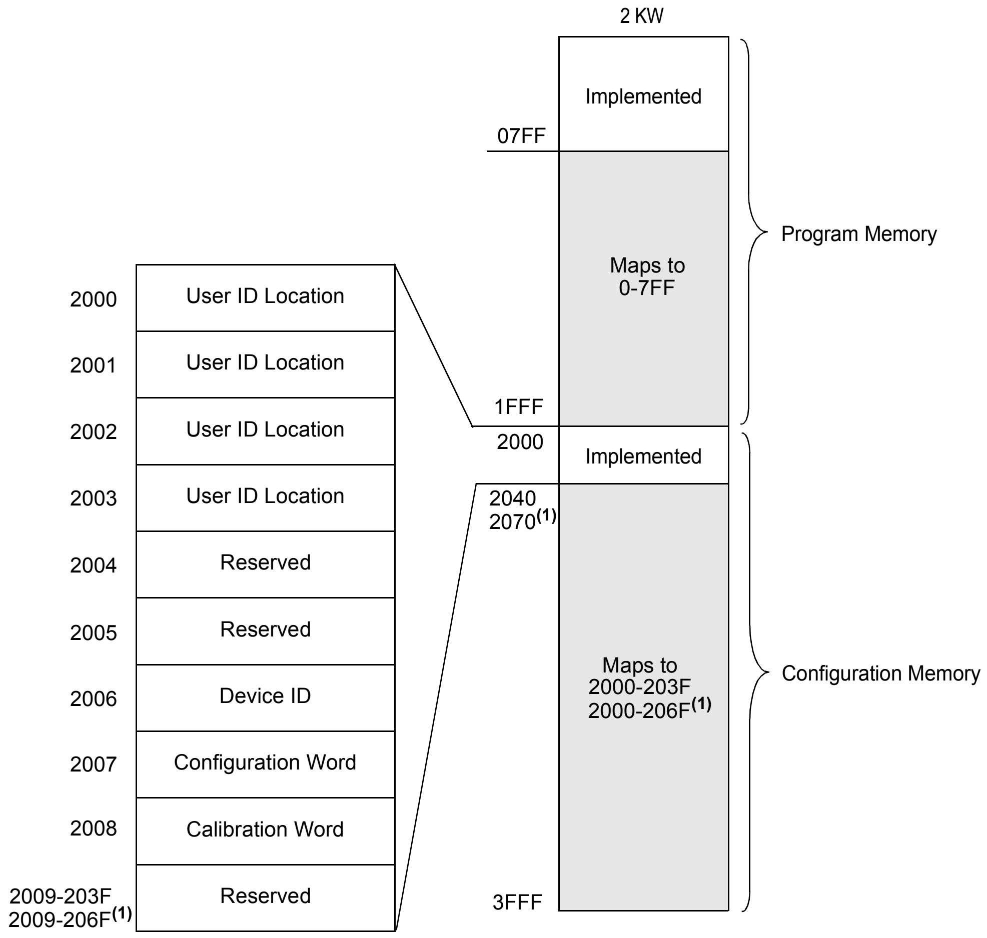


FIGURE 3-2: PIC12F617/PIC16F616/HV616 PROGRAM MEMORY MAPPING



Note 1: Applies to the PIC12F617 only.

4.0 PROGRAM/VERIFY MODE

Two methods are available to enter Program/Verify mode. "VPP-first" is entered by holding ICSPDAT and ICSPCLK low while raising the $\overline{\text{MCLR}}$ pin from VIL to VIHH (high voltage), then applying VDD and data. This method can be used for any Configuration Word selection and **must** be used if the INTOSC and internal $\overline{\text{MCLR}}$ options are selected (FOSC<2:0> = 100 or 101 and MCLRE = 0). The VPP-first entry prevents the device from executing code prior to entering Program/Verify mode. See the timing diagram in Figure 4-1.

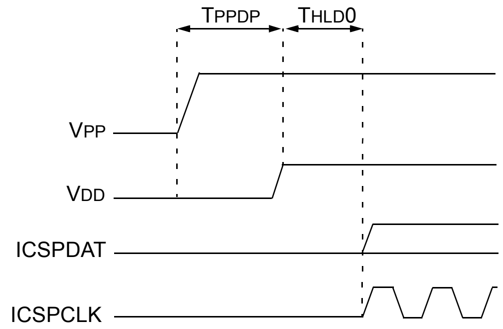
The second entry method, "VDD-first", is entered by applying VDD, holding ICSPDAT and ICSPCLK low, then raising $\overline{\text{MCLR}}$ pin from VIL to VIHH (high voltage), followed by data. This method can be used for any Configuration Word selection **except** when INTOSC and internal $\overline{\text{MCLR}}$ options are selected (FOSC<2:0> = 100 or 101 and MCLRE = 0). This technique is useful when programming the device when VDD is already applied, for it is not necessary to disconnect VDD to enter Program/Verify mode. See the timing diagram in Figure 4-2.

Once in Program/Verify mode, the program memory and configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are Schmitt Trigger inputs in this mode. RA4 is tri-state regardless of fuse setting.

The sequence that enters the device into the Program/Verify mode places all other logic into the Reset state (the $\overline{\text{MCLR}}$ pin was initially at VIL). Therefore, all I/Os are in the Reset state (high-impedance inputs) and the PC is cleared.

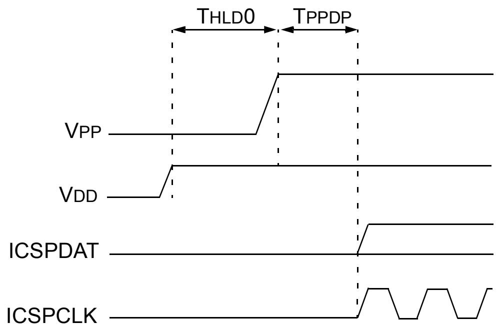
To prevent a device configured with INTOSC and internal $\overline{\text{MCLR}}$ from executing after exiting Program/Verify mode, VDD needs to power down before VPP. See Figure 4-3 for the timing.

FIGURE 4-1: VPP-FIRST PROGRAM/VERIFY MODE ENTRY



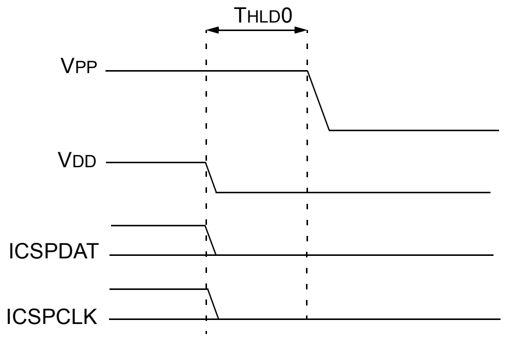
Note: This method of entry is valid, regardless of Configuration Word selected.

FIGURE 4-2: VDD-FIRST PROGRAM/VERIFY MODE ENTRY



Note: This method of entry is valid if INTOSC and internal $\overline{\text{MCLR}}$ are not selected.

FIGURE 4-3: PROGRAM/VERIFY MODE EXIT



4.1 Program/Erase Algorithms

The PIC16F616/PIC12F617 program memory may be written in two ways. The fastest method writes four words at a time. However, one-word writes are also supported for backward compatibility with previous 8-pin and 14-pin Flash devices. The four-word algorithm is used to program the program memory only. The one-word algorithm can write any available memory location (i.e., program memory, configuration memory and calibration memory).

> **Note:** The PIC12F615, PIC12F609, PIC16F610 program memories must be written in one-word writes only.

After writing the array, the PC may be reset and read back to verify the write. It is not possible to verify immediately following the write because the PC can only increment, not decrement.

A device Reset will clear the PC and set the address to '0'. The Increment Address command will increment the PC. The Load Configuration command will set the PC to 0x2000. The available commands are shown in Table 4-1.

4.1.1 ONE-WORD PROGRAMMING

The PIC12F615, PIC12F609, PIC16F616 and PIC16F610 program memories can be written one word at a time to allow compatibility with other 8-pin and 14-pin Flash PIC® devices. Configuration memory (>0x2000) must be written one word (or byte) at a time.

The sequences for programming one word of program memory at a time is:

1. Load a word at the current program memory address using the Load Data For Program Memory command.
2. Issue a Begin Programming (externally timed) command.
3. Wait TPROG1.
4. Issue End Programming command.
5. Issue an Increment Address command.
6. Repeat this sequence as required to write program, calibration or configuration memory.

See Figure 4-12 for more information.

4.1.2 FOUR-WORD PROGRAMMING

The PIC16F616/PIC12F617 program memory can be written four words at a time using the four-word algorithm. Configuration memory (addresses >0x2000) and non-aligned (addresses modulo 4 not equal to zero) starting addresses must use the one-word programming algorithm.

This algorithm writes four sequential addresses in program memory. The four addresses must point to a four-word block which address modulo 4 of 0, 1, 2 and 3. For example, programming address 4 through 7 can be programmed together. Programming addresses 2 through 5 will create an unexpected result.

The sequence for programming four words of program memory at a time is:

1. Load a word at the current program memory address using the Load Data For Program Memory command. This location must be address modulo 4 equal to 0.
2. Issue an Increment Address command to point to the next address in the block.
3. Load a word at the current program memory address using the Load Data For Program Memory command.
4. Issue an Increment Address command to point to the next address in the block.
5. Load a word at the current program memory address using the Load Data For Programming Memory command.
6. Issue and Increment Address command to point to the next address in the book.
7. Load a word at the current program memory address using the Load Data For Programming Memory command.
8. Issue a Begin Programming command externally timed.
9. Wait TPROG1.
10. Issue End Programming.
11. Wait TDIS.
12. Issue an Increment Address command to point to the start of the next block of addresses.
13. Repeat steps 1 through 12 as required to write the desired range of program memory.

See Figure 4-12 for more information.

Note:	Only the PIC16F616 and PIC12F617 program memory can be written to using the four-word programming algorithm.

4.1.3 ERASE ALGORITHMS

The PIC12F609/12F615/12F617/16F610/16F616 and PIC12HV609/12HV615/16HV610/16HV616 devices will erase different memory locations depending on the PC and $\overline{\text{CP}}$. The following sequences can be used to erase noted memory locations. To erase the program memory and Configuration Word (0x2007), the following sequence must be performed. Note the Calibration Word (0x2008) and User ID (0x2000-0x2003) **will not** be erased.

1. Do a Bulk Erase Program Memory command.
2. Wait TERA to complete erase.

To erase the User ID (0x2000-0x2003), Configuration Word (0x2007) and program memory, use the following sequence. Note that the Calibration Word (0x2008) **will not** be erased.

1. Perform Load Configuration with dummy data to point the PC to 0x2000.
2. Perform a Bulk Erase Program Memory command.
3. Wait TERA to complete erase.

4.1.4 SERIAL PROGRAM/VERIFY OPERATION

The ICSPCLK pin is used as a clock input and the ICSPDAT pin is used for entering command bits and data input/output during serial operation. To input a command, ICSPCLK is cycled six times. Each command bit is latched on the falling edge of the clock with the LSb of the command being input first. The data input onto the ICSPDAT pin is required to have a minimum setup and hold time (see Table 7-1), with respect to the falling edge of the clock. Commands that have data associated with them (Read and Load) are specified to have a minimum delay of 1 μs between the command and the data. After this delay, the clock pin is cycled 16 times with the first cycle being a Start bit and the last cycle being a Stop bit.

During a read operation, the LSb will be transmitted onto the ICSPDAT pin on the rising edge of the second cycle. For a load operation, the LSb will be latched on the falling edge of the second cycle. A minimum 1 μs delay is also specified between consecutive commands, except for the End Programming command, which requires a 100 μs (TDIS).

All commands and data words are transmitted LSb first. Data is transmitted on the rising edge and latched on the falling edge of the ICSPCLK. To allow for decoding of commands and reversal of data pin configuration, a time separation of at least 1 μs (TDLY1) is required between a command and a data word.

The commands that are available are described in Table 4-1.

TABLE 4-1: COMMAND MAPPING FOR PIC12F609/12F615/12F617/16F610/16F616 AND PIC12HV609/12HV615/16HV610/16HV616

Command	Mapping (MSb … LSb)						Data
Load Configuration	x	x	0	0	0	0	0, data (14), 0
Load Data for Program Memory	x	x	0	0	1	0	0, data (14), 0
Read Data from Program Memory	x	x	0	1	0	0	0, data (14), 0
Increment Address	x	x	0	1	1	0	
Begin Programming	x	1	1	0	0	0	Externally Timed
End Programming	x	0	1	0	1	0	
Bulk Erase Program Memory	x	x	1	0	0	1	Internally Timed
Row Erase Program Memory	x	1	0	0	0	1	Internally Timed

4.1.4.1 Load Configuration

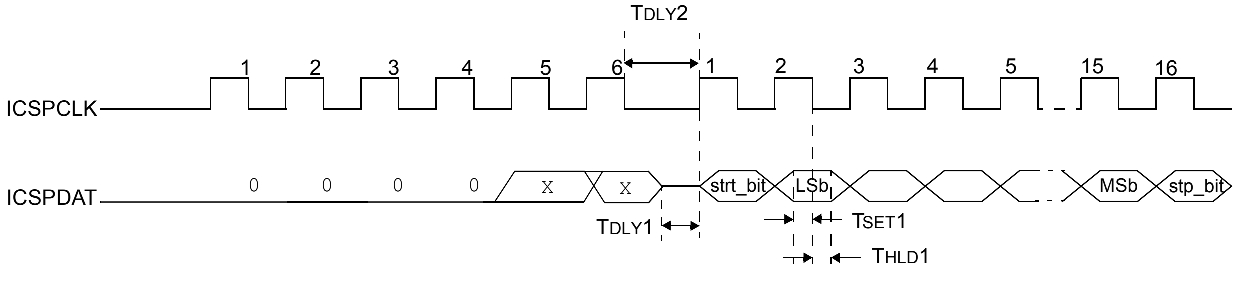
The Load Configuration command is used to access the Configuration Word (0x2007), User ID (0x2000-0x2003) and Calibration Word (0x2008). This command sets the PC to address 0x2000 and loads the data latches with one word of data.

To access the configuration memory, send the Load Configuration command. Individual words within the configuration memory can be accessed by sending Increment Address commands and using load or read data for program memory.

After the 6-bit command is input, the ICSPCLK pin is cycled an additional 16 times for the Start bit, 14 bits of data and the Stop bit (see Figure 4-4).

After the configuration memory is entered, the only way to get back to the program memory is to exit the Program/Verify mode by taking $\overline{\text{MCLR}}$ low (VIL).

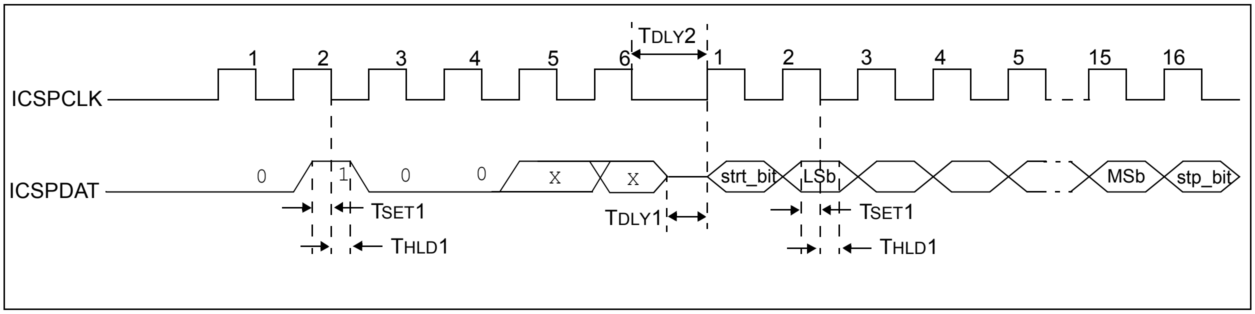
FIGURE 4-4: LOAD CONFIGURATION COMMAND



4.1.4.2 Load Data For Program Memory

After receiving this command, the chip will load in a 14-bit "data word" when 16 cycles are applied, as described in **Section 4.1.4.1 "Load Configuration"**. A timing diagram of this command is shown in Figure 4-5.

FIGURE 4-5: LOAD DATA FOR PROGRAM MEMORY COMMAND



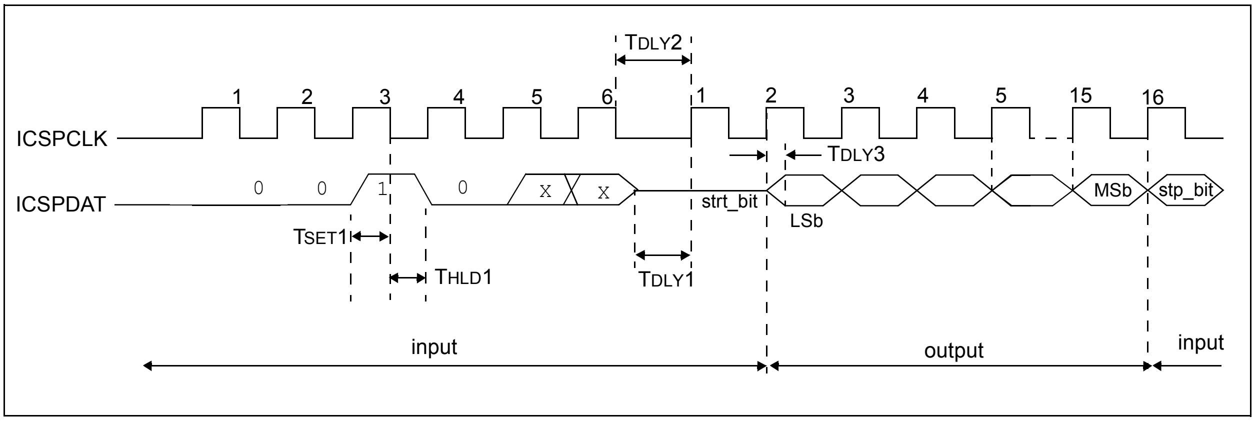
4.1.4.3 Read Data From Program Memory

After receiving this command, the chip will transmit data bits out of the program memory (user or configuration) currently accessed, starting with the second rising edge of the clock input. The data pin will go into Output mode on the second rising clock edge, and it will revert to Input mode (high-impedance) after the 16th rising edge.

If the program memory is code-protected ($\overline{CP}$ = 0), the data is read as zeros.

A timing diagram of this command is shown in Figure 4-6.

FIGURE 4-6: READ DATA FROM PROGRAM MEMORY COMMAND

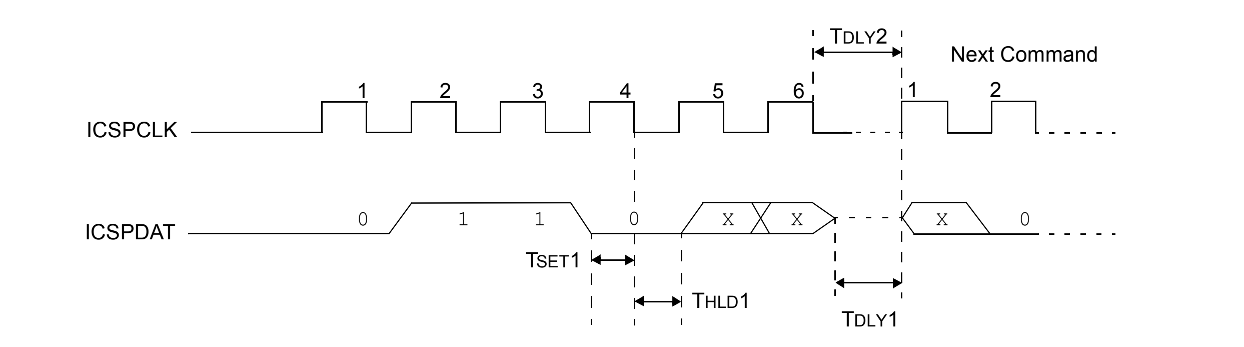


4.1.4.4 Increment Address

The PC is incremented when this command is received. A timing diagram of this command is shown in Figure 4-7.

It is not possible to decrement the address counter. To reset this counter, the user should exit and re-enter Program/Verify mode.

FIGURE 4-7: INCREMENT ADDRESS COMMAND (PROGRAM/VERIFY)

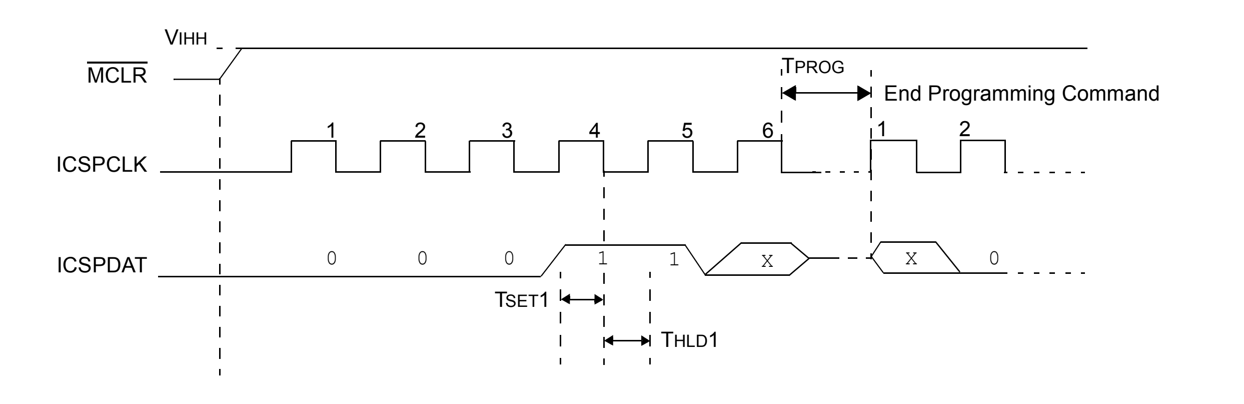


4.1.4.5 Begin Programming (Externally Timed)

A Load command must be given before every Begin Programming command. Programming of the appropriate memory (program memory, configuration or calibration memory) will begin after this command is received and decoded. Programming requires (TPROG) time and is terminated using an End Programming command. A timing diagram for this command is shown in Figure 4-8.

The addressed locations are not erased before programming.

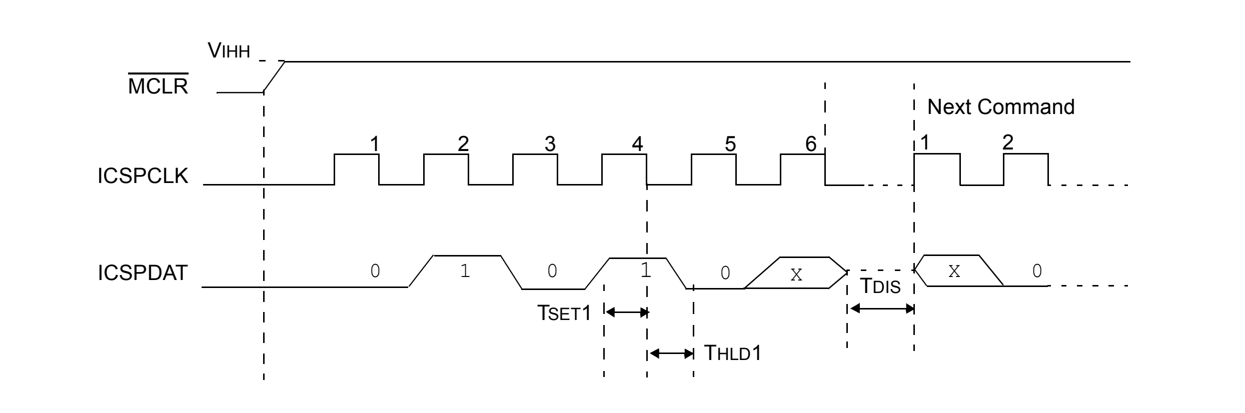
FIGURE 4-8: BEGIN PROGRAMMING (EXTERNALLY TIMED)



4.1.4.6 End Programming

After this command is performed, the write procedure will stop. A timing diagram of this command is shown in Figure 4-9.

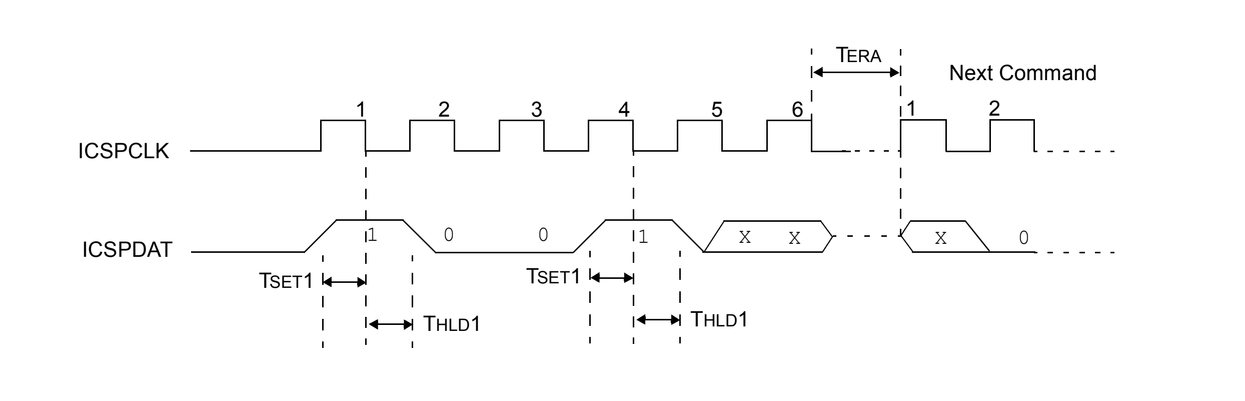
FIGURE 4-9: END PROGRAMMING (SERIAL PROGRAM/VERIFY)



4.1.4.7 Bulk Erase Program Memory

After this command is performed, the entire program memory and Configuration Word (0x2007) is erased. The user ID and calibration memory may also be erased, depending on the value of the PC. See **Section 4.1.3 "Erase Algorithms"** for erase sequences. A timing diagram for this command is shown in Figure 4-10.

FIGURE 4-10: BULK ERASE PROGRAM MEMORY COMMAND



4.1.4.8 Row Erase Program Memory

This command erases the 16-word row of program memory pointed to by PC<11:4>. If the program memory array is protected ($\overline{CP}$ = 0) or the PC points to the configuration memory (>0x2000), the command is ignored.

To perform a Row Erase Program Memory, the following sequence must be performed.

1. Execute a Row Erase Program Memory command.
2. Wait TERA to complete a row erase.

FIGURE 4-11: ROW ERASE PROGRAM MEMORY COMMAND

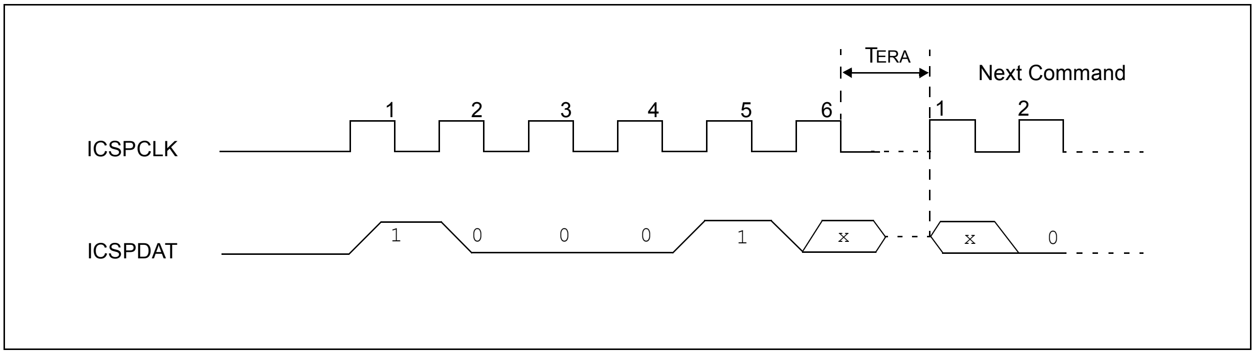
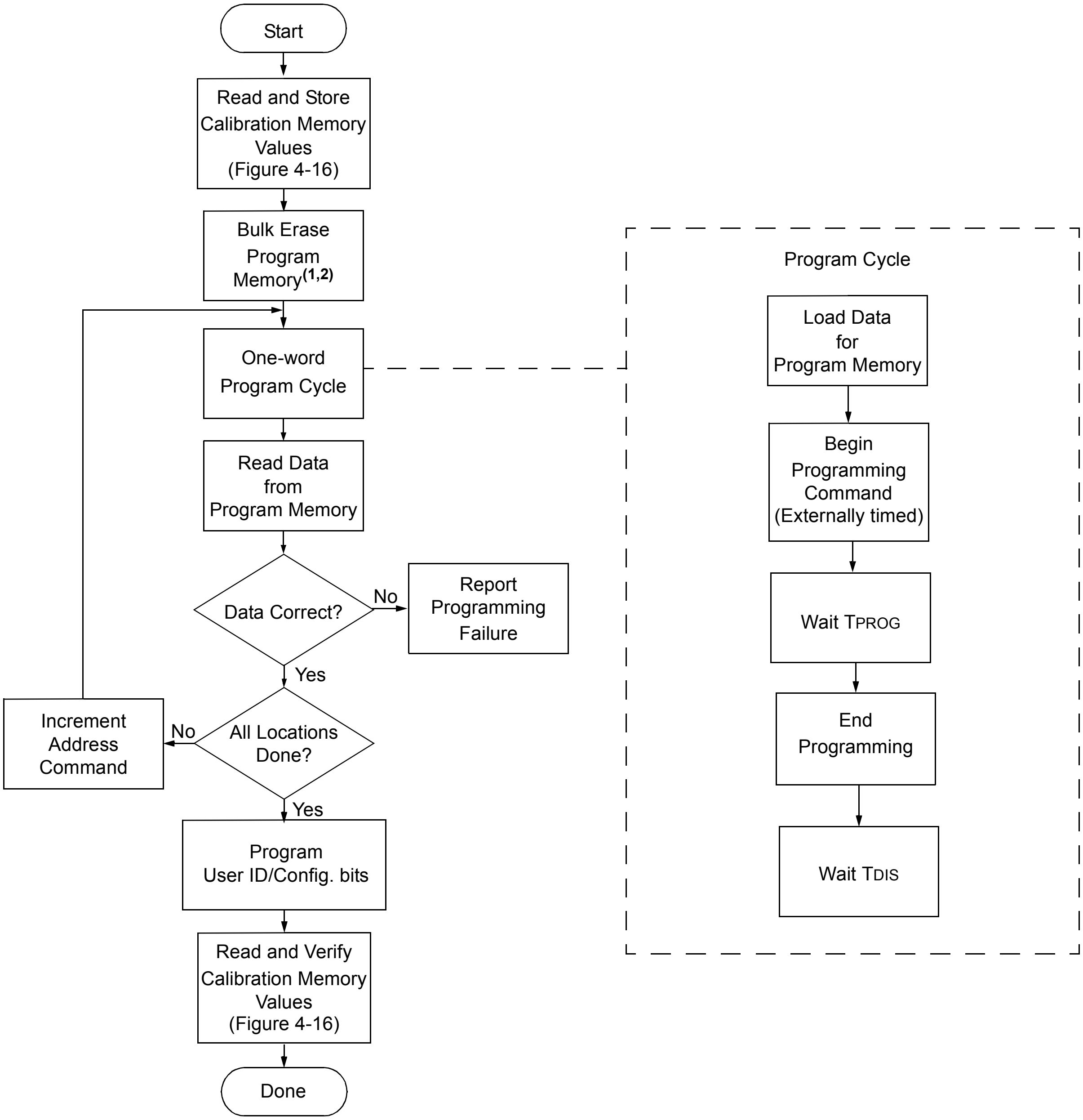


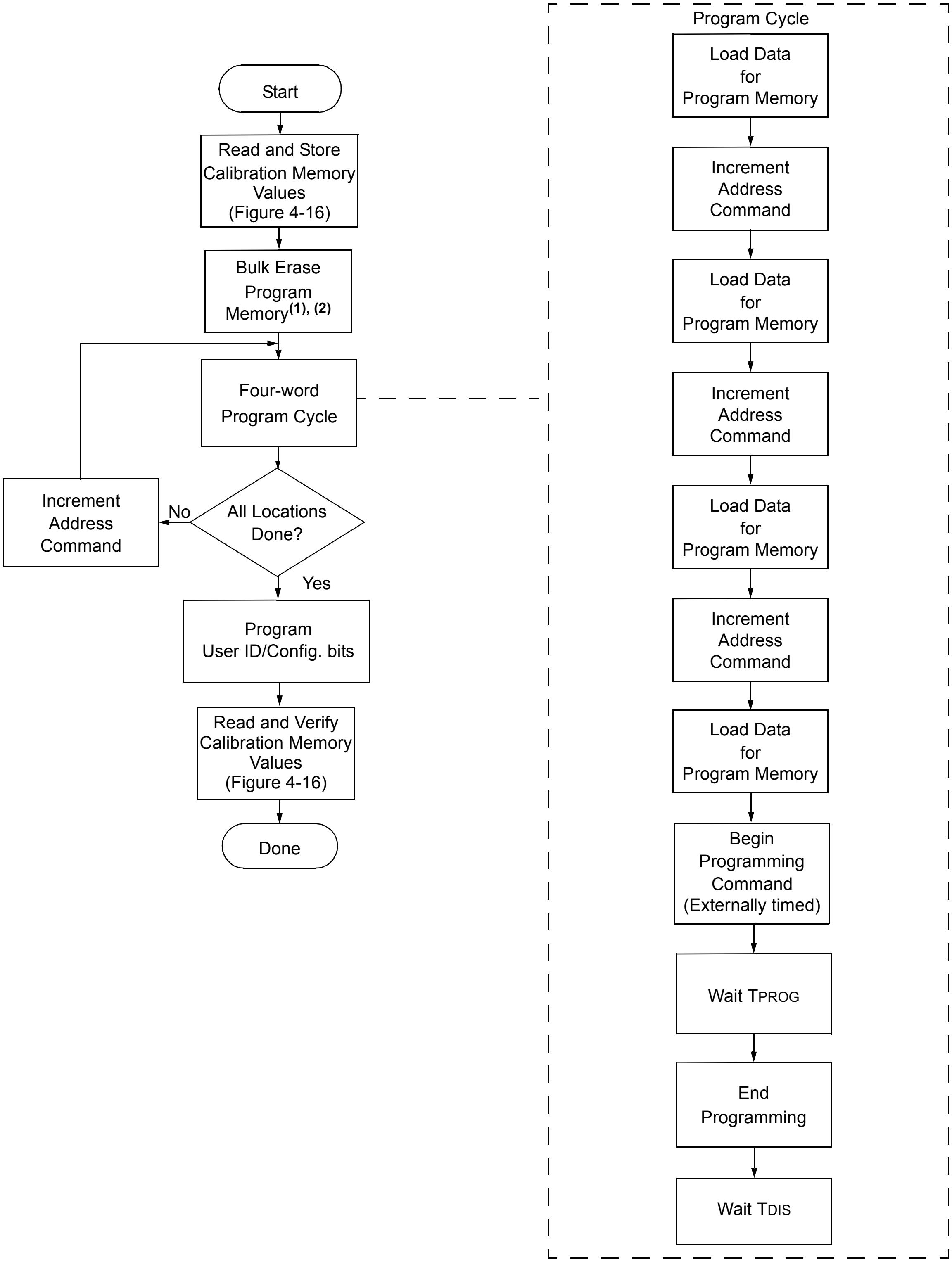
FIGURE 4-12: ONE-WORD PROGRAMMING FLOWCHART (PIC12F61X/16F61X AND PIC12F609)


Start
Read and Store Calibration Memory Values (Figure 4-16)
Bulk Erase Program Memory(1,2)
One-word Program Cycle
Read Data from Program Memory
Data Correct?
No
Report Programming Failure
Yes
All Locations Done?
No
Increment Address Command
Yes
Program User ID/Config. bits
Read and Verify Calibration Memory Values (Figure 4-16)
Done
Program Cycle
Load Data for Program Memory
Begin Programming Command (Externally timed)
Wait TPROG
End Programming
Wait TDIS

Note 1: This step is optional if the device has already been erased or has not been previously programmed.

2: If the device is code-protected or must be completely erased, then Bulk Erase the device per Figure 4-15.

FIGURE 4-13: FOUR-WORD PROGRAMMING FLOWCHART (PIC12F617/PIC16F616)


Start
Read and Store Calibration Memory Values (Figure 4-16)
Bulk Erase Program Memory(1), (2)
Four-word Program Cycle
All Locations Done?
No
Yes
Increment Address Command
Program User ID/Config. bits
Read and Verify Calibration Memory Values (Figure 4-16)
Done
Program Cycle
Load Data for Program Memory
Increment Address Command
Load Data for Program Memory
Increment Address Command
Load Data for Program Memory
Increment Address Command
Load Data for Program Memory
Begin Programming Command (Externally timed)
Wait TPROG
End Programming
Wait TDIS

Note 1: This step is optional if the device is erased or not previously programmed.

2: If the device is code-protected or must be completely erased, then Bulk Erase the device per Figure 4-15.

FIGURE 4-14: PROGRAM FLOWCHART – CONFIGURATION MEMORY

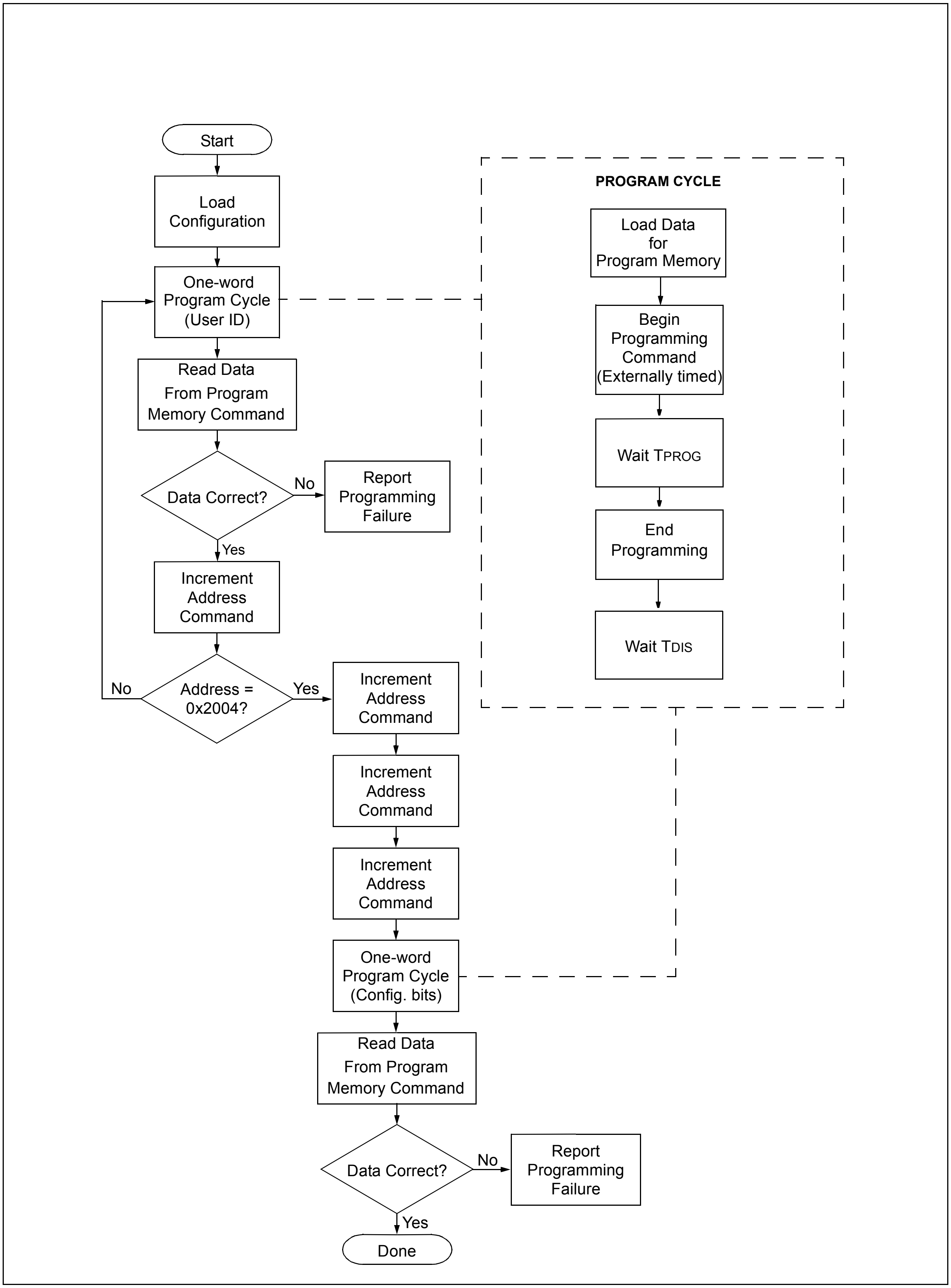
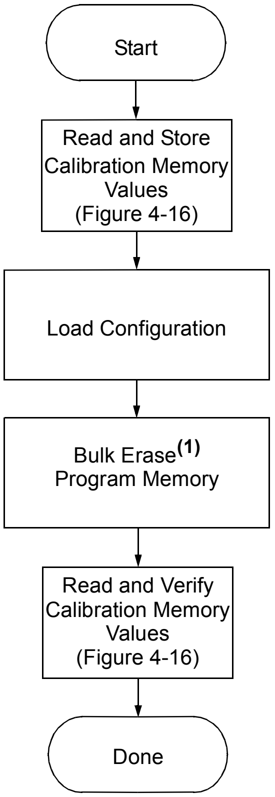
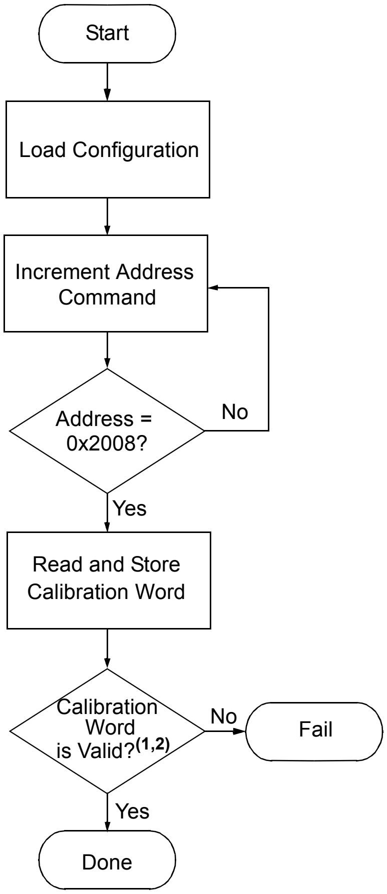

Start
Load Configuration
One-word Program Cycle (User ID)
Read Data From Program Memory Command
Data Correct?
No
Report Programming Failure
Yes
Increment Address Command
Address = 0x2004?
No
Yes
Increment Address Command
Increment Address Command
Increment Address Command
One-word Program Cycle (Config. bits)
Read Data From Program Memory Command
Data Correct?
No
Report Programming Failure
Yes
Done
PROGRAM CYCLE
Load Data for Program Memory
Begin Programming Command (Externally timed)
Wait TPROG
End Programming
Wait TDIS

FIGURE 4-15: PROGRAM FLOWCHART – ERASE FLASH DEVICE


Start
Read and Store Calibration Memory Values (Figure 4-16)
Load Configuration
Bulk Erase(1) Program Memory
Read and Verify Calibration Memory Values (Figure 4-16)
Done

Note 1: See **Section 4.1.4.7 "Bulk Erase Program Memory"** for more information on the Bulk Erase procedure.

FIGURE 4-16: CALIBRATION WORD VERIFICATION FLOWCHART


Start
Load Configuration
Increment Address Command
Address = 0x2008?
No
Yes
Read and Store Calibration Word
Calibration Word is Valid?(1,2)
No
Fail
Yes
Done

Note 1: This step is not required for the Read and Store Calibration Memory Values procedure.

2: The device should not be used if verification of the Calibration Word locations fails. This information should be reported to the user through the user interface of the device programmer.

5.0 CONFIGURATION WORD

The PIC12F609/12F615/12F617/16F610/16F616 and PIC12HV609/12HV615/16HV610/16HV616 devices have several Configuration bits. These bits can be programmed (reads '0') or left unchanged (reads '1'), to select various device configurations.

REGISTER 5-1: CONFIG: CONFIGURATION WORD (ADDRESS: 2007h)

U-1	U-1	U-1	U-1	R/P-1	R/P-1	R/P-1
—	—	—	—	BOREN1	BOREN0	IOSCFS
bit 13						

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE	FOSC2	FOSC1	FOSC0
bit 6						

Legend:	x = Bit is unknown	P = Programmable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared

bit 13-10 **Unimplemented:** Read as '1'

bit 9-8 **BOREN<1:0>:** Brown-out Reset Enable bits
11 = BOR enabled
10 = BOR enabled while running and disabled in Sleep
0x = BOR disabled

bit 7 **IOSCFS:** Internal Oscillator Frequency Select bit
1 = 8 MHz
0 = 4 MHz

bit 6 **$\overline{\text{CP}}$:** Code Protection bit
1 = Program memory is not code-protected
0 = Program memory is external read and write-protected

bit 5 **MCLRE:** $\overline{\text{MCLR}}$ Pin Function Select bit
1 = $\overline{\text{MCLR}}$ pin is $\overline{\text{MCLR}}$ function and weak internal pull-up is enabled
0 = $\overline{\text{MCLR}}$ pin is alternate function, $\overline{\text{MCLR}}$ function is internally disabled

bit 4 **$\overline{\text{PWRTE}}$:** Power-up Timer Enable bit[(1)]
1 = PWRT disabled
0 = PWRT enabled

bit 3 **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 2-0 **FOSC<2:0>:** Oscillator Selection bits
000 = LP oscillator: Low-power crystal on RA5/GP5 and RA4/GP4
001 = XT oscillator: Crystal/resonator on RA5/GP5 and RA4/GP4
010 = HS oscillator: High-speed crystal/resonator on RA5/GP5 and RA4/GP4
011 = EC: I/O function on RA4/GP4, CLKIN on RA5/GP5
100 = INTOSCIO oscillator: I/O function on RA4/GP4, I/O function on RA5/GP5
101 = INTOSC oscillator: CLKOUT function on RA4/GP4, I/O function on RA5/GP5
110 = EXTRCIO oscillator: I/O function on RA4/GP4, RC on RA5/GP5
111 = EXTRC oscillator: CLKOUT function on RA4/GP4, RC on RA5/GP5

Note 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.

REGISTER 5-2: CONFIG: CONFIGURATION WORD (ADDRESS: 2007h) FOR PIC12F617 ONLY

U-1	U-1	U-1	U-1	R/P-1	R/P-1	R/P-1
—	—	WRT1	WRT0	BOREN1	BOREN0	IOSCFS
bit 13						

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE	FOSC2	FOSC1	FOSC0
bit 6						

Legend:	x = Bit is unknown	P = Programmable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared

bit 13-12 **Unimplemented:** Read as ‘1’

bit 11-10 **WRT<1:0>:** Flash Program Memory Self Write Enable bit
11 =Write protection off
10 =000h to 1FFh write-protected, 200h to 7FFh may be modified by PMCON1 control
01 =000h to 3FFh write-protected, 400h to 7FFh may be modified by PMCON1 control
00 =000h to 7FFh write-protected, entire program memory is write-protected

bit 9-8 **BOREN<1:0>:** Brown-out Reset Enable bit
11 =BOR enabled
10 =BOR disabled during Sleep and enabled during operation
0x =BOR disabled

bit 7 **IOSCFS:** Internal Oscillator Frequency Select
1 = 8 MHz
0 = 4 MHz

bit 6 **$\overline{\text{CP}}$:** Code Protection
1 = Program memory is not code-protected
0 = Program memory is external read and write-protected

bit 5 **MCLRE:** $\overline{\text{MCLR}}$ Pin Function Select
1 = $\overline{\text{MCLR}}$ pin is $\overline{\text{MCLR}}$ function and weak internal pull-up is enabled
0 = $\overline{\text{MCLR}}$ pin is alternate function, $\overline{\text{MCLR}}$ function is internally disabled

bit 4 **$\overline{\text{PWRTE}}$:** Power-up Timer Enable bit(1)
1 = PWRT disabled
0 = PWRT enabled

bit 3 **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

Note 1: Enabling Brown-out Reset does not automatically enable Power-up Timer (PWRT).

REGISTER 5-2: CONFIG: CONFIGURATION WORD (ADDRESS: 2007h) (CONTINUED)FOR

bit 2-0 **FOSC<2:0>:** Oscillator Selection bits

`000` = LP oscillator: Low-power crystal on RA5/T1CKI/OSC1/CLKIN and RA4/AN3/T1G/OSC2/CLKOUT
`001` = XT oscillator: Crystal/resonator on RA5/T1CKI/OSC1/CLKIN and RA4/AN3/T1G/OSC2/CLKOUT
`010` = HS oscillator: High-speed crystal/resonator on RA5/T1CKI/OSC1/CLKIN and RA4/AN3/T1G/OSC2/CLKOUT
`011` = EC: I/O function on RA4/AN3/T1G/OSC2/CLKOUT, CLKIN on RA5/T1CKI/OSC1/CLKIN
`100` = INTOSCIO oscillator: I/O function on RA4/AN3/T1G/OSC2/CLKOUT, I/O function on RA5/T1CKI/OSC1/CLKIN
`101` = INTOSC oscillator: CLKOUT function on RA4/AN3/T1G/OSC2/CLKOUT, I/O function on RA5/T1CKI/OSC1/CLKIN
`110` = EXTRCIO oscillator: I/O function on RA4/AN3/T1G/OSC2/CLKOUT, RC on RA5/T1CKI/OSC1/CLKIN
`111` = EXTRC oscillator: CLKOUT function on RA4/AN3/T1G/OSC2/CLKOUT, RC on RA5/T1CKI/OSC1/CLKIN

Note 1: Enabling Brown-out Reset does not automatically enable Power-up Timer (PWRT).

5.1 Device ID Word

The device ID word for the PIC12F609/12F615/12F617/16F610/16F616 and PIC12HV609/12HV615/16HV610/16HV616 is loaded at 2006h. This location can not be erased.

TABLE 5-1: DEVICE ID VALUES

Device	Device ID Values	
	Dev	Rev
PIC12F615	`10 0001 100`	`x xxxx`
PIC12HV615	`10 0001 101`	`x xxxx`
PIC12F617	`01 0011 011`	`x xxxx`
PIC16F616	`01 0010 010`	`x xxxx`
PIC16HV616	`01 0010 011`	`x xxxx`
PIC12F609	`10 0010 010`	`x xxxx`
PIC12HV609	`10 0010 100`	`x xxxx`
PIC16F610	`10 0010 011`	`x xxxx`
PIC16HV610	`10 0010 101`	`x xxxx`

6.0 CODE PROTECTION

For PIC12F609/12F615/12F617/16F610/16F616 and PIC12HV609/12HV615/16HV610/16HV616, once the $\overline{\text{CP}}$ bit is programmed to '0', all program memory locations read all '0's. The user ID locations and the Configuration Word read out in an unprotected fashion. Further programming is disabled for the entire program memory.

The user ID locations and the Configuration Word can be programmed regardless of the state of the $\overline{\text{CP}}$ bit.

6.1 Disabling Code Protection

It is recommended to use the procedure in Figure 4-15 to disable code protection of the device. This sequence will erase the program memory, Configuration Word (0x2007) and user ID locations (0x2000-0x2003). The Calibration Word (0x2008) **will not** be erased.

6.2 Embedding Configuration Word and User ID Information in the Hex File

To allow portability of code, the programmer is required to read the Configuration Word and user ID locations from the hex file when loading the hex file. If Configuration Word information was not present in the hex file, a simple warning message may be issued. Similarly, while saving a hex file, Configuration Word and user ID information must be included. An option to not include this information may be provided.

Microchip Technology Incorporated feels strongly that this feature is important for the benefit of the end customer.

6.3 Checksum Computation

6.3.1 CHECKSUM

Checksum is calculated by reading the contents of the program memory locations and adding up the opcodes up to the maximum user addressable location (e.g., 0x7FF for the PIC16F616). Any carry bits exceeding 16 bits are neglected. Finally, the Configuration Word (appropriately masked) is added to the checksum. The checksum computation for the PIC12F609/12F615/12F617/16F610/16F616 and PIC12HV609/12HV615/16HV610/16HV616 devices is shown in Table 6-1.

The checksum is calculated by summing the following:

- The contents of all program memory locations
- The Configuration Word, appropriately masked
- Masked user ID locations (when applicable)

The Least Significant 16 bits of this sum is the checksum.

Table 6-1 describes how to calculate the checksum for each device. Note that the checksum calculation differs depending on the code-protect setting. Since the program memory locations read out zeroes when code-protected, the table describes how to manipulate the actual program memory values to simulate values that would be read from a protected device. When calculating a checksum by reading a device, the entire program memory can simply be read and summed. The Configuration Word and user ID locations can always be read regardless of code-protect setting.

Note: Some older devices have an additional value added in the checksum. This is to maintain compatibility with older device programmer checksums.

TABLE 6-1: CHECKSUM COMPUTATIONS

Device	Code Protect	Checksum*	Blank Value	0x25E6 at 0 and Max. Address
PIC12F615/HV615	$\overline{CP}$ = 1	SUM[0x000:0x03FF] + (CFGW & 0x03FF)	0xFFFF	0xCBCD
	$\overline{CP}$ = 0	(CFGW & 0x03FF) + SUM_ID	0x03BE	0xCF8C
PIC12F617	$\overline{CP}$ = 1	SUM[0x000:0x07FF] + (CFGW & 0x03FF)	0xFBFF	0xC7CD
	$\overline{CP}$ = 0	(CFGW & 0x03FF) + SUM_ID	0x03BE	0xCF8C
PIC12F609/HV609	$\overline{CP}$ = 1	SUM[0x000:0x03FF] + (CFGW & 0x03FF)	0xFFFF	0xCBCD
	$\overline{CP}$ = 0	(CFGW &0x03FF) + SUM_ID	0x03BE	0xCF8C
PIC16F610/HV610	$\overline{CP}$ = 1	SUM[0x000:0x03FF] + (CFGW & 0x03FF)	0xFFFF	0xCBCD
	$\overline{CP}$ = 0	(CFGW & 0x03FF) + SUM_ID	0x03BE	0xCF8C
PIC16F616/HV616	$\overline{CP}$ = 1	SUM[0x000:0x07FF] + (CFGW & 0x03FF)	0xFBFF	0xC7CD
	$\overline{CP}$ = 0	(CFGW & 0x03FF) + SUM_ID	0x03BE	0xCF8C

Legend: CFGW = Configuration Word. Example calculations assume Configuration Word is erased (all '1's).
SUM[a:b] = [Sum of locations a to b inclusive]
SUM_ID = User ID locations masked by 0xF then made into a 16-bit value with ID0 as the Most Significant nibble. For example, ID0 = 0x1, ID1 = 0x2, ID3 = 0x3, ID4 = 0x4, then SUM_ID = 0x1234. The 4 LSb's of the unprotected checksum is used for the example calculations.
*Checksum = [Sum of all the individual expressions] MODULO [0xFFFF]
+ = Addition
& = Bitwise AND

7.0 PROGRAM/VERIFY MODE ELECTRICAL CHARACTERISTICS

TABLE 7-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE

AC/DC CHARACTERISTICS		**Standard Operating Conditions (unless otherwise stated)** Operating Temperature -40°C ≤ TA ≤ +85°C Operating Voltage 4.5V ≤ VDD ≤ 5.5V				
Sym.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions/Comments**
General						
VDD	VDD level for read/write operations, program and data memory	2.0	—	5.5	V	PIC16F616/F610, PIC12F615/F617/F609
		2.0	—	4.7(1)	V	PIC16HV616/HV610, PIC12HV615/HV609
		2.0	—	5.25(2)	V	PIC16HV616/HV610, PIC12HV615/HV609
	VDD level for Bulk Erase operations, program and data memory	4.5	—	5.5	V	PIC16F616/F610, PIC12F615/F617/F609
		4.5	—	4.7(1)	V	PIC16HV616/HV610, PIC12HV615/HV609
		4.5	—	5.25(2)	V	PIC16HV616/HV610, PIC12HV615/HV609
VIHH	High voltage on $\overline{\text{MCLR}}$ for Program/Verify mode entry	10	—	13	V	
IIHH	$\overline{\text{MCLR}}$ current during programming	—	300	1000	μA	
TVHHR	$\overline{\text{MCLR}}$ rise time (VSS to VHH) for Program/Verify mode entry	—	—	1.0	μs	
TPPDP	Hold time after VPP changes	5	—	—	μs	
VIH1	(ICSPCLK, ICSPDAT) input high level	0.8 VDD	—	—	V	
VIL1	(ICSPCLK, ICSPDAT) input low level	0.2 VDD	—	—	V	
TSET0	ICSPCLK, ICSPDAT setup time before $\overline{\text{MCLR}}$↑ (Program/Verify mode selection pattern setup time)	100	—	—	ns	
THLD0	Hold time after VDD changes	5	—	—	μs	
Serial Program/Verify						
TSET1	Data in setup time before clock↓	100	—	—	ns	
THLD1	Data in hold time after clock↓	100	—	—	ns	
TDLY1	Data input not driven to next clock input (delay required between command/data or command/ command)	1.0	—	—	μs	
TDLY2	Delay between clock↓ to clock↑ of next command or data	1.0	—	—	μs	
TDLY3	Clock↓ to data out valid (during a Read Data command)	—	—	80	ns	
TERA	Erase cycle time	—	5	6	ms	
TPROG	Programming cycle time	3	—	—	ms	10°C ≤ TA ≤ +40°C
TDIS	Time delay from program to compare (HV discharge time)	100	—	—	μs	

Note 1: Maximum VDD voltage when programming the device without a current limiting series resistor. Voltages above this level will cause the shunt regulator to draw excessive current and damage the device.

2: Limiting the current through the shunt regulator to within max shunt current (device electrical characteristic SR02) with either a series resistor or with a current limited supply.

APPENDIX A: REVISION HISTORY

Revision A (2/06)

Original release.

Revision B (11/06)

Section 1.0 “Device Overview”	Added devices.
Section 2.1 “Hardware Requirements”	Reworded.
Section 2.2 “Program/Verify Mode”	Deleted data memory.
Figure 2-1	Added 16 pin and note 1.
Figure 2-1	Reworded Note 1.
Section 3.3 “Calibration Word”	Changed to 8 MHz.
Figure 3-1	Changed title.
Section 4.1 “Program/Erase Algorithms”	Added text under note.
Section 4.1.3 “Erase Algorithms”	Moved One word programming to section 4.1.1.
Figure 4-12	Changed title.
Figure 4-13	Changed title.
Register	Added GP4 and GP5, added note.
Register 5.1	Bit 13 and bits 5-0 changed to unimplemented read as “1”.
Section 6.3.1 “Checksum”	Changed Lease to Least. Changed CARRY to lowercase.

Revision C (05/07)

Changed device family name

Section 2.1	Revised Section 2.1
Section 3.1	Changed 0x000 to 0x0000
Table 6-1	Changed 1FFF to 0x03FF
Table 7-1	Revised VDD section Revised Note 1 and Added Note 2

Revision D (12/09)

Updated sections 2.2, 3.3, 4.1.3, 4.1.4.1; Updated Figures 4-11, 4-12, 4-13, 4-14; Added Figure 4-15.

Revision E (04/10)

Added PIC12F617 part number; minor edits.

This document replaces DS41396.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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Printed on recycled paper.

ISBN: 978-1-60932-165-9

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