Figure 3. Pin Configuration (Top View)

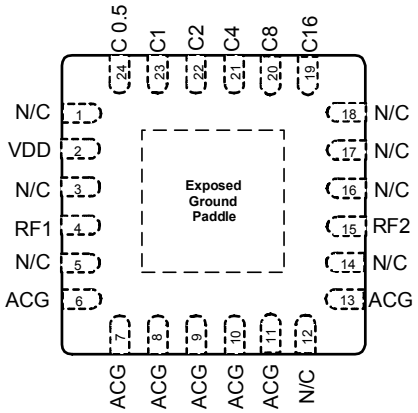


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	N/C[7]	No Connect
2	V_{DD}	Power supply pin
3	N/C[5]	No Connect
4	RF1	RF port
5	N/C[5]	No Connect
6	ACG[6]	AC Ground connection
7	ACG[6]	AC Ground connection
8	ACG[6]	AC Ground connection
9	ACG[6]	AC Ground connection
10	ACG[6]	AC Ground connection
11	ACG[6]	AC Ground connection
12	N/C[7]	No Connect
13	ACG[6]	AC Ground connection
14	N/C[5]	No Connect
15	RF2	RF port
16	N/C[5]	No Connect
17	N/C[5]	No Connect
18	N/C[5]	No Connect
19	C16	Attenuation control bit, 16 dB
20	C8	Attenuation control bit, 8 dB
21	C4	Attenuation control bit, 4 dB
22	C2	Attenuation control bit, 2 dB
23	C1	Attenuation control bit, 1 dB
24	C0.5	Attenuation control bit, 0.5 dB
Paddle	GND	Ground for proper operation

Notes: 5. For improved RF performance these No Connect pins can be connected to RF ground.
6. Pins can either be grounded directly or through coupling capacitors.
7. Pin can either be grounded or No Connect

Exposed Solder Pad Connection

The exposed solder pad on the bottom of the package must be grounded for proper device operation.

Table 3. Operating Ranges

Parameter	Min	Typ	Max	Units
V_{DD} Power Supply Voltage	3.0	3.3	5.5	V
I_{DD} Power Supply Current		100	250	µA
P_{IN} Input power (50Ω)			+24	dBm

Table 4. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	6.0	V
V_I	Voltage on any DC input	-0.3	6.0	V
T_{ST}	Storage temperature range	-65	150	°C
T_{OP}	Operating temperature range	-40	85	°C
P_{IN}	Input power (50Ω)		30	dBm
V_{ESD}	ESD voltage (Human Body Model)		2000	V

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rate specified in Table 4.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Switching Frequency

The PE4309 has a maximum 25 kHz switching rate.

Table 5. Control Voltage

State	Bias Condition
Low	0 to +1.0 Vdc at 2 µA (typ)
High	+2.0 to +5 Vdc at 10 µA (typ)

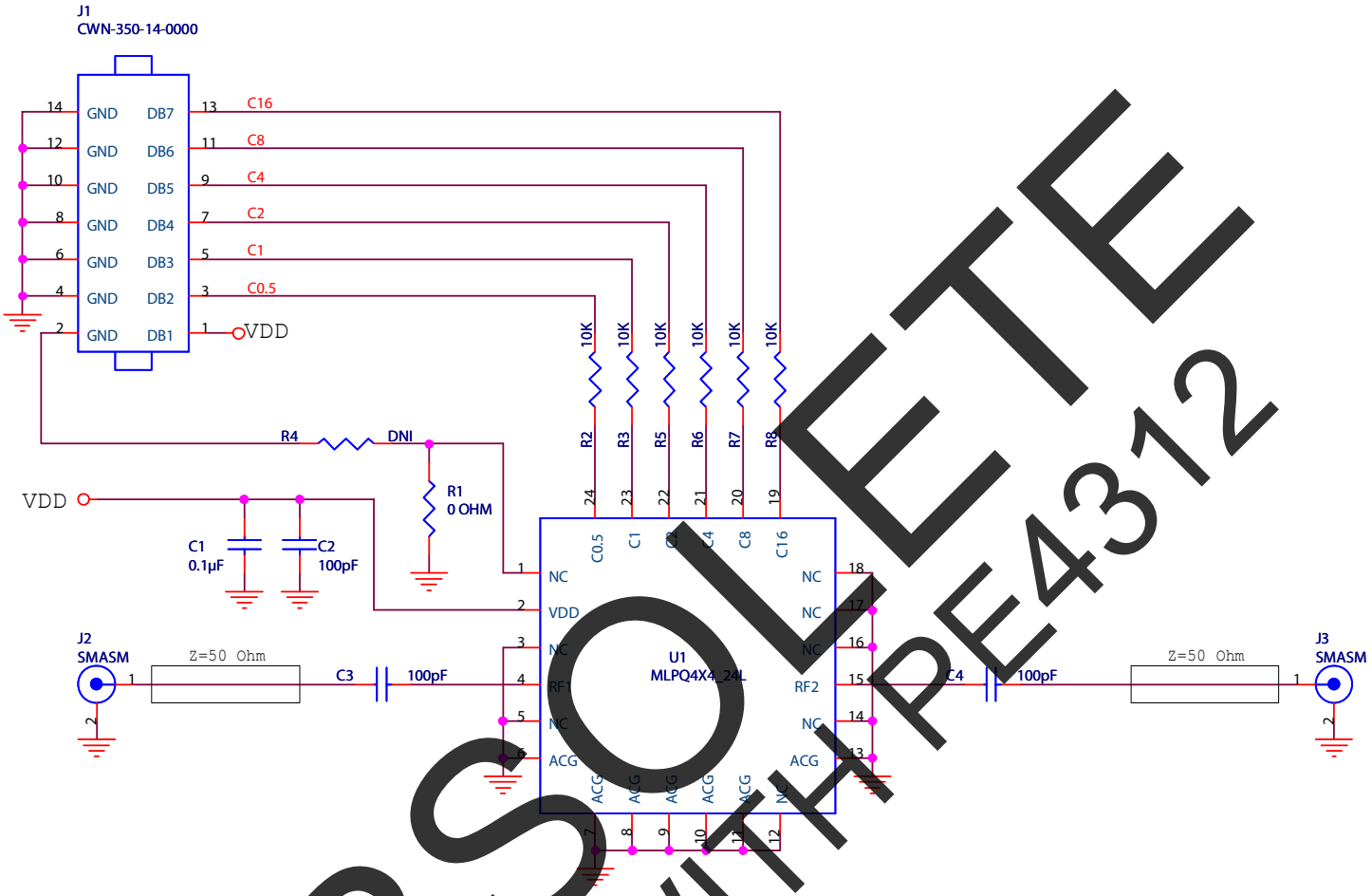
The standard 3V or 5V CMOS control logic is independent of supply voltage.

Table 6. Truth Table

C16	C8	C4	C2	C1	C0.5	Attenuation State
1	1	1	1	1	1	Reference Loss (IL)
1	1	1	1	1	0	0.5 dB
1	1	1	1	0	1	1 dB
1	1	1	0	1	1	2 dB
1	1	0	1	1	1	4 dB
1	0	1	1	1	1	8 dB
0	1	1	1	1	1	16 dB
0	0	0	0	0	0	31.5 dB

Figure 4. Test Circuit Block Diagram

Peregrine Specification 102-0371



Evaluation Kit

The Digital Attenuator Evaluation Kit board was designed to ease customer evaluation of the PE4309 Digital Step Attenuator. Connect J2 by mini clip to Vdd to power the IC. Connect J8 by mini clip to power the evaluation board support circuits. The control bits for the six parallel data inputs (C0.5 to C16) are controlled using S2-S7 to select bits or bit combinations. This allows any attenuation setting to be specified as shown in Table 6.

The de-embed trace (J6 to J7) estimates the PCB insertion loss for removal from the evaluation board measurement data.

To evaluate using customer software, J1 can be installed using a standard 0.100 IDC header (some circuit modification required, see schematic).

The ability to supply different voltages for the Control circuitry (using J8) and IC Vdd (using J2) circuits allows for evaluation of circuits using different control vs. supply voltages.

Figure 5. Evaluation Board Layout
Peregrine Specification 101/0299

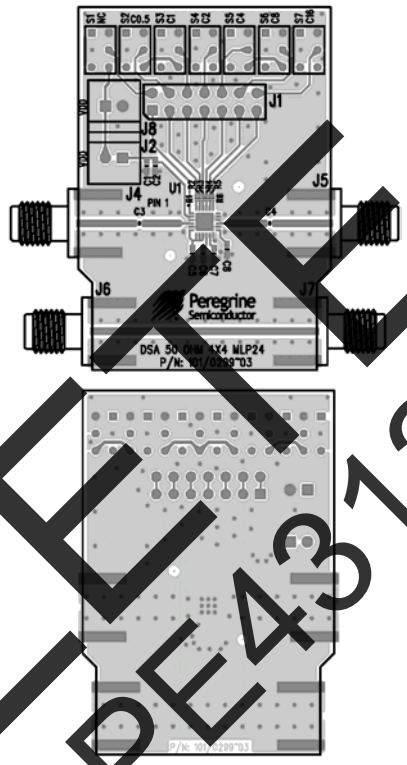
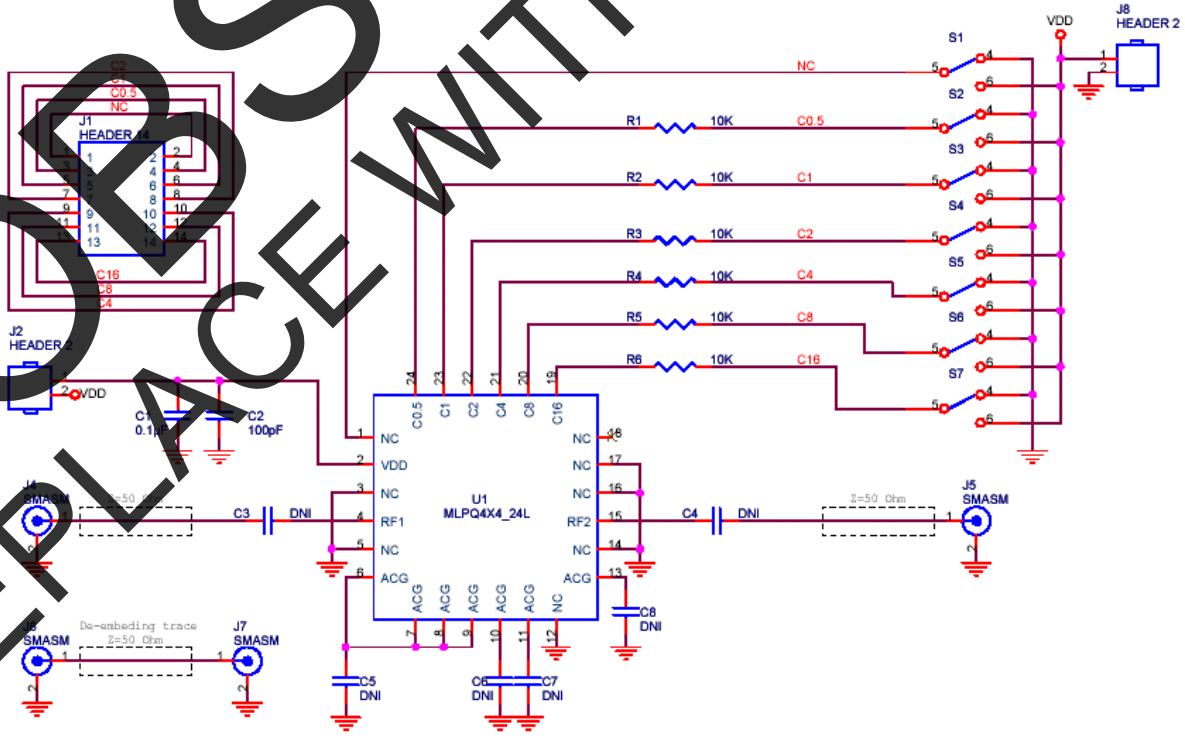


Figure 6. Evaluation Board Schematic
Peregrine Specification 102/0366



Typical Performance Data

Figure 7. Insertion Loss, V_{dd} = 3.0 V

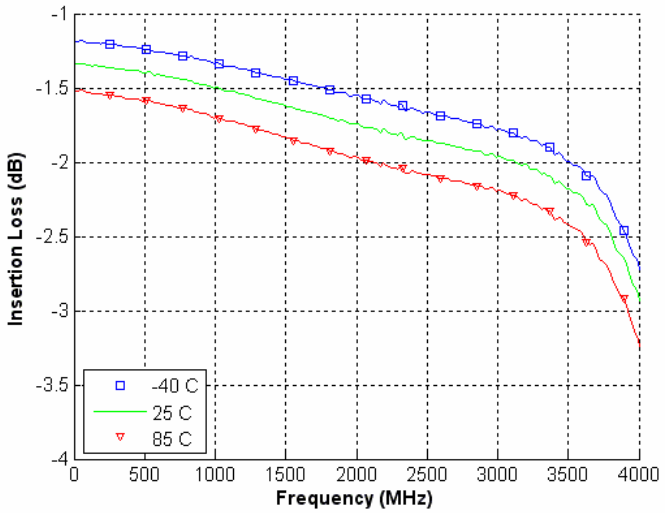


Figure 8. Attenuation at Major Steps

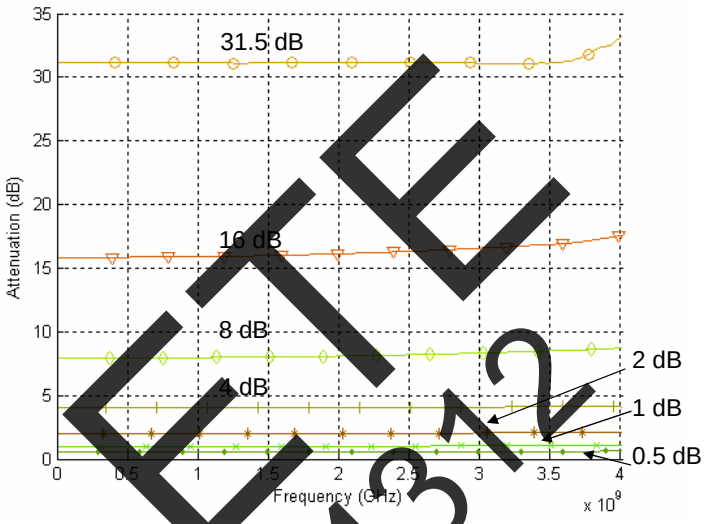


Figure 9. Input Return Loss at Major Attenuation Steps

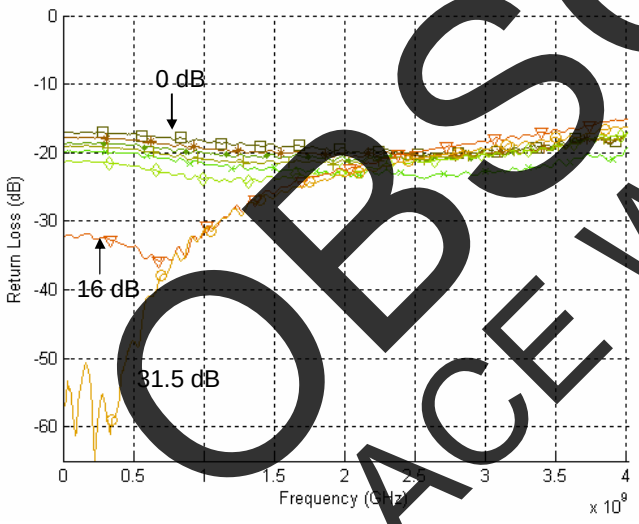
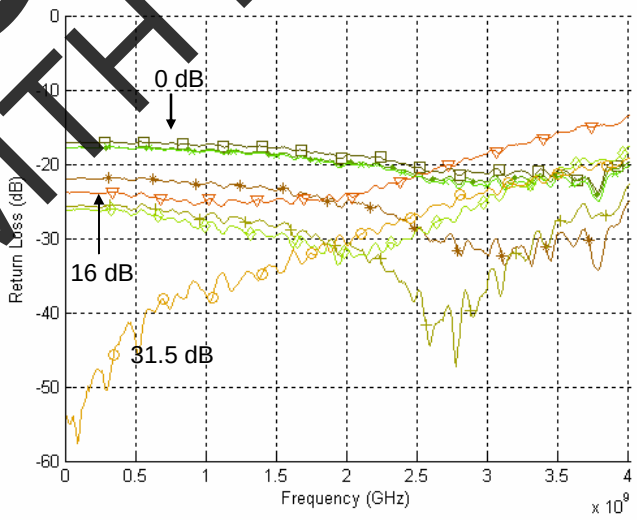


Figure 10. Output Return Loss at Major Attenuation Steps



Typical Performance Data

Figure 11. Attenuation Error Vs. Frequency

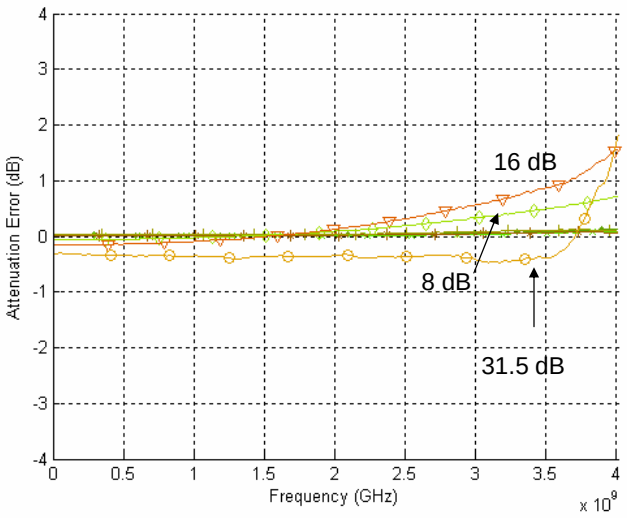


Figure 12. Attenuation Error vs. Setting: Low Frequency

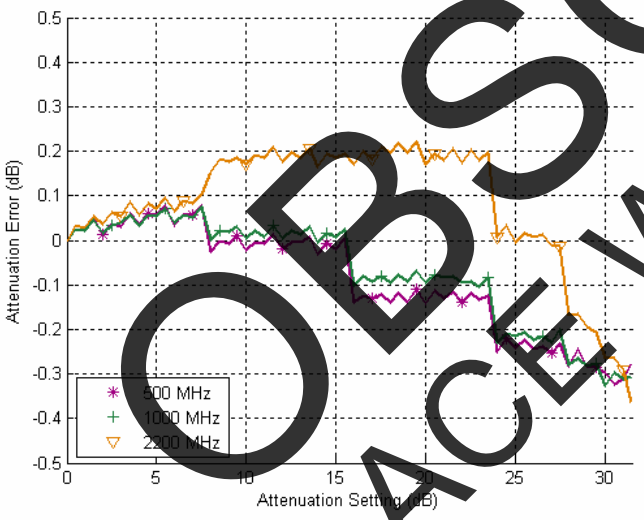


Figure 13. Attenuation Error vs. Setting: High Frequency

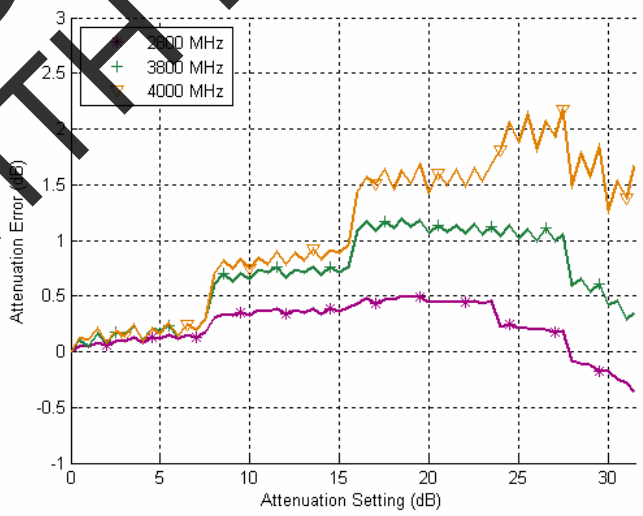
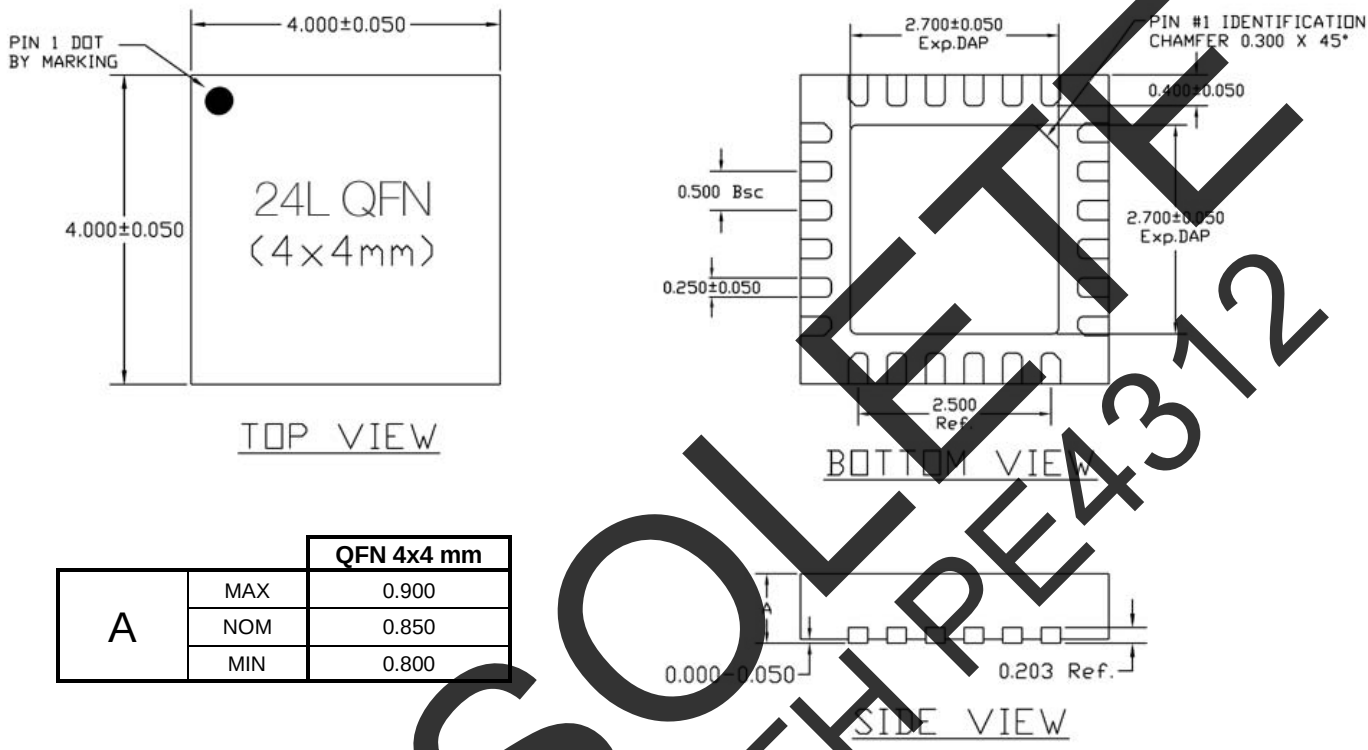


Figure 16. Package Drawing



		QFN 4x4 mm
A	MAX	0.900
	NOM	0.850
	MIN	0.800

Figure 17. Tape and Reel Drawing

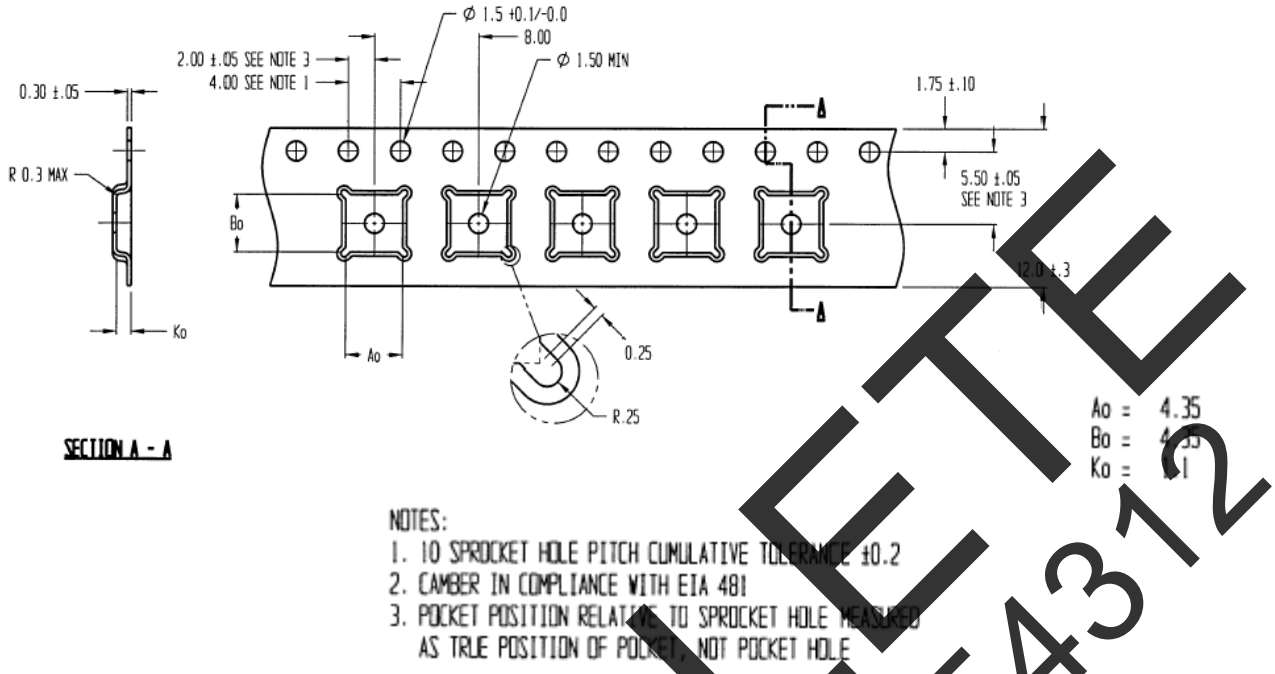
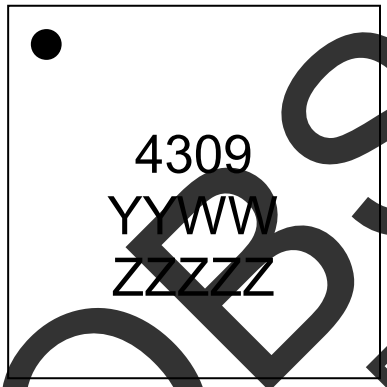


Figure 18. Marking Specifications



YYWW = Date Code
ZZZZZ = Last five digits of Lot Number

Table 7. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
4309-00	PE4309-EK	PE4309-24QFN 4x4mm-EK	Evaluation Kit	1 / Box
4309-51	4309	PE4309G-24QFN 4x4mm-75A	Green 24-lead 4x4mm QFN	75 units / Tube
4309-52	4309	PE4309G-24QFN 4x4mm-3000C	Green 24-lead 4x4mm QFN	3000 units / T&R

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Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a DCN (Document Change Notice).

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