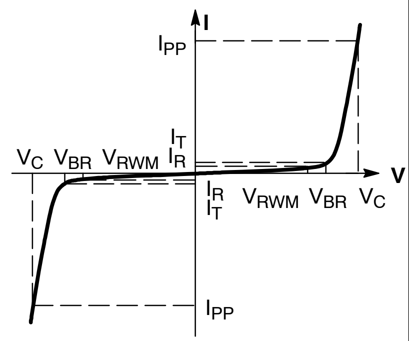
ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
ΘV_{BR}	Maximum Temperature Coefficient of V_{BR}



Bi−Directional TVS

ELECTRICAL CHARACTERISTICS (Devices listed in bold, italic are ON Semiconductor Preferred devices.)

Device*	Device Marking	V_{RWM} (Note 4)	I_R @ V_{RWM}	Breakdown Voltage				V_C @ I_{PP} (Note 6)		ΘV_{BR}	C_{typ} (Note 7)
				V_{BR} Volts (Note 5)			@ I_T	V_C	I_{PP}		
		Volts	μA	Min	Nom	Max	mA	Volts	Amps	%/°C	pF
P6SMB11CAT3, G	11C	9.4	5	10.5	11.05	11.6	1	15.6	38	0.075	865
P6SMB12CAT3, G	12C	10.2	5	11.4	12	12.6	1	16.7	36	0.078	800
P6SMB13CAT3, G	13C	11.1	5	12.4	13.05	13.7	1	18.2	33	0.081	740
P6SMB15CAT3, G	15C	12.8	5	14.3	15.05	15.8	1	21.2	28	0.084	645
P6SMB16CAT3, G	16C	13.6	5	15.2	16	16.8	1	22.5	27	0.086	610
P6SMB18CAT3, G	18C	15.3	5	17.1	18	18.9	1	25.2	24	0.088	545
P6SMB20CAT3, G	20C	17.1	5	19	20	21	1	27.7	22	0.09	490
P6SMB22CAT3, G	22C	18.8	5	20.9	22	23.1	1	30.6	20	0.09	450
P6SMB24CAT3, G	24C	20.5	5	22.8	24	25.2	1	33.2	18	0.094	415
P6SMB27CAT3, G	27C	23.1	5	25.7	27.05	28.4	1	37.5	16	0.096	370
P6SMB30CAT3, G	30C	25.6	5	28.5	30	31.5	1	41.4	14.4	0.097	335
P6SMB33CAT3, G	***33C***	***28.2***	***5***	***31.4***	***33.05***	***34.7***	***1***	***45.7***	***13.2***	***0.098***	***305***
P6SMB36CAT3, G	36C	30.8	5	34.2	36	37.8	1	49.9	12	0.099	280
P6SMB39CAT3, G	39C	33.3	5	37.1	39.05	41	1	53.9	11.2	0.1	260
P6SMB43CAT3, G	43C	36.8	5	40.9	43.05	45.2	1	59.3	10.1	0.101	240
P6SMB47CAT3, G	47C	40.2	5	44.7	47.05	49.4	1	64.8	9.3	0.101	220
P6SMB51CAT3, G	51C	43.6	5	48.5	51.05	53.6	1	70.1	8.6	0.102	205
P6SMB56CAT3, G	56C	47.8	5	53.2	56	58.8	1	77	7.8	0.103	185
P6SMB62CAT3, G	62C	53	5	58.9	62	65.1	1	85	7.1	0.104	170
P6SMB68CAT3, G	68C	58.1	5	64.6	68	71.4	1	92	6.5	0.104	155
P6SMB75CAT3, G	75C	64.1	5	71.3	75.05	78.8	1	103	5.8	0.105	140
P6SMB82CAT3, G	82C	70.1	5	77.9	82	86.1	1	113	5.3	0.105	130
P6SMB91CAT3, G	91C	77.8	5	86.5	91	95.5	1	125	4.8	0.106	120

4. A transient suppressor is normally selected according to the working peak reverse voltage (V_{RWM}), which should be equal to or greater than the DC or continuous peak operating voltage level.
5. V_{BR} measured at pulse test current I_T at an ambient temperature of 25°C.
6. Surge current waveform per Figure 2 and derate per Figure 3 of the General Data − 600 Watt at the beginning of this group.
7. Bias Voltage = 0 V, F = 1 MHz, T_J = 25°C

*The “G” suffix indicates Pb−Free package available. Please refer back to Ordering Information on front page.

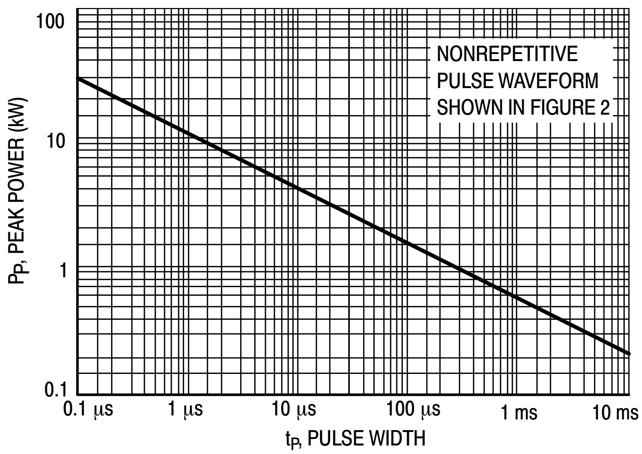


Figure 1. Pulse Rating Curve

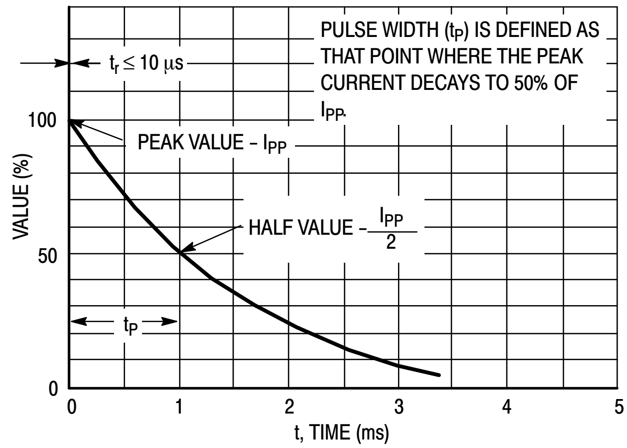


Figure 2. Pulse Waveform

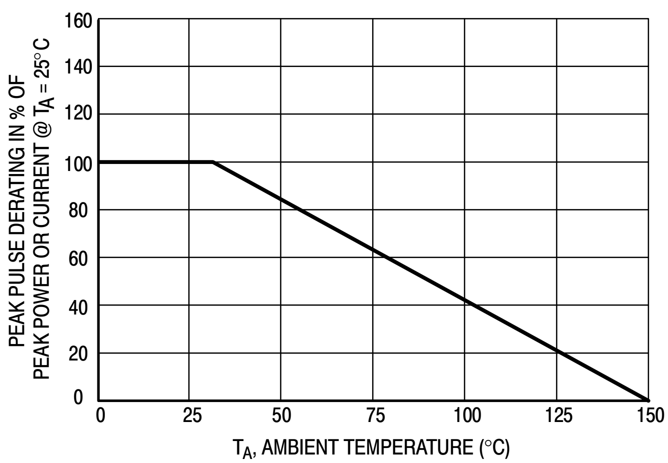


Figure 3. Pulse Derating Curve

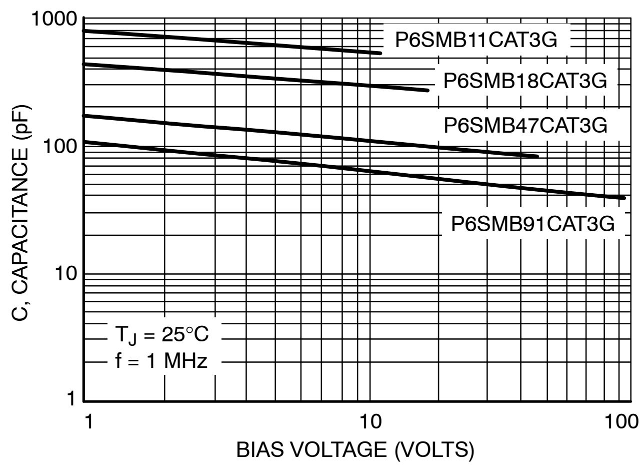
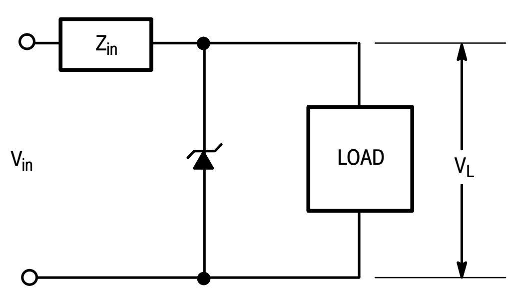


Figure 4. Typical Junction Capacitance vs. Bias Voltage

TYPICAL PROTECTION CIRCUIT



APPLICATION NOTES

RESPONSE TIME

In most applications, the transient suppressor device is placed in parallel with the equipment or component to be protected. In this situation, there is a time delay associated with the capacitance of the device and an overshoot condition associated with the inductance of the device and the inductance of the connection method. The capacitive effect is of minor importance in the parallel protection scheme because it only produces a time delay in the transition from the operating voltage to the clamp voltage as shown in Figure 4.

The inductive effects in the device are due to actual turn-on time (time required for the device to go from zero current to full current) and lead inductance. This inductive effect produces an overshoot in the voltage across the equipment or component being protected as shown in Figure 5. Minimizing this overshoot is very important in the application, since the main purpose for adding a transient suppressor is to clamp voltage spikes. The SMB series have a very good response time, typically < 1 ns and negligible inductance. However, external inductive effects could produce unacceptable overshoot. Proper circuit layout, minimum lead lengths and placing the suppressor device as close as possible to the equipment or components to be protected will minimize this overshoot.

Some input impedance represented by Z_{in} is essential to prevent overstress of the protection device. This impedance should be as high as possible, without restricting the circuit operation.

DUTY CYCLE DERATING

The data of Figure 1 applies for non-repetitive conditions and at a lead temperature of 25°C. If the duty cycle increases, the peak power must be reduced as indicated by the curves of Figure 6. Average power must be derated as the lead or ambient temperature rises above 25°C. The average power derating curve normally given on data sheets may be normalized and used for this purpose.

At first glance the derating curves of Figure 6 appear to be in error as the 10 ms pulse has a higher derating factor than the 10 μs pulse. However, when the derating factor for a given pulse of Figure 6 is multiplied by the peak power value of Figure 1 for the same pulse, the results follow the expected trend.

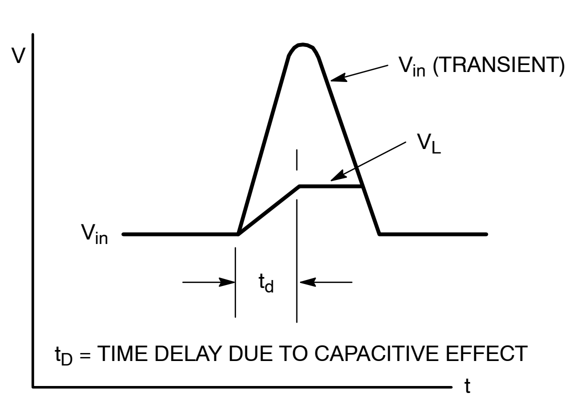


Figure 5.

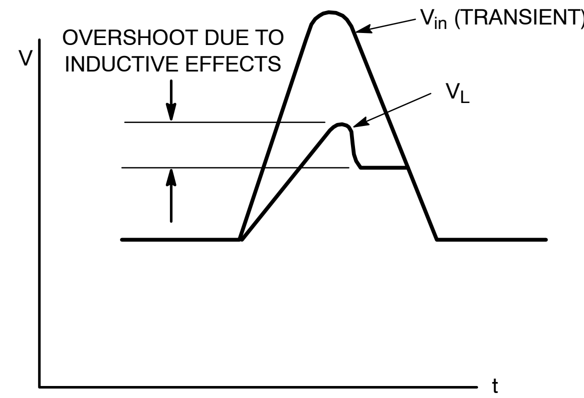


Figure 6.

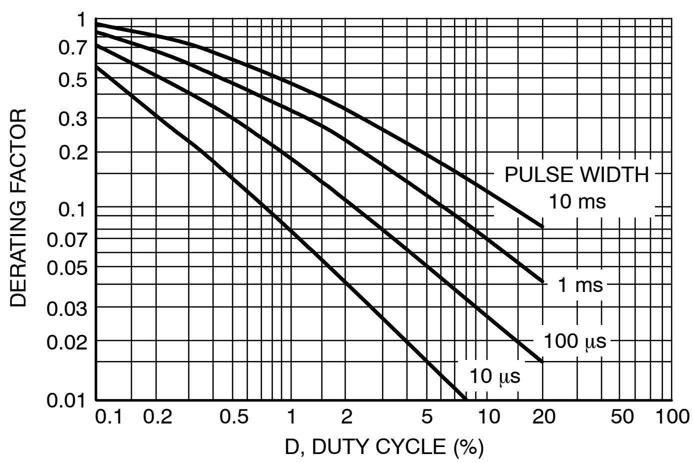


Figure 7. Typical Derating Factor for Duty Cycle

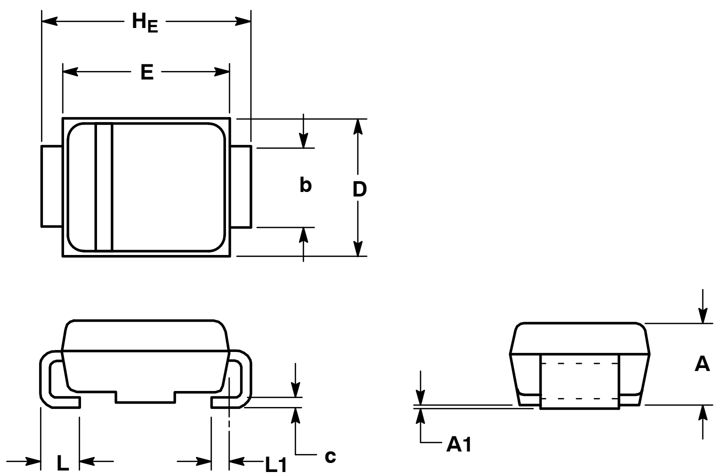
UL RECOGNITION

The entire series has *Underwriters Laboratory Recognition* for the classification of protectors (QVGQ2) under the UL standard for safety 497B and File #E210057. Many competitors only have one or two devices recognized or have recognition in a non-protective category. Some competitors have no recognition at all. With the UL497B recognition, our parts successfully passed several tests including Strike Voltage Breakdown test, Endurance Conditioning, Temperature test, Dielectric Voltage-Withstand test, Discharge test and several more.

Whereas, some competitors have only passed a flammability test for the package material, we have been recognized for much more to be included in their Protector category.

PACKAGE DIMENSIONS

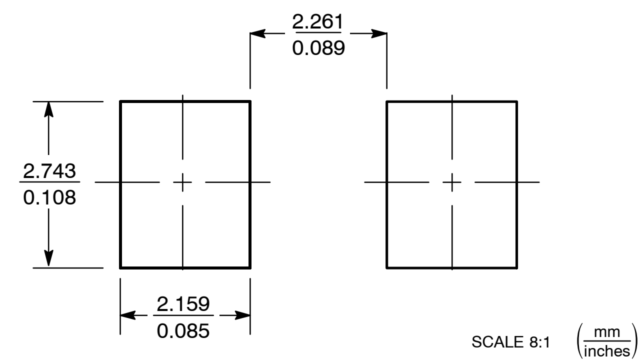
SMB
DO−214AA
CASE 403A−03
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. D DIMENSION SHALL BE MEASURED WITHIN DIMENSION P.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.90	2.13	2.45	0.075	0.084	0.096
A1	0.05	0.10	0.20	0.002	0.004	0.008
b	1.96	2.03	2.20	0.077	0.080	0.087
c	0.15	0.23	0.31	0.006	0.009	0.012
D	3.30	3.56	3.95	0.130	0.140	0.156
E	4.06	4.32	4.60	0.160	0.170	0.181
H_E	5.21	5.44	5.60	0.205	0.214	0.220
L	0.76	1.02	1.60	0.030	0.040	0.063
L1		0.51 REF			0.020 REF	

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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