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4M-BIT [x 1/x 2/x 4] 1.8V CMOS SERIAL FLASH
8M-BIT [x 1/x 2/x 4] 1.8V CMOS SERIAL FLASH

FEATURES

GENERAL

- Serial Peripheral Interface compatible -- Mode 0 and Mode 3
- 4M: 4,194,304 x 1 bit structure or 2,097,152 x 2 bits (two I/O read mode) structure or 1,048,576 x 4 bits (four I/O read mode) structure
8M: 8,388,608 x 1 bit structure or 4,194,304 x 2 bits (two I/O read mode) structure or 2,097,152 x 4 bits (four I/O read mode) structure
- Equal Sectors with 4K byte each, or Equal Blocks with 32K byte each or Equal Blocks with 64K byte each
 - Any Block can be erased individually
- Single Power Supply Operation
 - 1.65 to 2.0 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V

PERFORMANCE

- High Performance
 - Fast read
 - 1 I/O: 40MHz with 8 dummy cycles
 - 2 I/O: 40MHz with 4 dummy cycles, equivalent to 80MHz
 - 4 I/O: 33MHz with 6 dummy cycles, equivalent to 132MHz
 - Fast program time: 2ms(typ.) and 7ms(max.)/page (256-byte per page)
 - Byte program time: 30us (typical)
 - Continuously program mode (automatically increase address under word program mode)
 - Fast erase time: 90ms (typ.)/sector (4K-byte per sector); 0.8s(typ.) /block (32K-byte per block); 1.5s(typ.) /block (64K-byte per block); 7.5s(typ.) /chip for 4M; 15s(typ.) /chip for 8M
- Low Power Consumption
 - Low active read current: 12mA(max.) at 40MHz, 6mA(max.) at 25MHz
 - Low active erase/programming current: 22mA (max.)
 - Low standby current: 5uA (max.)
- Deep Power Down: 5uA(max.)
- Typical 100,000 erase/program cycles
- 20 years data retention

SOFTWARE FEATURES

- Input Data Format
 - 1-byte Command code
- Advanced Security Features
 - Block lock protection
The BP0-BP3 status bit defines the size of the area to be software protection against program and erase instructions
 - Additional 512-bit secured OTP for unique identifier
- Auto Erase and Auto Program Algorithm
 - Automatically erases and verifies data at selected sector or block
 - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programmed should have page in the erased state first)
- Status Register Feature
- Electronic Identification
 - JEDEC 1-byte manufacturer ID and 2-byte device ID

- RES command for 1-byte Device ID
- Both REMS,REMS2 and REMS4 commands for 1-byte manufacturer ID and 1-byte device ID

HARDWARE FEATURES

- SCLK Input
 - Serial clock input
- SI/SIO0
 - Serial Data Input or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- SO/SIO1
 - Serial Data Output or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- WP#/SIO2
 - Hardware write protection or serial data Input/Output for 4 x I/O read mode
- RESET#/HOLD#/SIO3
 - Hardware Reset/HOLD/Serial input & Output for 4 x I/O read mode, the pin defaults to be RESET#
- PACKAGE
 - 8-land USON (4x4mm)
 - 8-pin SOP (150mil)
 - 8-land WSON (6x5mm)
 - **All Pb-free devices are RoHS Compliant**

GENERAL DESCRIPTION

The MX25U4035 are 4,194,304 bit serial Flash memory, which is configured as 524,288 x 8 internally. When it is in two or four I/O read mode, the structure becomes 2,097,152 bits x 2 or 1,048,576 bits x 4. The MX25U8035 are 8,388,608 bit serial Flash memory, which is configured as 1,048,576 x 8 internally. When it is in two or four I/O read mode, the structure becomes 4,194,304 bits x 2 or 2,097,152 bits x 4. When it is in two or four I/O read mode, the structure becomes 8,388,608 bits x 2 or 4,194,304 bits x 4. The MX25U4035/MX25U8035 feature a serial peripheral interface and software protocol allowing operation on a simple 4-wire bus while it is in single I/O mode. The four bus signals are a clock input (SCLK), a serial data input (SI), a serial data output (SO) and a chip select (CS#). Serial access to the device is enabled by CS# input.

When it is in two I/O read mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output. When it is in four I/O read mode, the SI pin, SO pin, WP# pin and RESET#/HOLD# pin become SIO0 pin, SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data output.

The MX25U4035/MX25U8035 provides sequential read operation on whole chip.

After program/erase command is issued, auto program/ erase algorithms which program/ erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis for Continuously program mode, and erase command is executes on sector (4K-byte), block (32K-byte), or block (64K-byte), or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

Advanced security features enhance the protection and security functions, please see security features section for more details.

When the device is not in operation and CS# is high, it is put in standby mode and draws less than 5uA DC current.

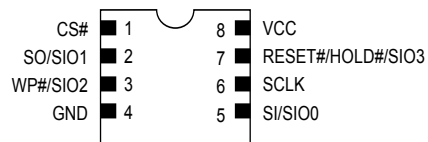
The MX25U4035/MX25U8035 utilizes MXIC's proprietary memory cell, which reliably stores memory contents even after typical 100,000 program and erase cycles.

Table 1. Additional Feature Comparison

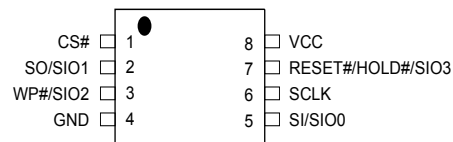
Part Name	Protection and Security		Read Performance		Identifier				
	Flexible Block Protection (BP0-BP3)	512-bit secured OTP	2 I/O Read	4 I/O Read	RES (command: AB hex)	REMS (command: 90 hex)	REMS2 (command: EF hex)	REMS4 (command: DF hex)	RDID (command: 9F hex)
MX25U4035	V	V	V	V	33 (hex)	C2 33 (hex) (if ADD=0)	C2 33 (hex) (if ADD=0)	C2 33 (hex) (if ADD=0)	C2 25 33 (hex)
MX25U8035	V	V	V	V	34 (hex)	C2 34 (hex) (if ADD=0)	C2 34 (hex) (if ADD=0)	C2 34 (hex) (if ADD=0)	C2 25 34 (hex)

PIN CONFIGURATIONS

8-LAND USON (4x4mm)/8-LAND WSON (6x5mm)



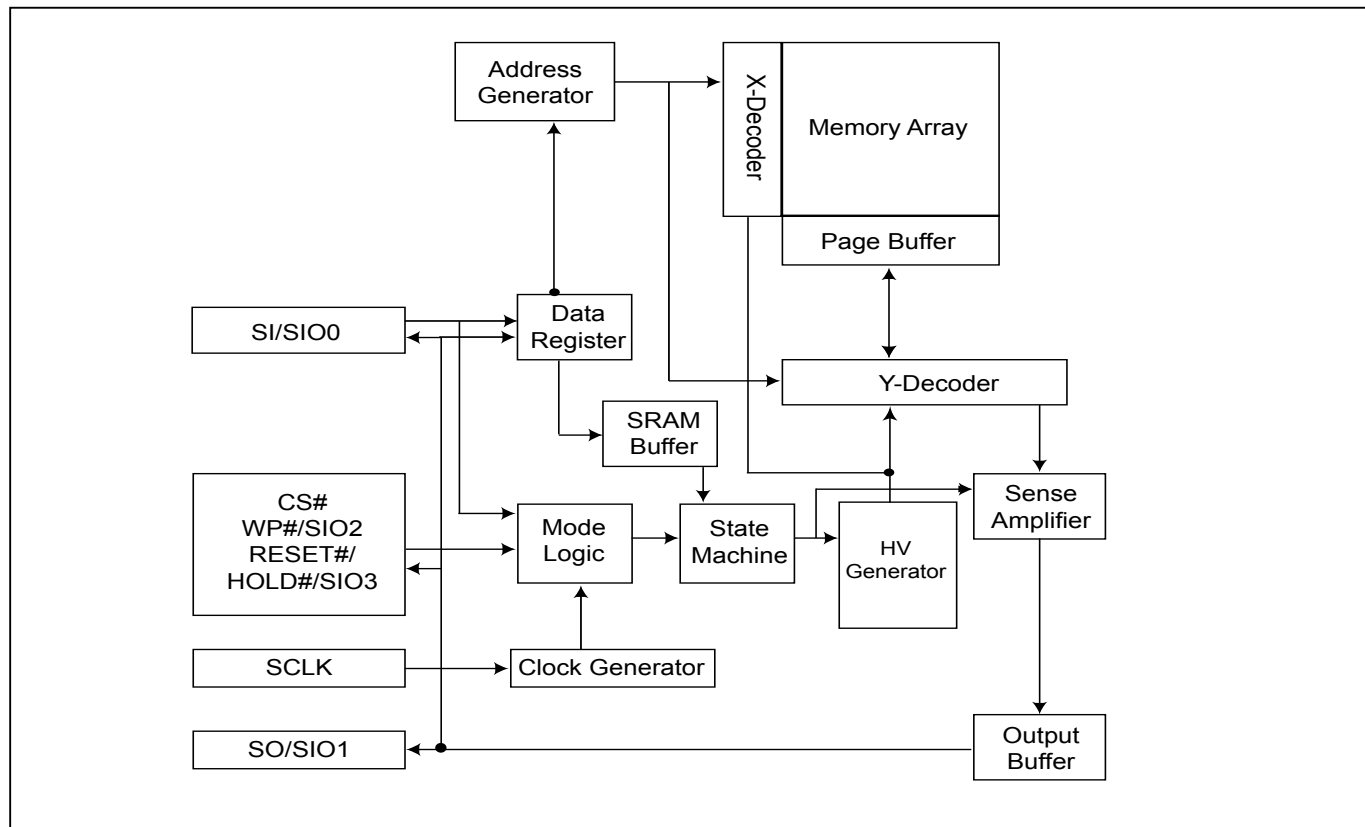
8-PIN SOP (150mil)



PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SCLK	Clock Input
WP#/SIO2	Write protection: connect to GND or Serial Data Input & Output (for 4xI/O read mode)
RESET#/HOLD#/SIO3	RESET#/HOLD# or Serial Data Input & Output (for 4xI/O read mode) (default RESET# for Single & Daul I/O)
VCC	+ 1.8V Power Supply
GND	Ground

BLOCK DIAGRAM



DATA PROTECTION

The MX25U4035/MX25U8035 is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the standby mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data. The WEL bit will return to reset stage under following situation:
 - Power-up
 - Write Disable (WRDI) command completion
 - Write Status Register (WRSR) command completion
 - Page Program (PP) command completion
 - Continuously Program mode (CP) instruction completion
 - Sector Erase (SE) command completion
 - Block Erase 32KB (BE32K) command completion
 - Block Erase (BE) command completion
 - Chip Erase (CE) command completion
- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from deep power down mode command (RDP) and Read Electronic Signature command (RES).
- Advanced Security Features: there are some protection and security features which protect content from inadvertent write and hostile access.

I. Block lock protection

- The Software Protected Mode (SPM) use (BP3, BP2, BP1, BP0) bits to allow part of memory to be protected as read only. The protected area definition is shown as table of "[Protected Area Sizes](#)", the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits. Please refer to table of "[protected area sizes](#)".
- The Hardware Protected Mode (HPM) use WP#/SIO2 to protect the (BP3, BP2, BP1, BP0) bits and SRWD bit. If the system goes into four I/O read mode, the feature of HPM will be disabled.

Table 2. Protected Area Sizes

Status bit				Protect Level	
BP3	BP2	BP1	BP0	4Mb	8Mb
0	0	0	0	0 (none)	0 (none)
0	0	0	1	1 (1 block, 1/8 area, block#7)	1 (1 block, 1/16 area, block#15)
0	0	1	0	2 (2 blocks, 1/4 area, block#6-7)	2 (2 blocks, 1/8 area, block#14-15)
0	0	1	1	3 (4 blocks, 1/2 area, block#4-7)	3 (4 blocks, 1/4 area, block#12-15)
0	1	0	0	4 (8 blocks, ALL)	4 (8 blocks, 1/2 area, block#8-15)
0	1	0	1	5 (8 blocks, ALL)	5 (16 blocks, ALL)
0	1	1	0	6 (8 blocks, ALL)	6 (16 blocks, ALL)
0	1	1	1	7 (8 blocks, ALL)	7 (16 blocks, ALL)
1	0	0	0	8 (none)	8 (none)
1	0	0	1	9 (1 block, 1/8 area, block#0)	9 (1 block, 1/16 area, block#0)
1	0	1	0	10 (2 blocks, 1/4 area, block#0-1)	10 (2 blocks, 1/8 area, block#0-1)
1	0	1	1	11 (4 blocks, 1/2 area, block#0-3)	11 (4 blocks, 1/4 area, block#0-3)
1	1	0	0	12 (8 blocks, ALL)	12 (8 blocks, 1/2 area, block#0-7)
1	1	0	1	13 (8 blocks, ALL)	13 (16 blocks, ALL)
1	1	1	0	14 (8 blocks, ALL)	14 (16 blocks, ALL)
1	1	1	1	15 (8 blocks, ALL)	15 (16 blocks, ALL)

II. Additional 512-bit secured OTP for unique identifier: to provide 512-bit one-time program area for setting device unique serial number - Which may be set by factory or system customer. Please refer to [table 3. 512-bit secured OTP definition](#).

- Security register bit 0 indicates whether the chip is locked by factory or not.
- To program the 512-bit secured OTP by entering 512-bit secured OTP mode (with ENSO command), and going through normal program procedure, and then exiting 512-bit secured OTP mode by writing EXSO command.
- Customer may lock-down the customer lockable secured OTP by writing WRSCUR (write security register) command to set customer lock-down bit1 as "1". Please refer to table of "[security register definition](#)" for security register bit definition and table of "512-bit secured OTP definition" for address range definition.
- **Note:** Once lock-down whatever by factory or customer, it cannot be changed any more. While in 512-bit secured OTP mode, array access is not allowed.

Table 3. 512-bit Secured OTP Definition

Address range	Size	Standard Factory Lock	Customer Lock
xxxx00~xxxx0F	128-bit	ESN (electrical serial number)	Determined by customer
xxxx10~xxxx3F	384-bit	N/A	

Memory Organization

Table 4-1. Memory Organization (4Mb)

Block (64KB)	Block (32KB)	Sector (4KB)	Address Range	
7	15	127	07F000h	07FFFFh
		:	:	:
	14	112	070000h	070FFFh
6	13	111	06F000h	06FFFFh
		:	:	:
	12	96	060000h	060FFFh
5	11	95	05F000h	05FFFFh
		:	:	:
	10	80	050000h	050FFFh
4	9	79	04F000h	04FFFFh
		:	:	:
	8	64	040000h	040FFFh
3	7	63	03F000h	03FFFFh
		:	:	:
	6	48	030000h	030FFFh
2	5	47	02F000h	02FFFFh
		:	:	:
	4	32	020000h	020FFFh
1	3	31	01F000h	01FFFFh
		:	:	:
	2	16	010000h	010FFFh
0	1 0	15	00F000h	00FFFFh
		:	:	:
		2	002000h	002FFFh
		1	001000h	001FFFh
		0	000000h	000FFFh

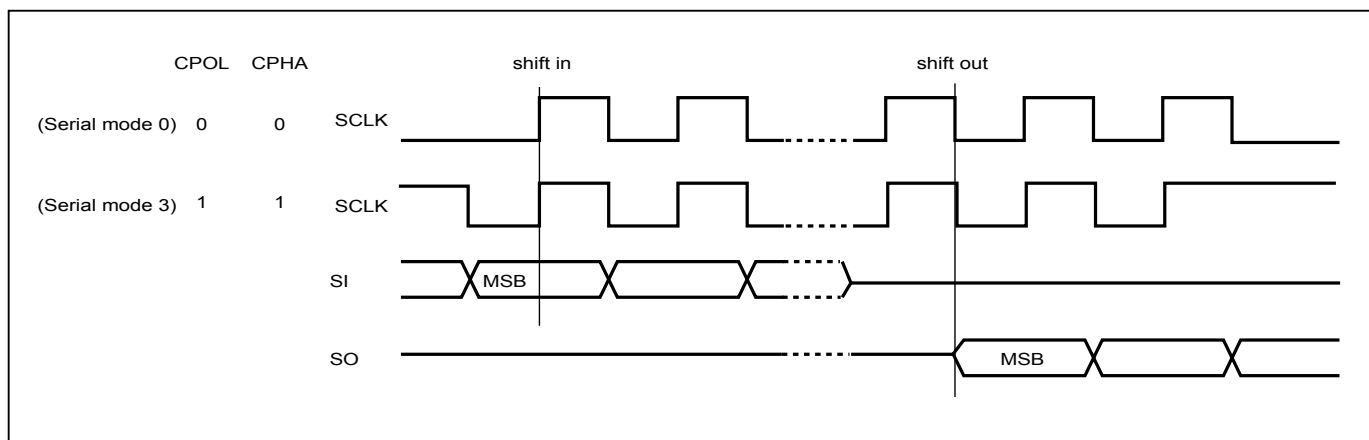
Table 4-2. Memory Organization (8Mb)

Block (64KB)	Block (32KB)	Sector (4KB)	Address Range	
15	31	255	0FF000h	0FFFFFFh
		:	:	:
	30	240	0F0000h	0F0FFFh
14	29	239	0EF000h	0EFFFFh
		:	:	:
	28	224	0E0000h	0E0FFFh
13	27	223	0DF000h	0DFFFFh
		:	:	:
	26	208	0D0000h	0D0FFFh
12	25	207	0CF000h	0CFFFFh
		:	:	:
	24	192	0C0000h	0C0FFFh
11	23	191	0BF000h	0BFFFFh
		:	:	:
	22	176	0B0000h	0B0FFFh
10	21	175	0AF000h	0AFFFFh
		:	:	:
	20	160	0A0000h	0A0FFFh
9	19	159	09F000h	09FFFFh
		:	:	:
	18	144	090000h	090FFFh
8	17	143	08F000h	08FFFFh
		:	:	:
	16	128	080000h	080FFFh
7	15	127	07F000h	07FFFFh
		:	:	:
	14	112	070000h	070FFFh
6	13	111	06F000h	06FFFFh
		:	:	:
	12	96	060000h	060FFFh
5	11	95	05F000h	05FFFFh
		:	:	:
	10	80	050000h	050FFFh
4	9	79	04F000h	04FFFFh
		:	:	:
	8	64	040000h	040FFFh
3	7	63	03F000h	03FFFFh
		:	:	:
	6	48	030000h	030FFFh
2	5	47	02F000h	02FFFFh
		:	:	:
	4	32	020000h	020FFFh
1	3	31	01F000h	01FFFFh
		:	:	:
	2	16	010000h	010FFFh
0	1 0	15	00F000h	00FFFFh
		:	:	:
		2	002000h	002FFFh
		1	001000h	001FFFh
		0	000000h	000FFFh

DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.
2. When incorrect command is inputted to this LSI, this LSI becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this LSI should be High-Z.
3. When correct command is inputted to this LSI, this LSI becomes active mode and keeps the active mode until next CS# rising edge.
4. Input data is latched on the rising edge of Serial Clock (SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as Figure 1. "Serial Modes Supported".
5. For the following instructions: RDID, RDSR, RDSCUR, READ, FAST_READ, 2READ, 4READ, RES, REMS, REMS2 and REMS4 the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE32K, BE, CE, PP, 4PP, CP, RDP, DP, ENSO, EXSO, and WRSCUR, the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.
6. During the progress of Write Status Register, Program, Erase operation, to access the memory array is neglected and not affect the current operation of Write Status Register, Program, Erase.

Figure 1. Serial Modes Supported



Note:

CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

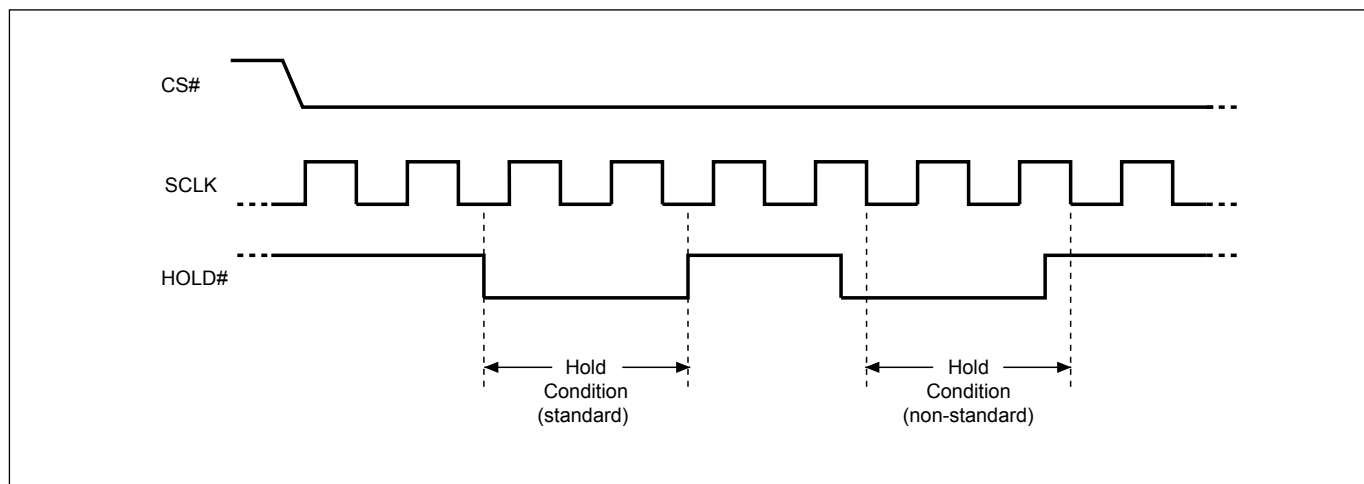
HOLD FEATURE

The HDE instruction is required to enable the HOLD# pin function.

HOLD# pin signal goes low to hold any serial communications with the device. The HOLD feature will not stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD requires Chip Select (CS#) keeping low and starts on falling edge of HOLD# pin signal while Serial Clock (SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not start until Serial Clock signal being low). The HOLD condition ends on the rising edge of HOLD# pin signal while Serial Clock (SCLK) signal is being low (if Serial Clock signal is not being low, HOLD operation will not end until Serial Clock being low), see Figure 2.

Figure 2. Hold Condition Operation



The Serial Data Output (SO) is high impedance, both Serial Data Input (SI) and Serial Clock (SCLK) are don't care during the HOLD operation. If Chip Select (CS#) drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and CS# must be at low.

COMMAND DESCRIPTION

Table 5. Command Set

COMMAND (byte)	WREN (write enable)	WRDI (write disable)	RDID (read identification)	RDSR (read status register)	WRSR (write status register)	READ (read data)	FAST READ (fast read data)
Command (hex)	06	04	9F	05	01	03	0B
Input Cycles					Data(8)	ADD(24)	ADD(24)
Dummy Cycles							8
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID	to read out the values of the status register	to write new values to the status register	n bytes read out until CS# goes high	n bytes read out until CS# goes high

COMMAND (byte)	2READ (2 x I/O read command) Note1	4READ (4 x I/O read command)	4PP (quad page program)	SE (sector erase)	BE (block erase 64KB)	BE 32K (block erase 32KB)	CE (chip erase)
Command (hex)	BB	EB	38	20	D8	52	60 or C7
Input Cycles	ADD(12)	ADD(6)+ Indicator (2)	ADD(6)+ Data(512)	ADD(24)	ADD(24)	ADD(24)	
Dummy Cycles	4	4					
Action	n bytes read out by 2 x I/O until CS# goes high	n bytes read out by 4 x I/O until CS# goes high	quad input to program the selected page	to erase the selected sector	to erase the selected 64KB block	to erase the selected 32KB block	to erase whole chip

COMMAND (byte)	PP (Page program)	CP (Continuously program mode)	DP (Deep power down)	RDP (Release from deep power down)	RES (read electronic ID)	REMS (read electronic manufacturer & device ID)	REMS2 (read ID for 2x I/O mode)
Command (hex)	02	AD	B9	AB	AB	90	EF
Input Cycles	ADD(24)+ Data(2048)	ADD(24)+ Data(16)				ADD(24)	ADD(24)
Dummy Cycles					24		
Action	to program the selected page	continuously program whole chip, the address is automatically increase	enters deep power down mode	release from deep power down mode	to read out 1-byte Device ID	output the Manufacturer ID & Device ID	output the Manufacturer ID & Device ID

COMMAND (byte)	REMS4 (read ID for 4x I/O mode)	ENSO (enter secured OTP)	EXSO (exit secured OTP)	RDSCUR (read security register)	WRSCUR (write security register)	ESRY (enable SO to output RY/BY#)	DSRY (disable SO to output RY/BY#)	HDE (HOLD# Enable)
Command (hex)	DF	B1	C1	2B	2F	70	80	AA
Input Cycles	ADD(24)							
Dummy Cycles								
Action	output the Manufact- urer ID & device ID	to enter the 512- bit Secured OTP mode	to exit the 512-bit Secured OTP mode	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be updated)	to enable SO to output RY/BY# during CP mode	to disable SO to output RY/BY# during CP mode	to enable HOLD# pin function

Note 1: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.

Note 2: In individual block write protection mode, all blocks/sectors is locked as default.

Note 3: The number in parentheses after "ADD" or "Data" stands for how many clock cycles it has. For example, "Data(8)" represents there are 8 clock cycles for the data in.

Note 4: The value of ADD of REMS/REMS2/REMS4 indicates the output of manufacturer ID or device ID. 00 will output manufacturer ID first and 01 will output device ID first.

(1) Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, 4PP, CP, SE, BE32K, BE, CE, and WRSR, which are intended to change the device content, should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→ sending WREN instruction code→ CS# goes high. (Please refer to [Figure 12](#))

(2) Write Disable (WRDI)

The Write Disable (WRDI) instruction is for resetting Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→ sending WRDI instruction code→ CS# goes high. (Please refer to [Figure 13](#))

The WEL bit is reset by following situations:

- Power-up
- Write Disable (WRDI) instruction completion
- Write Status Register (WRSR) instruction completion
- Page Program (PP) instruction completion
- Quad Page Program (4PP) instruction completion
- Sector Erase (SE) instruction completion
- Block Erase 32KB (BE32K) instruction completion
- Block Erase (BE) instruction completion
- Chip Erase (CE) instruction completion
- Continuously program mode (CP) instruction completion

(3) Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The MXIC Manufacturer ID is C2(hex), the memory type ID is 25(hex) as the first-byte device ID, and the individual device ID of second-byte ID are listed as table of "[ID Definitions](#)". (Please refer to [table 7](#))

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code→ 24-bits ID data out on SO→ to end RDID operation can use CS# to high at any time during data out. (Please refer to [Figure 14](#))

While Program/Erase operation is in progress, it will not decode the RDID instruction, so there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

(4) Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition) and continuously. It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low→ sending RDSR instruction code→ Status Register data out on SO (Please refer to [Figure 15](#))

The definition of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to 1, which means the internal write enable latch is set, the device can accept program/erase/write status register instruction. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase/write status register instruction. The program/erase command will be ignored and not affect value of WEL bit if it is applied to a protected memory area.

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3, BP2, BP1, BP0) bits, volatile bits, indicate the protected area (as defined in [table 2](#)) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase 32KB (BE32K), Block Erase (BE) and Chip Erase (CE) instructions (only if Block Protect bits (BP2:BP0) set to 0, the CE instruction can be executed).

The BP3, BP2, BP1, BP0 bits default value are "1". Which is protected.

QE bit. The Quad Enable (QE) bit, volatile bit, performs Quad when it is reset to "0" (factory default) to enable WP# or is set to "1" to enable Quad SIO2 and SIO3.

SRWD bit. The Status Register Write Disable (SRWD) bit, volatile bit, is operated together with Write Protection (WP#/SIO2) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP#/SIO2 pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP3, BP2, BP1, BP0) are read only. The SRWD bit defaults to be "0".

Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRWD (status register write protect)	QE (Quad Enable)	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
1=status register write disable	1=Quad Enable 0=not Quad Enable	(note 1)	(note 1)	(note 1)	(note 1)	1=write enable 0=not write enable	1=write operation 0=not in write operation

Note: see the [table 2 "Protected Area Size"](#).

(5) Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3, BP2, BP1, BP0) bits to define the protected area of memory (as shown in [table 2](#)). The WRSR also can set or reset the Quad enable (QE) bit and set or reset the Status Register Write Disable (SRWD) bit in accordance with Write Protection (WP#/SIO2) pin signal, but has no effect on bit1(WEL) and bit0 (WIP) of the status register. The WRSR instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

The sequence of issuing WRSR instruction is: CS# goes low→ sending WRSR instruction code→ Status Register data on SI→ CS# goes high. (Please refer to [Figure 16](#))

The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Table 6. Protection Modes

Mode	Status register condition	WP# and SRWD bit status	Memory
Software protection mode (SPM)	Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP3 bits can be changed	WP#=1 and SRWD bit=0, or WP#=0 and SRWD bit=0, or WP#=1 and SRWD=1	The protected area cannot be program or erase.
Hardware protection mode (HPM)	The SRWD, BP0-BP3 of status register bits cannot be changed	WP#=0, SRWD bit=1	The protected area cannot be program or erase.

Note: As defined by the values in the Block Protect (BP3, BP2, BP1, BP0) bits of the Status Register, as shown in [Table 2](#).

As the above table showing, the summary of the Software Protected Mode (SPM) and Hardware Protected Mode (HPM).

Software Protected Mode (SPM):

- When SRWD bit=0, no matter WP#/SIO2 is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM).
- When SRWD bit=1 and WP#/SIO2 is high, the WREN instruction may set the WEL bit which can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM).

Note:

If SRWD bit=1 but WP#/SIO2 is low, it is impossible to write the Status Register even if the WEL bit has previously been set. It is rejected to write the Status Register and not be executed.

Hardware Protected Mode (HPM):

- When SRWD bit=1, and then WP#/SIO2 is low (or WP#/SIO2 is low before SRWD bit=1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP3, BP2, BP1, BP0 and hardware protected mode by the WP#/SIO2 to against data modification.

Note:

To exit the hardware protected mode requires WP#/SIO2 driving high once the hardware protected mode is entered. If the WP#/SIO2 pin is permanently connected to high, the hardware protected mode can never be entered; only can use software protected mode via BP3, BP2, BP1, BP0.

If the system goes into four I/O read mode, the feature of HPM will be disabled.

(6) Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low→ sending READ instruction code→ 3-byte address on SI→ data out on SO→ to end READ operation can use CS# to high at any time during data out. (Please refer to [Figure 17](#))

(7) Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FAST_READ instruction is: CS# goes low→ sending FAST_READ instruction code→3-byte address on SI→1-dummy byte (default) address on SI→data out on SO→ to end FAST_READ operation can use CS# to high at any time during data out. (Please refer to [Figure 18](#))

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

(8) 2 x I/O Read Mode (2READ)

The 2READ instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 2READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 2READ instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing 2READ instruction is: CS# goes low→ sending 2READ instruction→ 24-bit address interleave on SIO1 & SIO0→ 4-bit dummy cycle on SIO1 & SIO0→ data out interleave on SIO1 & SIO0→ to end 2READ operation can use CS# to high at any time during data out (Please refer to [Figure 19 for 2 x I/O Read Mode Timing Waveform](#)).

While Program/Erase/Write Status Register cycle is in progress, 2READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

(9) 4 x I/O Read Mode (4READ)

The 4READ instruction enable quad throughput of Serial Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the 4READ instruction. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency f_Q . The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 4READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 4READ instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing 4READ instruction is: CS# goes low → sending 4READ instruction → 24-bit address interleave on SIO3, SIO2, SIO1 & SIO0 → 6 dummy cycles → data out interleave on SIO3, SIO2, SIO1 & SIO0 → to end 4READ operation can use CS# to high at any time during data out (Please refer to [figure 20 for 4 x I/O Read Mode Timing Waveform](#)).

Another sequence of issuing 4 READ instruction especially useful in random access is : CS# goes low → sending 4 READ instruction → 3-bytes address interleave on SIO3, SIO2, SIO1 & SIO0 → performance enhance toggling bit P[7:0] → 4 dummy cycles → data out still CS# goes high → CS# goes low (reduce 4 Read instruction) → 24-bit random access address (Please refer to [figure 21 for 4x I/O read enhance performance mode timing waveform](#)).

In the performance-enhancing mode, P[7:4] must be toggling with P[3:0] ; likewise P[7:0]=A5h,5Ah,F0h or 0Fh can make this mode continue and reduce the next 4READ instruction. Once P[7:4] is no longer toggling with P[3:0]; likewise P[7:0]=FFh,00h,AAh or 55h and afterwards CS# is raised and then lowered, the system then will escape from performance enhance mode and return to normal operation.

While Program/Erase/Write Status Register cycle is in progress, 4READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

(10) Sector Erase (SE)

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (see table of [memory organization](#)) is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

Address bits [Am-A12] (Am is the most significant address) select the sector address.

The sequence of issuing SE instruction is: CS# goes low → sending SE instruction code → 3-byte address on SI → CS# goes high. (Please refer to [Figure 25](#))

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the sector is protected by BP3, BP2, BP1, BP0 bits, the Sector Erase (SE) instruction will not be executed on the sector.

(11) Block Erase (BE32K)

The Block Erase (BE32K) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 32K-byte block erase operation. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE32K). Any address of the block (see table of [memory organization](#)) is a valid address for Block Erase (BE32K) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE32K instruction is: CS# goes low → sending BE32K instruction code → 3-byte address on SI → CS# goes high. (see [Figure 26](#))

The self-timed Block Erase Cycle time (tBE32K) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked out during the Block Erase cycle is in progress. The WIP sets 1 during the tBE32K timing, and sets 0 when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the block is protected by BP3, BP2, BP1, BP0 bits, the Block Erase (tBE32K) instruction will not be executed on the block.

(12) Block Erase (BE)

The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte block erase operation. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (see table of [memory organization](#)) is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE instruction is: CS# goes low → sending BE instruction code → 3-byte address on SI → CS# goes high. (see [Figure 27](#))

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Block Erase cycle is in progress. The WIP sets 1 during the tBE timing, and sets 0 when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the block is protected by BP3, BP2, BP1, BP0 bits, the Block Erase (BE) instruction will not be executed on the block.

(13) Chip Erase (CE)

The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). The CS# must go high exactly at the byte boundary, otherwise the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low → sending CE instruction code → CS# goes high. (Please refer to [Figure 28](#))

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Chip Erase cycle is in progress. The WIP sets 1 during the tCE timing, and sets 0 when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the chip is protected by BP2, BP1, BP0 bits, the Chip Erase (CE) instruction will not be executed. It will be only executed when BP2, BP1, BP0 all set to "0".

(14) Page Program (PP)

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). The device programs only the last 256 data bytes sent to the device. If the entire 256 data bytes are going to be programmed, A7-A0 (The eight least significant address bits) should be set to 0. If the eight least significant address bits (A7-A0) are not all 0, all transmitted data going beyond the end of the current page are programmed from the start address of the same page (from the address A7-A0 are all 0). If more than 256 bytes are sent to the device, the data of the last 256-byte is programmed at the request page and previous data will be disregarded. If less than 256 bytes are sent to the device, the data is programmed at the requested address of the page without effect on other address of the same page.

The sequence of issuing PP instruction is: CS# goes low→ sending PP instruction code→3-byte address on SI→ at least 1-byte on data on SI→ CS# goes high. (Please refer to [Figure 22](#))

The CS# must go high exactly at the byte boundary(the latest eighth bit of data being latched in), otherwise the instruction will be rejected and will not be executed.

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Page Program cycle is in progress. The WIP sets 1 during the tPP timing, and sets 0 when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP3, BP2, BP1, BP0 bits, the Page Program (PP) instruction will not be executed.

(15) 4 x I/O Page Program (4PP)

The Quad Page Program (4PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit and Quad Enable (QE) bit must be set to "1" before sending the Quad Page Program (4PP). The Quad Page Programming takes four pins: SIO0, SIO1, SIO2, and SIO3 as address and data input, which can improve programmer performance and the effectiveness of application of lower clock less than 20MHz. For system with faster clock, the Quad page program cannot provide more actual favors, because the required internal page program time is far more than the time data flows in. Therefore, we suggest that while executing this command (especially during sending data), user can slow the clock speed down to 20MHz below. The other function descriptions are as same as standard page program.

The sequence of issuing 4PP instruction is: CS# goes low→sending 4PP instruction code→3-byte address on SIO[3:0]→ at least 1-byte on data on SIO[3:0]→CS# goes high. (Please refer to [Figure 23](#))

(16) Continuously program mode (CP mode)

The CP mode may enhance program performance by automatically increasing address to the next higher address after each byte data has been programmed.

The Continuously program (CP) instruction is for multiple byte program to Flash. A write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Continuously program (CP) instruction. CS# requires to go high before CP instruction is executing. After CP instruction and address input, two bytes of data is input sequentially from MSB(bit7) to LSB(bit0). The first byte data will be programmed to the initial address range with A0=0 and second byte data with A0=1. If only one byte data is input, the CP mode will not process. If more than two bytes data are input, the additional data will be ignored and only the first two byte data are valid. The CP program instruction will be ignored and not affect the WEL bit if it is applied to a protected memory area. Any byte to be programmed should be in the erase state (FF) first. It will not roll over during the CP mode, once the

last unprotected address has been reached, the chip will exit CP mode and reset write Enable Latch bit (WEL) as "0" and CP mode bit as "0". Please check the WIP bit status if it is not in write progress before entering next valid instruction. During CP mode, the valid commands are CP command (AD hex), WRDI command (04 hex), RDSR command (05 hex), and RDSCUR command (2B hex). And the WRDI command is valid after completion of a CP programming cycle, which means the WIP bit=0.

The sequence of issuing CP instruction is : CS# high to low→ sending CP instruction code→ 3-byte address on SI→ Data Byte on SI→CS# goes high to low→ sending CP instruction.....→ last desired byte programmed or sending Write Disable (WRDI) instruction to end CP mode-> sending RDSR instruction to verify if CP mode is ended. (Please refer to [Figure 24 of CP mode timing waveform](#))

Three methods to detect the completion of a program cycle during CP mode:

- 1) Software method-I: by checking WIP bit of Status Register to detect the completion of CP mode.
- 2) Software method-II: by waiting for a tBP time out to determine if it may load next valid command or not.
- 3) Hardware method: by writing ESRY (enable SO to output RY/BY#) instruction to detect the completion of a program cycle during CP mode. The ESRY instruction must be executed before CP mode instruction issuing. Once it is enabled in CP mode, the CS# goes low will drive out the RY/BY# status on SO, "0" indicates busy stage, "1" indicates ready stage, SO pin outputs tri-state if CS# goes high. DSRY (disable SO to output RY/BY#) instruction to disable the SO to output RY/BY# and return to status register data output during CP mode. Please note that the ESRY/DSRY commands are not accepted unless the completion of CP mode.

(17) Deep Power-down (DP)

The Deep Power-down (DP) instruction is for setting the device on the minimizing the power consumption (to entering the Deep Power-down mode), the standby current is reduced from ISB1 to ISB2). The Deep Power-down mode requires the Deep Power-down (DP) instruction to enter, during the Deep Power-down mode, the device is not active and all Write/Program/Erase instruction are ignored. When CS# goes high, it's only in standby mode not deep power-down mode. It's different from Standby mode.

The sequence of issuing DP instruction is: CS# goes low→ sending DP instruction code→CS# goes high. (Please refer to [Figure 29](#))

Once the DP instruction is set, all instruction will be ignored except the Release from Deep Power-down mode (RDP) and Read Electronic Signature (RES) instruction. (Those instructions allow the ID being reading out). When Power-down, the deep power-down mode automatically stops, and when power-up, the device automatically is in standby mode. For RDP instruction the CS# must go high exactly at the byte boundary (the latest eighth bit of instruction code been latched-in); otherwise, the instruction will not executed. As soon as Chip Select (CS#) goes high, a delay of tDP is required before entering the Deep Power-down mode.

(18) Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is terminated by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by tRES2, and Chip Select (CS#) must remain High for at least tRES2(max), as specified in [Table 10.AC Characteristics](#). Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions. The RDP instruction is only for releasing from Deep Power Down Mode.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as table of [ID Definitions](#) on next page. This is not the same as RDID instruction. It is not recommended to use for new design.

For new design, please use RDID instruction.

The sequence is shown as [Figure 30, 31](#). Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycle; there's no effect on the current program/erase/write cycle in progress.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2(max). Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

(19) Read Electronic Manufacturer ID & Device ID (REMS), (REMS2), (REMS4)

The REMS, REMS2 & REMS4 instruction is an alternative to the Release from Power-down/Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID. The REMS4 instruction is recommended to use for 4 I/O identification and REMS2 instruction is recommended to use for 2 I/O identification.

The REMS, REMS2 & REMS4 instruction is very similar to the Release from Power-down/Device ID instruction. The instruction is initiated by driving the CS# pin low and shift the instruction code "90h" or "EFh" or "DFh" followed by two dummy bytes and one bytes address (A7~A0). After which, the Manufacturer ID for MXIC (C2h) and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in [figure 32](#). The Device ID values are listed in [Table 7 of ID Definitions](#). If the one-byte address is initially set to 01h, then the device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Table 7. ID Definitions

Command Type	MX25U4035			MX25U8035		
RDID (JEDEC ID)	manufacturer ID	memory type	memory density	manufacturer ID	memory type	memory density
	C2	25	33	C2	25	34
RES	electronic ID			electronic ID		
	33			34		
REMS/REMS2/ REMS4	manufacturer ID	device ID		manufacturer ID	device ID	
	C2	33		C2	34	

(20) Enter Secured OTP (ENSO)

The ENSO instruction is for entering the additional 512-bit secured OTP mode. The additional 512-bit secured OTP is independent from main array, which may use to store unique serial number for system identifier. After entering the Secured OTP mode, and then follow standard read or program, procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is lock-down.

The sequence of issuing ENSO instruction is: CS# goes low→ sending ENSO instruction to enter Secured OTP mode→ CS# goes high.

Please note that WRSR/WRSCUR commands are not acceptable during the access of secure OTP region, once security OTP is lock down, only read related commands are valid.

(21) Exit Secured OTP (EXSO)

The EXSO instruction is for exiting the additional 512-bit secured OTP mode.

The sequence of issuing EXSO instruction is: CS# goes low→ sending EXSO instruction to exit Secured OTP mode→ CS# goes high.

(22) Read Security Register (RDSCUR)

The RDSCUR instruction is for reading the value of Security Register bits. The Read Security Register can be read at any time (even in program/erase/write status register/write security register condition) and continuously.

The sequence of issuing RDSCUR instruction is : CS# goes low→ sending RDSCUR instruction →Security Register data out on SO→ CS# goes high.

The definition of the Security Register bits is as below:

Secured OTP Indicator bit. The Secured OTP indicator bit shows the chip is locked by factory before ex- factory or not. When it is "0", it indicates non-factory lock; "1" indicates factory- lock.

Lock-down Secured OTP (LDSO) bit. By writing WRSCUR instruction, the LDSO bit may be set to "1" for customer lock-down purpose. However, once the bit is set to "1" (lock-down), the LDSO bit and the 512-bit Secured OTP area cannot be update any more. While it is in 512-bit secured OTP mode, main array access is not allowed.

Continuously Program Mode(CP mode) bit. The Continuously Program Mode bit indicates the status of CP mode, "0" indicates not in CP mode; "1" indicates in CP mode.

Table 8. Security Register Definition

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
x	x	x	Continuously Program mode (CP mode)	x	x	LDSO (indicate if lock-down	Secured OTP indicator bit
reserved	reserved	reserved	0=normal Program mode 1=CP mode (default=0)	reserved	reserved	0 = not lock- down 1 = lock-down (cannot program/erase OTP)	0 = non-factory lock 1 = factory lock
volatile bit	volatile bit	volatile bit	volatile bit	volatile bit	volatile bit	non-volatile bit	non-volatile bit

(23) Write Security Register (WRSCUR)

The WRSCUR instruction is for changing the values of Security Register Bits. Unlike write status register, the WREN instruction is not required before sending WRSCUR instruction. The WRSCUR instruction may change the values of bit1 (LDSO bit) for customer to lock-down the 512-bit Secured OTP area. Once the LDSO bit is set to "1", the Secured OTP area cannot be updated any more.

The sequence of issuing WRSCUR instruction is :CS# goes low→sending WRSCUR instruction→ CS# goes high.

The CS# must go high exactly at the boundary; otherwise, the instruction will be rejected and not executed.

(24) HOLD# pin function enable (HDE)

The HDE instruction is for enabling the HOLD# pin function. The RESET#/HOLD#/SIO# pin defaults to be as RESET# pin function. When HDE instruction is writing to the Flash, and then pin is set to be HOLD# pin. The HOLD mode will continue until power off. The pin is RESET# pin while power on stage. The HDE instruction is invalid during deep power down mode.

POWER-ON STATE

The device is at below states when power-up:

- Standby mode (please note it is not deep power-down mode)
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage unless the VCC achieves below correct level:

- VCC minimum at power-up stage and then after a delay of tVSL
- GND at power-down

Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

An internal power-on reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state.

For further protection on the device, if the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The read, write, erase, and program command should be sent after the below time delay:

- tVSL after VCC reached VCC minimum level

The device can accept read command after VCC reached VCC minimum and a time delay of tVSL.

Please refer to the figure of "*power-up timing*".

Note:

- To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended. (generally around 0.1uF)

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	-40°C to 85°C
Storage Temperature	-65°C to 150°C
Applied Input Voltage	-0.5V to VCC+0.5V
Applied Output Voltage	-0.5V to VCC+0.5V
VCC to Ground Potential	-0.5V to VCC+0.5V

NOTICE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot to VCC+1.0V to VCC or -0.5V to GND for period up to 20ns.

Figure 3. Maximum Negative Overshoot Waveform

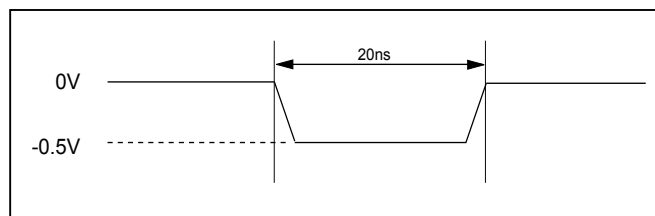
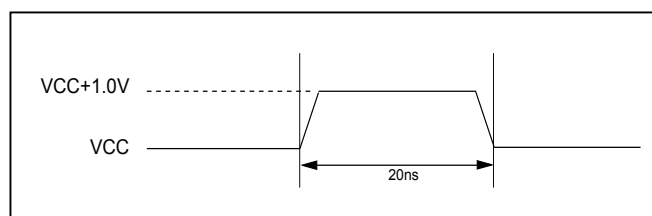


Figure 4. Maximum Positive Overshoot Waveform



CAPACITANCE TA = 25°C, f = 1.0 MHz

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance			6	pF	VIN = 0V
COUT	Output Capacitance			8	pF	VOUT = 0V

Figure 5. INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL

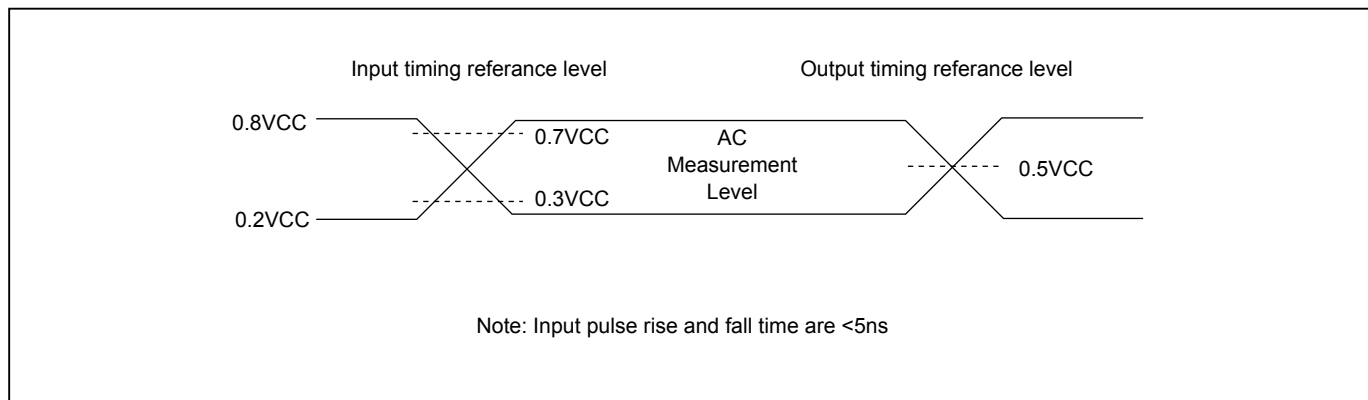


Figure 6. OUTPUT LOADING

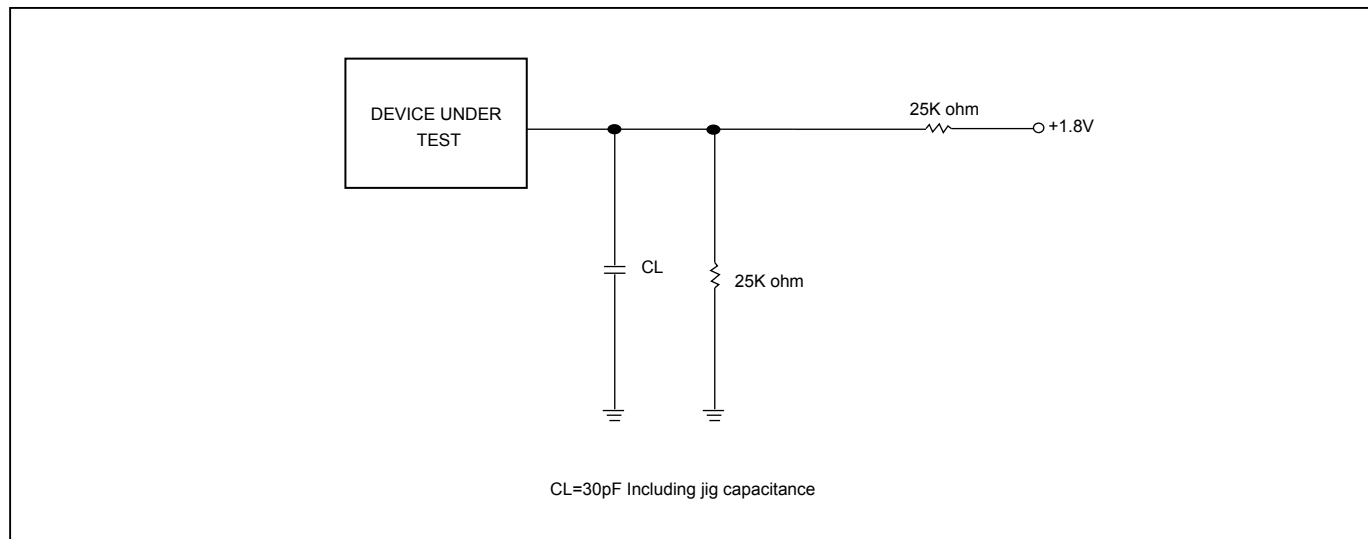


Table 9. DC CHARACTERISTICS (Temperature = -40°C to 85°C, VCC = 1.65V ~ 2.0V)

SYMBOL	PARAMETER	NOTES	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
ILI	Input Load Current	1			± 1	uA	VCC = VCC Max, VIN = VCC or GND
ILO	Output Leakage Current	1			± 1	uA	VCC = VCC Max, VIN = VCC or GND
ISB1	VCC Standby Current	1		1	5	uA	VIN = VCC or GND, CS# = VCC
ISB2	Deep Power-down Current			1	5	uA	VIN = VCC or GND, CS# = VCC
ICC1	VCC Read	1			12	mA	f=40MHz, fQ=33MHz (4 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
					6	mA	f=25MHz, SCLK=0.1VCC/0.9VCC, SO=Open
ICC2	VCC Program Current (PP)	1		15	22	mA	Program in Progress, CS# = VCC
ICC3	VCC Write Status Register (WRSR) Current			15	22	mA	Program status register in progress, CS#=VCC
ICC4	VCC Sector/Block (32K, 64K) Erase Current (SE/BE/BE32K)	1		15	22	mA	Erase in Progress, CS#=VCC
ICC5	VCC Chip Erase Current (CE)	1		15	22	mA	Erase in Progress, CS#=VCC
VIL	Input Low Voltage		-0.5		0.3VCC	V	
VIH	Input High Voltage		0.7VCC		VCC+0.4	V	
VOL	Output Low Voltage				0.2	V	IOL = 100uA
VOH	Output High Voltage		VCC-0.2			V	IOH = -100uA

Notes :

1. Typical values at VCC = 1.8V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.

Table 10. AC CHARACTERISTICS (Temperature = -40°C to 85°C, VCC = 1.65V ~ 2.0V)

Symbol	Alt.	Parameter		Min.	Typ.	Max.	Unit
fSCLK	fC	Clock Frequency for the following instructions: FAST_READ, PP, SE, BE, CE, DP, RES,RDP WREN, WRDI, RDID, RDSR, WRSR		1KHz		40	MHz
fRCLK	fR	Clock Frequency for READ instructions		1KHz		25	MHz
fTCLK	fT	Clock Frequency for 2READ instructions		1KHz		40	MHz
	fQ	Clock Frequency for 4READ instructions		1KHz		33	MHz
tCH(1)	tCLH	Clock High Time	fR	16			ns
			fT/fQ	12			ns
			fC	10			ns
tCL(1)	tCLL	Clock Low Time	fR	16			ns
			fT/fQ	12			ns
			fC	10			ns
tCLCH(2)		Clock Rise Time (3) (peak to peak)		0.1			V/ns
tCHCL(2)		Clock Fall Time (3) (peak to peak)		0.1			V/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)	fR	16			ns
			fT/fQ	12			ns
			fC	8			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)		10			ns
tDVCH	tDSU	Data In Setup Time	fR	5			ns
			fT/fQ	3			ns
			fC	2			ns
tCHDX	tDH	Data In Hold Time		5			ns
tCHSH		CS# Active Hold Time (relative to SCLK)	fR	16			ns
			fT/fQ	12			ns
			fC	8			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)		10			ns
tSHSL(3)	tCSH	CS# Deselect Time		30			ns
tSHQZ(2)	tDIS	Output Disable Time	fR			20	ns
			fT/fQ			19	ns
			fC			19	ns
tCLQV	tV	Clock Low to Output Valid	Single I/O	Loading: 30pF		10	ns
				Loading: 15pF		9	ns
			Multi-I/O	Loading: 30pF		12	ns
				Loading: 15pF		10	ns
tCLQX	tHO	Output Hold Time		0			ns
tHLCH		HOLD# setup time (relative to SCLK)		5			ns
tCHHH		HOLD# hold time (relative to SCLK)		5			ns
tHHCH		HOLD setup time (relative to SCLK)		5			ns
tCHHL		HOLD hold time (relative to SCLK)		5			ns
tHHQZ	tLZ	HOLD to output Low-Z				20	ns
tHLQZ	tHZ	HOLD to output High-Z				20	ns
tWHSL		Write Protect Setup Time		20			ns
tSHWL		Write Protect Hold Time		100			ns
tDP(2)		CS# High to Deep Power-down Mode				10	us
tRES1(2)		CS# High to Standby Mode without Electronic Signature Read				8.8	us
tRES2(2)		CS# High to Standby Mode with Electronic Signature Read				8.8	us

Symbol	Alt.	Parameter	Min.	Typ.	Max.	Unit
tRESET		Pulse width of RESET	100			ns
tRCR		Recovery Time to Read			100	ns
tRCP		Recovery Time to Program			10	us
tRCE		Recovery Time to Erase			1	ms
tREHZ		Time from RESET to High-Z output			100	ns
tW		Write Status Register Cycle Time			200	ns
tBP		Byte-Program		30	300	us
tPP		Page Program Cycle Time		2	7	ms
tSE		Sector Erase Cycle Time		0.09	2	s
tBE32		Block Erase (32KB) Cycle Time		0.8	1.6	s
tBE		Block Erase (64KB) Cycle Time		1.5	3	s
tCE		Chip Erase Cycle Time	4Mb	7.5	13	s
			8Mb	15	25	s

Notes:

1. tCH + tCL must be greater than or equal to 1/ Frequency.
2. Value guaranteed by characterization, not 100% tested in production.
3. tSHSL=30ns for read instruction, tSHSL=50ns for Write/Erase/Program instruction.
4. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.

Timing Analysis

Figure 7. Serial Input Timing

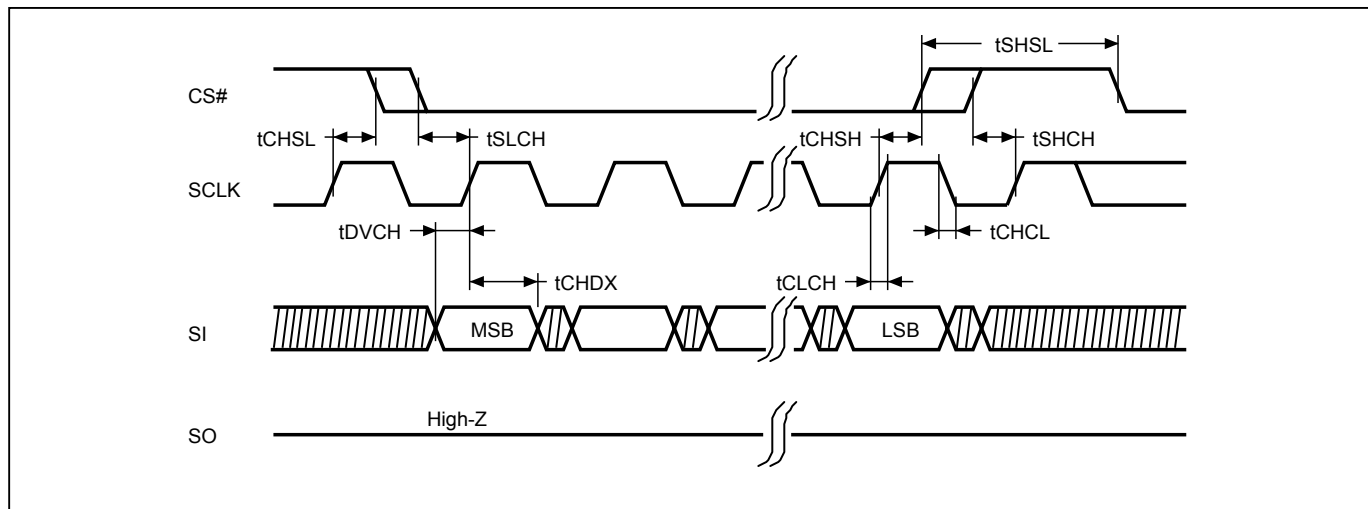


Figure 8. Output Timing

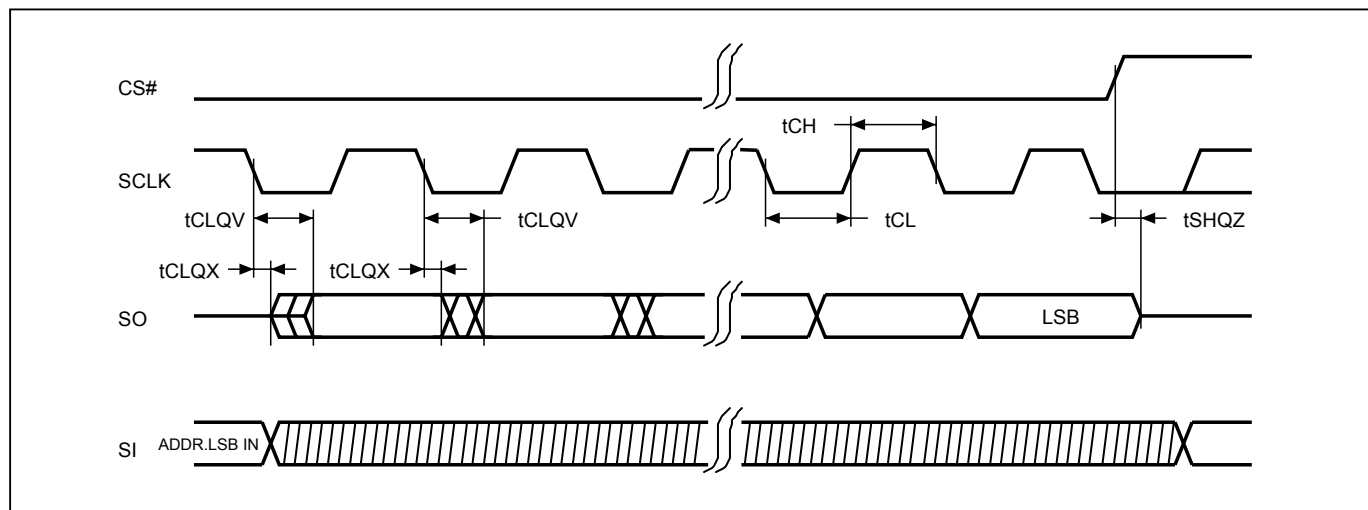
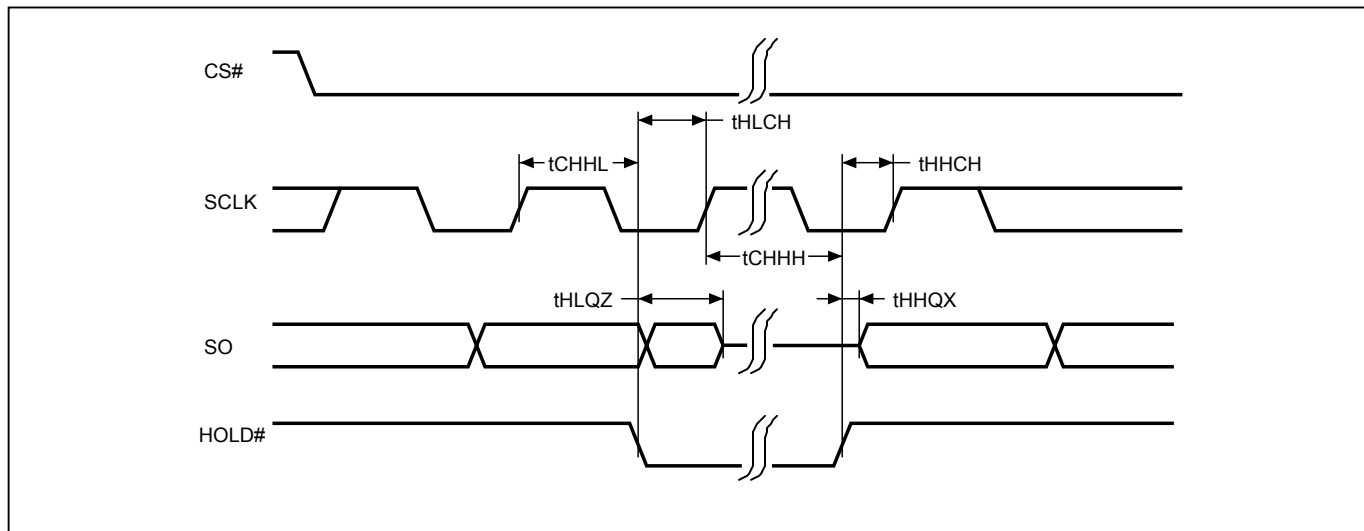


Figure 9. Hold Timing



* SI is "don't care" during HOLD operation.

Figure 10. WP# Setup Timing and Hold Timing during WRSR when SRWD=1

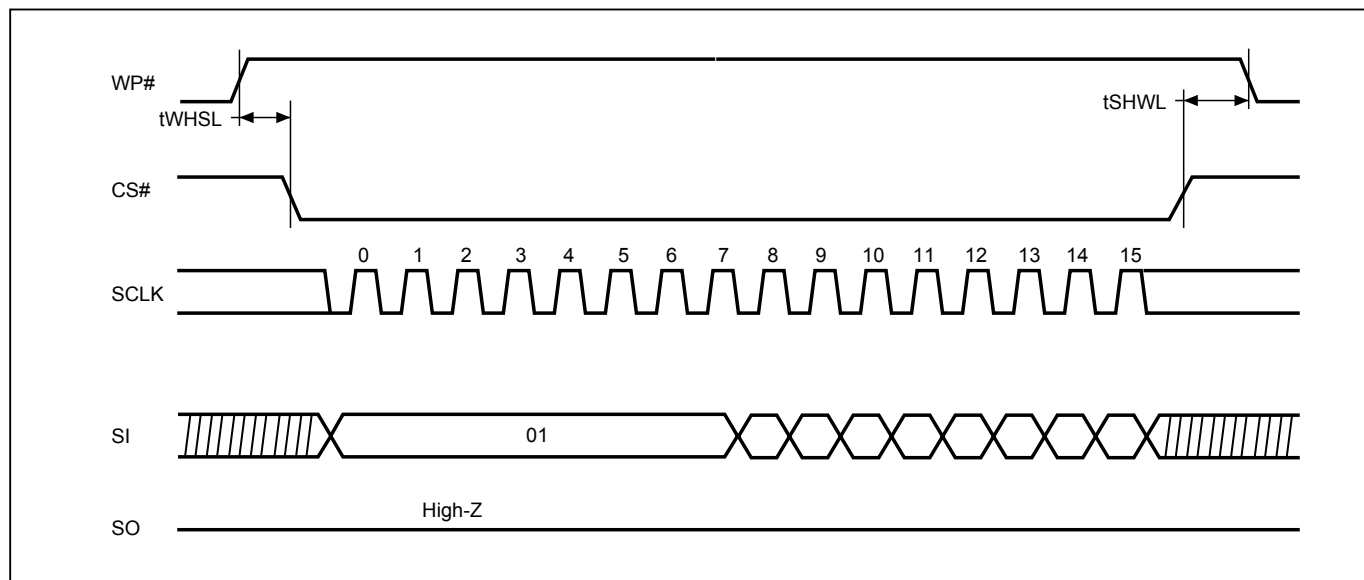


Figure 11. Hardware Reset Timing

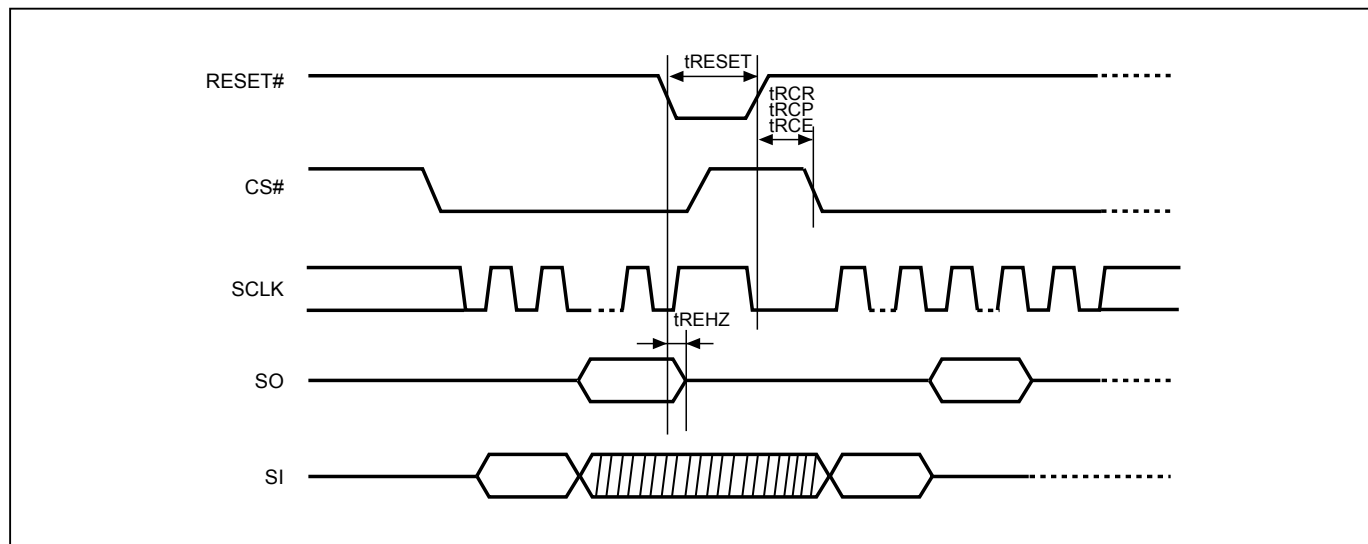


Figure 12. Write Enable (WREN) Sequence (Command 06)

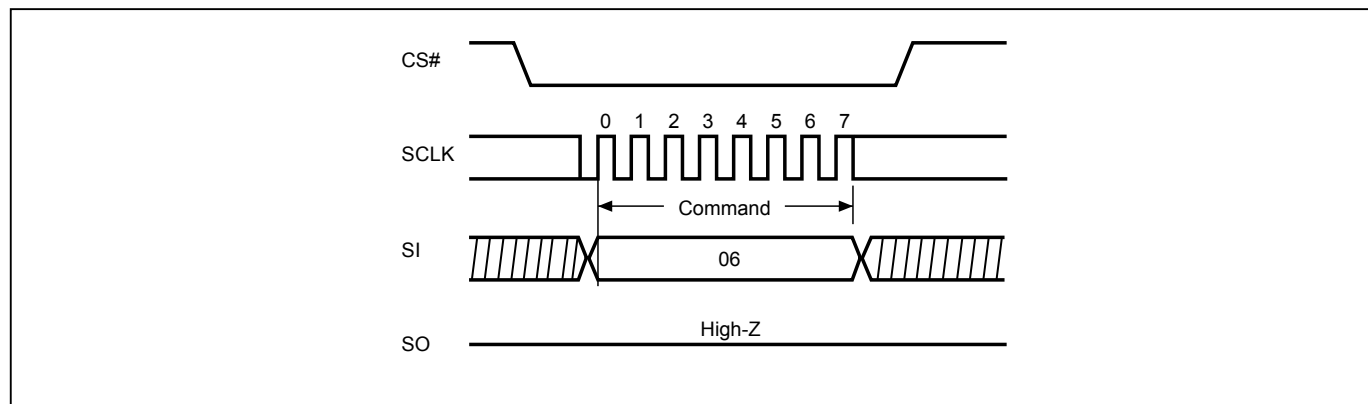


Figure 13. Write Disable (WRDI) Sequence (Command 04)

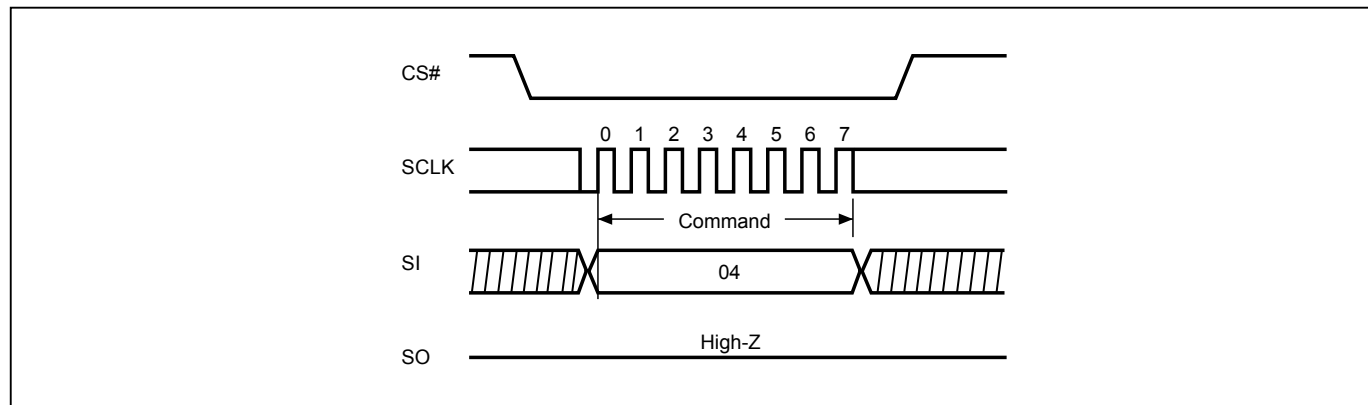


Figure 14. Read Identification (RDID) Sequence (Command 9F)

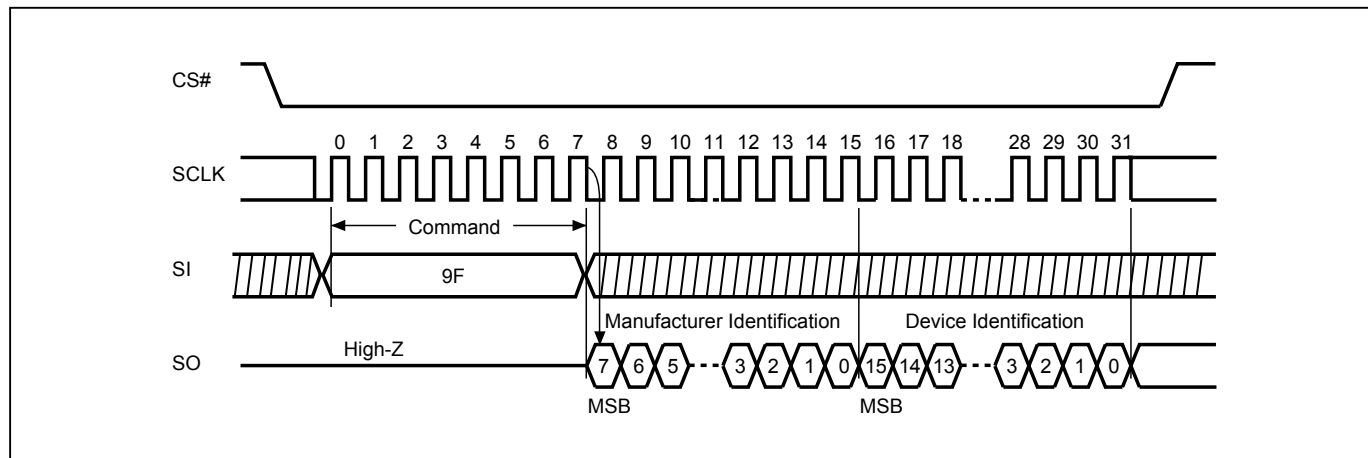


Figure 15. Read Status Register (RDSR) Sequence (Command 05)

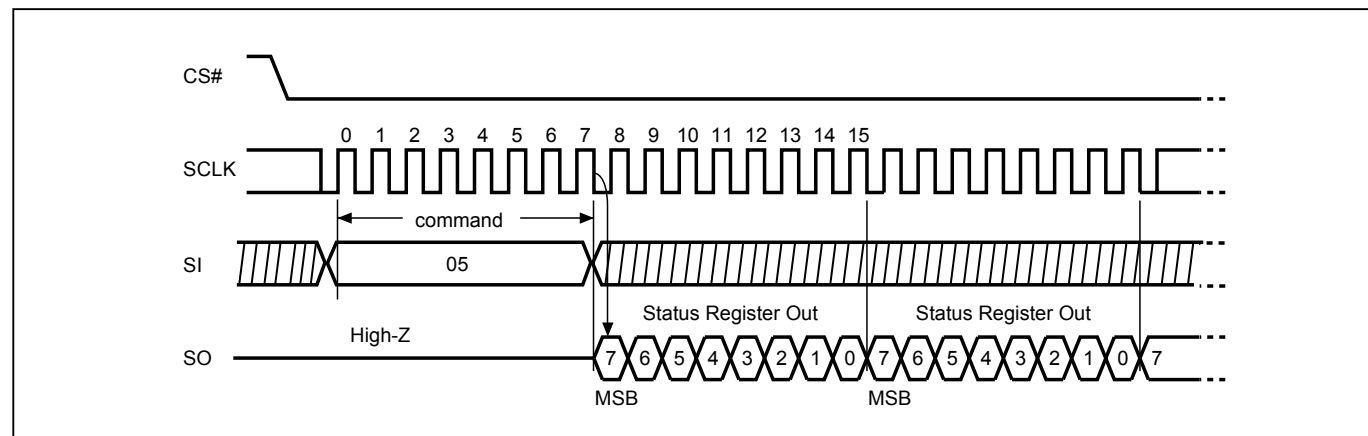


Figure 16. Write Status Register (WRSR) Sequence (Command 01)

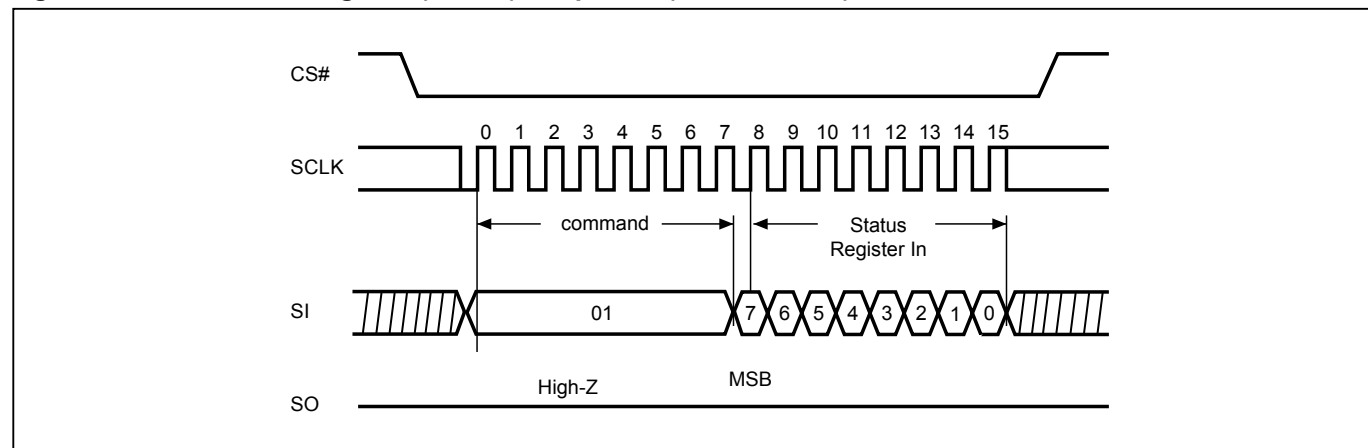


Figure 17. Read Data Bytes (READ) Sequence (Command 03)

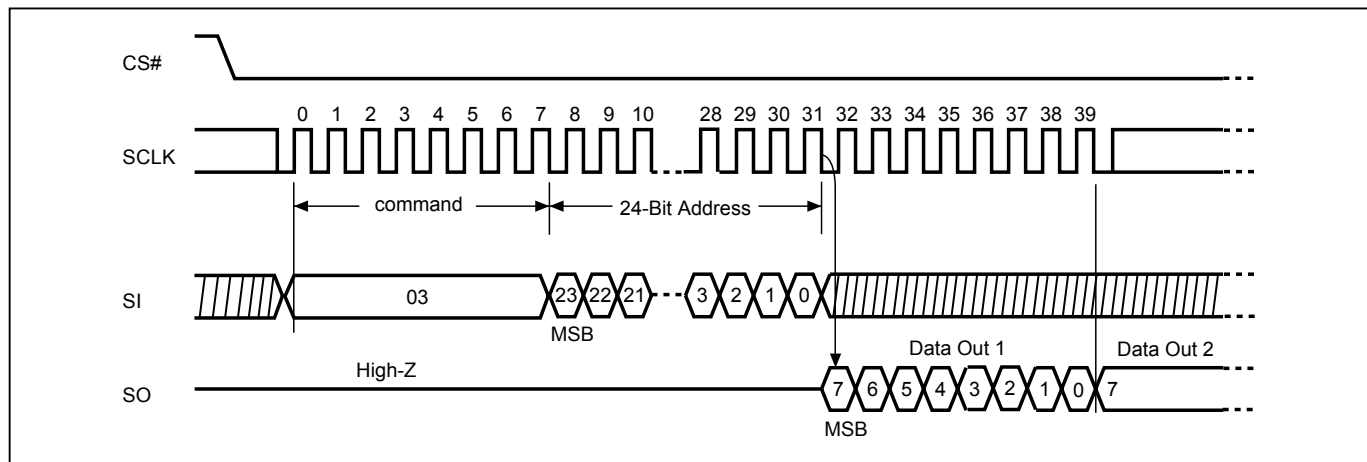


Figure 18. Read at Higher Speed (FAST_READ) Sequence (Command 0B)

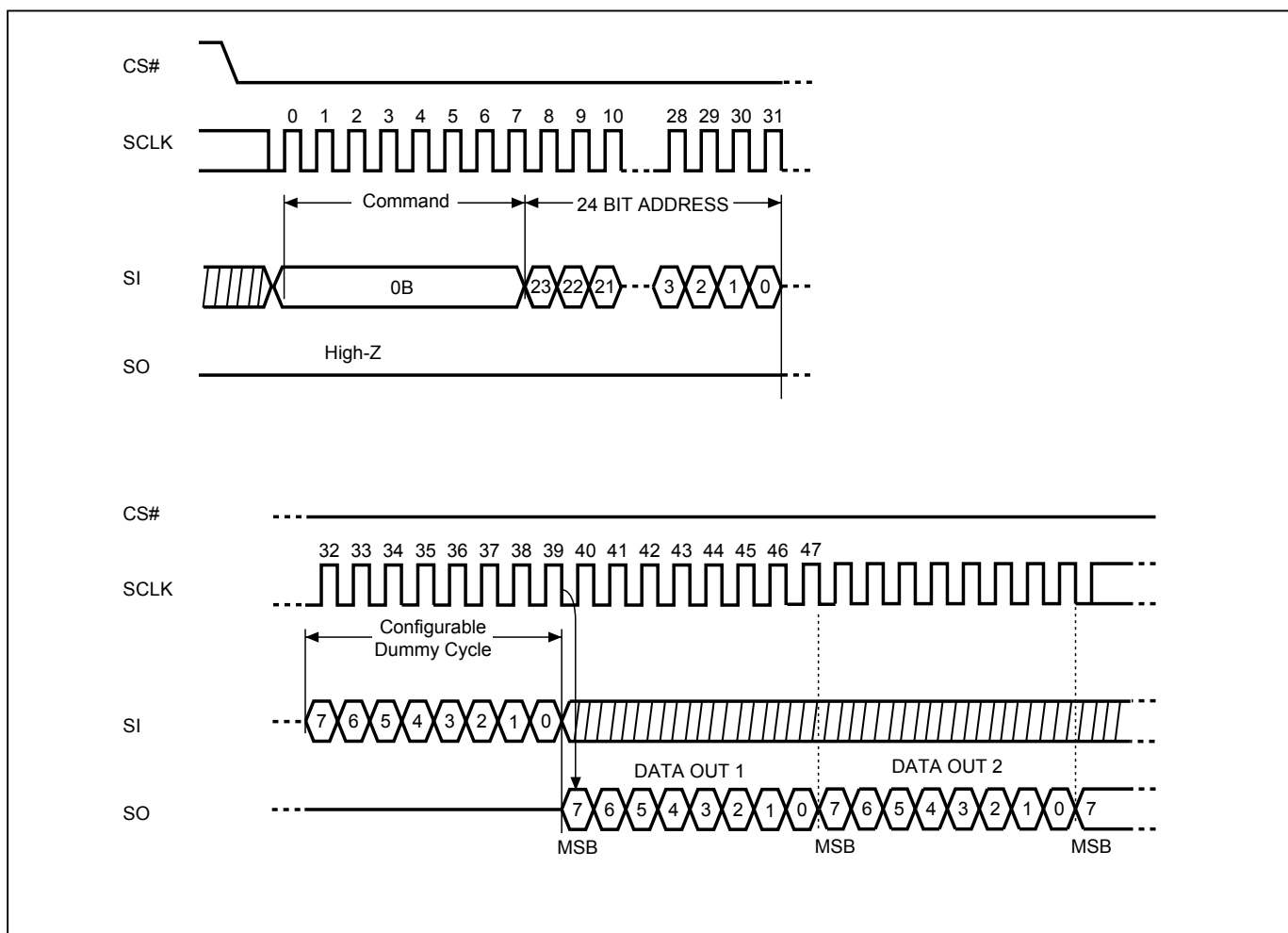
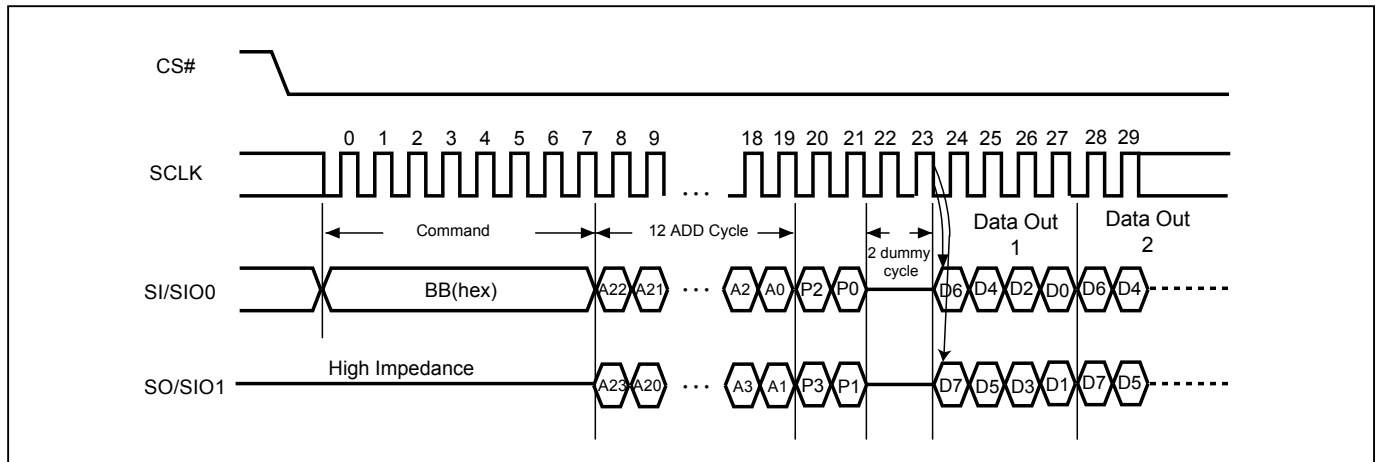
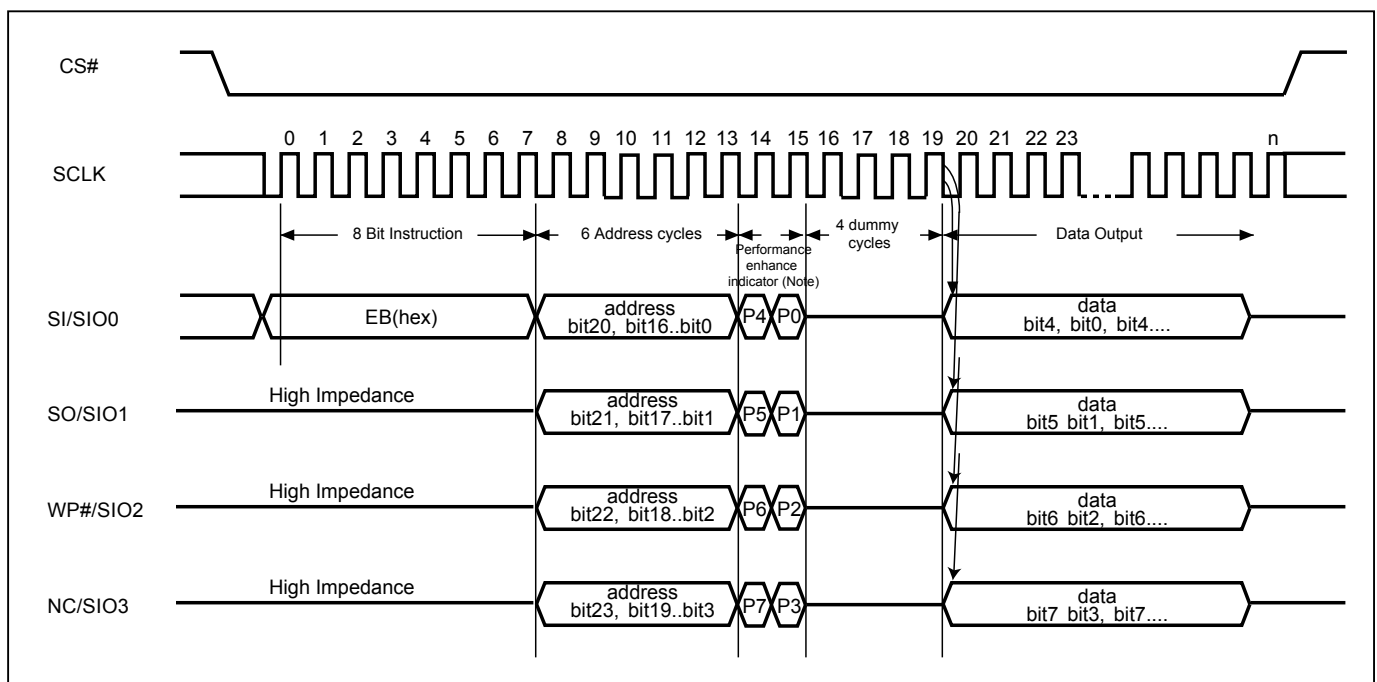


Figure 19. 2 x I/O Read Mode Sequence (Command BB)



Note: SI/SIO0 or SO/SIO1 should be kept "0h" or "Fh" in the first two dummy cycles. In other words, P2=P0 or P3=P1 is necessary.

Figure 20. 4 x I/O Read Mode Sequence (Command EB)



Notes:

1. Hi-impedance is inhibited for the two clock cycles.
2. P7≠P3, P6≠P2, P5≠P1 & P4≠P0 (Toggling) is inhibited.

Figure 21. 4 x I/O Read enhance performance Mode Sequence (Command EB)

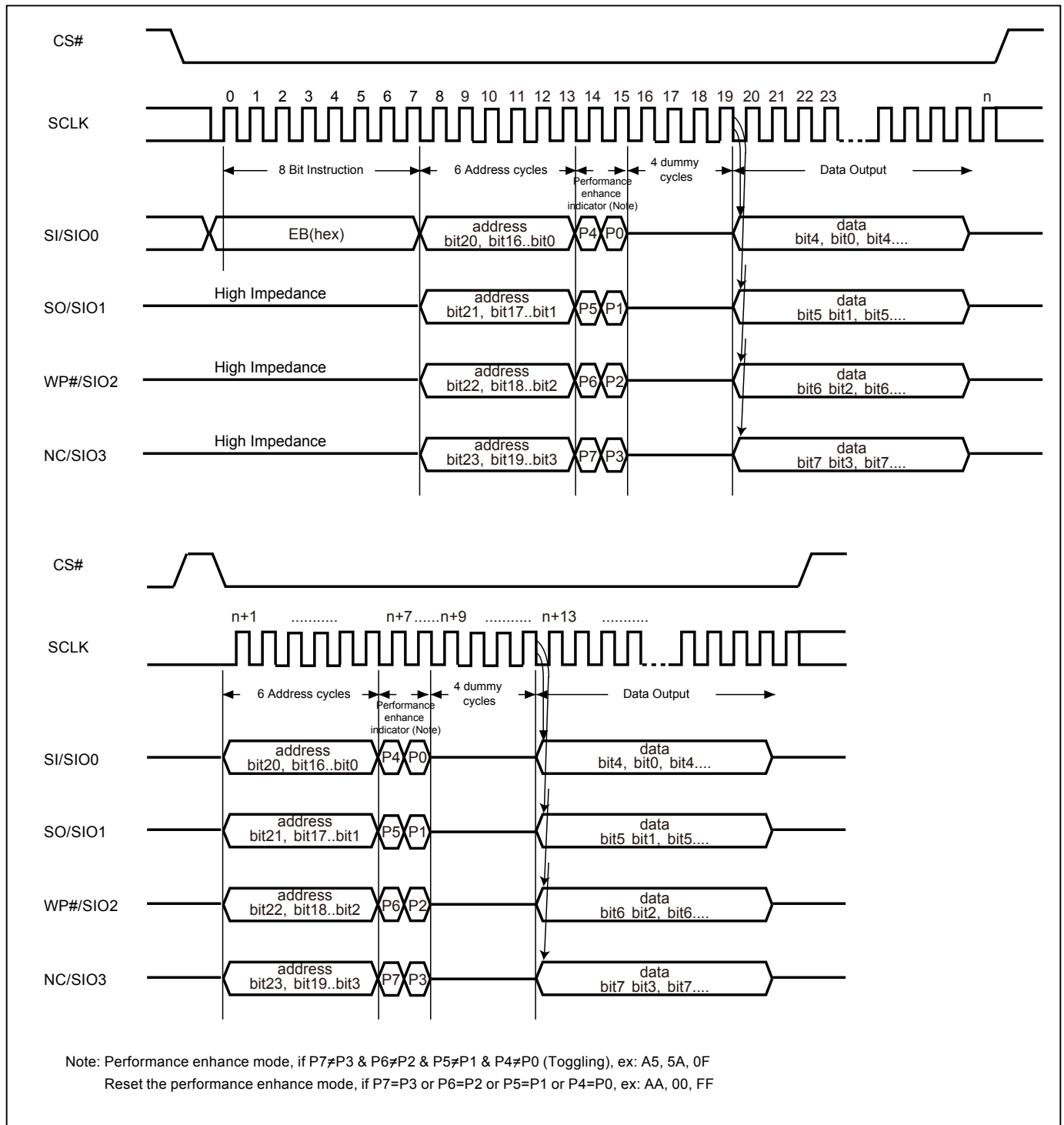


Figure 22. Page Program (PP) Sequence (Command 02)

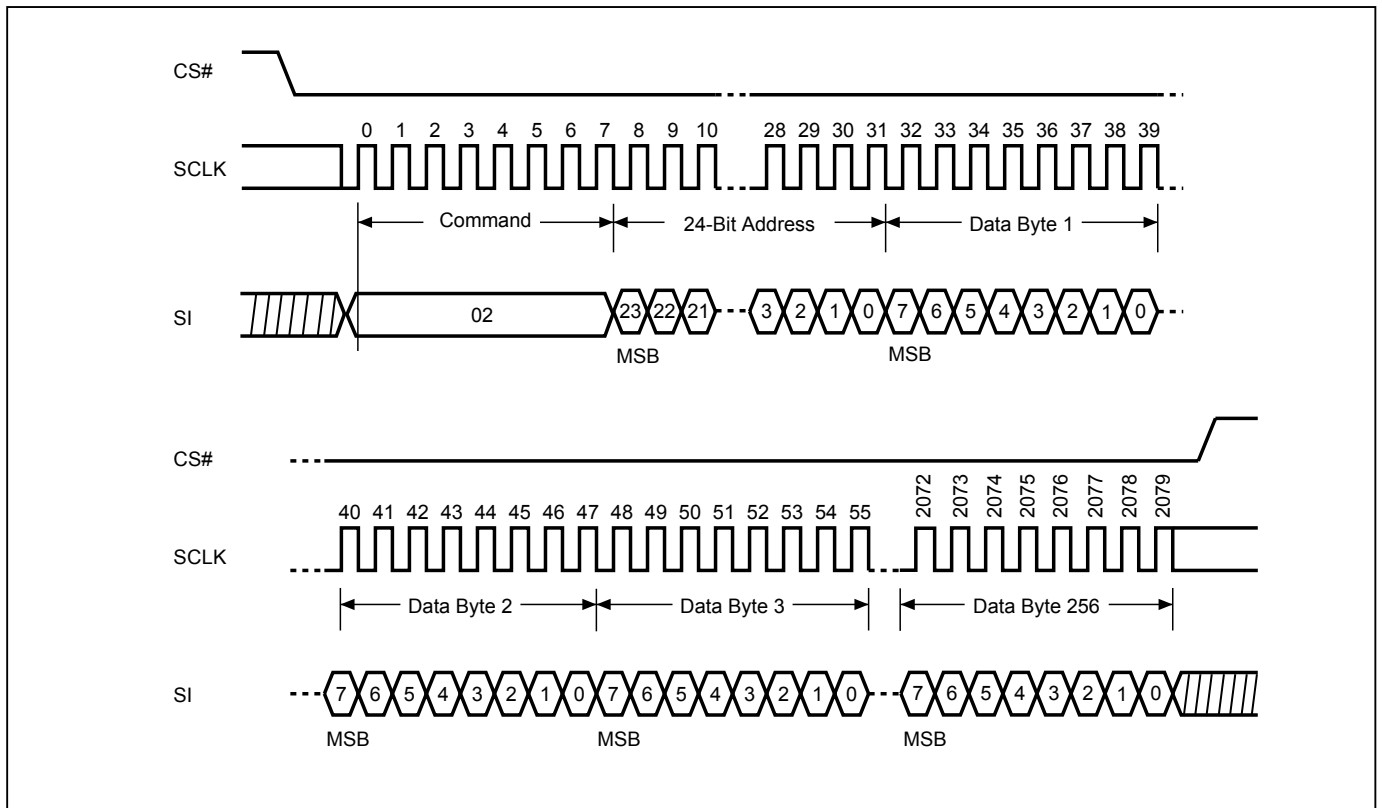


Figure 23. 4 x I/O Page Program (4PP) Sequence (Command 38)

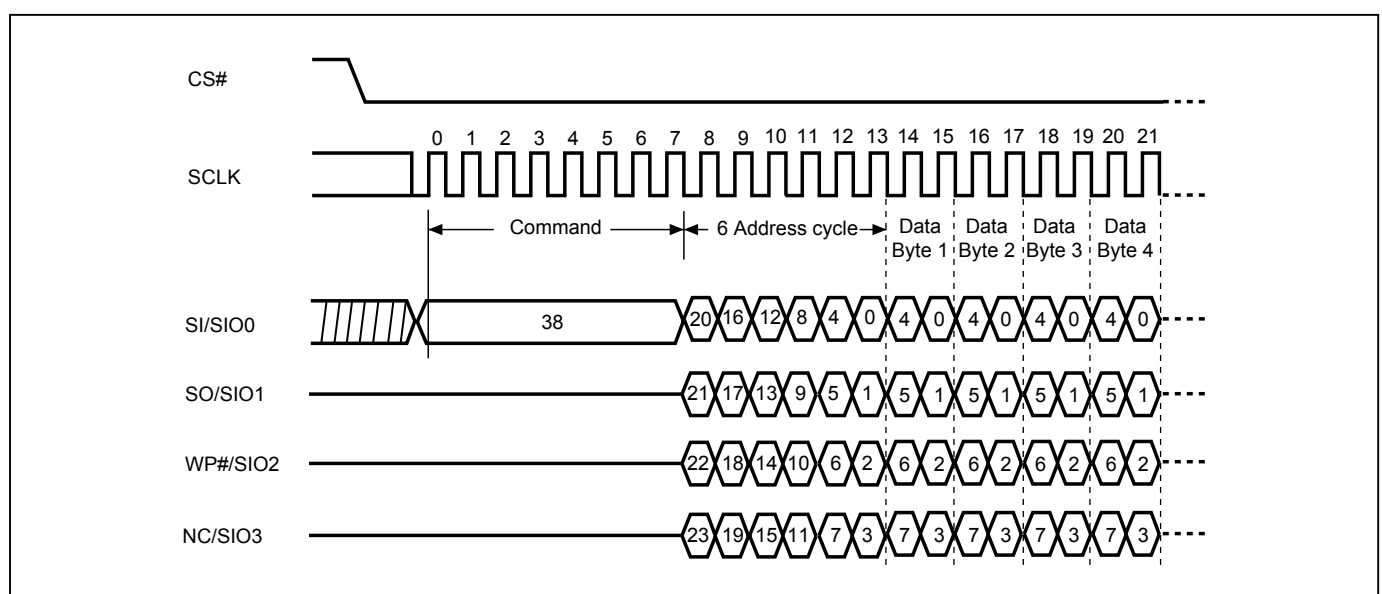
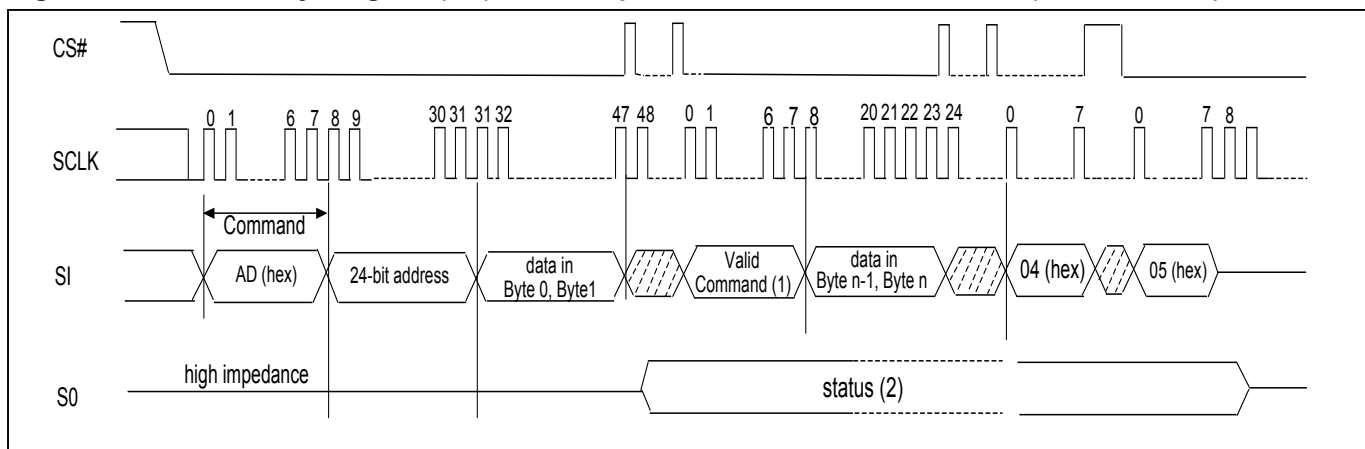
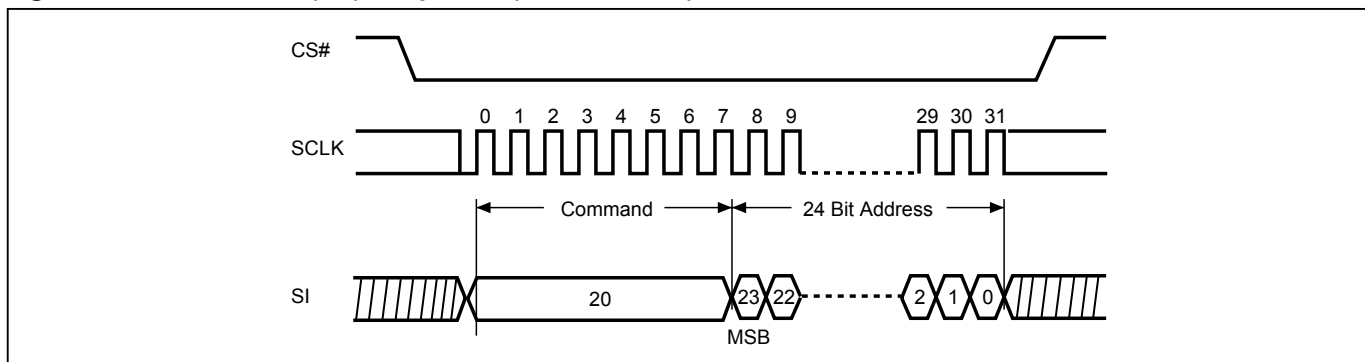


Figure 24. Continuously Program (CP) Mode Sequence with Hardware Detection (Command AD)



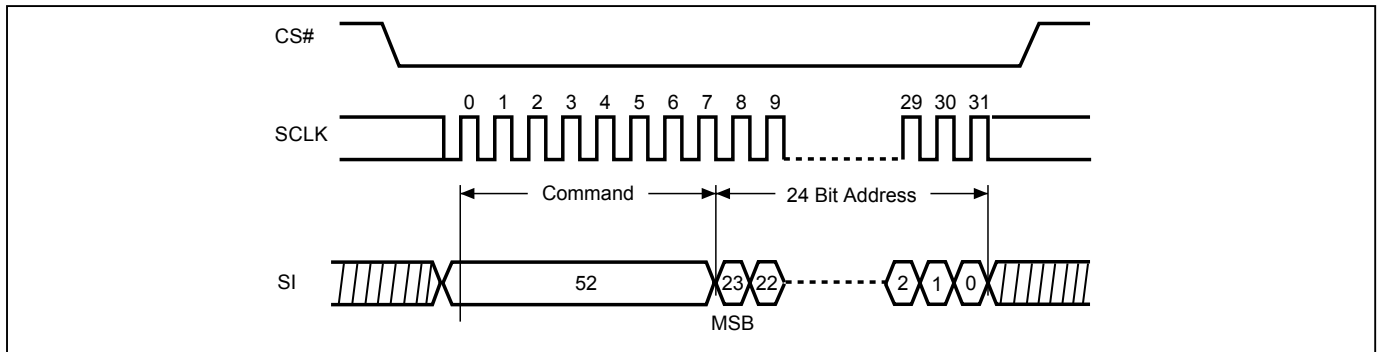
- Notes:** (1) During CP mode, the valid commands are CP command (AD hex), WRDI command (04 hex), RDSR command (05 hex), and RDSCUR command (2B hex).
 (2) Once an internal programming operation begins, CS# goes low will drive the status on the SO pin and CS# goes high will return the SO pin to tri-state.
 (3) To end the CP mode, either reaching the highest unprotected address or sending Write Disable (WRDI) command (04 hex) may achieve it and then it is recommended to send RDSCUR command (2B hex) to verify if CP mode is ended

Figure 25. Sector Erase (SE) Sequence (Command 20)



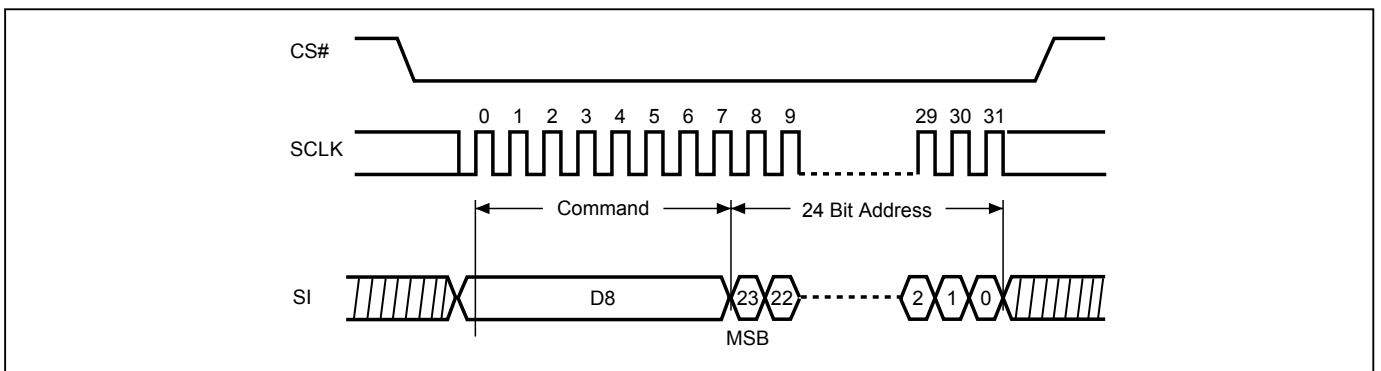
Note: SE command is 20(hex).

Figure 26. Block Erase 32KB (BE32K) Sequence (Command 52)



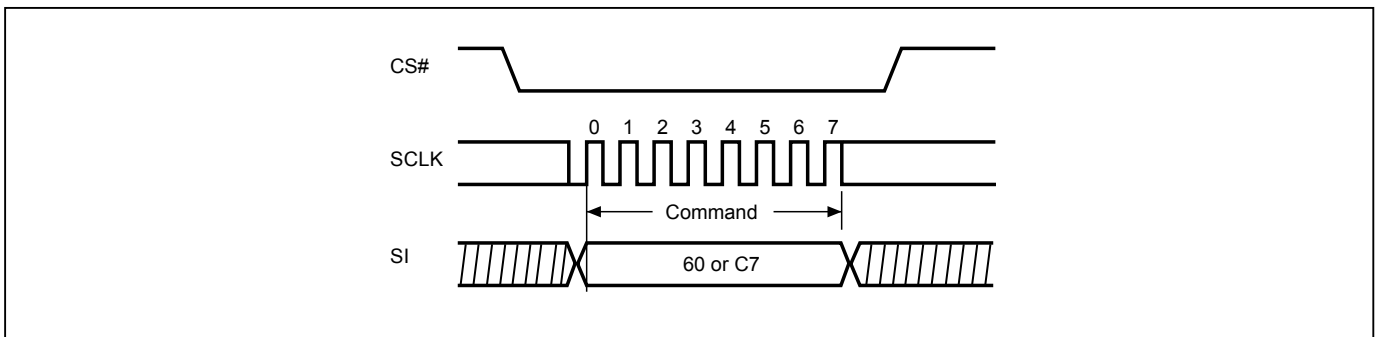
Note: BE32K command is 52(hex).

Figure 27. Block Erase (BE) Sequence (Command D8)



Note: BE command is D8(hex).

Figure 28. Chip Erase (CE) Sequence (Command 60 or C7)



Note: CE command is 60(hex) or C7(hex).

Figure 29. Deep Power-down (DP) Sequence (Command B9)

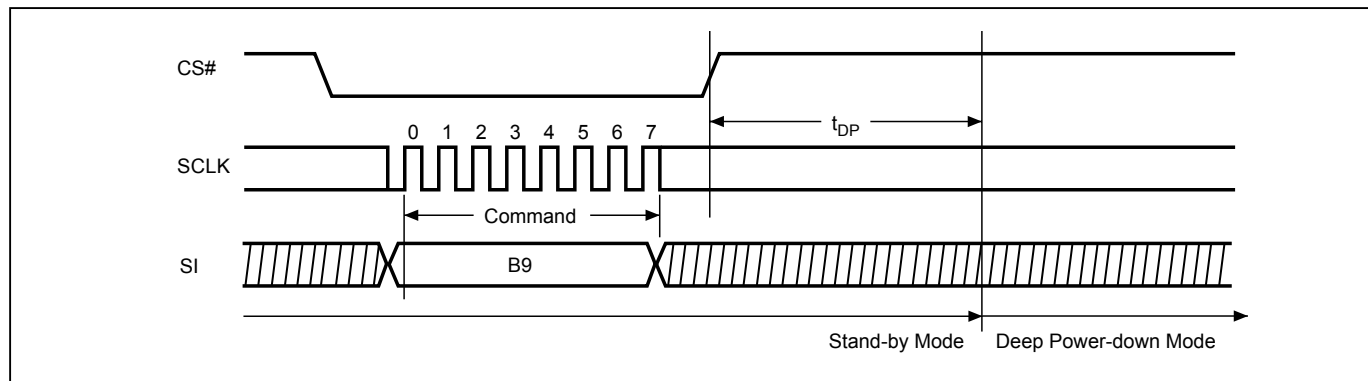


Figure 30. Release from Deep Power-down and Read Electronic Signature (RES) Sequence (Command AB)

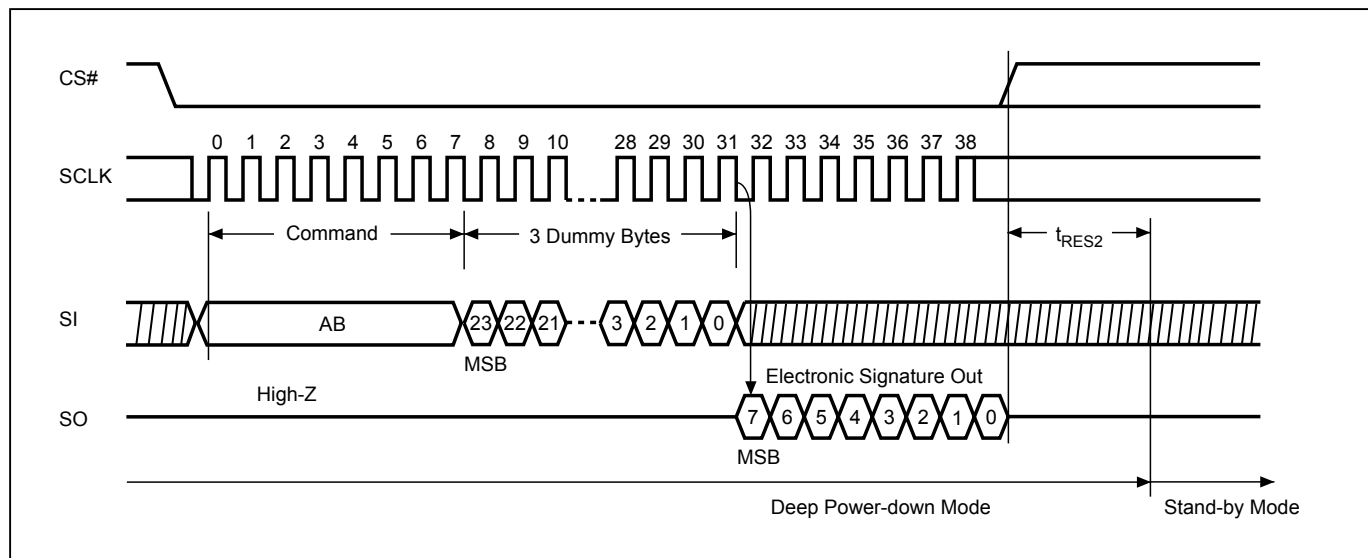


Figure 31. Release from Deep Power-down (RDP) Sequence (Command AB)

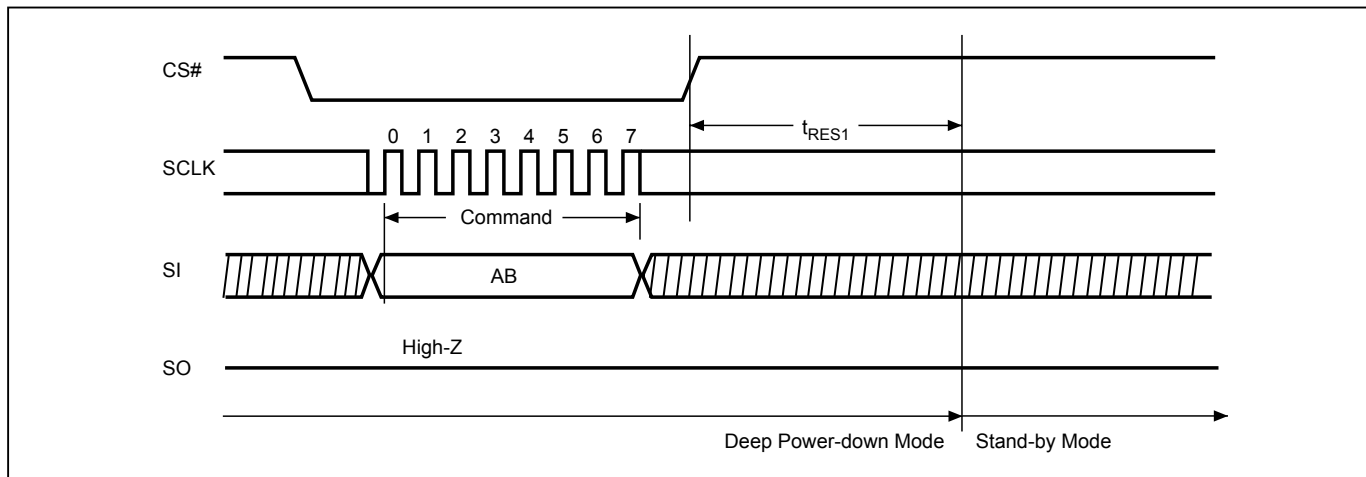
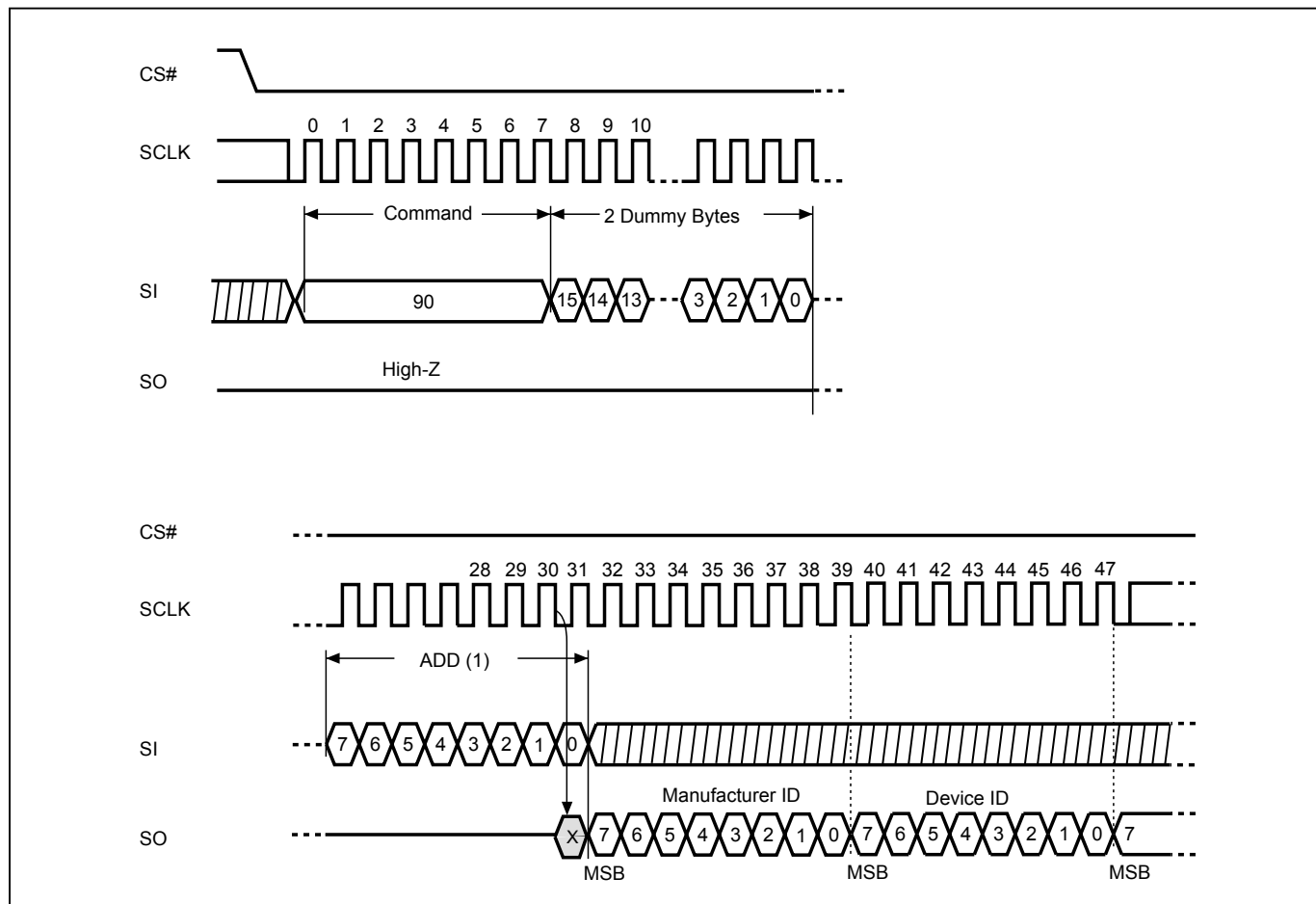


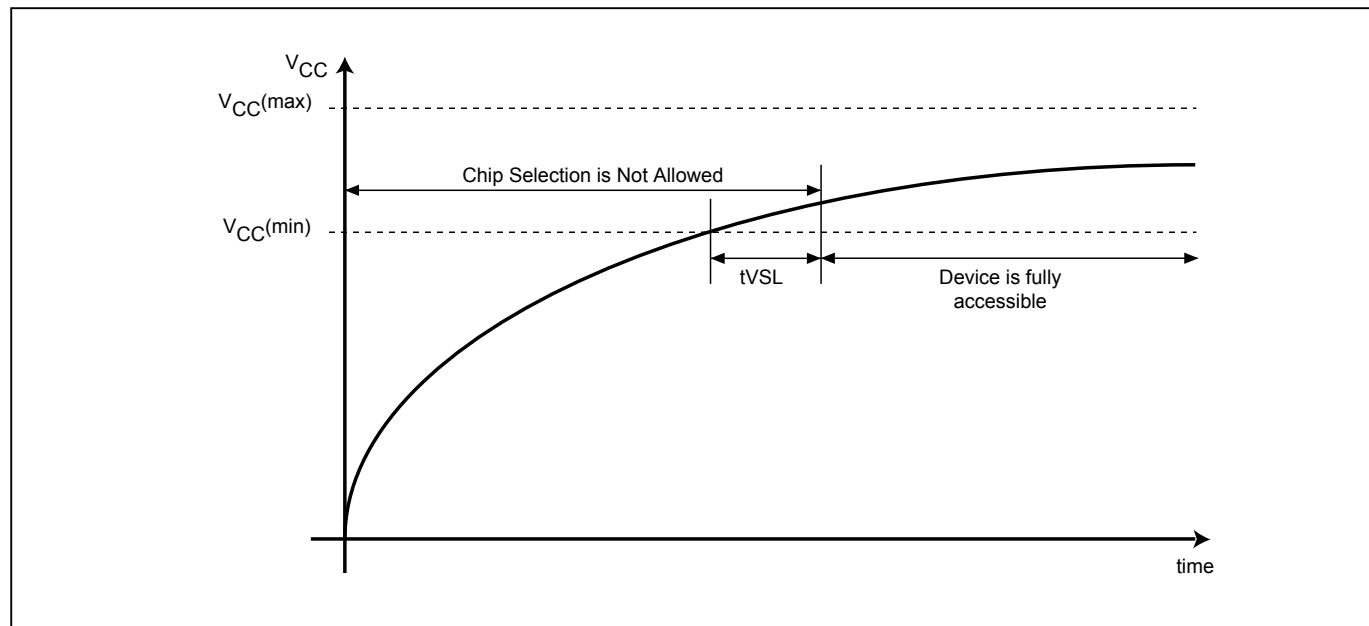
Figure 32. Read Electronic Manufacturer & Device ID (REMS) Sequence (Command 90 or EF or DF)



Notes:

- (1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first
- (2) Instruction is either 90(hex) or EF(hex) or DF(hex).

Figure 33. Power-up Timing



Note: VCC (max.) is 2.0V and VCC (min.) is 1.65V.

Table 11. Power-Up Timing

Symbol	Parameter	Min.	Max.	Unit
tVSL(1)	VCC(min) to CS# low	50		us

Note: These parameters are characterized only.

INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

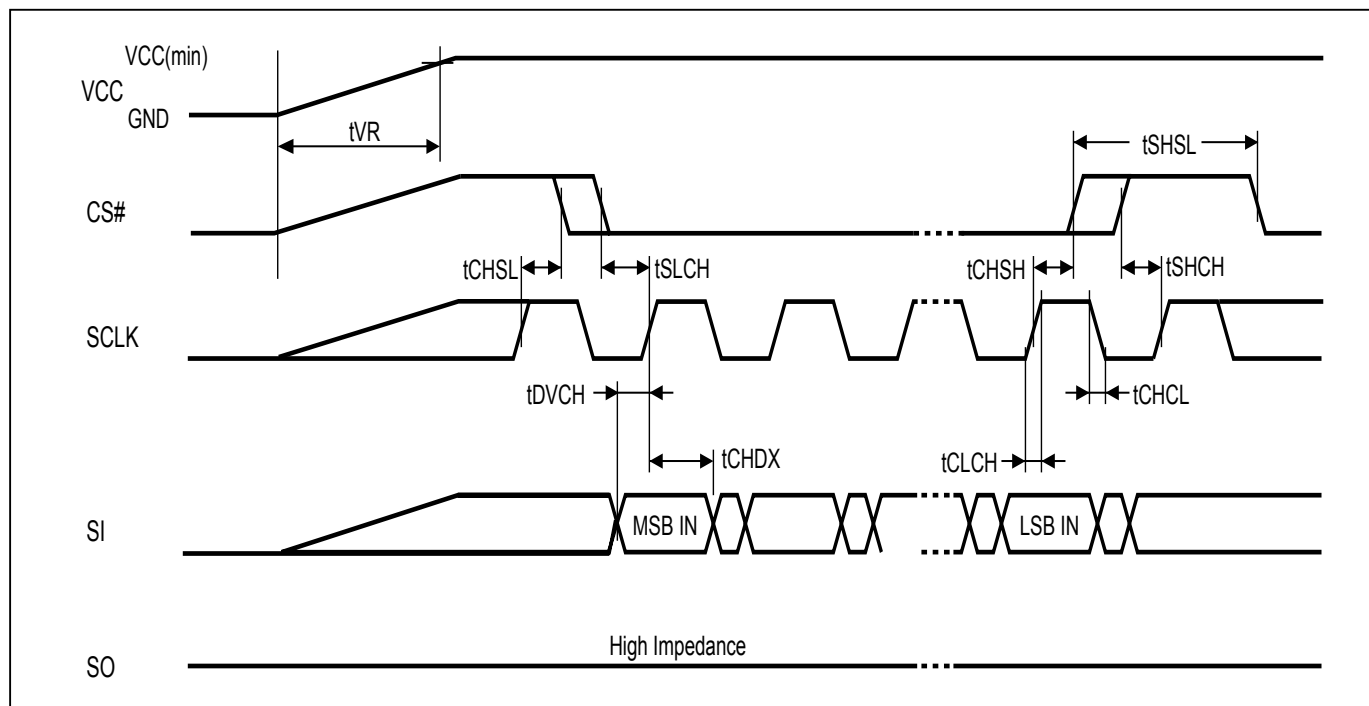
OPERATING CONDITIONS

At Device Power-Up and Power-Down

AC timing illustrated in [Figure 34](#) and [Figure 35](#) are for the supply voltages and the control signals at device power-up and power-down. If the timing in the figures is ignored, the device will not operate correctly.

During power-up and power-down, CS# needs to follow the voltage applied on VCC to keep the device not to be selected. The CS# can be driven low when VCC reach Vcc(min.) and wait a period of tVSL.

Figure 34. AC Timing at Device Power-Up



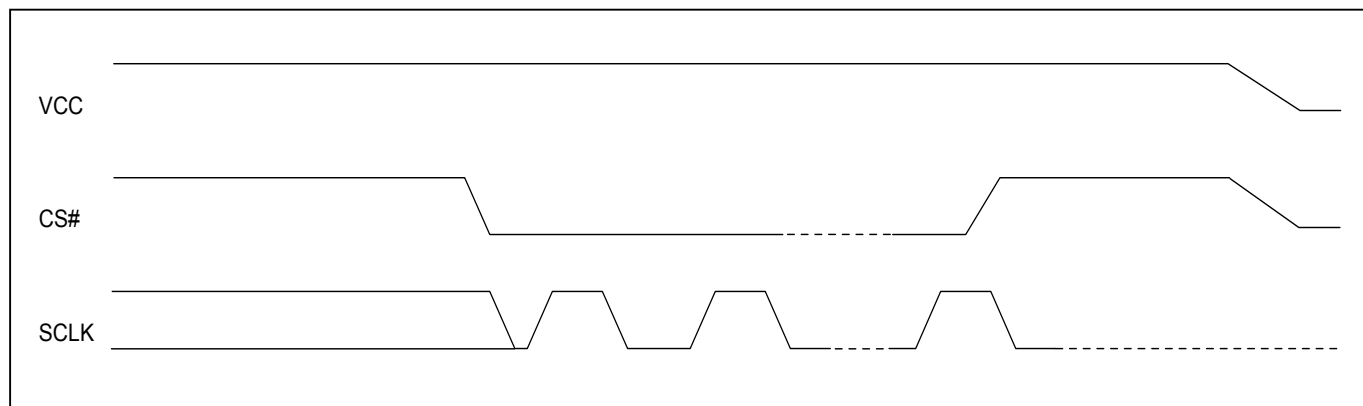
Symbol	Parameter	Notes	Min.	Max.	Unit
tVR	VCC Set Up Time	1	20	500000	us/V
tVSL	VCC (min) to CS# low		50		us

Notes:

1. Sampled, not 100% tested.
2. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to "[AC CHARACTERISTICS](#)" table.

Figure 35. Power-Down Sequence

During power-down, CS# needs to follow the voltage drop on VCC to avoid mis-operation.



ERASE AND PROGRAMMING PERFORMANCE

PARAMETER		Min.	TYP. (1)	Max. (2)	UNIT
Write Status Register Cycle Time				200	ns
Sector Erase Cycle Time (4KB)			0.09	2	s
Block Erase Cycle Time (32KB)			0.8	1.6	s
Block Erase Cycle Time (64KB)			1.5	3	s
Chip Erase Cycle Time	4M		7.5	13	s
	8M		15	25	s
Byte Program Time (via page program command)			30	300	us
Page Program Cycle Time			2	7	ms
Erase/Program Cycle			100,000		cycles

Note:

1. Typical program and erase time assumes the following conditions: 25°C, 1.8V, and checker board pattern.
2. Under worst conditions of 85°C and 1.65V.
3. System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.

DATA RETENTION

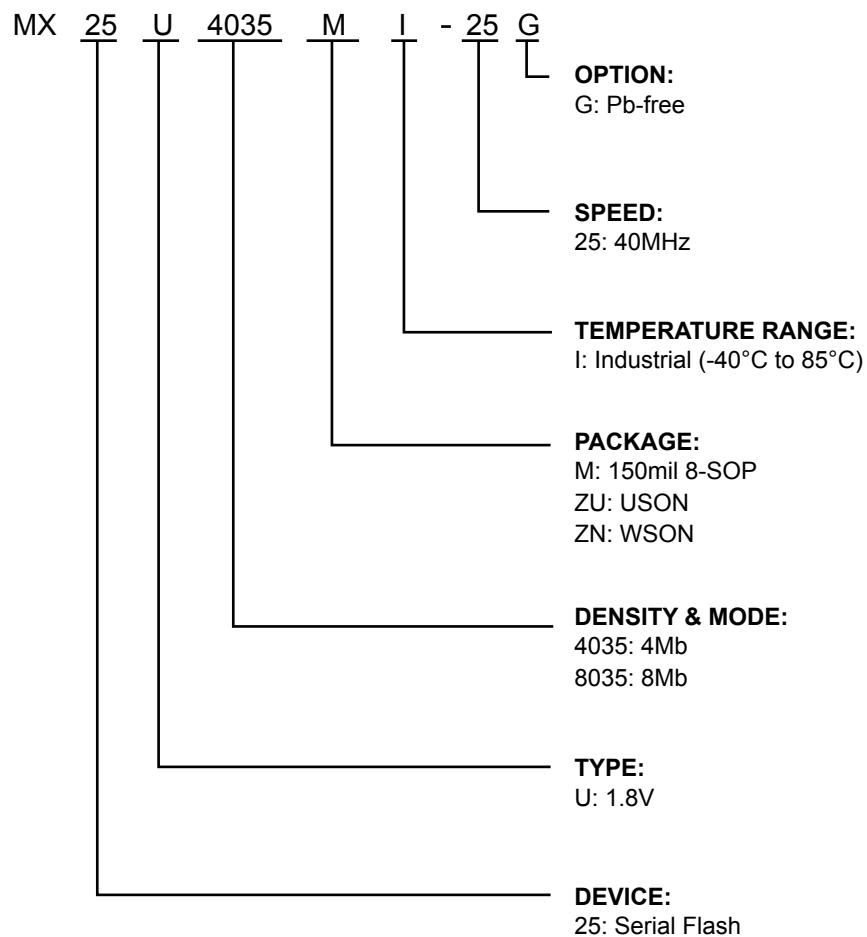
PARAMETER	Condition	Min.	Max.	UNIT
Data retention	55°C	20		years

LATCH-UP CHARACTERISTICS

	MIN.	MAX.
Input Voltage with respect to GND on all power pins, SI, CS#	-1.0V	2 VCCmax
Input Voltage with respect to GND on SO	-1.0V	VCC + 1.0V
Current	-100mA	+100mA
Includes all pins except VCC. Test conditions: VCC = 1.8V, one pin at a time.		

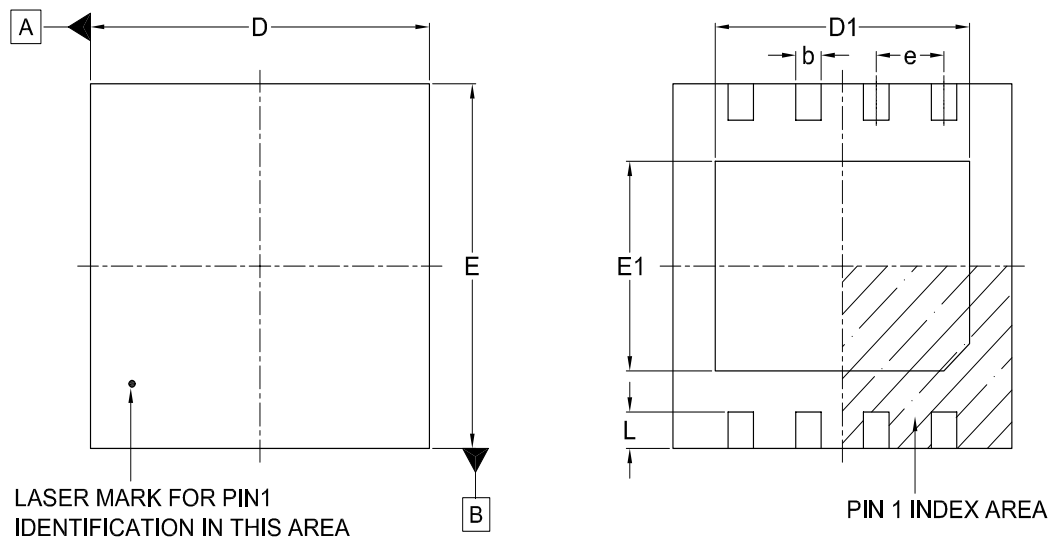
ORDERING INFORMATION

PART NO.	CLOCK (MHz)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (uA)	TEMPERATURE	PACKAGE	Remark
MX25U4035MI-25G	40	12	5	-40°C~85°C	8-SOP (150mil)	Pb-free
MX25U8035MI-25G	40	12	5	-40°C~85°C	8-SOP (150mil)	Pb-free
MX25U4035ZUI-25G	40	12	5	-40°C~85°C	8-USON (4x4mm)	Pb-free
MX25U8035ZUI-25G	40	12	5	-40°C~85°C	8-USON (4x4mm)	Pb-free
MX25U4035ZNI-25G	40	12	5	-40°C~85°C	8-WSON (6x5mm)	Pb-free
MX25U8035ZNI-25G	40	12	5	-40°C~85°C	8-WSON (6x5mm)	Pb-free

PART NAME DESCRIPTION

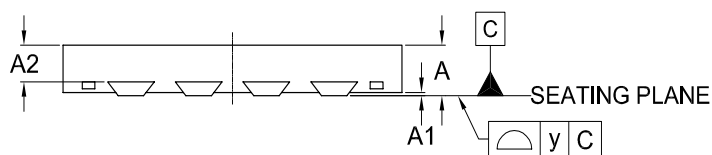
PACKAGE INFORMATION

Title: Package Outline for USON 8L (4x4x0.6MM, LEAD PITCH 0.8MM)



TOP VIEW

BOTTOM VIEW



SIDE VIEW

Dimensions (inch dimensions are derived from the original mm dimensions)

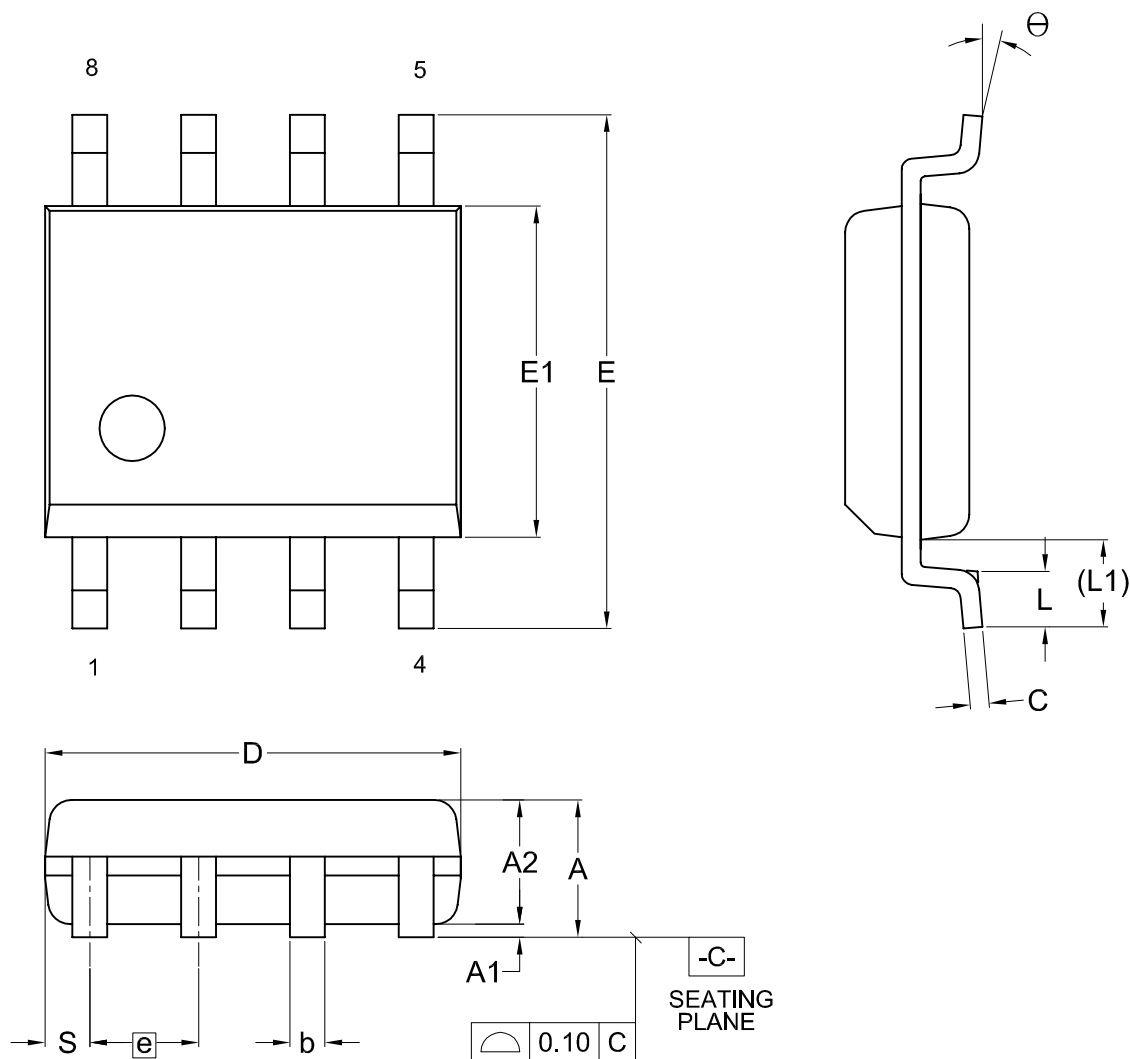
*1 : This package has exposed metal pad underneath the package , it can't contact to metal trace or pad on board.

*2 : The exposed pad size must not violate the min. metal separation requirement, 0.2mm with terminals.

SYMBOL		A	A1	A2	b	D	D1	E	E1	L	e	y
UNIT												
mm	Min.	0.50	---	---	0.25	3.90	2.90	3.90	2.20	0.35	---	0.00
	Nom.	0.55	0.04	0.40	0.30	4.00	3.00	4.00	2.30	0.40	0.80	---
	Max.	0.60	0.05	0.43	0.35	4.10	3.10	4.10	2.40	0.45	---	0.08
Inch	Min.	0.020	---	---	0.010	0.154	0.114	0.154	0.087	0.014	---	0.00
	Nom.	0.022	0.002	0.016	0.011	0.157	0.118	0.157	0.091	0.016	0.031	---
	Max.	0.024	0.002	0.017	0.014	0.161	0.122	0.161	0.094	0.018	---	0.003

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-3601	3	MO-252			2008/03/12

Title: Package Outline for SOP 8L (150MIL)

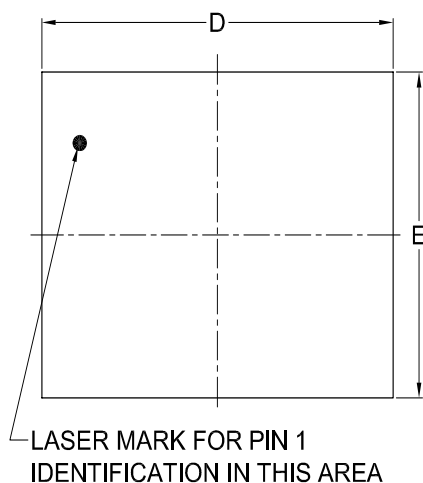


Dimensions (inch dimensions are derived from the original mm dimensions)

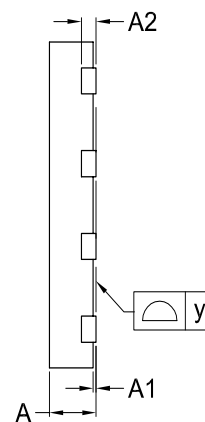
SYMBOL		A	A1	A2	b	C	D	E	E1	e	L	L1	S	Θ
UNIT														
mm	Min.	---	0.10	1.35	0.36	0.15	4.77	5.80	3.80		0.46	0.85	0.41	0
	Nom.	---	0.15	1.45	0.41	0.20	4.90	5.99	3.90	1.27	0.66	1.05	0.54	5
	Max.	1.75	0.20	1.55	0.51	0.25	5.03	6.20	4.00		0.86	1.25	0.67	8
Inch	Min.	---	0.004	0.053	0.014	0.006	0.188	0.228	0.150		0.018	0.033	0.016	0
	Nom.	---	0.006	0.057	0.016	0.008	0.193	0.236	0.154	0.050	0.026	0.041	0.021	5
	Max.	0.069	0.008	0.061	0.020	0.010	0.198	0.244	0.158		0.034	0.049	0.026	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1401	6	MS-012			11-26-'03

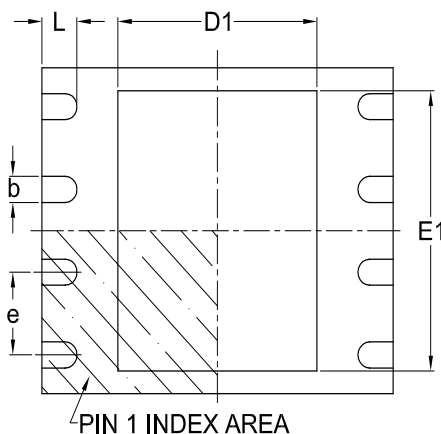
Title: Package Outline for WSON 8L (6x5x0.8MM, LEAD PITCH 1.27MM)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Dimensions (inch dimensions are derived from the original mm dimensions)

*1 : This package has exposed metal pad underneath the package , it can't contact to metal trace or pad on board.

*2 : The exposed pad size must not violate the min. metal separation requirement, 0.2mm with terminals.

SYMBOL		A	A1	A2	b	D	D1	E	E1	L	e	y
UNIT												
mm	Min.	0.70	---	---	0.35	5.90	3.30	4.90	3.90	0.50	---	0.00
	Nom.	---	---	0.20	0.40	6.00	3.40	5.00	4.00	0.60	1.27	---
	Max.	0.80	0.05	---	0.48	6.10	3.50	5.10	4.10	0.75	---	0.08
Inch	Min.	0.028	---	---	0.014	0.232	0.129	0.193	0.154	0.020	---	0.00
	Nom.	---	---	0.008	0.016	0.236	0.134	0.197	0.157	0.024	0.05	---
	Max.	0.032	0.002	---	0.019	0.240	0.138	0.201	0.161	0.030	---	0.003

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-3401	4	MO-220			2007/09/20

REVISION HISTORY

Revision No.	Description	Page	Date
1.0	1. Removed title of "Advanced Information"	P5	MAR/09/2009
	2. Revised 4KB erase time	P48	
	3. Modified erase/program cycle to be typical 100,000 times	P1,48	
	4. Revised QE bit attribute from non-volatile to volatile	P18	
1.1	1. Supplemented the HOLD# waveform and timing spec	P15,33,36	JUN/30/2009
	2. Added condition of data retention	P49	
	3. Supplemented on the dual I/O read mode sequence	P40	
	4. Rationalized the content	P5,7,16,17,19	
		P20,22~25	
	5. Added advanced information of WSON	P6,8,50,51,54	
1.2	1. Revised 3-wire bus as 4-wire bus	P7	DEC/18/2009
1.3	1. Modified data retention from 10 years to 20 years	P5,50	APR/22/2010
	2. 8-and WSON package released	P6,8,51,52	
	3. Modified Figure 34. AC Timing at Device Power-Up	P48	
	4. Added Figure 35. Power-Down Sequence	P49	
	5. Modified Figure 8 & Figure 25	P35,43	
	6. Removed note 4 from Erase and Programming Performance	P50	
1.4	1. Revised Table 5 . ENSO and EXSO action	P17	JUL/23/2010
	2. Revised Sector Erase Cycle Time in Table 10 and Erase and Programming Performance	P34, 50	



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