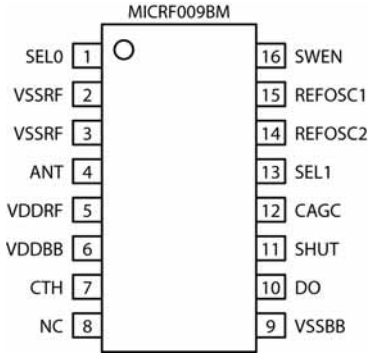
Pin Configuration



Standard 16-Pin SOIC (M)

SEL0	Demodulator Bandwidth	
	Sweep-Mode	Fixed-Mode
1	1250Hz	2500Hz
0	625Hz	1250Hz

Table 1. Nominal Demodulator Filter Bandwidth vs. SEL0, Operating Mode at 433.92 MHz

Note:
SEL0 must connect to VDD = 1 or VSS = 0. Do not float SEL0

Pin Description

Pin Number	Pin Name	Pin Function
1	SEL0	Bandwidth Selection Bit 0 (Input): Configure to set the desired demodulator filter bandwidth. See Table 1. 0 = VSS, 1 = VDD, don not float SEL0
2, 3	VSSRF	RF [Analog] Return (Input): Ground return to the RF section power supply. See “Applications Information” for bypass capacitor details.
4	ANT	Antenna (Input): See “Applications Information” for information on input impedance. For optimal performance the antenna impedance should be matched to the antenna pin impedance.
5	VDDRF	RF [Analog] Supply (Input): Positive supply input for the RF section of the IC. VDDBB and VDDRF should be connected together directly at the IC pins.
6	VDDBB	Baseband [Digital] Supply (Input): Positive supply input for the baseband section of the IC. VDDBB and VDDRF should be connected together at the IC pins.
7	CTH	[Data Slicing] Threshold Capacitor (External Component): Capacitor extracts the DC average value from the demodulated waveform, which becomes the reference for the internal data slicing comparator. See “Applications Information” for selection.
8	NC	No connect.
9	VSSBB	Baseband [Digital] Return (Input): Ground return to the baseband section power supply. See “Applications Information” for bypass capacitor and layout details.
10	DO	Digital Output (Output): CMOS level compatible data output signal.
11	SHUT	Shutdown (Input): Shutdown-mode logic-level control input. Pull low to enable the receiver. This input has an internal pulled-up to VDDRF.
12	CAGC	AGC Capacitor (External Component): Integrating capacitor for on-chip AGC (automatic gain control). See “Applications Information” for capacitor selection.
13	SEL1	Bandwidth Selection Bit 1 (Input): Must tie to ground. Reserved for future use.
14	REFOSC2	Reference Oscillator (External Component or Input): Timing reference for on-chip tuning and alignment.
15	REFOSC1	Reference Oscillator (External Component or Input): Timing reference for on-chip tuning and alignment.
16	SWEN	Sweep-Mode Enable (Input): Sweep- or fixed-mode operation control input. When SWEN is high, the MICRF009 is in sweep mode; when SWEN is low, the receiver operates as a conventional single-conversion superheterodyne receiver. This pin is internally pulled-up to VDDRF.

Absolute Maximum Ratings[1]

Supply Voltage (V_{DDRF}, V_{DDBB}) ..... +7V
Input/Output Voltage ($V_{I/O}$) ..... V_{SS}–0.3 to V_{DD}+0.3
Max. Input Power ..... +20dBm
Junction Temperature (T_J) ..... +150°C
Storage Temperature Range (T_S) ..... –65°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +260°C
ESD Rating ..... **Note 3**

Operating Ratings[2]

Supply Voltage (V_{DDRF}, V_{DDBB}) ..... +4.75V to +5.5V
Max. Input Power 0dBm
RF Frequency Range ..... 300MHz to 440Hz
Data Duty-Cycle ..... 20% to 80%
Reference Oscillator Input Range ..... $0.1V_{PP}$ to $1.5V_{PP}$
Ambient Temperature (T_A) ..... –40°C to +85°C

Electrical Characteristics[4]

V_{DDRF} = V_{DDBB} = V_{DD} where +4.75V ≤ V_{DD} ≤ 5.5V, V_{SS} = 0V; C_{AGC} = 4.7µF, C_{TH} = 0.022µF; SEL0 = V_{DD}; SEL1 = V_{SS}; fixed mode (SWEN = V_{SS}); f_{REFOSC} = 9.794MHz (equivalent to f_{RF} = 315MHz); datarate = 600bps (Manchester encoded). T_A = 25°C, **bold** values indicate –40°C ≤ T_A ≤ +85°C; current flow into device pins is positive, unless noted.

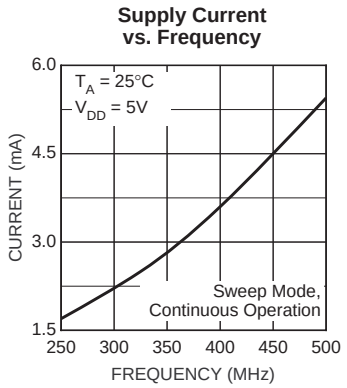
Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{OP}	Operating Current	continuous operation, f_{RF} = 315MHz		2.9	**4.5**	mA
		Polled with 10:1 duty cycle, f_{RF} = 315MHz		290		µA
		Continuous operation, f_{RF} = 433.92MHz		4.7	**7.5**	µA
		Polled with 10:1 duty cycle, f_{RF} = 433.92MHz		470		µA
I_{STBY}	Standby Current	V_{SHUT} = 0.8VDD		0.15	**0.5**	µA
RF Section, IF Section						
	Receiver Sensitivity(4)	f_{RF} = 315MHz		–102		dBm
		f_{RF} = 433.92MHz		–104		dBm
f_{IF}	IF Center Frequency	Note 5		0.86		MHz
f_{BW}	IF 3dB Bandwidth	Note 5		0.68		MHz
	Spurious Reverse Isolation	ANT pin, R_{SC} = 50Ω[6]		30		µVrms
	AGC Attack to Decay Ratio	$t_{ATTACK} \div t_{DECAY}$		0.1		
	AGC Leakage Current	T_A = +85°		±100		nA
Reference Oscillator						
Z_{REFOSC}	Reference Oscillator Input Impedance	Note 7		290		kΩ
	Reference Oscillator Source	Note 8		5.0		µA
Demodulator						
Z_{CTH}	CTH Source Impedance	Note 9		145		kΩ
$I_{ZCTH(leak)}$	CTH Leakage Current	T_A = +85°C		±100		nA
	Demodulator Filter Bandwidth Sweep Mode (SWEN = V_{DD} or OPEN)[5]	V_{SEL0} = V_{DD} V_{SEL0} = V_{SS}		1000 500		Hz Hz
	Demodulator Filter Bandwidth Fixed Mode (SWEN = V_{SS})[5]	V_{SEL0} = V_{DD} V_{SEL0} = V_{SS}		2000 1000		Hz Hz

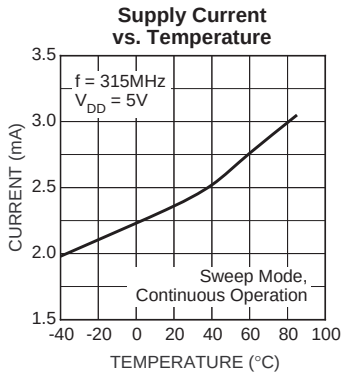
Symbol	Parameter	Condition	Min	Typ	Max	U
Digital/Control Section						
V_{IH}	Input High Voltage	SEL0, SEL1, SWEN			**0.8**	V_{DD}
V_{IL}	Input Low Voltage	SEL0, SEL1, SWEN	**0.2**			V_{DD}
I_{OUT}	Output Current	DO pin, push-pull		45		µA
V_{OH}	Output High Voltage	DO pin, I_{OUT} = –30µA	**0.9**			V_{DD}
V_{OL}	Output Low Voltage	DO pin, I_{OUT} = +30µA			**0.1**	V_{DD}
t_R, t_F	Output Rise and Fall Time	DO pin, C_{LOAD} = 15pF		4		µs

Notes:

1. Exceeding absolute maximum ratings may damage the device.
2. The device is not guaranteed to function outside its operating ratings.
3. Devices are ESD sensitive, use appropriate ESD precautions. The device meets Class 1 ESD test requirements, (human body model HBM), in accordance with MIL-STD-883C, method 3015. Do not operate or store near strong electrostatic fields.
4. Sensitivity is defined as the average signal level measured at the input necessary to achieve 10^{-2} BER (bit error rate). The RF input is assumed to be matched to 50Ω.
5. Parameter scales linearly with reference oscillator frequency f_T. For any reference oscillator frequency other than 9.794MHz, compute new parameter value as the ratio:
$$\frac{f_{REFOSC}MHZ}{9.794MHz} \times (\text{parameter value at 9.79MHz})$$
6. Spurious reverse isolation represents the spurious components, which appear on the RF input pin (ANT) measured into 50Ω with an input RF matching network.
7. Series resistance of the resonator (ceramic resonator or crystal) should be minimized to the extent possible. In cases where the resonator series resistance is too great, the oscillator may oscillate at a diminished peak-to-peak level, or may fail to oscillate entirely. Micrel recommends that series resistances for ceramic resonators and crystals not exceed 50Ω and 100Ω, respectively.
8. Crystal load capacitor is 10pF. See Figure 5 in “REFOSC” section for reference oscillator operation.
9. Parameter scales inversely with reference oscillator frequency f_T. For any reference oscillator frequency other than 9.794MHz, compute new parameter value as the ratio:
$$\frac{9.794MHz}{f_{REFOSC}MHZ} \times (\text{parameter value at 9.794MHz})$$

Typical Characteristics





Functional Diagram

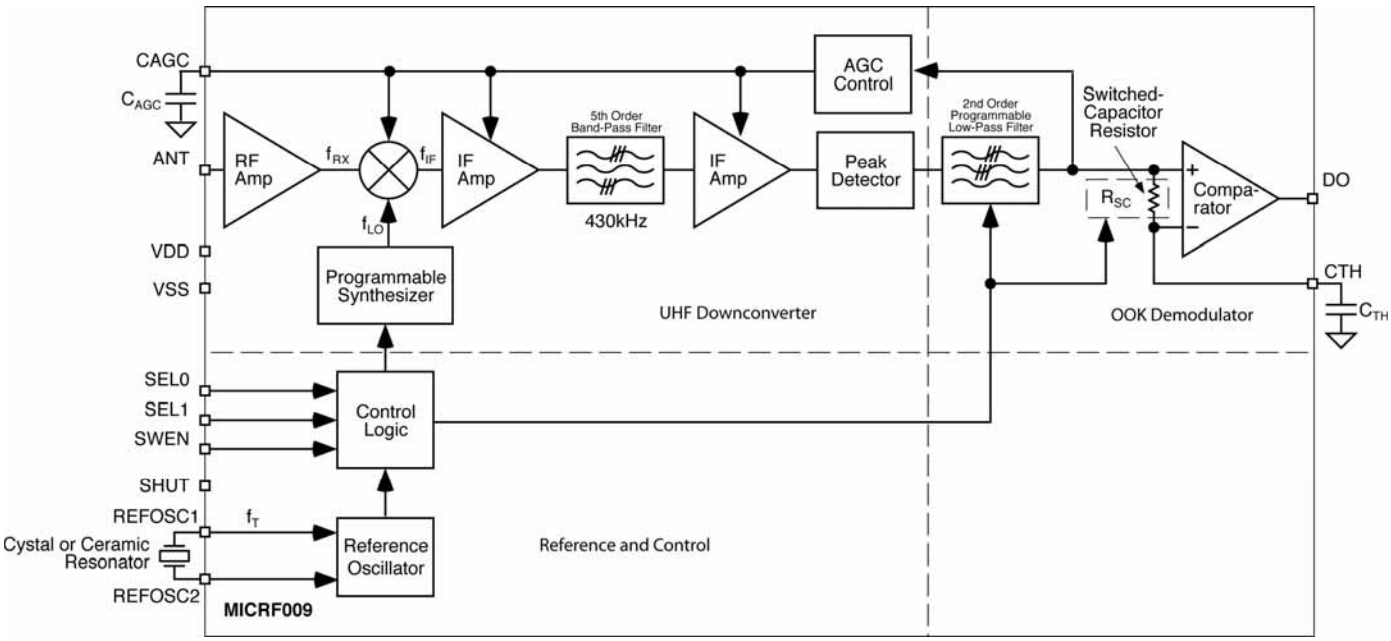


Figure 1. MICRF009 Block Diagram

Application Information and Function Description

Refer to "MICRF009 Block Diagram." Identified in the block diagram are the three sections of the IC: 1) UHF Downconverter, 2) OOK Demodulator, 3) Reference and Control. Also shown in the figure are two capacitors (C_{TH}, C_{AGC}) and one timing component, which is usually a crystal or ceramic resonator. With the exception of a supply decoupling capacitor and antenna impedance matching network, these are the only external components needed by the MICRF009 to assemble a complete UHF receiver.

For optimal performance it is highly recommended that the MICRF009 is impedance-matched to the antenna. The matching network will add additional two or three components.

Four control inputs are shown in the block diagram: SEL0, SEL1, SWEN, and SHUT. Using these logic inputs, the user can control the operating mode and selectable features of the IC. These inputs are CMOS compatible and are internally pulled-up. The IF Bandpass Filter Roll-off response of the IF Filter is 5th order, while the demodulator data filter exhibits a 2nd order response.

Design Steps

The following steps are the basic design steps for using the MICRF009 receiver:

1. Select the operating mode (sweep or fixed)
2. Select the reference oscillator
3. Select the demodulator filter bandwidth
4. Select the C_{TH} capacitor
5. Select the C_{AGC} capacitor

Step 1: Selecting The Operating Mode

Fixed-Mode Operation

For applications where the transmit frequency is set accurately (that is, applications where a SAW or crystal-based transmitter is used), the MICRF009 may be configured as a standard superheterodyne receiver (fixed-mode). In fixed-mode operation, the RF bandwidth is narrower making the receiver less susceptible to interfering signals. Fixed-mode is selected by connecting SWEN to ground.

Sweep-Mode Operation

When used in conjunction with low-cost LC transmitters, the MICRF009 should be configured in sweep-mode. In sweep-mode, while the topology is still superheterodynes, the local oscillator (LO) is swept over a range of frequencies at rates greater than the data rate. This technique effectively increases the RF bandwidth of the

MICRF009, allowing the device to operate in applications where significant transmitter-receiver frequency misalignment may exist. The transmit frequency may vary up to ±0.5% over initial tolerance, aging, and temperature. In sweep-mode, a band approximately 1.5% around the nominal transmit frequency is captured. The transmitter may drift up to ±0.5% without the need to retune the receiver and without impacting system performance.

The swept-LO technique does not affect the IF bandwidth, therefore noise performance is not degraded relative to fixed-mode. The IF bandwidth is 680kHz whether the device is operating in fixed or sweep-mode.

Due to limitations imposed by the LO sweeping process, the upper limit on data rate in sweep-mode is approximately 1250Hz.

Similar performance is not currently available with crystal-based superheterodyne receivers, which can operate only with SAW- or crystal-based transmitters.

In sweep-mode, a range reduction will occur in installation where there is a strong interferer in the swept RF band. This is because the process indiscriminately includes all signals within the sweep range. An MICRF009 may be used in place of a super-regenerative receiver in most applications.

Step 2: Selecting The Reference Oscillator

All timing and tuning operations on the MICRF009 are derived from the internal Colpitts reference oscillator. Timing and tuning is controlled through the REFOSC pin in one of three ways:

1. Connect a ceramic resonator.
2. Connect a crystal.
3. Drive this pin with an external timing signal.

The specific reference frequency required is related to the system transmit frequency and to the operating mode of the receiver as set by the SWEN pin.

Crystal or Ceramic Resonator Selection

Do not use resonators with integral capacitors since capacitors are included in the IC, also care should be taken to ensure low ESR crystals are selected. Contact Micrel RF Applications for suggested suppliers and part numbers.

If operating in fixed-mode, a crystal is recommended. In sweep-mode either a crystal or ceramic resonator may be used. When a crystal or ceramic resonator is used, the minimum voltage is $300mV_{PP}$. If using an externally applied signal, it should be AC-coupled and limited to the operating range of $0.1V_{PP}$ to $1.5V_{PP}$.

Selecting Reference Oscillator Frequency f_T

(Fixed-Mode)

As with any superheterodynes receiver, the difference between the internal LO (local oscillator) frequency f_{LO} and the incoming transmit frequency f_{TX}, should equal the IF center frequency. Equation 1 may be used to compute the appropriate f_{LO} for a given f_{TX}:

$$f_{LO} = f_{TX} \pm \left(0.86 \frac{f_{TX}}{315}\right) \quad (1)$$

Frequencies f_{TX} and f_{LO} are in MHz. Note that two values of f_{LO} exist for any given f_{TX}, distinguished as “high-side mixing” and “low-side mixing.” High-side mixing results in an image frequency above the frequency of interest and low-side mixing results in a frequency below. There is generally no preference of one over the other.

After choosing one of the two acceptable values of f_{LO}, use Equation 2 to compute the reference oscillator frequency f_T:

$$f_T = 2 \times \frac{f_{LO}}{64.5} \quad (2)$$

Frequency f_T is in MHz. Connect a crystal of frequency f_T to REFOSC on the MICRF009. Four-decimal-place accuracy on the frequency is generally adequate. The following table identifies f_T for some common transmit frequencies when the MICRF009 is operated in fixed-mode.

Transmit Frequency (f_{TX})	Reference Oscillator Frequency (f_T)
315MHz	9.7941MHz
390MHz	12.1260MHz
418MHz	12.9966MHz
433.92MHz	13.4916MHz

Table 1. Fixed-Mode Recommended Reference Oscillator Values For Typical Transmit Frequencies (high-side mixing)

Selecting REFOSC Frequency f_T

(Sweep Mode)

Selection of the reference oscillator frequency f_T in sweep mode is much simpler than in fixed mode due to the LO sweeping process. Also, accuracy requirements of the frequency reference component are significantly relaxed.

In sweep mode, f_T is given by Equation 3:

$$f_T = 2 \times \frac{f_{TX}}{64.25} \quad (3)$$

In sweep mode a reference oscillator with frequency accurate to two-decimal-places is generally adequate. A crystal may be used and may be necessary in some cases if the transmit frequency is particularly imprecise.

Transmit Frequency (f_{TX})	Reference Oscillator Frequency (f_T)

315MHz	9.81MHz
390MHz	12.140MHz
418MHz	13.01MHz
433.92MHz	13.51MHz

Table 2. Sweep-Mode Recommended Reference Oscillator Values For Typical Transmit Frequencies

Step 3: Selecting C_{TH} Capacitor

Extraction of the DC value of the demodulated signal for purposes of logic-level data slicing is accomplished using the external threshold capacitor C_{TH} and the on-chip switched capacitor "resistor" RSC, shown in the block diagram.

Slicing level time constant values vary somewhat with decoder type, data pattern, and data rate, but typically values range from 5ms to 50ms.This issue is covered in more detail in "Application Note 22." Optimization of the value of C_{TH} is required to maximize range.

Selecting Capacitor C_{TH}

The first step in the process is selection of a data-slicing-level time constant. This selection is strongly dependent on system issues including system decode response time and data code structure (that is, existence of data preamble, etc.) This issue is also covered in more detail in "Application Note 22."

The effective resistance of RSC is listed in the electrical characteristics table as 145kΩ at 315MHz, this value scales linearly with frequency. Source impedance of the CTH pin at other frequencies is given by equation (4), where f_T is in MHz:

$$R_{SC} = 145\Omega \frac{9.7940}{f_T} \quad (4)$$

τ of 5x the bit-rate is recommended. The effective resistance of RSC is listed in the electrical characteristics table as 145kΩ at 315MHz, this value scales inversely with frequency. Source impedance of the CTH pin at other frequencies is given by equation (5), where f_T is in MHz:

$$C_{TH} = \frac{\tau}{R_{SC}} \quad (5)$$

A standard ±20% X7R ceramic capacitor is generally sufficient. Refer to "Application Hint 42" for C_{TH} and C_{AGC} selection examples.

Step 4: Selecting C_{AGC} Capacitor

The signal path has AGC (automatic gain control) to increase input dynamic range. The attack time constant of the AGC is set externally by the value of the CAGC capacitor connected to the CAGC pin of the device. To maximize system range, it is important to keep the AGC control voltage ripple low, preferably under $10mV_{PP}$ once the control voltage has attained its quiescent value. For this reason, capacitor values of at least 0.47µF are recommended.

The AGC control voltage is carefully managed on-chip to allow duty-cycle operation of the MICRF009. When the device is placed into shutdown mode (SHUT pin is pulled high), the AGC capacitor floats to retain the voltage. When operation is resumed, only the voltage droop due to capacitor leakage must be replenished. A relatively low-leakage capacitor is recommended when the devices are used in duty-cycled operation.

To further enhance duty-cycled operation, the AGC push and pull currents are boosted for approximately 10ms immediately after the device is taken out of shutdown. This compensates for AGC capacitor voltage droop and reduces the time to restore the correct AGC voltage. The current is boosted by a factor of 45.

Selecting CAGC Capacitor in Continuous Mode

A CAGC capacitor in the range of 0.47µF to 4.7µF is typically recommended. Caution! If the capacitor is too large, the AGC may react too slowly to incoming signals. AGC settling time, from a completely discharged (zero-volt) state is given approximately by Equation 6:

$$\Delta t = 1.333 \times C_{AGC} - 0.44 \quad (6)$$

where:

C_{AGC} is in µF, and Δt is in seconds.

Selecting CAGC Capacitor in Duty-Cycle Mode

Voltage droop across the CAGC capacitor during shutdown should be replenished as quickly as possible after the IC is enabled. As mentioned above, the MICRF009 boosts the push-pull current by a factor of 45 immediately after start-up. This fixed time period is based on the reference oscillator frequency f_T. The time is 10.9ms for f_T = 6.00MHz, and varies inversely with f_T. The value of CAGC capacitor and the duration of the shutdown time period should be selected such that the droop can be replenished within this 10ms period.

Polarity of the droop is unknown, meaning the AGC voltage could droop up or down. The worst-case from a recovery standpoint is downward droop, since the AGC pull-up current is 1/10th magnitude of the pull-down current. The downward droop is replenished according to the Equation 7:

$$\frac{I}{C_{AGC}} = \frac{\Delta V}{\Delta t} \quad (7)$$

where:

I = AGC pull-up current for the initial 10ms (67.5µA)

C_{AGC} = AGC capacitor value

Δt = droop recovery time

ΔV = droop voltage

For example, if user desires Δt = 10ms and chooses a 4.7µF CAGC, then the allowable droop is about 144mV. Using the same equation with 200nA, the worst-case pin leakage, and assuming 1µA of capacitor leakage in the same direction, the maximum allowable Δt (shutdown time) is about 0.56s for droop recovery in 10ms.

The ratio of decay-to-attack time-constant is fixed at 1:10 (that is, the attack time constant is 10 times of the decay time constant). Generally the design value of 1:10 is adequate for the vast majority of applications. If adjustment is required, adding a resistor in parallel of the C_{AGC} capacitor may vary the ratio. The value of the resistor must be determined on a case-by-case basis.

Step 5: Selecting The Demodulator Filter Bandwidth

The input SEL0 controls the demodulator filter bandwidth in two binary steps, (625Hz to 1250Hz in sweep, 1250Hz to 2500Hz in fixed mode), see Table 3. Bandwidth must be selected according to the application. The demodulator bandwidth should be set according to equation 8. SEL1 tied to VSS by default.

$$\text{Demodulator Bandwidth} = \frac{0.65}{\text{shortest pulse - width}} \quad (8)$$

It should be noted that the values indicated in Table 1 are the nominal values. The filter bandwidth scales linearly with frequency so the exact value will depend on the operating frequency. Refer to the “Electrical Characteristics” for the exact filter bandwidth at a chosen frequency.

SEL0	Demodulator Bandwidth	
	Sweep Mode	Fixed Mode
1	1250Hz	2500Hz
0	625Hz	1250Hz

Table 3. Nominal Demodulator Filter Bandwidth vs. SEL0 and Operating Mode at 433.92MHz

Power Supply Bypass Capacitors

Supply bypass capacitors are strongly recommended. They should be connected to VDDBB and VDDRF and should have the shortest possible lead lengths. For best performance, connect VSSRF to VSSBB, VDDBB to VDDRF at the power supply only (that is, keep base-band currents from flowing through the RF return path).

Increasing Selectivity with Optional Bandpass Filter

For applications located in high ambient noise environments, a fixed value band-pass network may be connected between the ANT pin and VSSRF to provide additional receiver selectivity and input overload protection. A minimum input configuration is included in Figure 9. It provides some filtering and necessary overload protection.

Data Squelching

During quiet periods (no signal), the data output (DO pin) transitions randomly with noise. Most decoders can discriminate between this random noise and actual data. For some systems, it does present a problem. There are three possible approaches to reduce this output noise:

1. Analog squelch to raise the demodulator threshold.
2. Digital squelch to disable the output when data is not present.
3. Output filter to filter the (high frequency) noise glitches on the data output pin.

The simplest solution is to add analog squelch by introducing a small offset, or squelch voltage, on the CTH pin so that noise does not trigger the internal comparator. Usually 20mV to 30mV is sufficient, and may be achieved by connecting a several-meg-ohm resistor from the CTH pin to either VSSBB or VDDBB, depending on the desired offset polarity. Since MICRF009’s receiver AGC noise at the internal comparator input is always the same (set by the AGC), the squelch-offset requirement does not change as the local noise strength changes from installation to installation. Introducing squelch will reduce sensitivity and also reduce range. Only introduce an amount of offset sufficient to quiet the output. Typical squelch resistor values range from 10MΩ to 6.8MΩ for low to high squelch strength.

I/O Pin Interface Circuitry

Interface circuitry for the various I/O pins of the MICRF009 are diagrammed in Figures 2 through 8. The ESD protection diodes at all input and output pins are not shown.

CTH Pin

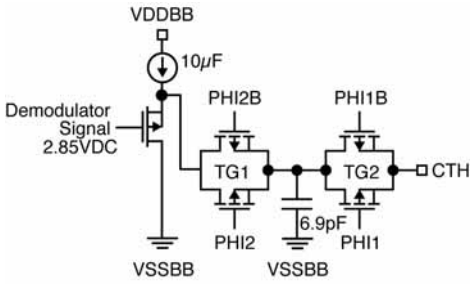


Figure 2. CTH Pin

Figure 2 illustrates the CTH pin interface circuit. The CTH pin is driven from a P-Channel MOSFET source-follower with approximately 10µA of bias. Transmission gates TG1 and TG2 isolate the 6.9pF capacitor. Internal control signals PHI1/PHI2 are related in a manner such that the impedance across the transmission gates looks like a “resistance” of approximately 145kΩ. The DC potential at the CTH pin is approximately 1.6V

CAGC Pin

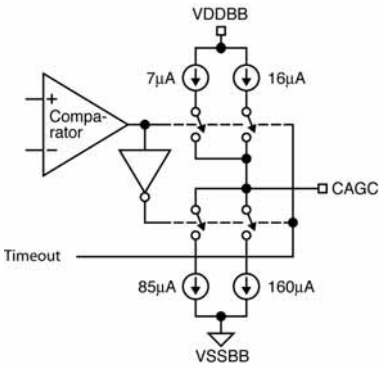


Figure 3. CAGC Pin

Figure 3 illustrates the CAGC pin interface circuit. The AGC control voltage is developed as an integrated current into a capacitor CAGC. The attack current is nominally 7µA, while the decay current is a 10 times scaling of this, approximately 85µA. Signal gain of the RF/IF strip inside the IC diminishes as the voltage on CAGC decreases. By simply adding a capacitor to CAGC pin, the attack/decay time constant ratio is fixed at 10:1. Modification of the attack/decay ratio is possible by adding resistance from the CAGC pin to either VDDBB or VSSBB, as desired.

Both the push and pull current sources are disabled during shutdown, which maintains the voltage across CAGC, and improves recovery time in duty-cycled applications. To further improve duty-cycle recovery, both push and pull currents are increased by 2 times for approximately 10ms after release of the SHUT pin. This allows rapid recovery of any voltage droop on CAGC while in shutdown.

DO Pin

The output stage for the digital output (DO) is shown in Figure 4. The output is a 45µA push and 45µA pull switched-current stage. This output stage is capable of driving CMOS loads. An external buffer-driver is recommended for driving high capacitance loads.

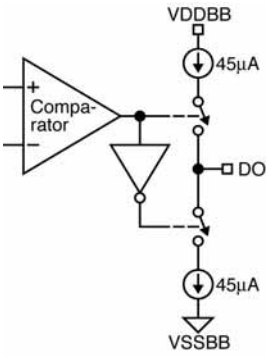


Figure 4. DO Pin

REFOSC1 and REFOSC2 Pin

The REFOSC input circuit is shown in Figure 5. Input impedance is quite high (200kΩ). This is a Colpitts oscillator, with internal 10pF capacitors. This input is intended to work with standard crystal resonators, connected from this pin to REFOSC2.

This REFOSC2 pin appears as a low resistance path to VSS during normal operation and is an input to a buffer amplifier used during the initial start up phase to ensure rapid build up of crystal oscillations.

The resonators should not contain integral capacitors, since these capacitors are contained inside the IC. Externally applied signals should be AC-coupled, amplitude limited to approximately $0.5V_{PP}$. The nominal DC bias voltage on this pin is 1.4V

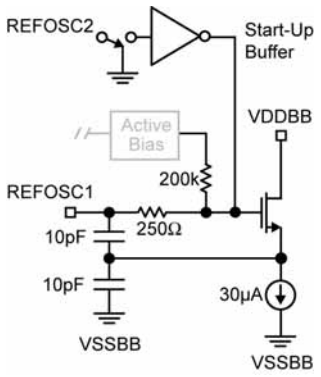


Figure 5. REFOSC Pin

SEL0, SEL1, SWEN, and SHUT Pins

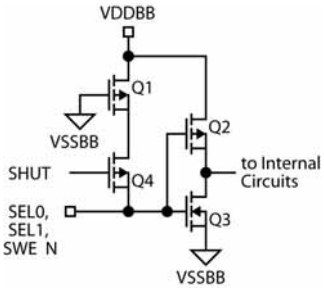


Figure 6a. SEL0/SEL1/SWEN Pins

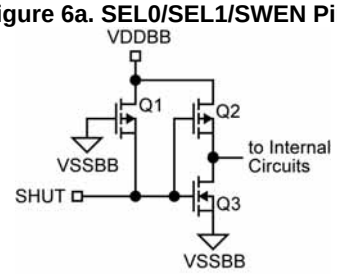


Figure 6b. SHUT Pin

Control input circuitry is shown in Figure 6a and 6b. The standard input is a logic inverter constructed with minimum geometry MOSFETs (Q2, Q3). P-Channel MOSFET Q1 is a large channel length device, which functions essentially as a “weak” pull-up to VDDBB. Typical pull-up current is 5µA, leading to an impedance to the VDDBB supply of typically 1MΩ.

Additional Applications Information

In addition to the basic operation of the MICRF009, the following enhancements can be made. In particular, it is strongly recommended that the antenna impedance is matched to the input of the IC.

Antenna Impedance Matching

As shown in Figure 7, and Table 4, the antenna pin input impedance is frequency dependent.

The ANT pin can be matched to 50Ω with an L-type circuit as shown in Figure 3. That is, a shunt inductor from the antenna input to ground and another in series from the antenna input to the ANT pin.

Inductor values may be different from Table 4, depending on PCB material, PCB thickness, ground configuration, and how long the traces are in the layout. Values shown were characterized for a 0.031" thickness, FR4 board, solid ground plane on bottom layer, and very short traces. MuRata and Coilcraft wire-wound 0603 or 0805 surface mount inductors were tested, however, any wire-wound inductor with high SRF (self-resonance frequency) should do the job.

Shutdown Function

Duty-cycled operation of the MICRF009 (often referred to as polling) is achieved by turning the MICRF009 on and off via the SHUT pin. The shutdown function is controlled by a logic state applied to the SHUT pin. When VSHUT is high, the device goes into low-power standby mode. This pin is pulled high internally, and it must be externally pulled low to enable the receiver.

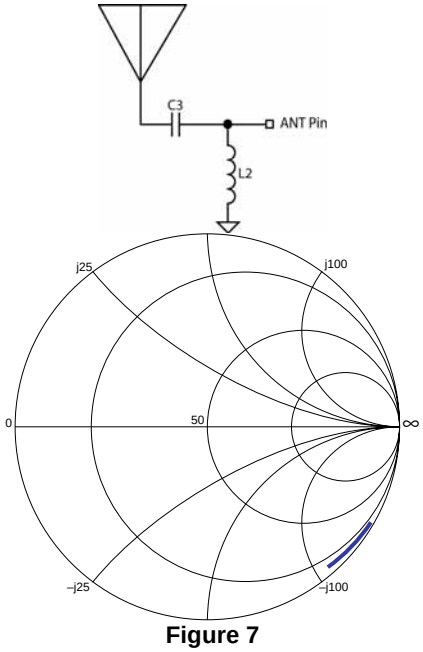


Figure 7

Frequency (Mhz)	S11 Mag, angle	Z11, ohms	C3, pF	L2, nH
300	0.944,-36.65	14.45-j150	2.2	47
305	0.940,-37.499	14.84-j145	2.2	47
310	0.942,-37.579	14.28-j145	2.2	47
315	0.945, -37.66	13.48-j145	2.2	47
320	0.943,-38.237	13.58-j143	2	47
325	0.942, -38.814	13.43-j140	1.8	47
330	0.94, -39.39	13.5-j138	1.8	47
335	0.938, -39.967	13.59-j136	1.8	43
340	0.937, -40.544	13.44-j134	1.8	43
345	0.935, -41.12	13.51-j132	1.8	43
350	0.933, -41.697	13.57-j130	2	39
355	0.931, -42.274	13.62-j123	2.2	36
360	0.93, 42.85	13.48-j126	2.2	36
365	0.928, -43.427	13.52-j124	2	36
370	0.926, -44.004	13.57-j122	1.8	36
375	0.925, -44.581	13.42-j120	2.2	33
380	0.923, -45.157	13.46-j118	2	33
385	0.921, -45.734	13.49-j117	1.8	33
390	0.92, -46.311	13.35-j115	1.8	33
395	0.917, -46.729	13.6-j114	1.8	33
400	0.914, -47.148	13.89-j113	2	30
405	0.912, -47.566	14.00-j112	1.8	30
410	0.909, -47.985	14.25-j110	1.8	30
415	0.907, -48.403	14.34-j109	2.2	27
420	0.906, -48.797	14.28-j108	2	27
425	0.909, -49.152	13.63-j107	2	27
430	0.911, -49.507	13.15-j107	1.8	27
435	0.911, -49.925	12.94-j106	1.8	27
440	0.904, -50.571	13.66-j104	1.8	27

Table 4

Application Example

315MHz Receiver/Decoder Application

Figure 8 illustrates a typical application for the MICRF009 UHF Receiver IC. This receiver operates continuously (not duty cycled) in sweep mode, and features 6-bit address decoding and two output code bits.

Operation in this example is at 315MHz, and may be customized by selection of the appropriate frequency reference (Y1), and adjustment of the antenna length. The value of C4 would also change if the optional input filter is used. Changes from the 1kbps data rate may require a change in the value of R1. A bill of materials accompanies the schematic.

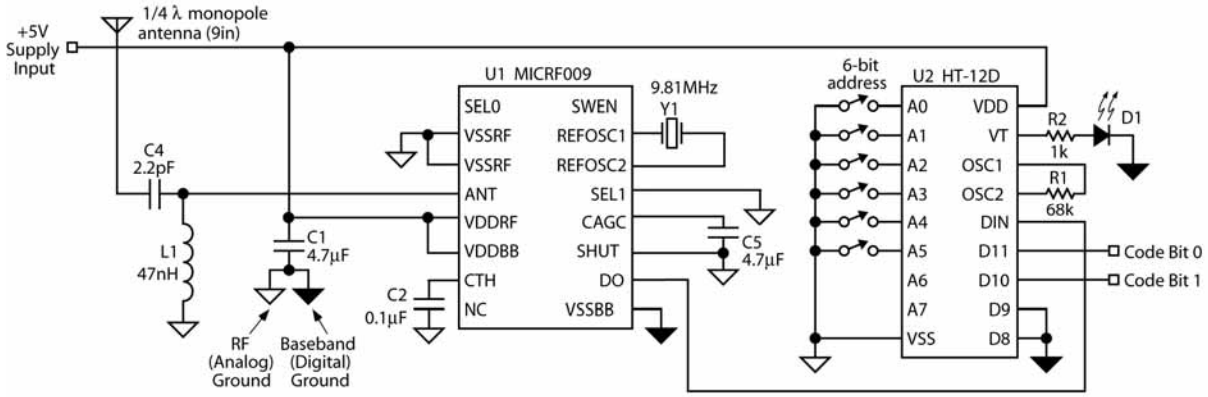


Figure 8. 315Mhz, 1.2kbps On-Off Keyed Receiver with Decoder Sweep Mode

Bill of Materials

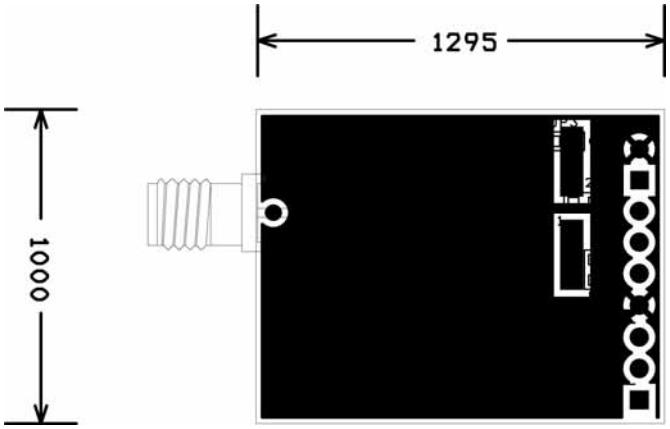
Item	Part Number	Manufacturer	Description	Qty
C1, C5		Vishay[1]	4.7µF ceramic or tantalum capacitor	2
C2		Vishay[1]	0.1µF ceramic or tantalum capacitor	1
C3		Vishay[1]	2.2µF ceramic or tantalum capacitor	1
C4		Vishay[1]	8.2pF COG ceramic capacitor	1
Y1	See Crystal App. Note		9.81 ceramic resonator	1
D1	SSF-LX100LID	Lumex[2]	Red LED	1
L1	0603CS-47NX_BC	Coil Craft[5]	47nH Inductor	1
R1			68k, 1/4W, 5%	1
R2		Vishay[1]	1k, 1/4W, 5%	1
U1	**MICRF009**	**Micrel[3]**	**UHF receiver**	**1**
U2	HT-12D	Holtek[4]	Logic decoder	1

Notes:

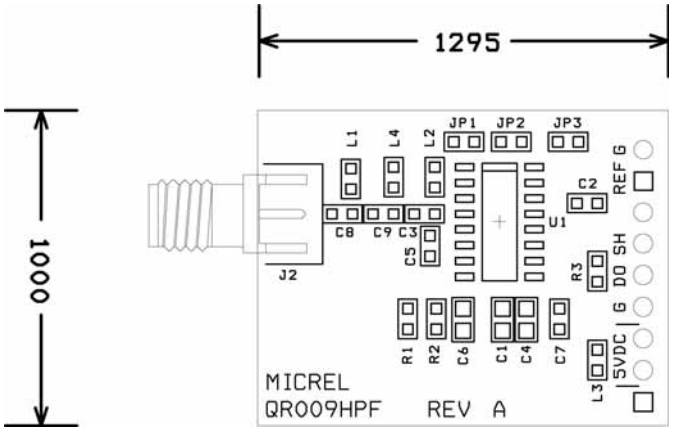
1. Vishay tel: 203-268-6261
2. Lumex tel: 800-278-5666
3. **Micrel Semiconductor** tel: 408-944-0800
4. Holtek tel: 408-894-9046
5. Coil Craft tel: 847-639-2361

PCB Layout Information

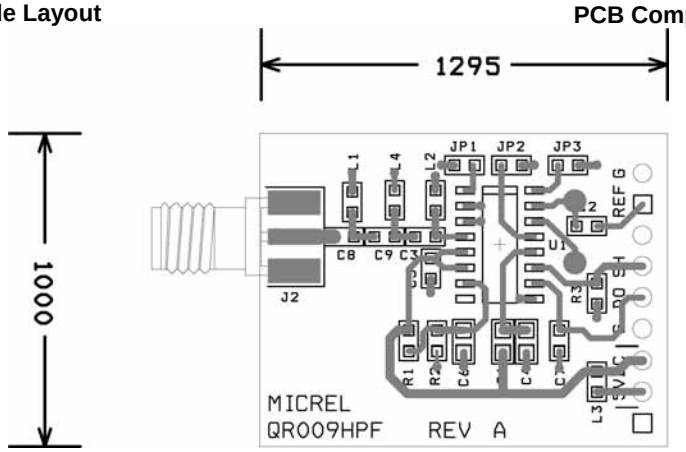
The MICRF009 evaluation board was designed and characterized using two sided 0.031 inch thick FR4 material with 1 ounce copper clad. If another type of printed circuit board material were to be substituted, impedance matching and characterization data stated in this document may not be valid. The Bill of Materials and gerber files for this board can be downloaded from the Micrel website at www.micrel.com.



PCB Solder Side Layout



PCB Component Layout



PCB Silk Screen

PCB for QR009HPF

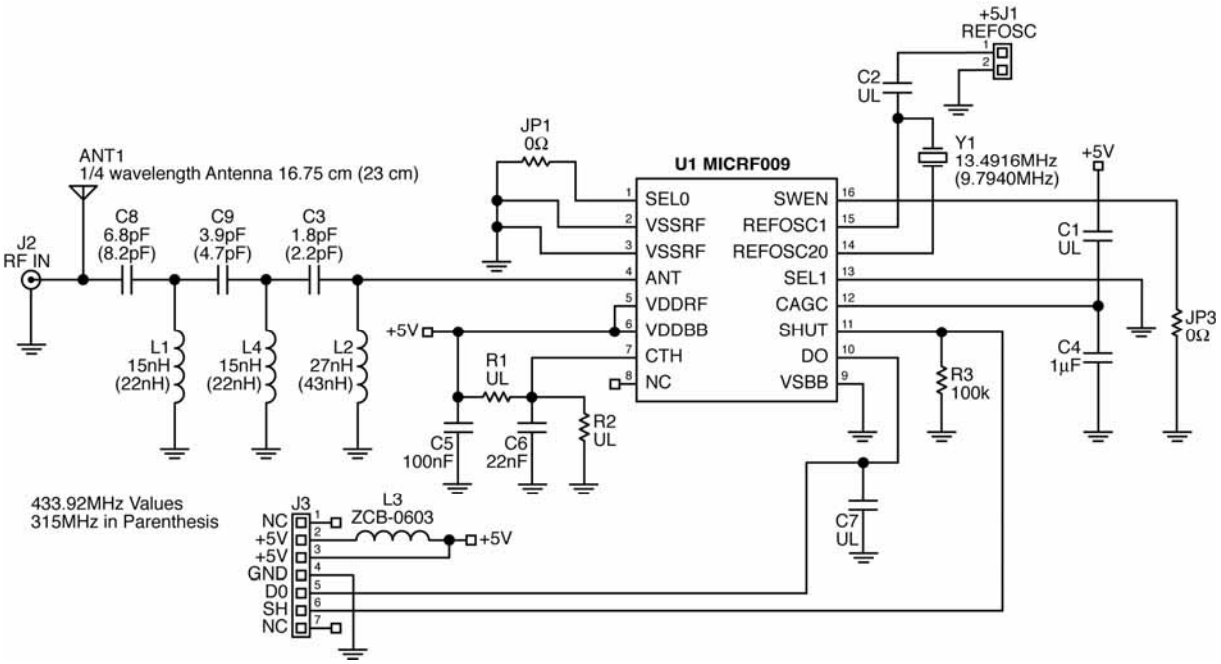
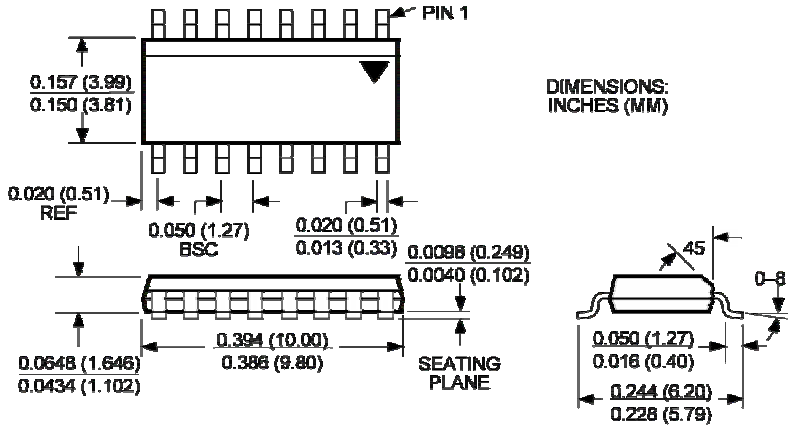


Figure 9. 433.92MHz, 1200bps, High Pass Filter Input

Package Information



16-Pin SOIC (M)

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