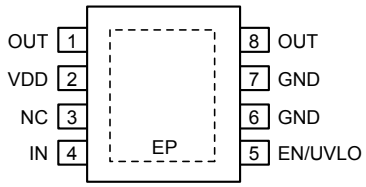
Ordering Information

Part Number	Marking	Configuration	Junction Temp. Range	Package	Lead Finish
MIC44F18YML	$\overline{D12}$	Non-Inverting	–40°C to 125°C	2x2 MLF-8	Pb-Free
MIC44F18YMME		Non-Inverting	–40°C to 125°C	ePAD MSOP-8	Pb-Free
MIC44F19YML	$\overline{D13}$	Inverting Output high when disabled	–40°C to 125°C	2x2 MLF-8	Pb-Free
MIC44F19YMME		Inverting Output high when disabled	–40°C to 125°C	ePAD MSOP-8	Pb-Free
MIC44F20YML	$\overline{D14}$	Inverting Output low when disabled	–40°C to 125°C	2x2 MLF-8	Pb-Free
MIC44F20YMME		Inverting Output low when disabled	–40°C to 125°C	ePAD MSOP-8	Pb-Free

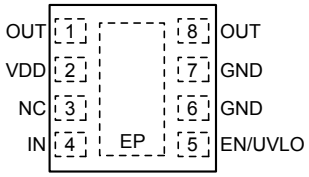
Note:

1. Over bar symbol may not be to scale.

Pin Configuration



8-Pin ePAD MSOP (MME)



8-Pin MLF (ML)

Pin Description

Pin Number	Pin Name	Pin Function
1,8	OUT	Driver Output
2	VDD	Supply Input
3	NC	No Connect
4	IN	Input (Input): Logic high produces a high output voltage for the MIC44F18 and a low output voltage for the MIC44F19/20. Logic low produces a low output voltage for the MIC44F18 and a high output voltage for the MIC44F19/20.
5	EN/UVLO	EN / Under-Voltage Lockout (Input): Pulling this pin below low disables the driver. When disabled, the output is in the off state (low for the MIC44F18/20 and high for the MIC44F19). Floating this pin enables the driver and the UVLO circuitry when V_{DD} reaches the UVLO threshold. A resistor divider can set a different UVLO threshold voltage as shown on page 1 (See “Application Information” section for more details).
6,7	GND	Ground
EP	GND	Ground. Exposed Backside Pad.

Logic Table

EN/UVLO	IN	MIC44F18 OUTPUT	MIC44F19 OUTPUT	MIC44F20 OUTPUT
0	0	LOW	HI	LOW
0	1	LOW	HI	LOW
1	0	LOW	HI	HI
1	1	HI	LOW	LOW

Absolute Maximum Ratings[1]

Supply Voltage (V_{dd}). 14V
UVLO/Enable Voltage ($V_{UVLO/EN}$)..... 14V
Input Voltage (V_{IN}) ..... (V_S + 0.1V) to (GND-5V)
Output Voltage (V_{OUT}) 14V
Junction Temperature (T_J)..... .....150°C
Ambient Storage Temperature (T_{dd}) ..... -65°C to +150°C
Lead Temperature (10 sec).....300°C
ESD Rating, **Note 3**
Pins 1,2,3,5,6,7,8.....2KV
Pin 4..... 500V

Operating Ratings[2]

Supply Voltage (V_{dd}) ..... 4.5V to 13.2V
Package Thermal Impedance
ePAD MSOP-8 (θ_{JA})..... ...78°C/W
2x2 MLF-8L (θ_{JA}).....93°C/W
Operating Junction Temperature (T_J)..... 125°C

Electrical Characteristics[4]

4.5V≤ V_{dd}≤ 13.2V; C_L =1000pf; T_A = 25°C, **bold** values indicate –40°C≤ T_j ≤ +125°C, unless noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Power Supply						
V_{dd}	Supply Voltage Range		**4.5**		**13.2**	V
I_S	High Output Quiescent Current	V_{IN} = 5V (MIC44F18), V_{IN} = 0V (MIC44F19/20)			**2.5**	mA
	Low Output Quiescent Current	V_{IN} = 0V (MIC44F18), V_{IN} = 5V (MIC44F19/20)			**2.5**	mA
I_{SD}	Shutdown Current	V_{EN} = 0V			**200**	µA
EN/UVLO						
V_{EN}	Enable Threshold		**1.3**	**1.4**	**1.5**	V
	Enable Hysteresis			120		mV
V_{UVLO}	Under-Voltage Lockout Threshold (Internally Set)	V_{EN} = open V_{DD} rising	3.6	4.2	4.4	V
	UVLO Hysteresis			370		mV
V_{UVLO}	Under-Voltage Lockout Threshold (Externally Set)	V_{DD} rising	V_{EN} (MAX)		V_{dd}	V
Input						
V_{IN}	Input Voltage Range	Steady State Voltage (note 5)	**0**		**Vdd**	
V_{IH}	Logic 1 Input Voltage	T_A = 25°C (+/-5%) Over temperature range **(+/-10%)**	1.615 **1.53**	1.7 **1.7**	1.785 **1.87**	V
V_{IL}	Logic 0 Input Voltage	T_A = 25°C (+/-5%) Over temperature range **(+/-10%)**	1.45 **1.377**	1.53 **1.53**	1.607 **1.683**	V
I_{IN}	Input Current	4.5V≤ V_{IN}≤ 10V			**5**	µA

Electrical Characteristics (Continued)

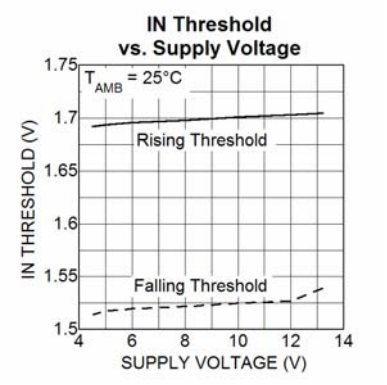
4.5V≤ V_{dd}≤ 13.2V; C_L =1000pf; T_A = 25°C, **bold** values indicate –40°C≤ T_j ≤ +125°C, unless noted.

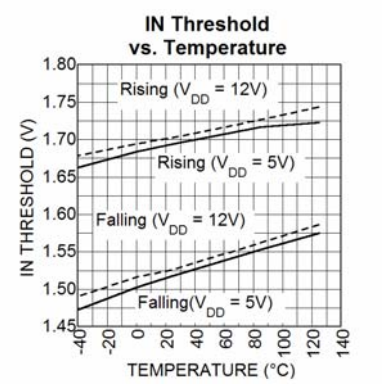
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Output						
V_{OH}	High Output Voltage	See Figure 1	**V_S- 0.025**			V
V_{OL}	Low Output Voltage	See Figure 1			**0.025**	V
R_O	Output Resistance, Output High	I_{OUT} = 100mA, V_{dd} = 12V I_{OUT} = 100mA, V_{dd} = 5V			**2** **3**	Ω
	Output Resistance, Output Low	I_{OUT} = 100mA, V_{dd} = 12V I_{OUT} = 100mA, V_{dd} = 5V			**2** **3**	Ω
I_{PEAK}	Peak Output Sink Current	V_{dd} = 12V	**6**			A
	Peak Output Source Current	V_S = 12V	**6**			A
I_R	Latch-Up Protection Withstand Reverse Current		**>500**			mA
Switching Time						
t_R	Rise Time	V_S = 12V, C_L=1000pF See Timing Diagram		10	**20**	ns
t_F	Fall Time	V_S = 12V, C_L=1000pF See Timing Diagram		10	**20**	ns
t_{D1}	Delay Time	V_S = 12V, C_L=1000pF See Timing Diagram		15	**35**	ns
t_{D2}	Delay Time	V_S = 12V, C_L=1000pF See Timing Diagram		13	**35**	ns
t_{PW}	Pulse Width	V_S = 12V See Timing Diagram	**50**			ns
f_{MAX}	Maximum Input Frequency	V_S = 12V See Timing Diagram 2		**Note 6**		MHz

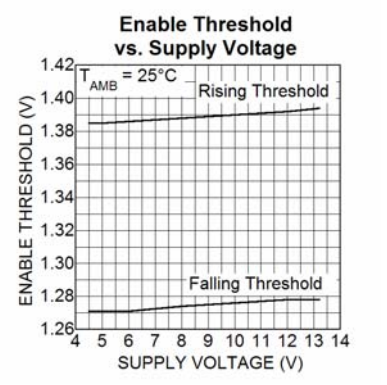
Notes:

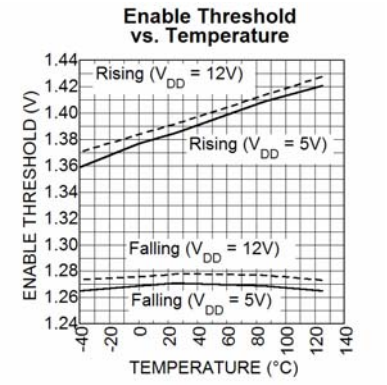
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.
4. Specification for packaged product only.
5. The device is protected from damage when -5V< Vin< 0V. However, 0V is the recommended minimum continuous V_{IL} voltage. See the applications section for additional information.
6. See applications section for information on the maximum operating frequency.

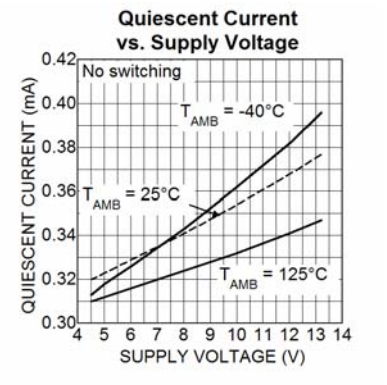
Typical Characteristics

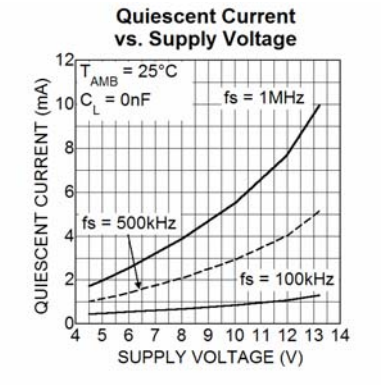


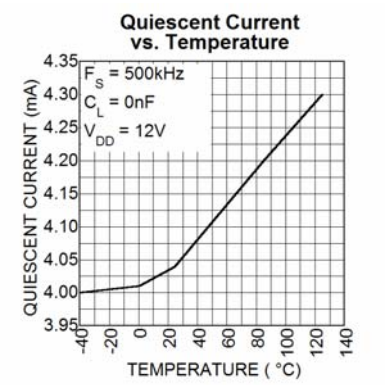


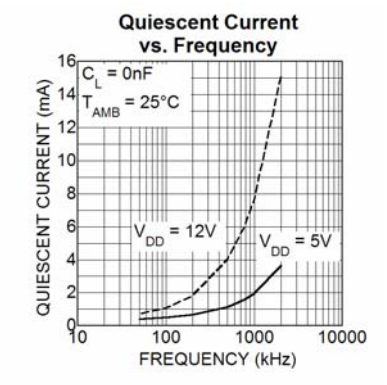


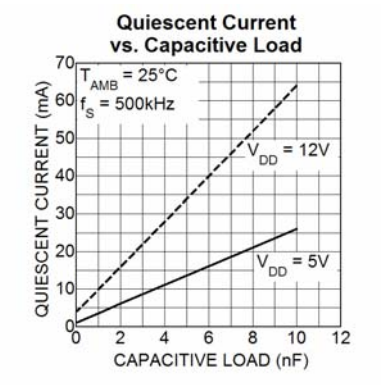


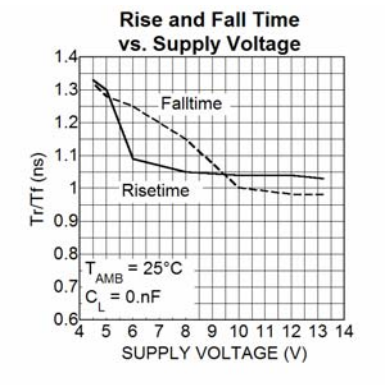


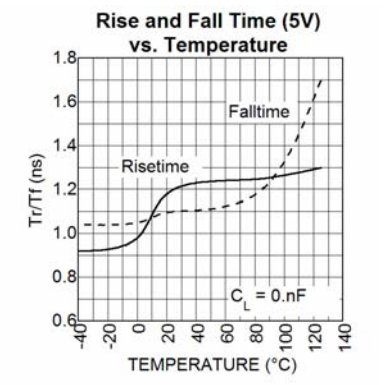


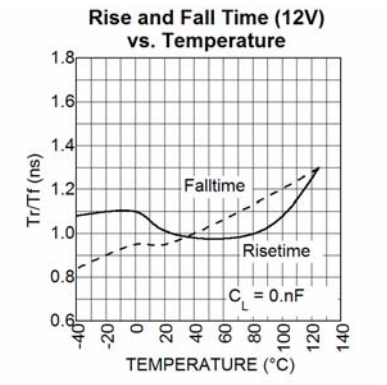




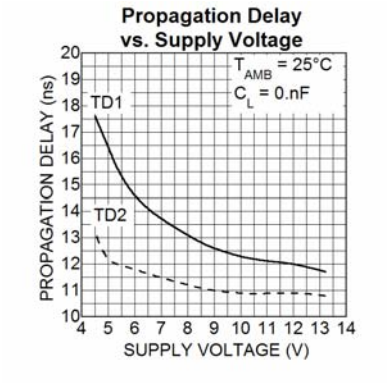


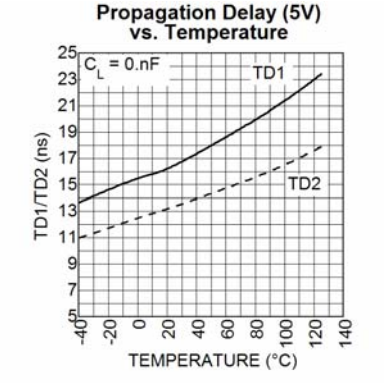


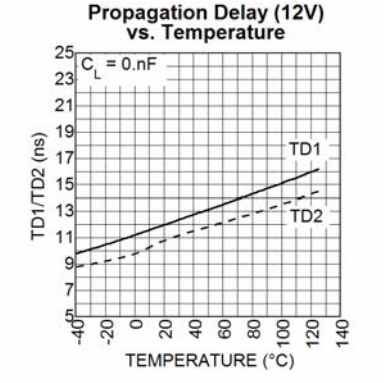


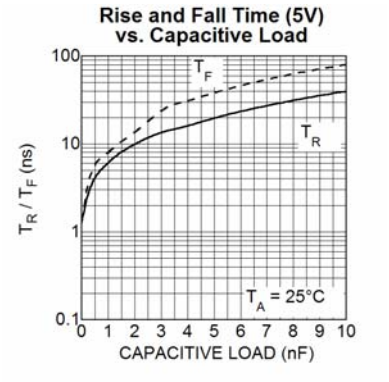


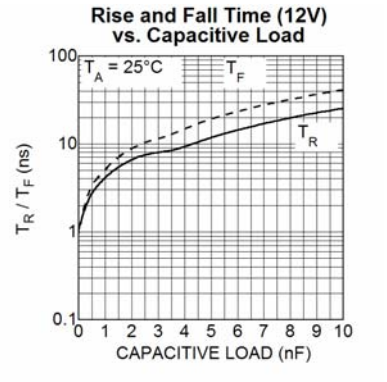
Typical Characteristics cont.

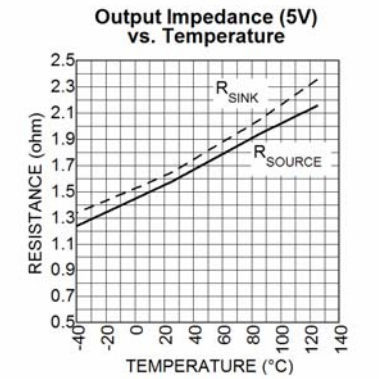


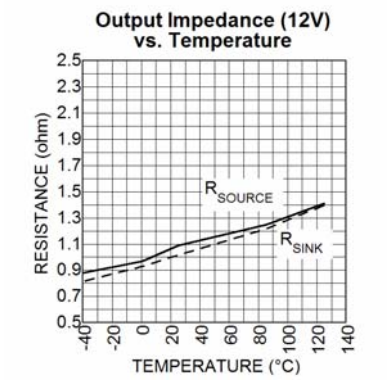




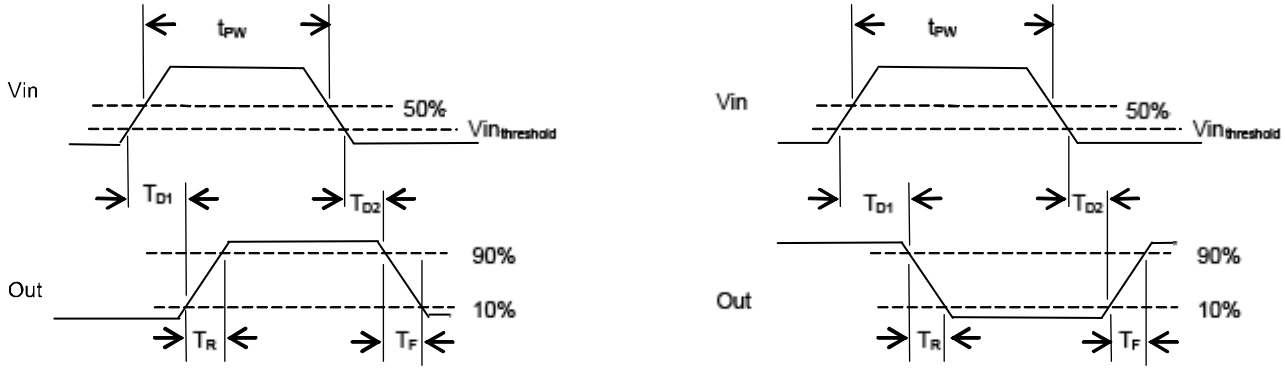








Timing Diagram



Functional Diagram

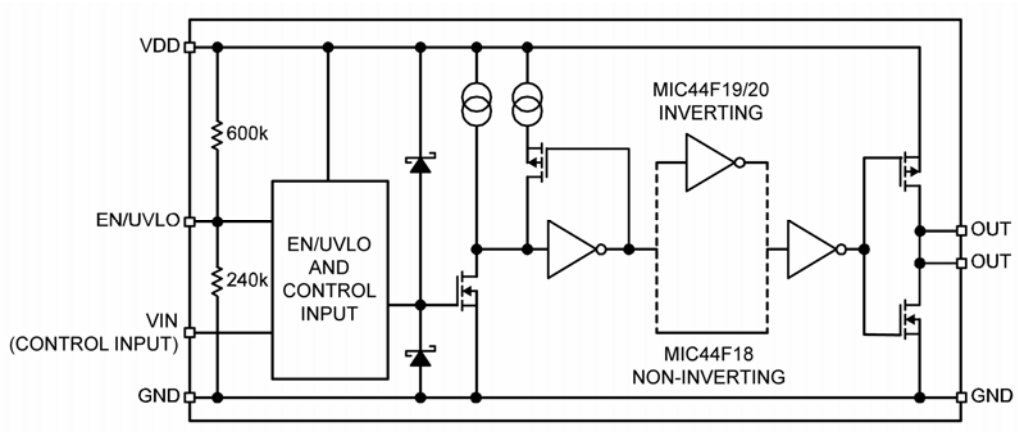


Figure 1. MIC44F18/19/20 Functional Block Diagram

Functional Description

The MIC44F18/19/20 family of drivers are high speed, high current drivers that are designed to drive P-channel and N-channel MOSFETs. The drivers come in both inverting and non-inverting versions. The block diagram of the MIC44Fxx driver is shown in Figure 1.

The MIC44F18 is a non-inverting driver. When disabled, the VOUT pin is pulled low. The MIC44F19 is an inverting driver that is optimized to drive P-channel MOSFETs. When disabled, the VOUT pin is pulled high, which turns off the P-channel MOSFET. The MIC44F20 is an inverting driver, whose VOUT pin is pulled low when disabled. This allows it to drive an N-channel MOSFETs and turn it off when the driver is disabled. The logic table below summarizes the driver operation.

EN/UVLO	IN	MIC44F18 OUTPUT	MIC44F19 OUTPUT	MIC44F20 OUTPUT
0	0	LOW	HI	LOW
0	1	LOW	HI	LOW
1	0	LOW	HI	HI
1	1	HI	LOW	LOW

Startup and UVLO

The UVLO circuit disables the output until the V_{DD} supply voltage exceeds the UVLO threshold. Hysteresis in the UVLO circuit prevents noise and finite circuit impedance from causing chatter during turn-on and turn-off.

As shown in figure 2, with the EN/UVLO pin open, an internal resistor divider senses the V_{DD} voltage and the UVLO threshold is set at the minimum operating voltage of the driver. The driver can be set to turn on at a higher voltage by adding an external resistor to the UVLO pin.

With an external divider, the V_{DD} turn on (rising V_{DD}) threshold is calculated as:

$$V_{DDenable} = V_{TH} \times \left[1 + \frac{R1}{R2}\right]$$

$$V_{DDhysteresis} = V_{Hyst} \times \left[1 + \frac{R1}{R2}\right]$$

where: V_{TH} = Enable Threshold Voltage

$VDD_{Hysteresis}$ = Hysteresis Voltage at the VDD pin

V_{Hyst} = Enable Hysteresis Voltage

Because the external resistors are parallel with the internal resistors, it is important to keep the value of the external resistors at least 10 times lower than the typical values of the internal resistors. This prevents the internal resistors from affecting the accuracy of the enable calculation as well as preventing the large tolerance of the internal resistors from affecting the tolerance of the enable voltage setting.

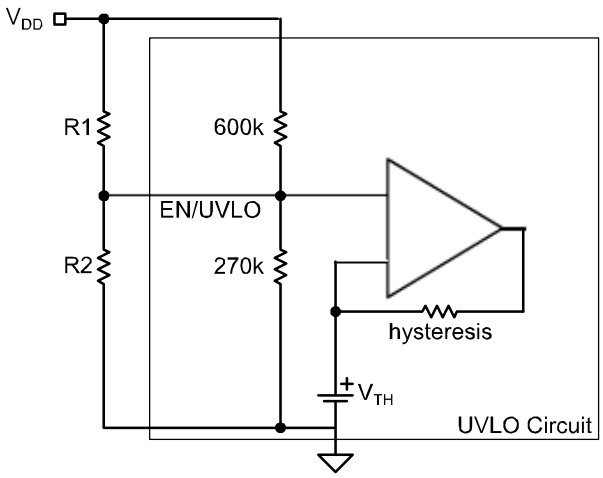


Figure 2. UVLO Circuit

Input Stage

The MIC44Fxx family of drivers have a high impedance, TTL compatible input stage. The tight tolerance of the input threshold makes it compatible with CMOS devices powered from any supply voltage between 3V and VDD. Hysteresis on the input pin improves noise immunity and prevents input signals with slow rise times from falsely triggering the output. The amplitude of the input voltage has no effect on the supply current draw of the driver.

The input voltage signal may go up to -5V below ground without damaging the driver or causing a latch up condition. Negative input voltages 0.7V below ground or greater will cause an increase in propagation delay.

Output Driver Section

A block diagram of the low-side driver is shown in Figure 3. Low driver impedances allow the external MOSFET to be turned on and off quickly. The rail-to-rail drive capability of the output ensures a low R_{DSON} from the external MOSFET.

Redundant Vout pins lower the driver circuit impedance, which helps increase the drive current and minimize LC circuit ringing between the MOSFET gate and driver output.

The slew rate of the output is non-adjustable and depends only on the V_{DD} voltage and how much capacitance is present at the VOUT pin. The slew rate at the MOSFET gate can be adjusted by adding a resistor between the MOSFET gate and the driver output.

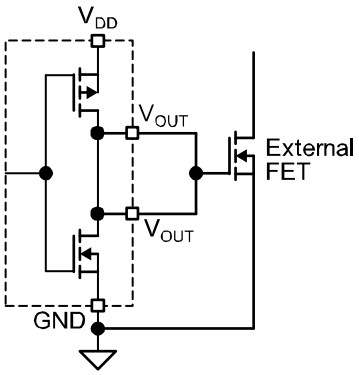


Figure 3. Output Driver Section

Application Information

Power Dissipation Considerations

Power dissipation in the driver can be separated into two areas:

- Output driver stage dissipation
- Quiescent current dissipation used to supply the internal logic and control functions.

Output Driver Stage Power Dissipation

Power dissipation in the output driver stage is mainly caused by charging and discharging the gate to source and gate to drain capacitance of the external MOSFET. Figure 4 shows a simplified equivalent circuit of the MIC44F18 driving an external MOSFET.

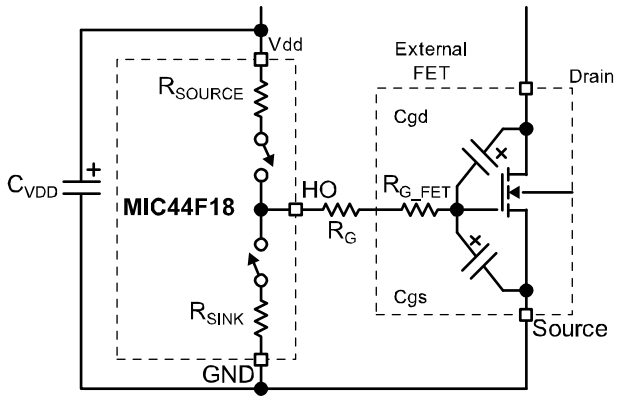


Figure 4. Output Driver Stage Power Dissipation

Dissipation during the External MOSFET Turn-On

Energy from capacitor C_{VDD} is used to charge up the input capacitance of the MOSFET (C_{GD} and C_{GS}). The energy delivered to the MOSFET is dissipated in the three resistive components, R_{ON}, R_G and R_{G_FET}. R_{ON} is the on resistance of the upper driver MOSFET in the MIC44F18. R_G is the series resistor (if any) between the driver IC and the MOSFET. R_{G_FET} is the gate resistance of the MOSFET. R_{G_FET} is usually listed in the power MOSFET's specifications. The ESR of capacitor C_B and the resistance of the connecting etch can be ignored since they are much less than R_{ON} and R_{G_FET}.

The effective capacitance of C_{GD} and C_{GS} is difficult to calculate since they vary non-linearly with I_D, V_{GS}, and V_{DS}. Fortunately, most power MOSFET specifications include a typical graph of total gate charge vs. V_{GS}. Figure 5 shows a typical gate charge curve for an arbitrary power MOSFET. This illustrates that for a gate voltage of 10V, the MOSFET requires about 23.5nC of charge.

The energy dissipated by the resistive components of the gate drive circuit during turn-on is calculated as:

$$E = \frac{1}{2} \times Ciss \times V_{GS}{}^2$$

but

$$Q = C \times V$$

so

$$E = 1/2 \times Qg \times V_{GS}$$

where

Ciss is the total gate capacitance of the MOSFET

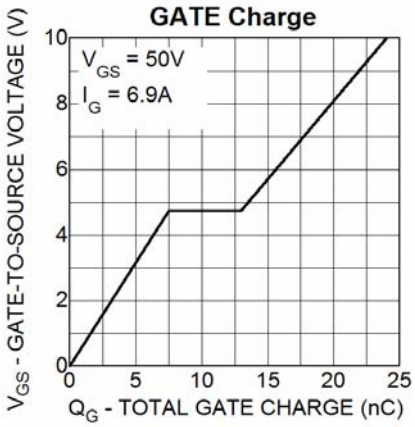


Figure 5. GATE Charge

The same energy is dissipated by R_{OFF}, R_G and R_{G_FET} when the driver IC turns the MOSFET off. Assuming Ron is approximately equal to R_{OFF}, the total energy and power dissipated by the resistive drive elements is:

$$E_{DRIVER} = Q_G \times V_{GS}$$

and

$$P_{DRIVER} = Q_G \times V_{GS} \times f_S$$

Where

E_{DRIVER} is the energy dissipated per switching power

P_{DRIVER} is the power dissipated by switching the MOSFET on and off

Q_G is the total GATE charge at V_{GS}

V_{GS} is the GATE to SOURCE voltage on the MOSFET

f_S is the switching frequency of the GATE drive circuit

The power dissipated inside the MIC4100/4101 is equal to the ratio of R_{ON} & R_{OFF} to the external resistive losses in R_G and R_{G_FET}. Letting R_{ON} = R_{OFF}, the power dissipated in the MIC44F18 due to driving the external MOSFET is:

$$Pdiss_{drive} = P_{DRIVER} \frac{R_{ON}}{R_{ON} + R_G + R_{G\_FET}}$$

Supply Current Power Dissipation

Power is dissipated in the MIC44F18 even if is there is nothing being driven. The supply current is drawn by the bias for the internal circuitry, the level shifting circuitry and shoot-through current in the output drivers. The supply current is proportional to operating frequency and the V_{DD} voltage. The typical characteristic graphs show how supply current varies with switching frequency and supply voltage.

The power dissipated by the MIC44F18 due to supply current is:

$$Pdiss_{SUPPLY} = V_{DD} \times I_{DD}$$

Total Power Dissipation and Thermal Considerations

Total power dissipation in the Driver equals the power dissipation caused by driving the external MOSFETs plus the supply current:

$$Pdiss_{TOTAL} = Pdiss_{SUPPLY} + Pdiss_{DRIVE}$$

The die temperature may be calculated once the total power dissipation is known:

$$T_J = T_A + Pdiss_{TOTAL} \times \theta_{JA}$$

Where

T_A is the Maximum ambient temperature

T_J is the junction temperature (°C)

$Pdiss_{TOTAL}$ is the power dissipation of the Driver

θJC is the thermal resistance from junction-to-ambient air (°C/W)

The following graphs help determine the maximum gate charge that can be driven with respect to switching frequency, supply voltage and ambient temperature.

Figure 6A shows the power dissipation in the driver for different values of gate charge with V_{DD}=5V. Figure 6B shows the power dissipation at V_{DD}=12V. Figure 6C show the maximum power dissipation for a given ambient temperature for the MLF and ePad packages.

The maximum operating frequency of the driver may be limited by the maximum power dissipation of the driver package.

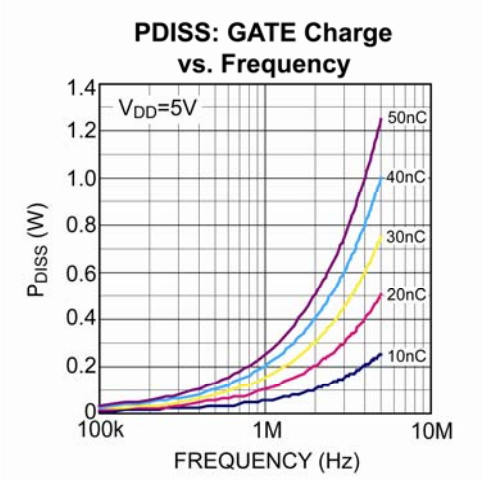


Figure 6A. Driver Power Dissipation

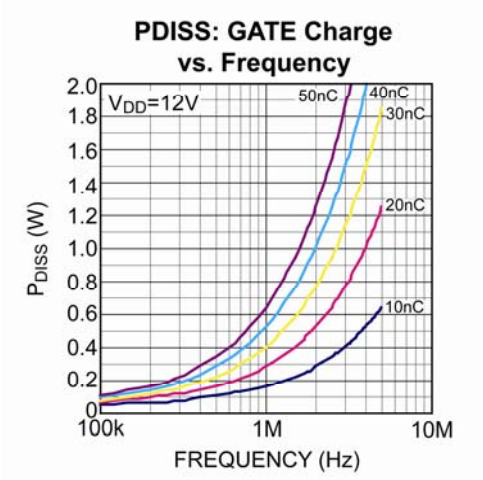


Figure 6B. Driver Power Dissipation

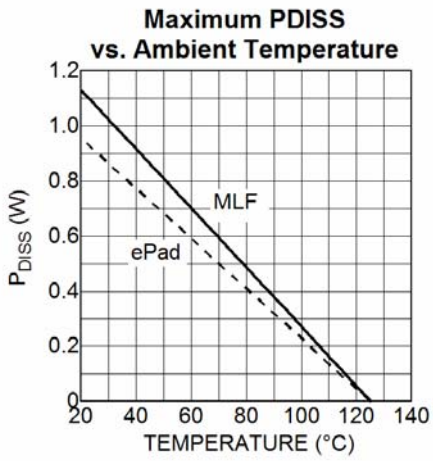


Figure 6C. Maximum Driver Power Dissipation

Propagation Delay and Delay Matching and Other Timing Considerations

Fast propagation delay between the input and output drive waveform is desirable. It improves overcurrent protection by decreasing the response time between the control signal and the MOSFET gate drive. Minimizing propagation delay also minimizes phase shift errors in power supplies with wide bandwidth control loops.

Care must be taken to insure the input signal pulse width is greater than the minimum specified pulse width. An input signal that is less than the minimum pulse width may result in no output pulse or an output pulse whose width is significantly less than the input.

Decoupling and Bootstrap Capacitor Selection

Decoupling capacitors are required for proper operation by supplying the charge necessary to drive the external MOSFETs as well as minimizing the voltage ripple on the supply pins.

Ceramic capacitors are recommended because of their low impedance and small size. Z5U type ceramic capacitor dielectrics are not recommended due to the large change in capacitance over temperature and voltage. A minimum value of 0.1µf is required for each of the capacitors, regardless of the MOSFETs being driven. Larger MOSFETs may require larger capacitance values for proper operation. The voltage rating of the capacitors depends upon the supply voltage, ambient temperature and the voltage derating used for reliability.

Placement of the decoupling capacitors is critical. The bypass capacitor for VDD should be placed as close as possible between the VDD and VSS pins. The etch connections must be short, wide and direct. The use of a ground plane to minimize connection impedance is recommended. Refer to the section on layout and component placement for more information.

Grounding, Component Placement and Circuit Layout

Nanosecond switching speeds and ampere peak currents in and around the MOSFET driver requires proper placement and trace routing of all components. Improper placement may cause degraded noise immunity, false switching and excessive ringing.

Figure 7 shows the critical current paths when the driver outputs go high and turn on the external MOSFETs. It also helps demonstrate the need for a low impedance ground plane. Charge needed to turn-on the MOSFET gates comes from the decoupling capacitors C_{VDD}. Current in the gate driver flows from C_{VDD} through the internal driver, into the MOSFET gate and out the source. The return connection back to the decoupling capacitor is made through the ground plane. Any inductance or resistance in the ground return path causes a voltage spike or ringing to appear on the source of the MOSFET. This voltage works against the gate drive voltage and can either slow down or turn off the MOSFET during the period when it should be turned on.

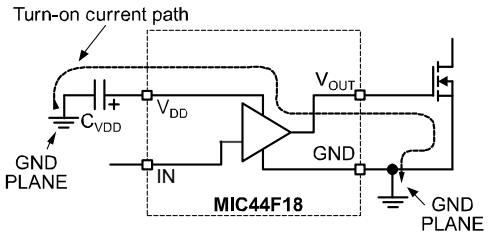


Figure 7. Critical Current Paths for High Driver Outputs

Figure 8 shows the critical current paths when the driver outputs go low and turn off the external MOSFETs. Short, low impedance connections are important during turn-off for the same reasons given in the turn-on explanation. Current from the V_{DD} supply replenishes charge in the decoupling capacitor, C_{Vdd}.

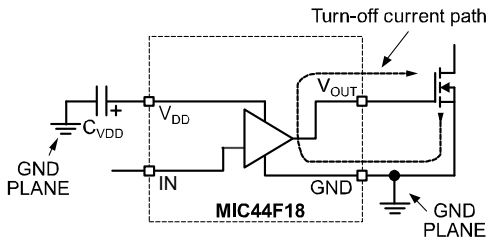
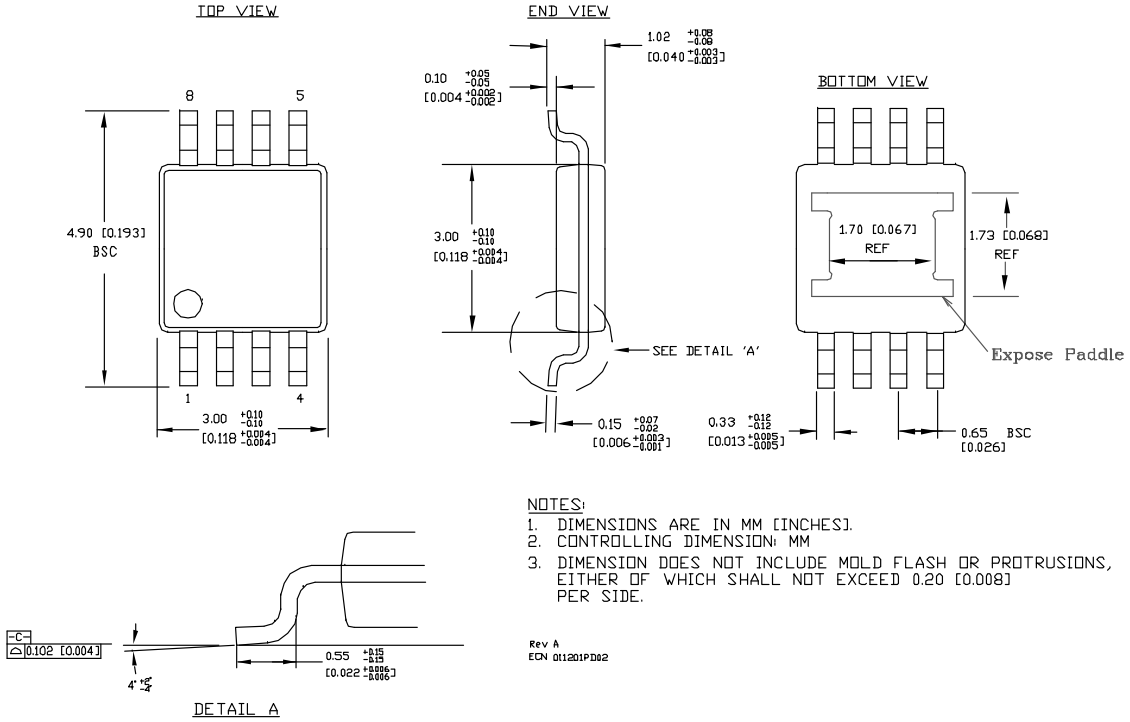


Figure 8. Critical Current Paths for High Driver Outputs

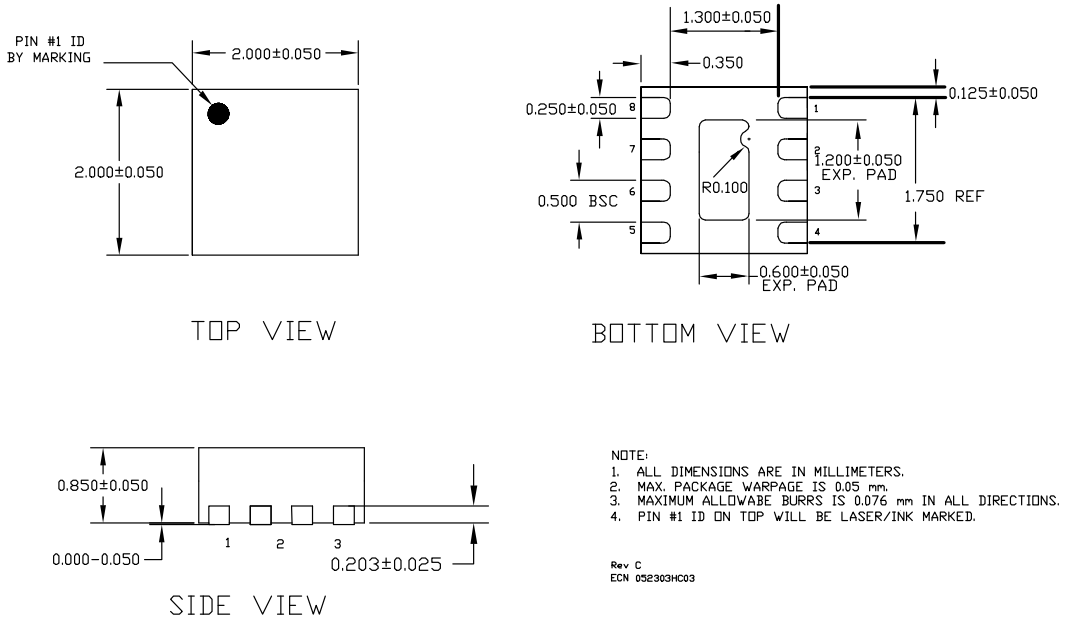
The following circuit guidelines should be adhered to for optimum circuit performance:

1. The V_{CC} bypass capacitor must be placed close to the VDD and ground pins. It is critical that the etch length between the decoupling capacitor and the VDD & GND pins be minimized to reduce pin inductance.
2. A ground plane is recommended to minimize parasitic inductance and impedance of the return paths. The MIC44F18 family of drivers is capable of high peak currents and very fast transition times. Any impedance between the driver, the decoupling capacitors and the external MOSFET will degrade the performance of the circuit.
3. Trace out the high di/dt and dv/dt paths, as shown in Figures 7 and 8 and minimize etch length and loop area for these connections. Minimizing these parameters decreases the parasitic inductance and the radiated EMI generated by fast rise and fall times.

Package Information



8-Pin ePad MSOP (MME)



8-Pin 2mm x 2mm MLF (ML)

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