NOTES:

1.0 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ 6.5V
Current at Analog Input Pins ($V_{IN}+$, $V_{IN}-$) ..... ±2 mA
Analog Inputs ($V_{IN}+$, $V_{IN}-$)†† ..... V_{SS} – 1.0V to V_{DD} + 1.0V
All Other Inputs and Outputs ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Difference Input Voltage ..... $|V_{DD} - V_{SS}|$
Output Short-Circuit Current ..... Continuous
Current at Input Pins ..... ±2 mA
Current at Output and Supply Pins ..... ±30 mA
Storage Temperature ..... -65°C to +150°C
Maximum Junction Temperature (T_J) ..... +150°C
ESD Protection on All Pins (HBM; MM) ..... ≥ 4 kV; 400V
ESD Protection on All Pins (HBM; MM) (Dual and Quad) ..... ≥ 4 kV; 300V

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1.2 “Input Voltage Limits”**.

1.2 Specifications

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A= +25°C, V_{DD} = +1.8V to +5.5V, V_{SS}= GND, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 30 pF (refer to Figure 1-1).						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Input Offset						
Input Offset Voltage	V_{OS}	-1.0	—	1.0	mV	V_{DD} = 3.0V; V_{CM} = V_{DD}/4
Input Offset Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	±3.0	—	µV/°C	T_A= -40°C to +125°C, V_{CM} = V_{SS}
Power Supply Rejection Ratio	PSRR	75	90	—	dB	V_{CM} = V_{SS}
Input Bias Current and Impedance						
Input Bias Current	I_B	—	±1	50	pA	
		—	20	—	pA	T_A = +85°C
		—	800	—	pA	T_A = +125°C
Input Offset Current	I_{OS}	—	±1	—	pA	
Common Mode Input Impedance	Z_{CM}	—	10^{13}||12	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||12	—	Ω||pF	
Common Mode						
Common Mode Input Voltage Range	V_{CMR}	V_{SS} – 0.3	—	V_{DD} + 0.3	V	
Common Mode Rejection Ratio	CMRR	75	90	—	dB	V_{DD} = 5.5V V_{CM} = -0.3V to 5.8V
		70	85	—	dB	V_{DD} = 1.8V V_{CM} = -0.3V to 2.1V

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, T_A= +25°C, V_{DD} = +1.8V to +5.5V, V_{SS}= GND, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 30 pF (refer to Figure 1-1).						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Open-Loop Gain						
DC Open-Loop Gain (Large Signal)	A_{OL}	95	115	—	dB	0.3 < V_{OUT} < (V_{DD} –0.3V) V_{CM}= V_{SS} V_{DD} = 5.5V
Output						
High-Level Output Voltage	V_{OH}	V_{DD} – 4	V_{DD} – 1	—	mV	V_{DD} = 1.8V
		V_{DD} – 5	V_{DD} – 1	—	mV	V_{DD} = 5.5V
Low-Level Output Voltage	V_{OL}	—	V_{SS} + 1	V_{SS} + 4	mV	V_{DD} = 1.8V
		—	V_{SS} + 1	V_{SS} + 5	mV	V_{DD} = 5.5V
Output Short-Circuit Current	I_{SC}	—	±6	—	mA	V_{DD} = 1.8V
		—	±22	—	mA	V_{DD} = 5.5V
Power Supply						
Supply Voltage	V_{DD}	1.8	—	5.5	V	
Quiescent Current per Amplifier	I_Q	3	4.4	5.5	µA	I_O = 0, V_{CM} = V_{DD}/4

TABLE 1-2: AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A= +25°C, V_{DD} = +1.8V to +5.5V, V_{SS}= GND, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 30 pF (refer to Figure 1-1).						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
AC Response						
Gain Bandwidth Product	GBWP	—	90	—	kHz	
Phase Margin	PM	—	55	—	°	G = +1 V/V
Slew Rate	SR	—	0.05	—	V/µs	
Noise						
Input Noise Voltage	E_{ni}	—	15	—	$µV_{P-P}$	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	95	—	nV/√Hz	f = 1 kHz
		—	90	—	nV/√Hz	f = 10 kHz
Input Noise Current Density	i_{ni}	—	0.6	—	fA/√Hz	f = 1 kHz
Electromagnetic Interference Rejection Ratio	EMIRR	—	77	—	dB	V_{IN} = 100 mV_{PK}, 400 MHz
		—	92	—		V_{IN} = 100 mV_{PK}, 900 MHz
		—	97	—		V_{IN} = 100 mV_{PK}, 1800 MHz
		—	99	—		V_{IN} = 100 mV_{PK}, 2400 MHz

TABLE 1-3: TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V and V_{SS} = GND.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SC70	θ_{JA}	—	331	—	°C/W	
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	221	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	211	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	150	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	95	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note 1: The internal junction temperature (T_J) must not exceed the absolute maximum specification of +150°C.

1.3 Test Circuits

The circuit used for most DC and AC tests is shown in Figure 1-1. This circuit can independently set V_{CM} and V_{OUT} (see Equation 1-1). Note that V_{CM} is not the circuit's Common mode voltage ((V_P + V_M)/2), and that V_{OST} includes V_{OS} plus the effects (on the input offset error, V_{OST}) of the temperature, CMRR, PSRR and A_{OL}.

EQUATION 1-1:

$$G_{DM} = R_F / R_G$$
$$V_{CM} = (V_P + V_{DD}/2)/2$$
$$V_{OST} = V_{IN-} - V_{IN+}$$
$$V_{OUT} = (V_{DD}/2) + (V_P - V_M) + V_{OST}(1 + G_{DM})$$

Where:

G_{DM}	= Differential Mode Gain	(V/V)
V_{CM}	= Op Amp's Common Mode Input Voltage	(V)
V_{OST}	= Op Amp's Total Input Offset Voltage	(mV)

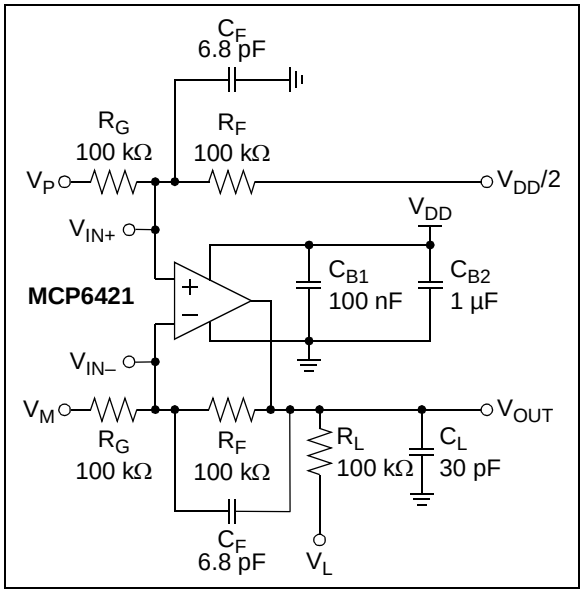


FIGURE 1-1: *AC and DC Test Circuit for Most Specifications.*

NOTES:

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A= +25°C, V_{DD} = +1.8V to +5.5V, V_{SS}= GND, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 30 pF.

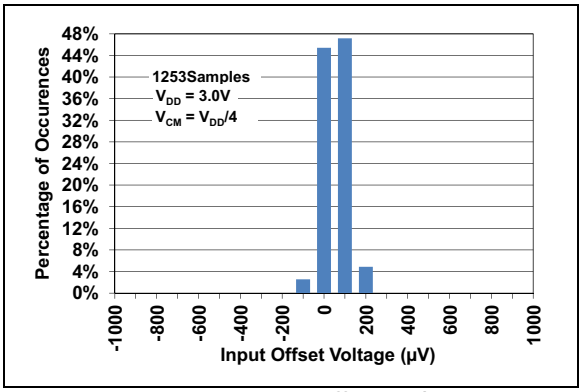


FIGURE 2-1: *Input Offset Voltage.*

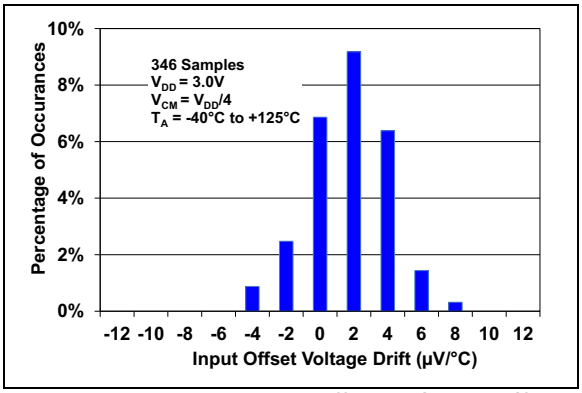


FIGURE 2-2: *Input Offset Voltage Drift.*

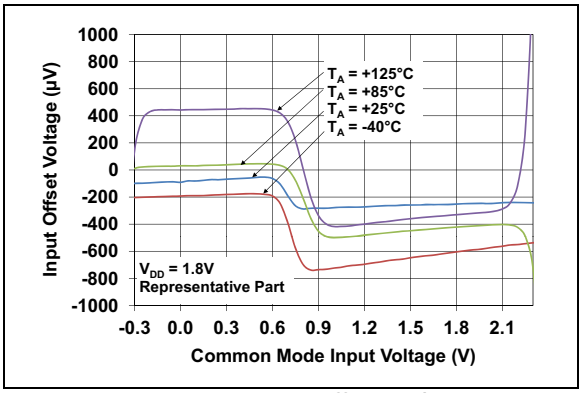


FIGURE 2-3: *Input Offset Voltage vs. Common Mode Input Voltage.*

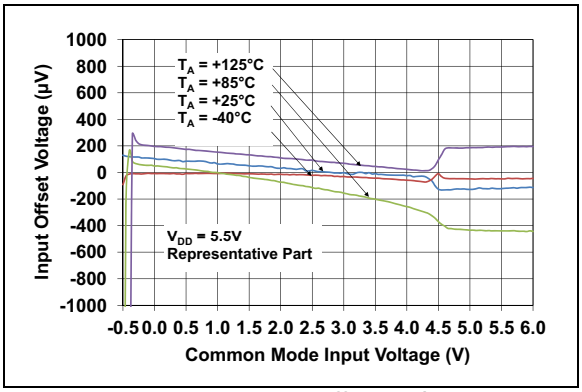


FIGURE 2-4: *Input Offset Voltage vs. Common Mode Input Voltage.*

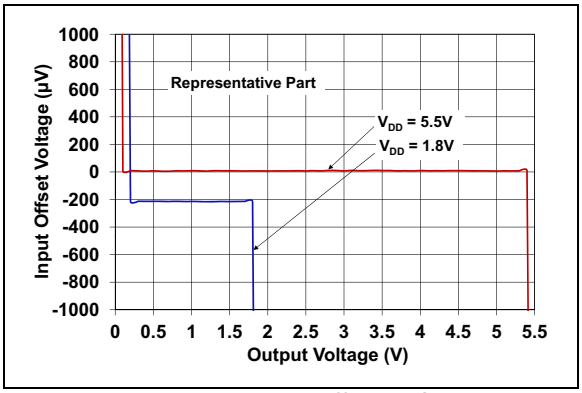


FIGURE 2-5: *Input Offset Voltage vs. Output Voltage.*

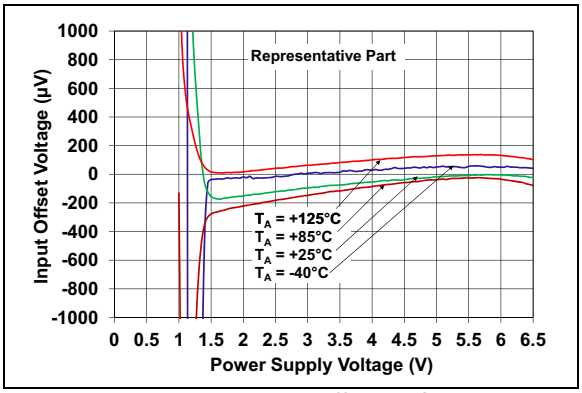


FIGURE 2-6: *Input Offset Voltage vs. Power Supply Voltage.*

Note: Unless otherwise indicated, T_A= +25°C, V_{DD} = +1.8V to +5.5V, V_{SS}= GND, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 30 pF.

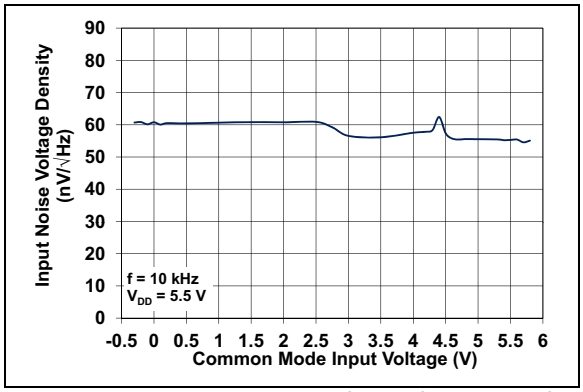


FIGURE 2-7: *Input Noise Voltage Density vs. Common Mode Input Voltage.*

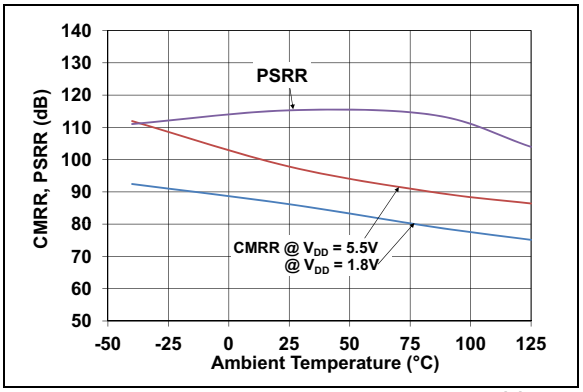


FIGURE 2-10: *CMRR, PSRR vs. Ambient Temperature.*

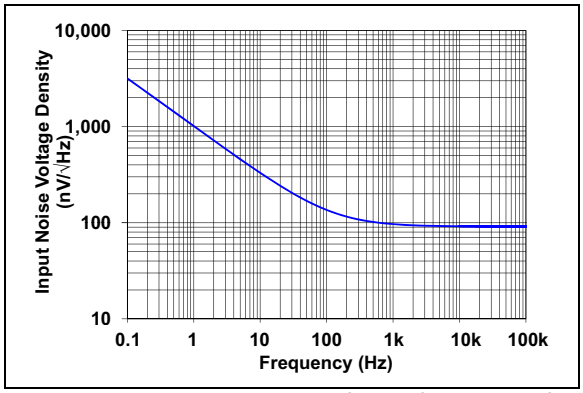


FIGURE 2-8: *Input Noise Voltage Density vs. Frequency.*

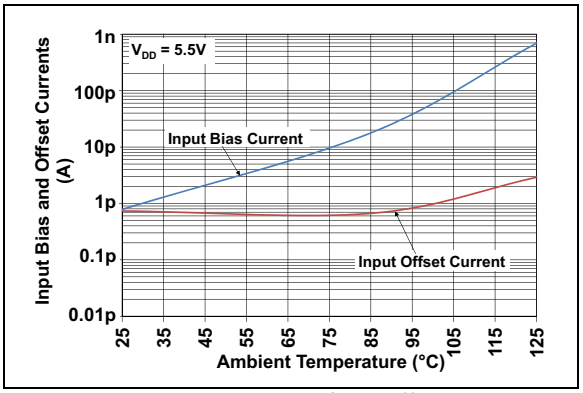


FIGURE 2-11: *Input Bias, Offset Current vs. Ambient Temperature.*

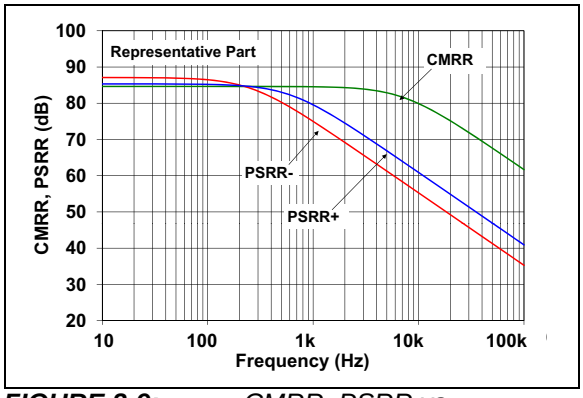


FIGURE 2-9: *CMRR, PSRR vs. Frequency.*

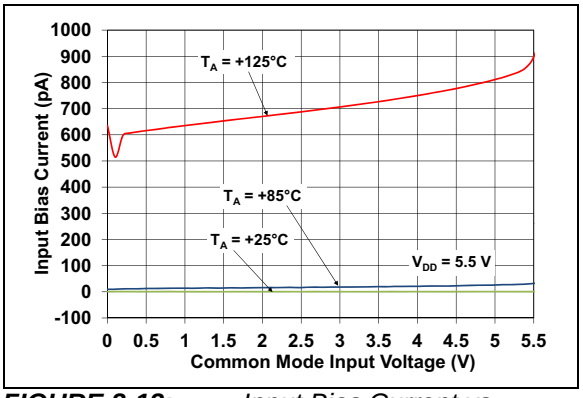


FIGURE 2-12: *Input Bias Current vs. Common Mode Input Voltage.*

Note: Unless otherwise indicated, T_A= +25°C, V_{DD} = +1.8V to +5.5V, V_{SS}= GND, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 30 pF.

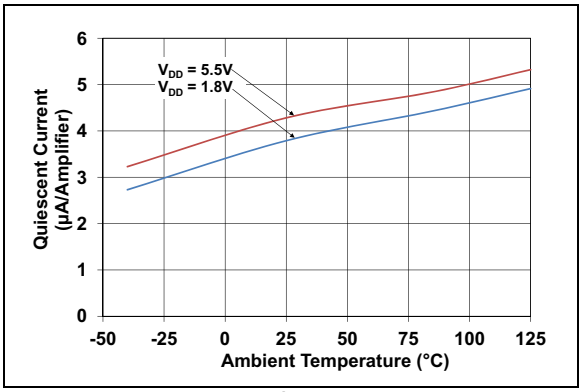


FIGURE 2-13: *Quiescent Current vs. Ambient Temperature.*

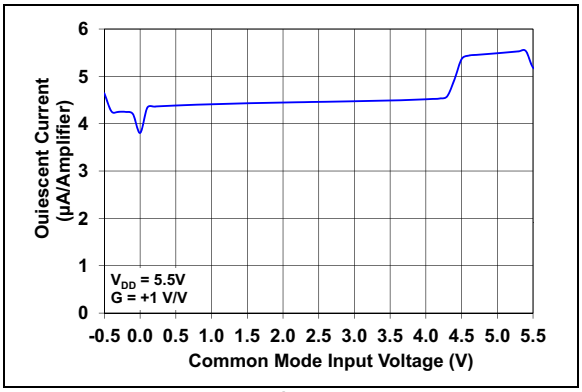


FIGURE 2-16: *Quiescent Current vs. Common Mode Input Voltage.*

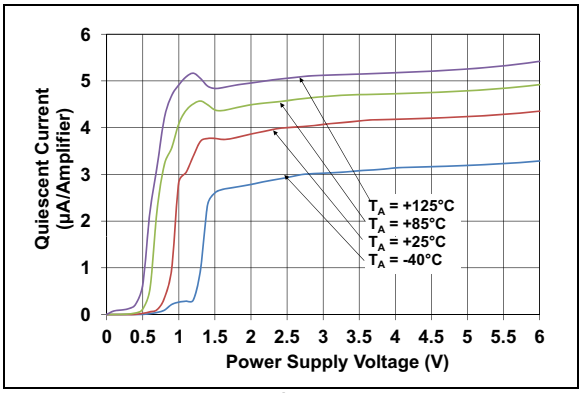


FIGURE 2-14: *Quiescent Current vs. Power Supply Voltage.*

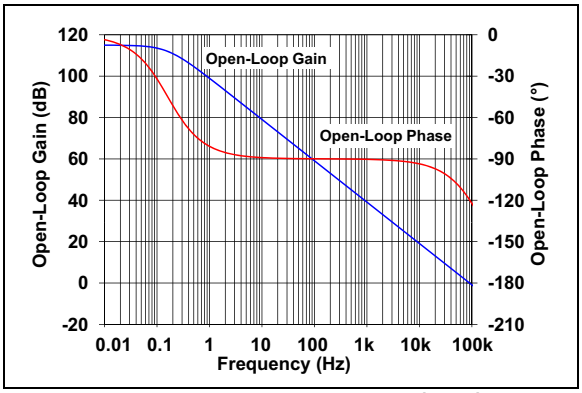


FIGURE 2-17: *Open-Loop Gain, Phase vs. Frequency.*

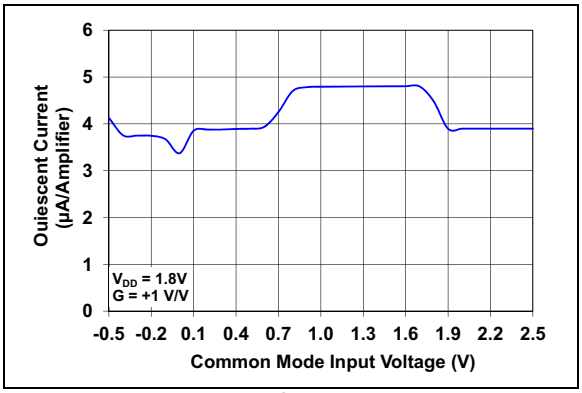


FIGURE 2-15: *Quiescent Current vs. Common Mode Input Voltage.*

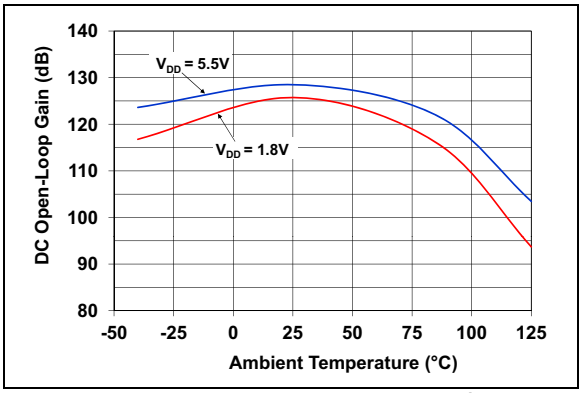


FIGURE 2-18: *DC Open-Loop Gain vs. Ambient Temperature.*

Note: Unless otherwise indicated, T_A= +25°C, V_{DD} = +1.8V to +5.5V, V_{SS}= GND, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 30 pF.

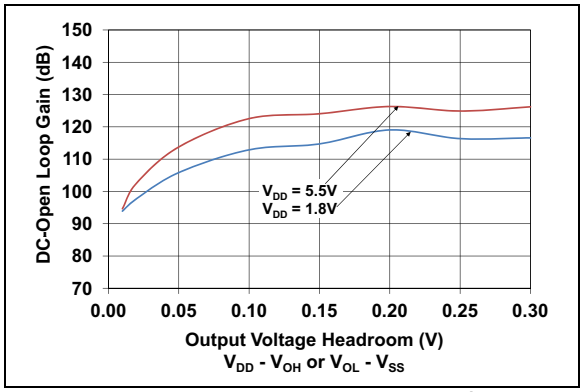


FIGURE 2-19: *DC Open-Loop Gain vs. Output Voltage Headroom.*

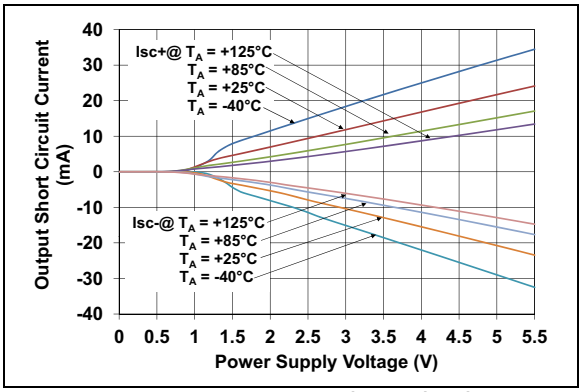


FIGURE 2-22: *Output Short Circuit Current vs. Power Supply Voltage.*

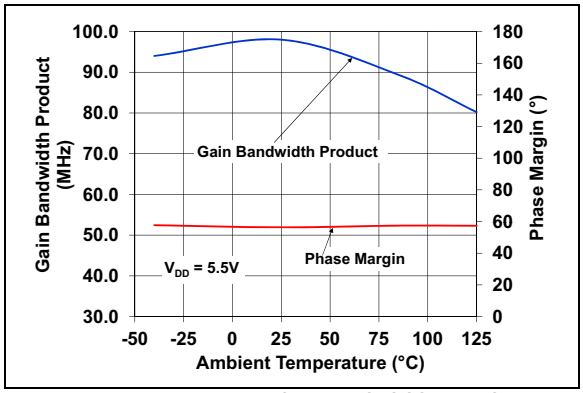


FIGURE 2-20: *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature.*

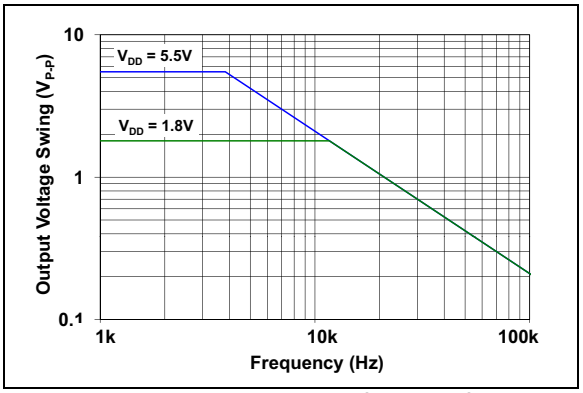


FIGURE 2-23: *Output Voltage Swing vs. Frequency.*

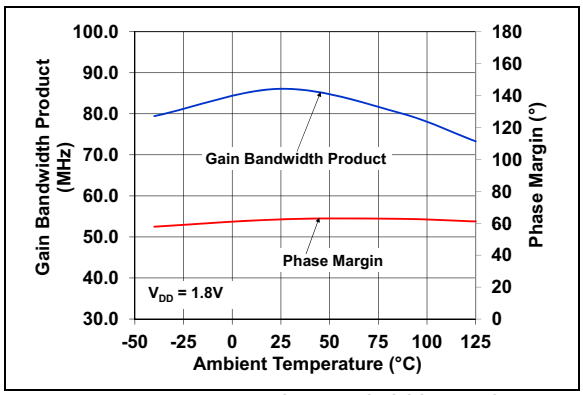


FIGURE 2-21: *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature.*

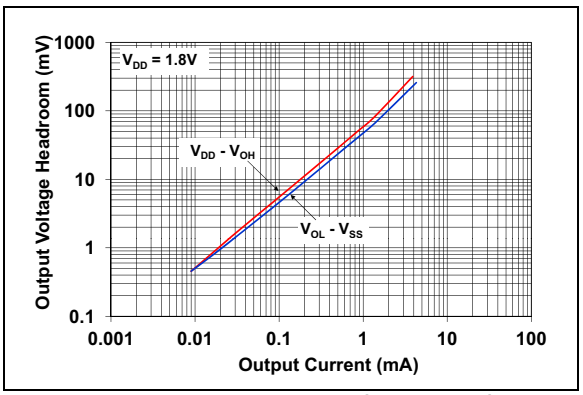


FIGURE 2-24: *Output Voltage Headroom vs. Output Current.*

Note: Unless otherwise indicated, T_A= +25°C, V_{DD} = +1.8V to +5.5V, V_{SS}= GND, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 30 pF.

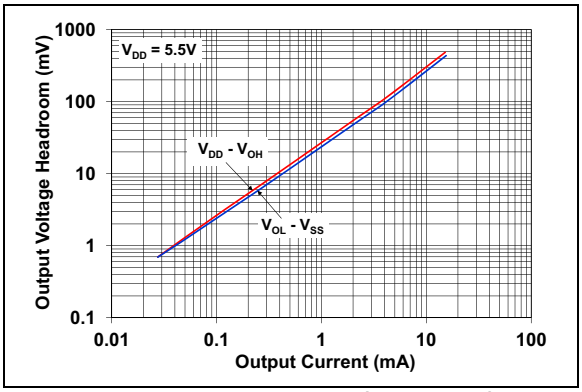


FIGURE 2-25: *Output Voltage Headroom vs. Output Current.*

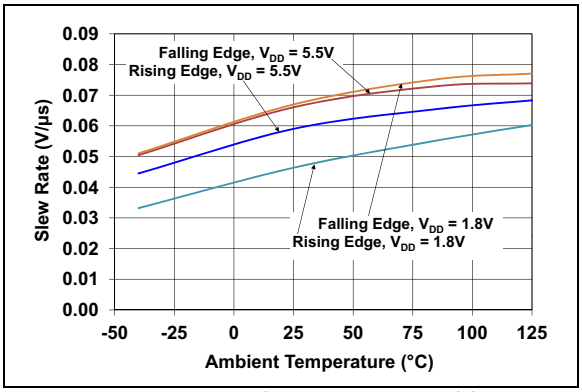


FIGURE 2-28: *Slew Rate vs. Ambient Temperature.*

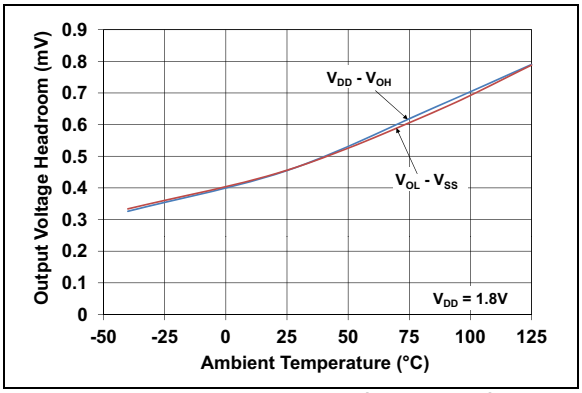


FIGURE 2-26: *Output Voltage Headroom vs. Ambient Temperature.*

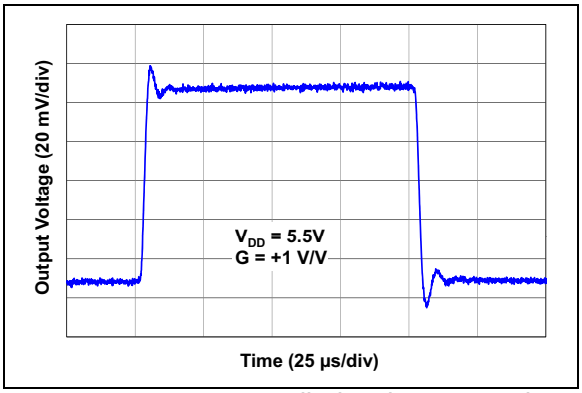


FIGURE 2-29: *Small Signal Non-Inverting Pulse Response.*

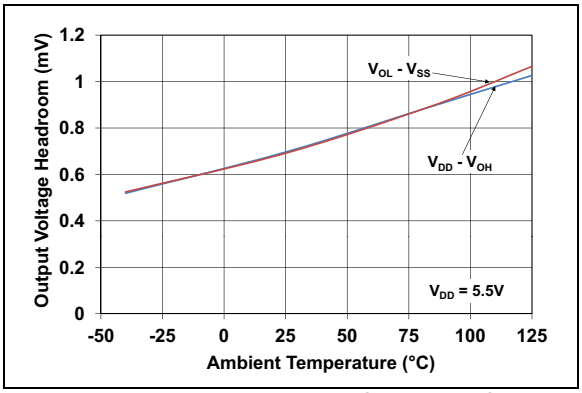


FIGURE 2-27: *Output Voltage Headroom vs. Ambient Temperature.*

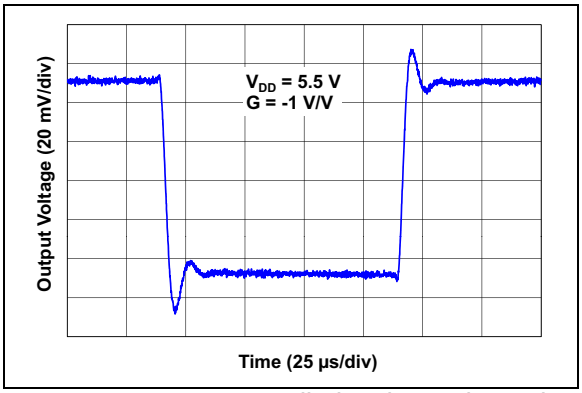


FIGURE 2-30: *Small Signal Inverting Pulse Response.*

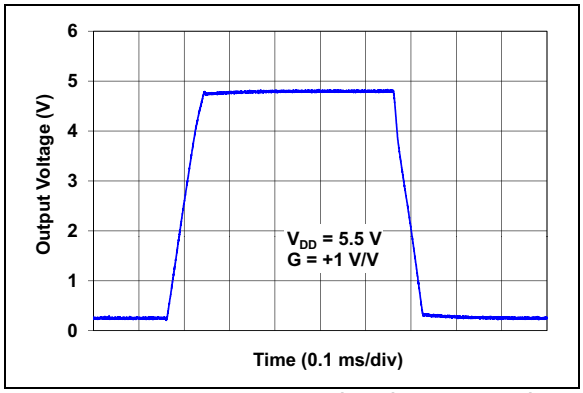


FIGURE 2-31: *Large Signal Non-Inverting Pulse Response.*

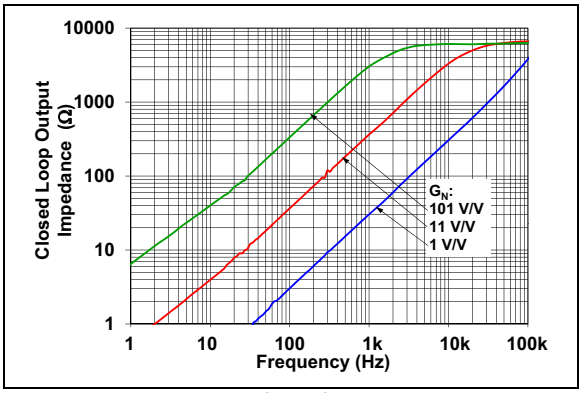


FIGURE 2-34: *Closed Loop Output Impedance vs. Frequency.*

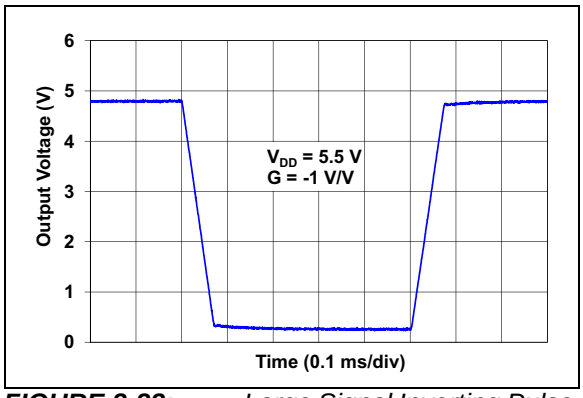


FIGURE 2-32: *Large Signal Inverting Pulse Response.*

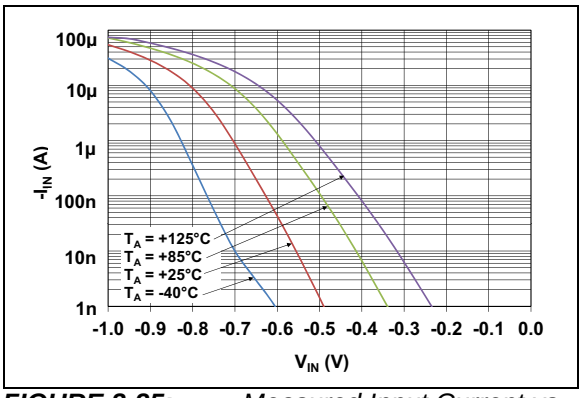


FIGURE 2-35: *Measured Input Current vs. Input Voltage (below V_{SS}).*

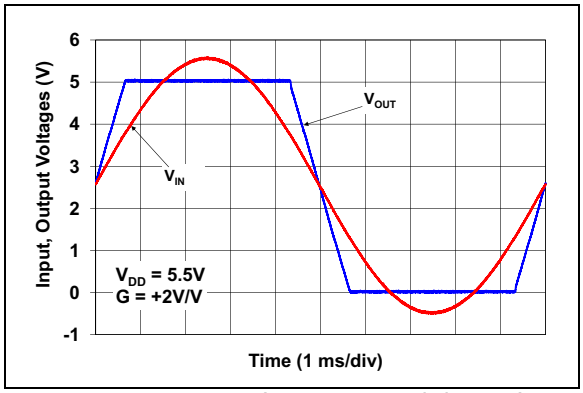


FIGURE 2-33: *The MCP6421/2/4 Device Shows No Phase Reversal.*

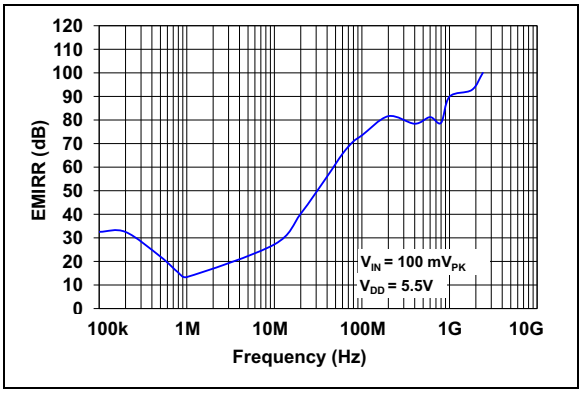


FIGURE 2-36: *EMIRR vs. Frequency.*

Note: Unless otherwise indicated, T_A= +25°C, V_{DD} = +1.8V to +5.5V, V_{SS}= GND, V_{CM} = V_{DD}/2, V_{OUT} = V_{DD}/2, V_L = V_{DD}/2, R_L = 100 kΩ to V_L and C_L = 30 pF.

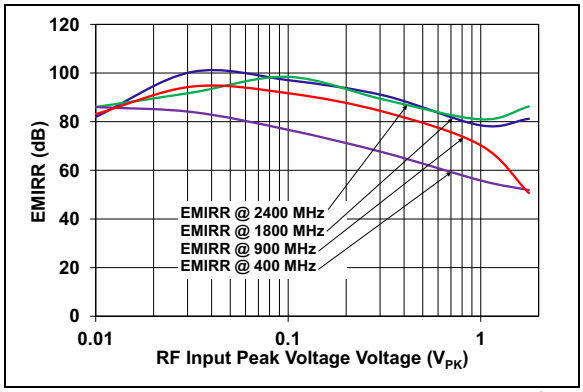


FIGURE 2-37: *EMIRR vs. RF Input Peak-to-Peak Voltage.*

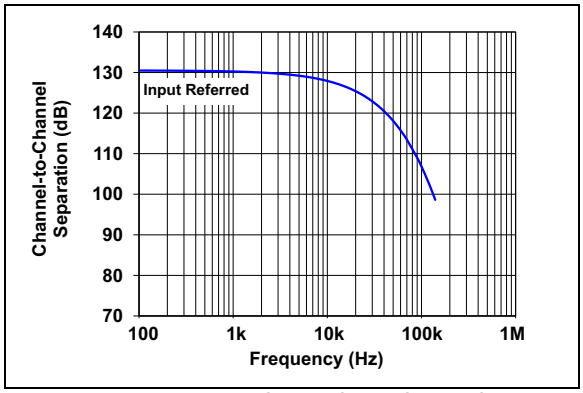


FIGURE 2-38: *Channel-to-Channel Separation vs. Frequency.*

NOTES:

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP6421	MCP6422	MCP6424	Symbol	Description
SC70-5, SOT-23-5	MSOP, SOIC	SOIC, TSSOP		
1	1	1	V_{OUT}, V_{OUTA}	Analog Output (op amp A)
4	2	2	$V_{IN}-$, $V_{INA}-$	Inverting Input (op amp A)
3	3	3	$V_{IN}+$, $V_{INA}+$	Non-inverting Input (op amp A)
5	8	4	V_{DD}	Positive Power Supply
—	5	5	$V_{INB}+$	Non-inverting Input (op amp B)
—	6	6	$V_{INB}-$	Inverting Input (op amp B)
—	7	7	V_{OUTB}	Analog Output (op amp B)
—	—	8	V_{OUTC}	Analog Output (op amp C)
—	—	9	$V_{INC}-$	Inverting Input (op amp C)
—	—	10	$V_{INC}+$	Non-inverting Input (op amp C)
2	4	11	V_{SS}	Negative Power Supply
—	—	12	$V_{IND}+$	Non-inverting Input (op amp D)
—	—	13	$V_{IND}-$	Inverting Input (op amp D)
—	—	14	V_{OUTD}	Analog Output (op amp D)

3.1 Analog Outputs

The output pin is a low-impedance voltage source.

3.2 Analog Inputs

The non-inverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.3 Power Supply Pins (V_{SS}, V_{DD})

The positive power supply (V_{DD}) is 1.8V to 5.5V higher than the negative power supply (V_{SS}). For normal operation, the other pins are at voltages between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need bypass capacitors.

NOTES:

4.0 APPLICATION INFORMATION

The MCP6421/2/4 op amps are manufactured using Microchip's state-of-the-art CMOS process. This op amp is unity gain stable and suitable for a wide range of general purpose applications.

4.1 Rail-to-Rail Input

4.1.1 PHASE REVERSAL

The MCP6421/2/4 op amps are designed to prevent phase reversal, when the input pins exceed the supply voltages. Figure 2-33 shows the input voltage exceeding the supply voltage with no phase reversal.

4.1.2 INPUT VOLTAGE LIMITS

In order to prevent damage and/or improper operation of the amplifier, the circuit must limit the voltages at the input pins (see **Section 1.1, Absolute Maximum Ratings †**).

The Electrostatic Discharge (ESD) protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors against many, but not all, over-voltage conditions, and to minimize the input bias current (I_B).

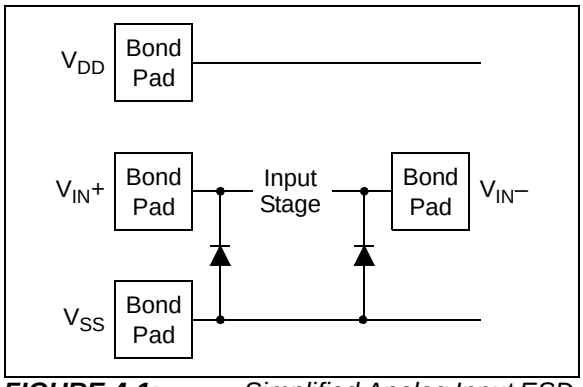


FIGURE 4-1: *Simplified Analog Input ESD Structures.*

The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS}. They also clamp any voltages that go well above V_{DD}; their breakdown voltage is high enough to allow normal operation, but not low enough to protect against slow over-voltage (beyond V_{DD}) events. Very fast ESD events that meet the spec are limited so that damage does not occur.

In some applications, it may be necessary to prevent excessive voltages from reaching the op amp inputs; Figure 4-2 shows one approach to protecting these inputs.

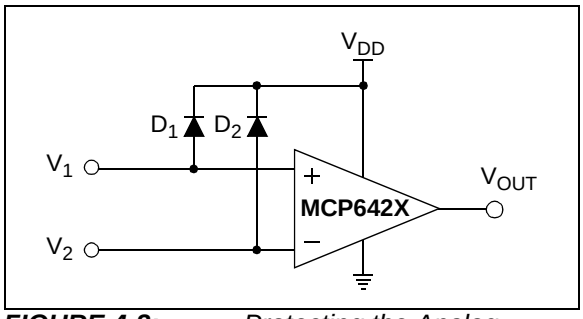


FIGURE 4-2: *Protecting the Analog Inputs.*

A significant amount of current can flow out of the inputs when the Common mode voltage (V_{CM}) is below ground (V_{SS}); see Figure 2-35.

4.1.3 INPUT CURRENT LIMITS

In order to prevent damage and/or improper operation of the amplifier, the circuit must limit the currents into the input pins (see **Section 1.1, Absolute Maximum Ratings †**).

Figure 4-3 shows one approach to protecting these inputs. The resistors R_1 and R_2 limit the possible currents in or out of the input pins (and the ESD diodes, D_1 and D_2). The diode currents will go through either V_{DD} or V_{SS}.

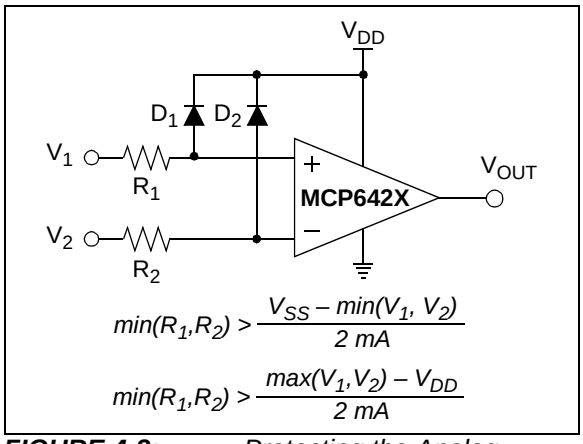


FIGURE 4-3: *Protecting the Analog Inputs.*

4.1.4 NORMAL OPERATION

The input stage of the MCP6421/2/4 op amps uses two differential input stages in parallel. One operates at a low Common mode input voltage (V_{CM}), while the other operates at a high V_{CM}. With this topology, the device operates with a V_{CM} up to 300 mV above V_{DD} and 300 mV below V_{SS}. The input offset voltage is measured at $V_{CM} = V_{SS} - 0.3V$ and $V_{DD} + 0.3V$, to ensure proper operation.

The transition between the input stages occurs when V_{CM} is near $V_{DD} - 0.6V$ (see Figures 2-3 and 2-4). For the best distortion performance and gain linearity, with non-inverting gains, avoid this region of operation.

4.2 Rail-to-Rail Output

The output voltage range of the MCP6421/2/4 op amps is 0.001V (typical) and 5.499V (typical) when R_L = 100 kΩ is connected to $V_{DD}/2$ and V_{DD} = 5.5V. Refer to Figures 2-24 and 2-26 for more information.

4.3 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases, and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. While a unity-gain buffer (G = +1 V/V) is the most sensitive to the capacitive loads, all gains show the same general behavior.

When driving large capacitive loads with the MCP6421/2/4 op amps (e.g., > 60 pF when G = +1 V/V), a small series resistor at the output (R_{ISO} in Figure 4-5) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitance load.

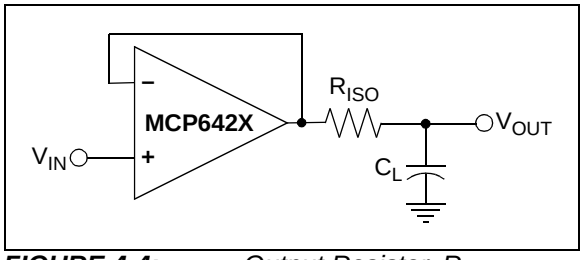


FIGURE 4-4: *Output Resistor, R_{ISO} Stabilizes Large Capacitive Loads.*

Figure 4-5 gives the recommended R_{ISO} values for the different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the circuit's noise gain. For non-inverting gains, G_N and the Signal Gain are equal. For inverting gains, G_N is 1+|Signal Gain| (e.g., -1 V/V gives G_N = +2 V/V).

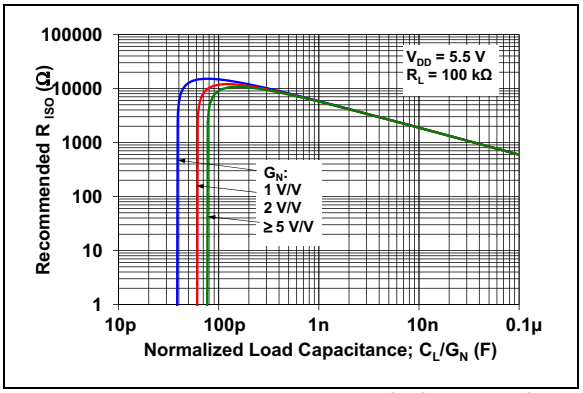


FIGURE 4-5: *Recommended R_{ISO} Values for Capacitive Loads.*

After selecting R_{ISO} for your circuit, double-check the resulting frequency response peaking and step response overshoot. Modify R_{ISO}'s value until the response is reasonable. Bench evaluation and simulations with the MCP6421/2/4 SPICE macro model are very helpful.

4.4 Supply Bypass

The MCP6421/2/4 op amps' power supply pin (V_{DD} for single-supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high frequency performance. It can use a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

4.5 Unused Op Amps

An unused op amp in a quad package (MCP6424) should be configured as shown in Figure 4-6. These circuits prevent the output from toggling and causing crosstalk. Circuit A sets the op amp at its minimum noise gain. The resistor divider produces any desired reference voltage within the output voltage range of the op amp, and the op amp buffers that reference voltage.

Circuit B uses the minimum number of components and operates as a comparator, but it may draw more current.

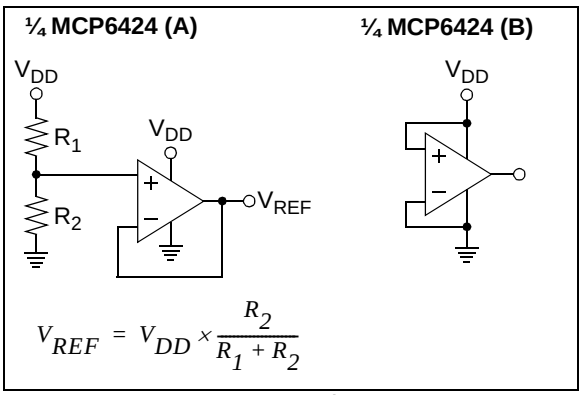


FIGURE 4-6: *Unused Op Amps.*

4.6 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow, which is greater than the MCP6421/2/4 family's bias current at +25°C (±1 pA, typical).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-7.

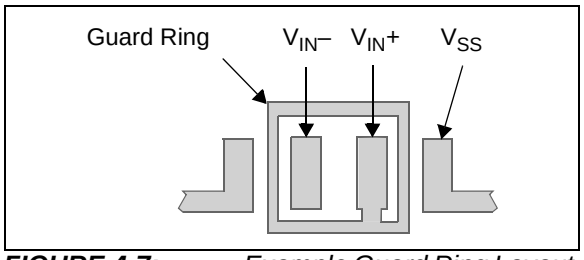


FIGURE 4-7: *Example Guard Ring Layout for Inverting Gain.*

1. Non-inverting Gain and Unity-Gain Buffer:
   a) Connect the non-inverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
   b) Connect the guard ring to the inverting input pin (V_{IN}–). This biases the guard ring to the Common mode input voltage.
2. Inverting Gain and Transimpedance Gain Amplifiers (convert current to voltage, such as photo detectors):
   a) Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the op amp (e.g., $V_{DD}/2$ or ground).
   b) Connect the inverting pin (V_{IN}–) to the input with a wire that does not touch the PCB surface.

4.7 Electromagnetic Interference Rejection Ratio (EMIRR) Definitions

The electromagnetic interference (EMI) is the disturbance that affects an electrical circuit due to either electromagnetic induction or electromagnetic radiation emitted from an external source.

The parameter which describes the EMI robustness of an op amp is the Electromagnetic Interference Rejection Ratio (EMIRR). It quantitatively describes the effect that an RF interfering signal has on op amp performance. Internal passive filters make EMIRR better compared with older parts. This means that, with good PCB layout techniques, your EMC performance should be better.

EMIRR is defined as:

EQUATION 4-1:

$$EMIRR(dB) = 20 \bullet log\left(\frac{V_{RF}}{\Delta V_{OS}}\right)$$

Where:

V_{RF} = Peak Amplitude of RF Interfering Signal (V_{PK})

ΔV_{OS} = Input Offset Voltage Shift (V)

4.8 Application Circuits

4.8.1 CARBON MONOXIDE GAS SENSOR

A carbon monoxide (CO) gas detector is a device which detects the presence of carbon monoxide gas level. Usually this is battery powered and transmits audible and visible warnings.

The sensor responds to CO gas by reducing its resistance proportionaly to the amount of CO present in the air exposed to the internal element. On the sensor module, this variable is part of a voltage divider formed by the internal element and potentiometer R_1. The output of this voltage divider is fed into the non-inverting inputs of the MCP6421 op amp. The device is configured as a buffer with unity gain and is used to provide a non-loaded test point for sensor sensitivity.

Because this sensor can be corrupted by parasitic electromagnetic signals, the MCP6421 op amp can be used for conditioning this sensor.

In Figure 4-8, the variable resistor is used to calibrate the sensor in different environments.

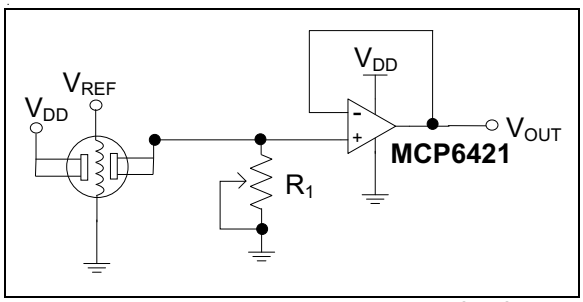


FIGURE 4-8: *CO Gas Sensor Circuit.*

4.8.2 PRESSURE SENSOR AMPLIFIER

The MCP6421/2/4 op amps are well suited for conditioning sensor signals in battery-powered applications. Many sensors are configured as Wheatstone bridges. Strain gauges and pressure sensors are two common examples.

Figure 4-9 shows a strain gauge amplifier, using the MCP6421/2/4 Enhanced EMI protection device. The difference amplifier with EMI robustness op amp is used to amplify the signal from the Wheatstone bridge. The two op amps, configured as buffers and connected at outputs of pressure sensors, prevents resistive loading of the bridge by resistor R1 and R2. Resistors R_1,R_2 and R_3,R_5 need to be chosen with very low tolerance to match the CMRR.

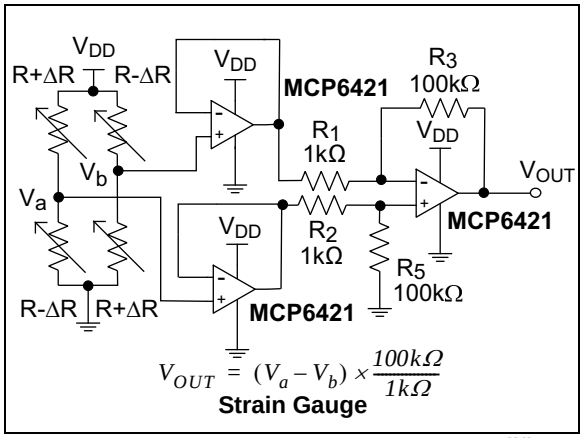


FIGURE 4-9: *Pressure Sensor Amplifier.*

4.8.3 BATTERY CURRENT SENSING

The MCP6421/2/4 op amps' Common Mode Input Range, which goes 0.3V beyond both supply rails, supports their use in high-side and low-side battery current sensing applications. The low quiescent current helps prolong battery life, and the rail-to-rail output supports detection of low currents.

Figure 4-10 shows a high side battery current sensor circuit. The 10Ω resistor is sized to minimize power losses. The battery current (I_{DD}) through the 10Ω resistor causes its top terminal to be more negative than the bottom terminal. This keeps the Common mode input voltage of the op amp below V_{DD}, which is within its allowed range. The output of the op amp will also be below V_{DD}, within its Maximum Output Voltage Swing specification.

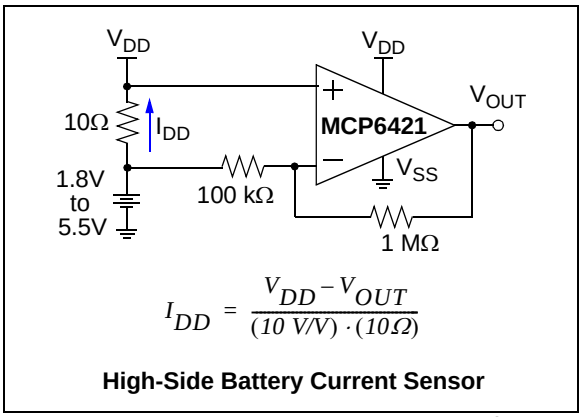


FIGURE 4-10: *Battery Current Sensing.*

5.0 DESIGN AIDS

Microchip provides the basic design tools needed for the MCP6421/2/4 op amps.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP6421/2/4 op amp is available on the Microchip web site at www.microchip.com. The model was written and tested in the official OrCAD (Cadence®) owned PSpice®. For the other simulators, translation may be required.

The model covers a wide aspect of the op amp's electrical specifications. Not only does the model cover voltage, current and resistance of the op amp, but it also covers the temperature and the noise effects on the behavior of the op amp. The model has not been verified outside of the specification range listed in the op amp data sheet. The model behaviors under these conditions cannot ensure it will match the actual op amp performance.

Moreover, the model is intended to be an initial design tool. Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

5.2 FilterLab® Software

Microchip's FilterLab software is an innovative software tool that simplifies analog active filter design using op amps. Available at no cost from the Microchip web site at www.microchip.com/filterlab, the FilterLab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate the actual filter performance.

5.3 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps semiconductor professionals efficiently identify the Microchip devices that fit a particular design requirement. Available at no cost from the Microchip website at www.microchip.com/ maps, the MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool, you can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for data sheets, purchase and sampling of Microchip parts.

5.4 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip web site at www.microchip.com/analogtools.

Some boards that are especially useful are:

- MCP6XXX Amplifier Evaluation Board 1
- MCP6XXX Amplifier Evaluation Board 2
- MCP6XXX Amplifier Evaluation Board 3
- MCP6XXX Amplifier Evaluation Board 4
- Active Filter Demo Board Kit
- 5/6-Pin SOT-23 Evaluation Board, P/N VSUPEV2

5.5 Application Notes

The following Microchip Analog Design Note and Application Notes are available on the Microchip web site at www.microchip.com/appnotes, and are recommended as supplemental reference resources.

- **ADN003 –** *"Select the Right Operational Amplifier for your Filtering Circuits",* DS21821
- **AN722 –** *"Operational Amplifier Topologies and DC Specifications",* DS00722
- **AN723 –** *"Operational Amplifier AC Specifications and Applications",* DS00723
- **AN884 –** *"Driving Capacitive Loads With Op Amps",* DS00884
- **AN990 –** *"Analog Sensor Conditioning Circuits – An Overview",* DS00990
- **AN1177 –** *"Op Amp Precision Design: DC Errors",* DS01177
- **AN1228 –** *"Op Amp Precision Design: Random Noise",* DS01228
- **AN1297 –** *"Microchip's Op Amp SPICE Macro Models",* DS01297
- **AN1332:** *"Current Sensing Circuit Concepts and Fundamentals"'* DS01332
- **AN1494:** *"Using MCP6491 Op Amps for Photodetection Applications"'* DS01494

These application notes and others are listed in the design guide:

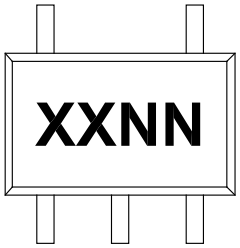
- *"Signal Chain Design Guide",* DS21825

NOTES:

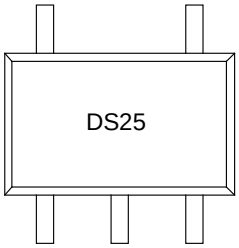
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

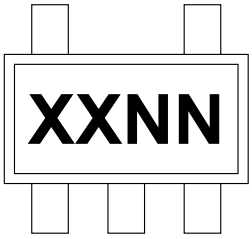
5-Lead SC70 **(MCP6421 only)**



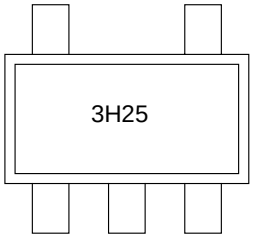
Example:



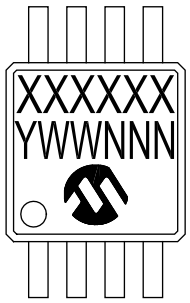
5-Lead SOT-23 **(MCP6421 only)**



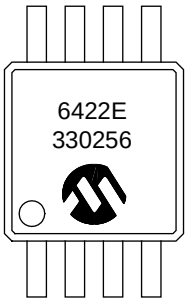
Example:



8-Lead MSOP (3x3 mm) **(MCP6422 only)**



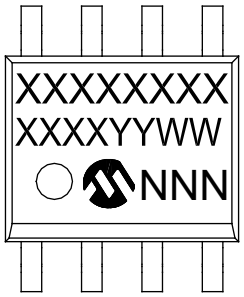
Example



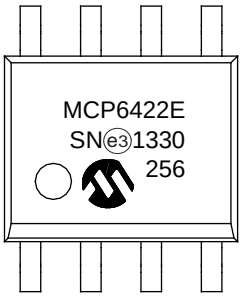
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

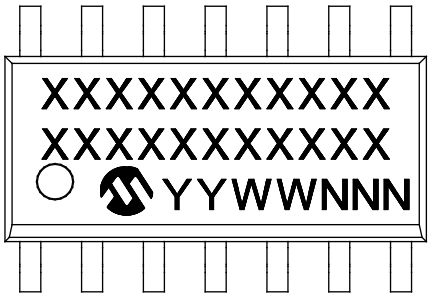
8-Lead SOIC (150 mil.) **(MCP6422 only)**



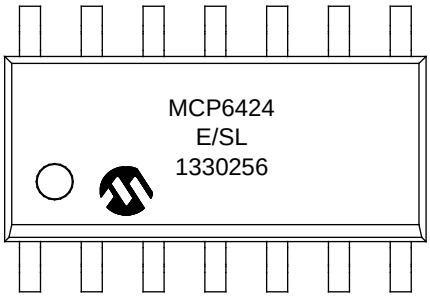
Example



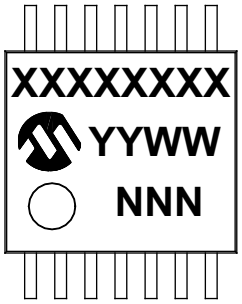
14-Lead SOIC (3.90 mm) **(MCP6424 only)**



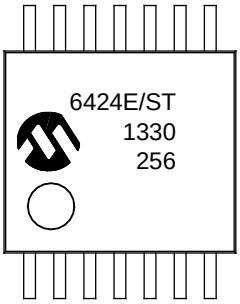
Example



14-Lead TSSOP (4.4 mm) **(MCP6424 only)**

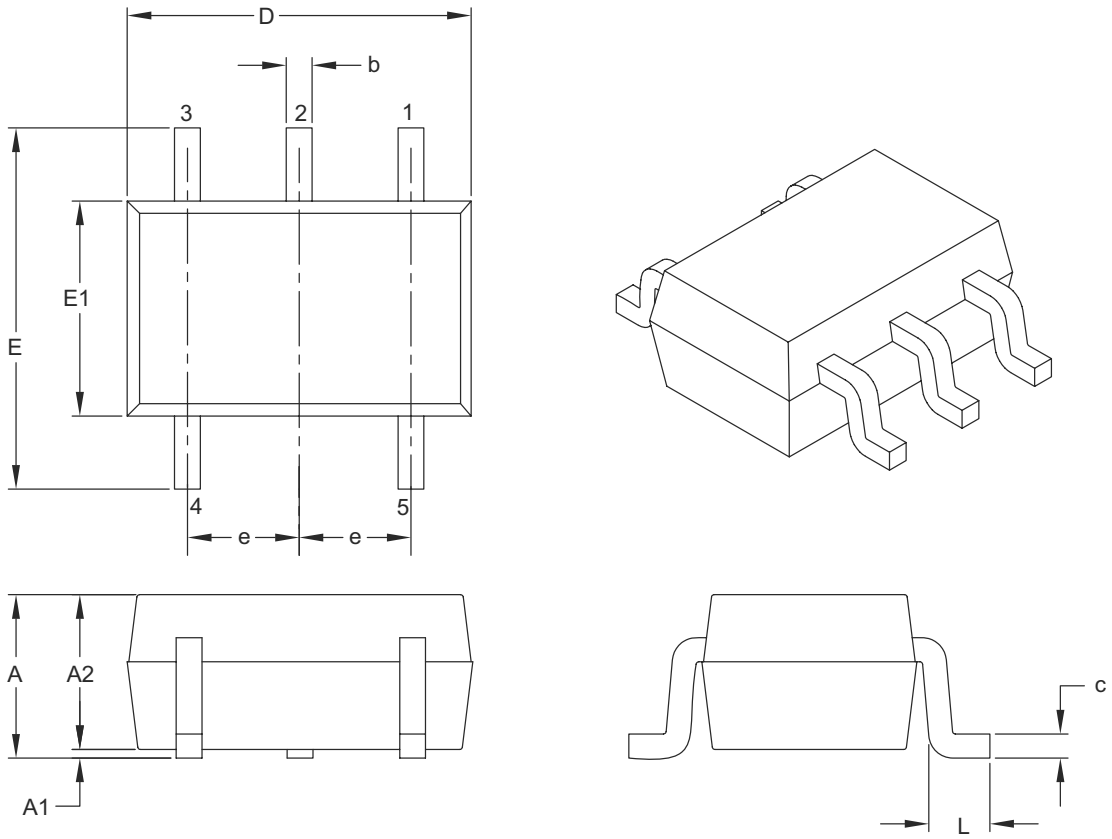


Example



5-Lead Plastic Small Outine Transistor (LTY) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	–	1.10
Molded Package Thickness	A2	0.80	–	1.00
Standoff	A1	0.00	–	0.10
Overall Width	E	1.80	2.10	2.40
Molded Package Width	E1	1.15	1.25	1.35
Overall Length	D	1.80	2.00	2.25
Foot Length	L	0.10	0.20	0.46
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.15	–	0.40

Notes:

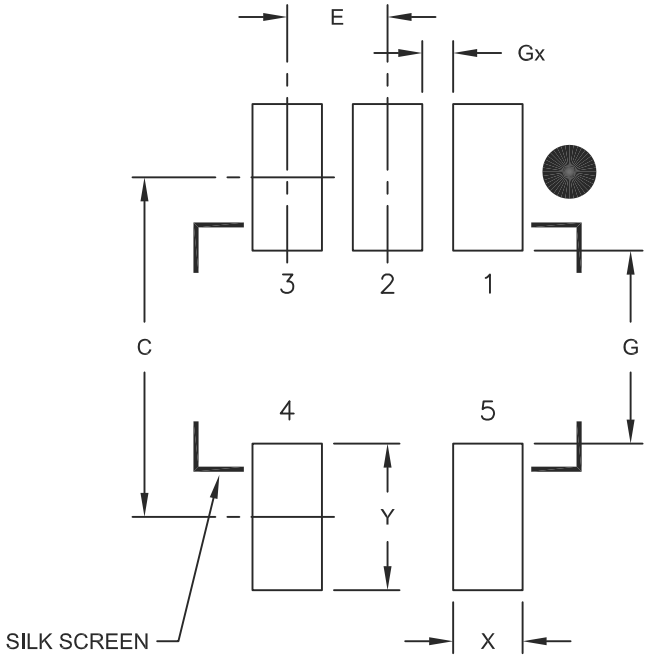
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-061B

5-Lead Plastic Small Outine Transistor (LTY) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		2.20	
Contact Pad Width	X			0.45
Contact Pad Length	Y			0.95
Distance Between Pads	G	1.25		
Distance Between Pads	Gx	0.20		

Notes:

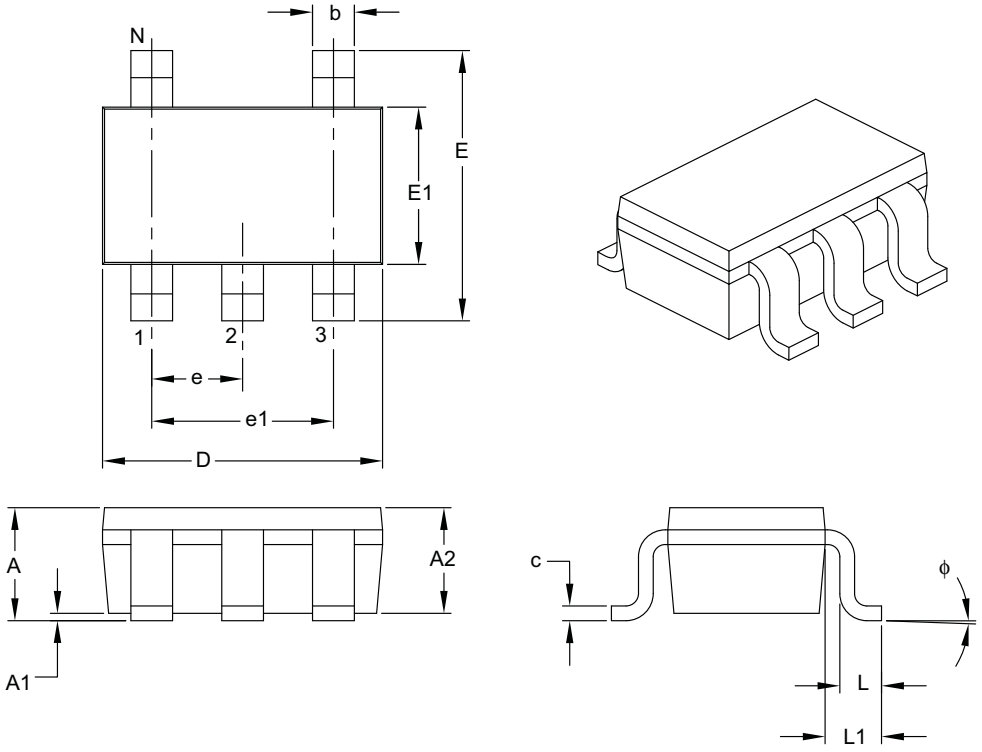
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2061A

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Lead Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

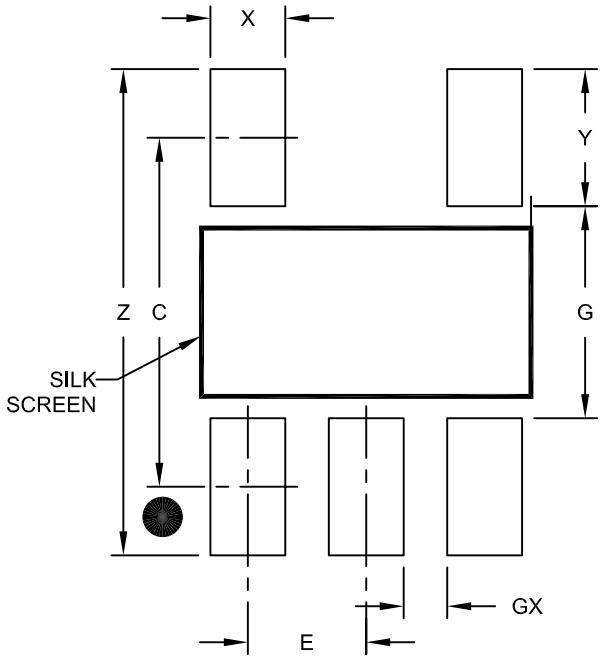
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-091B

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

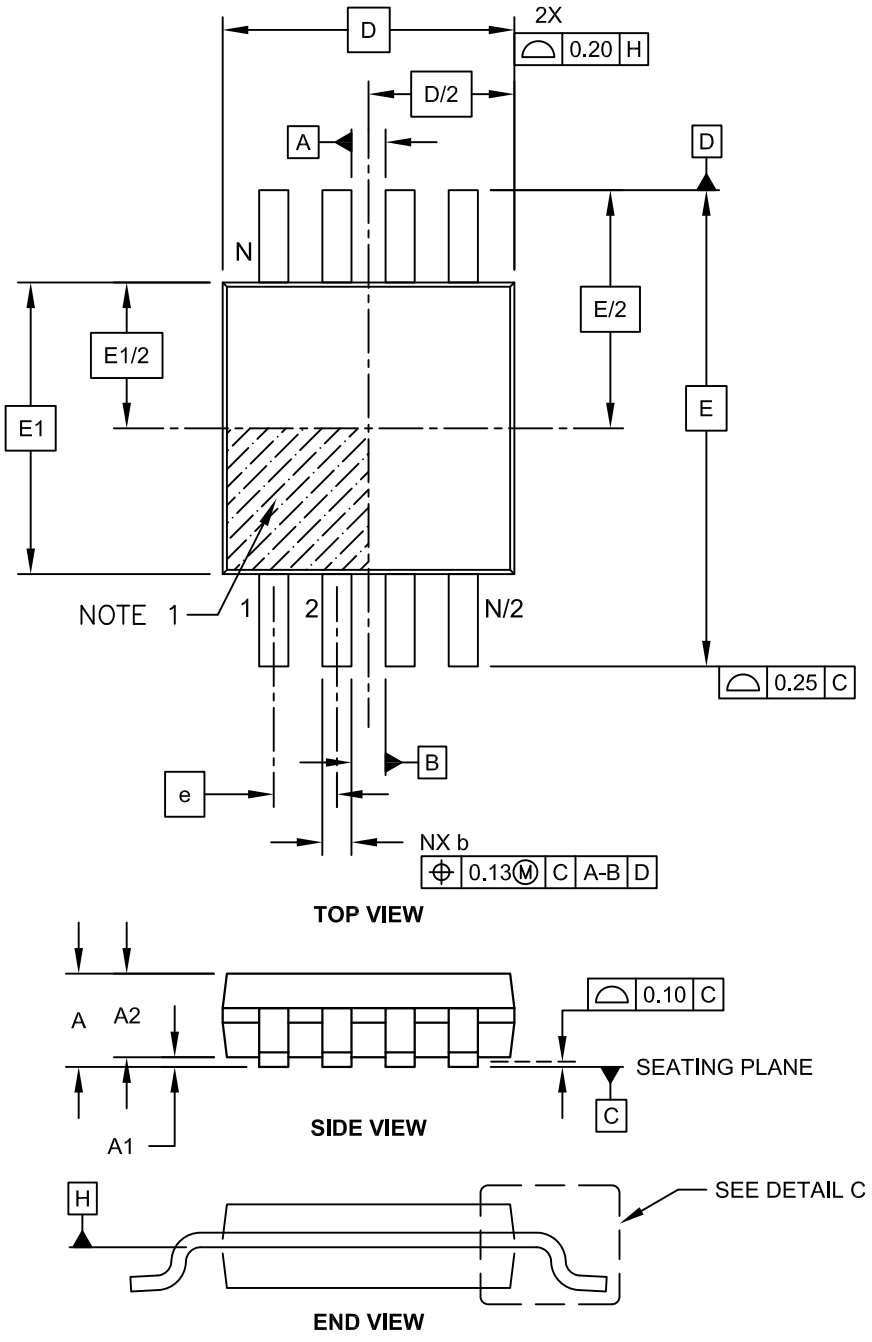
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091A

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

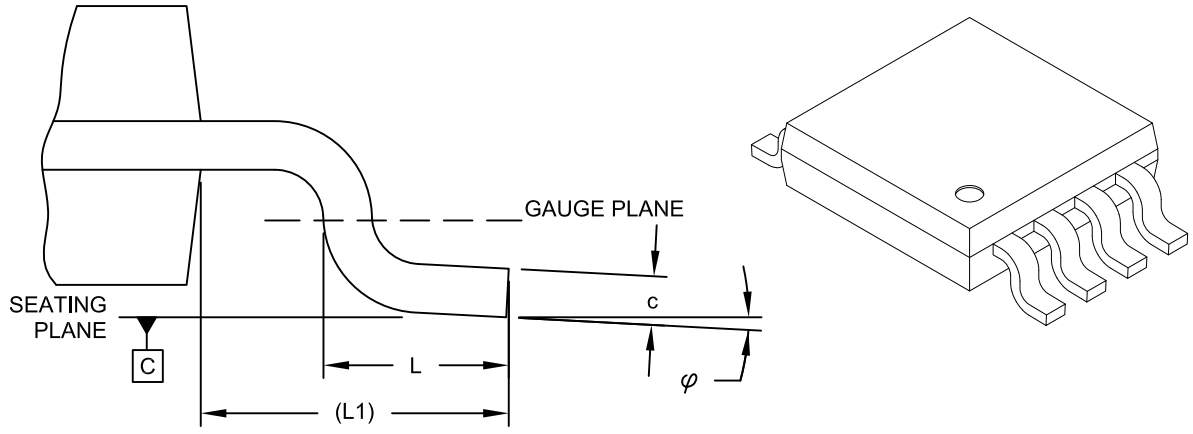
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-111C Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.22	-	0.40

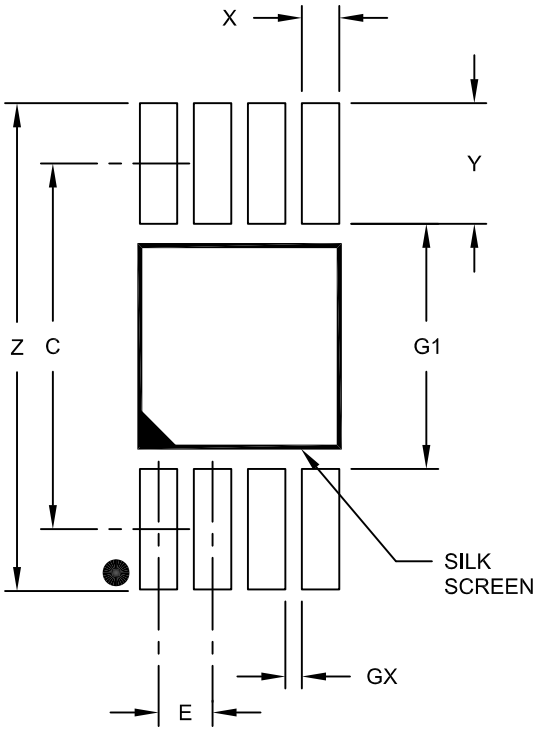
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

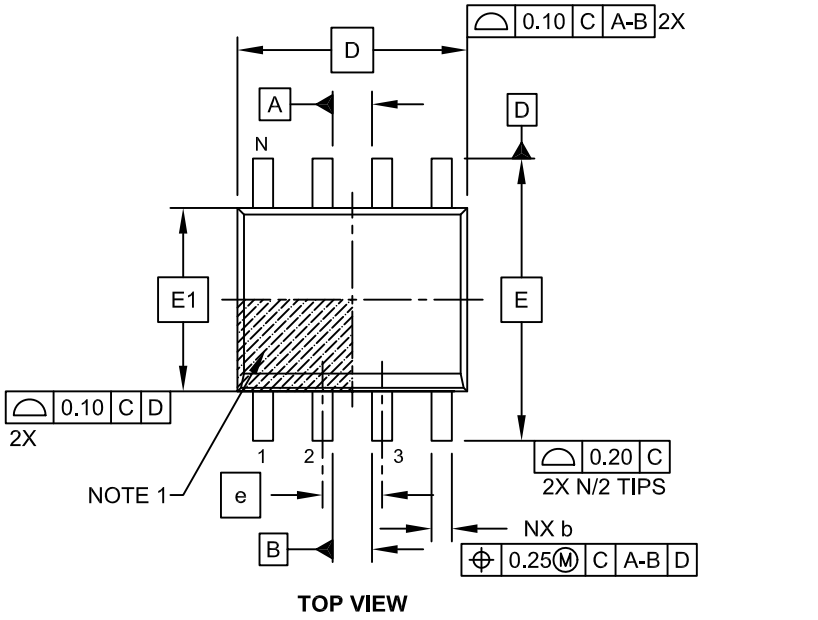
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

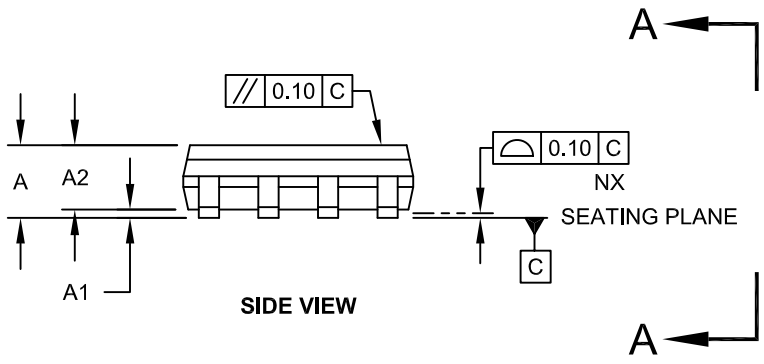
Microchip Technology Drawing No. C04-2111A

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

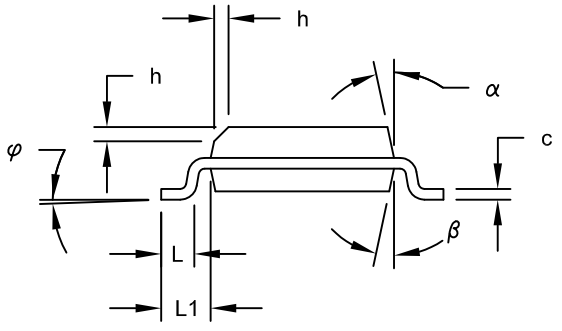
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

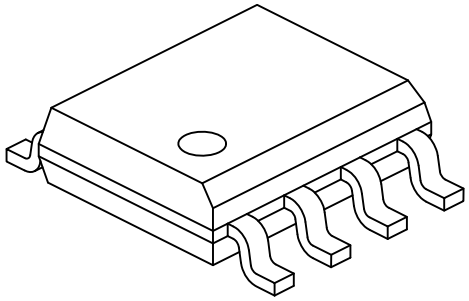


VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

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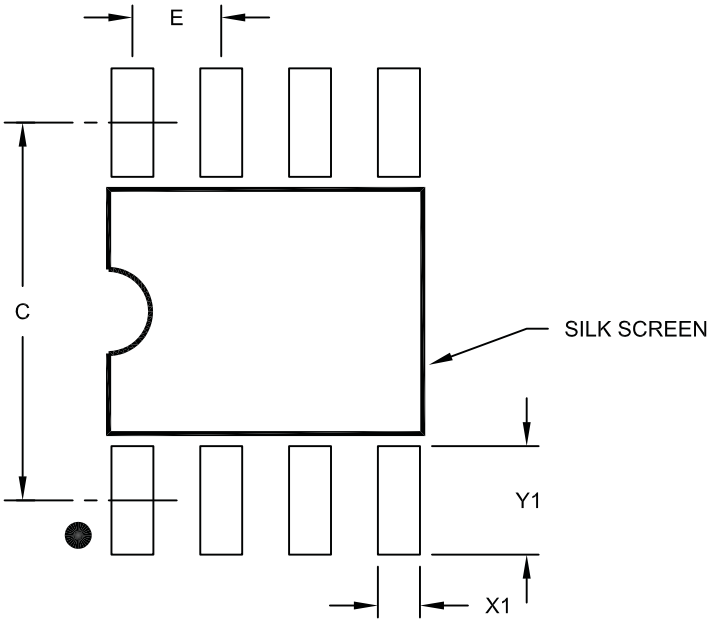
8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

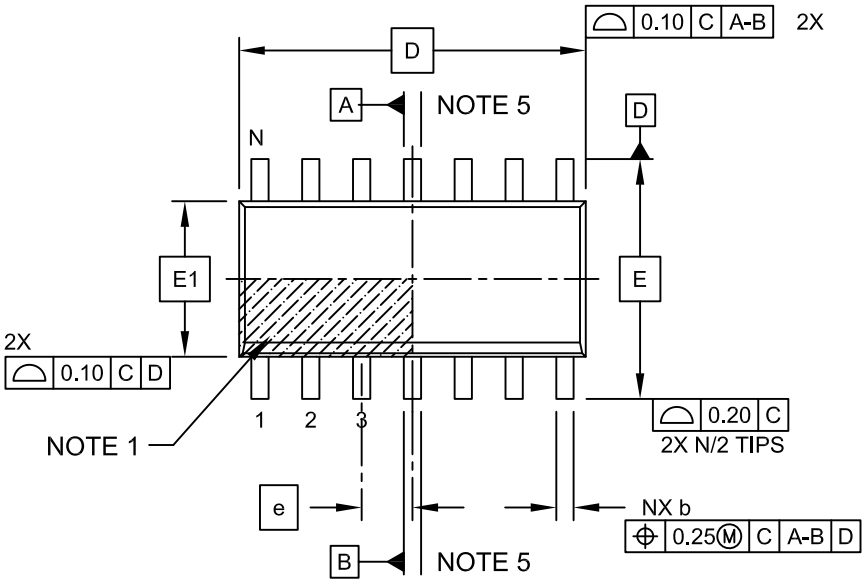
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

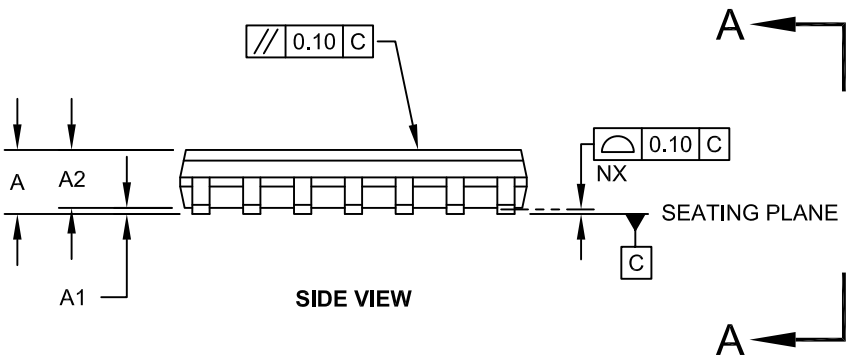
Microchip Technology Drawing No. C04-2057A

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

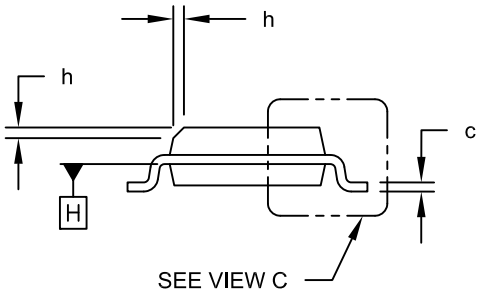
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

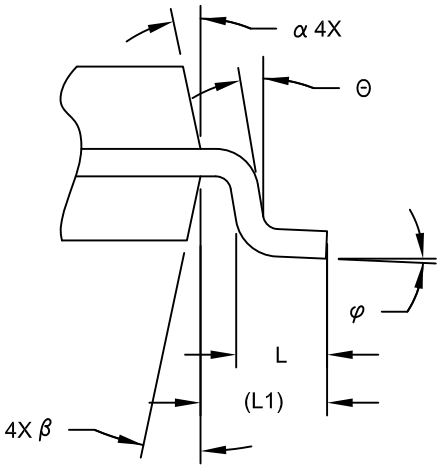


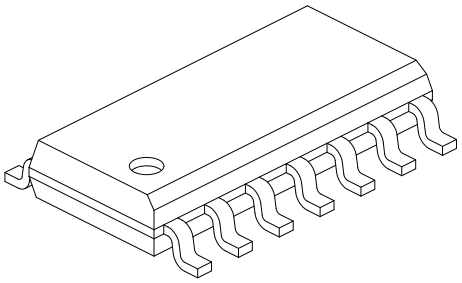
VIEW A-A

Microchip Technology Drawing No. C04-065C Sheet 1 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





VIEW C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

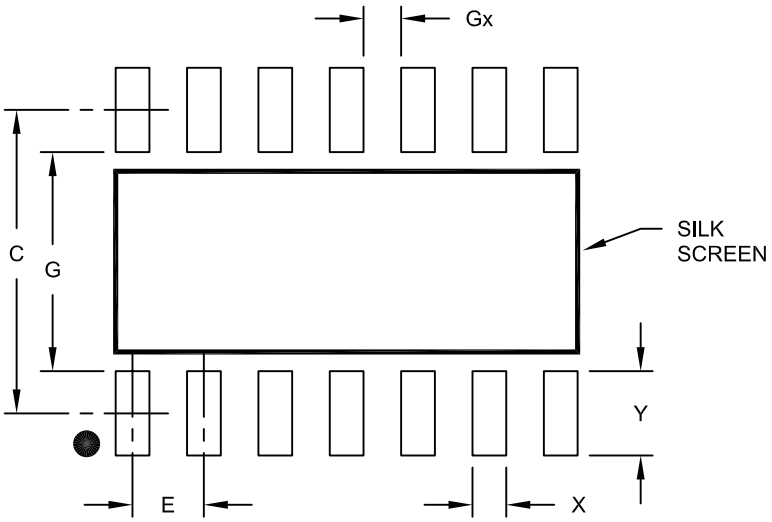
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065C Sheet 2 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

Notes:

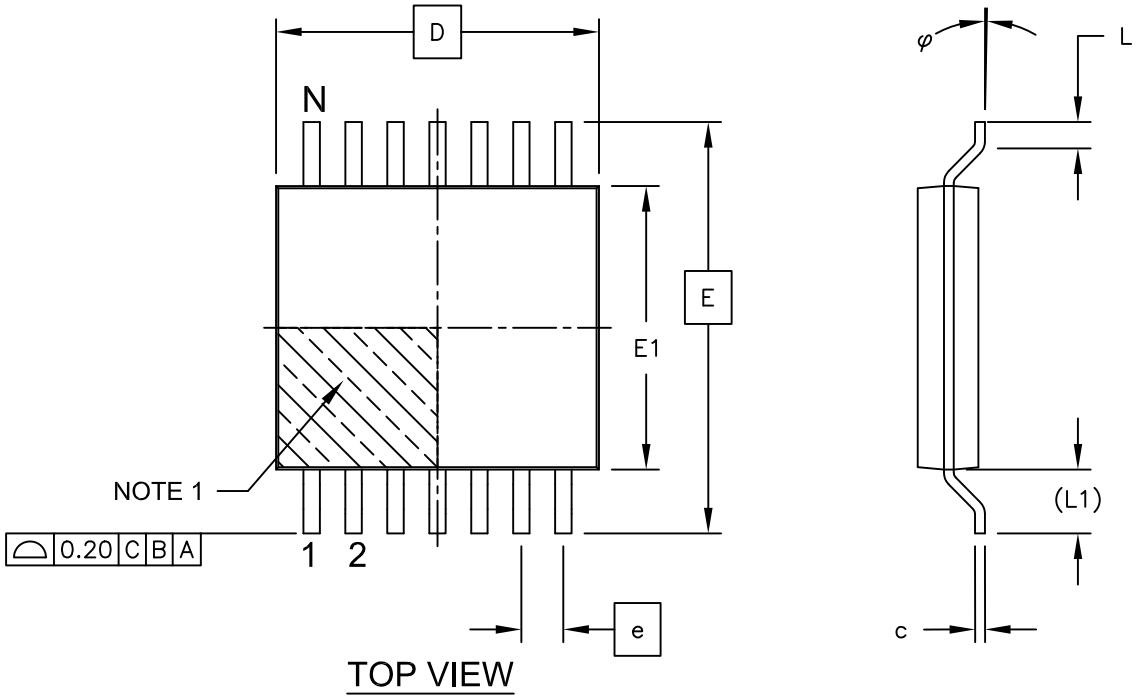
1. Dimensioning and tolerancing per ASME Y14.5M

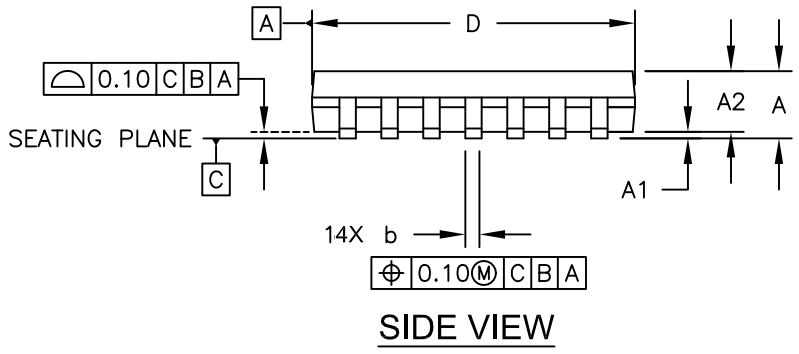
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

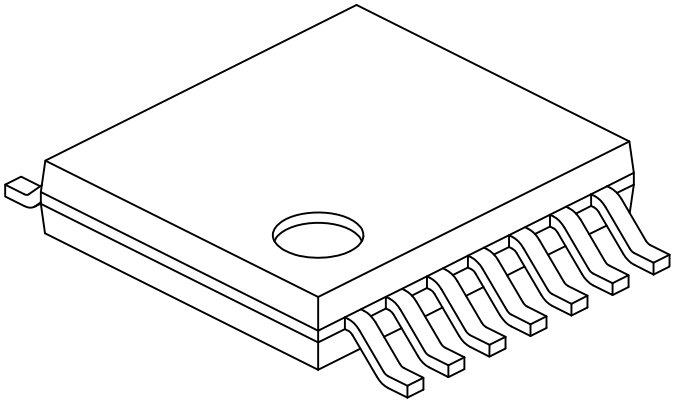




Microchip Technology Drawing C04-087C Sheet 1 of 2

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	(L1)		1.00 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.19	-	0.30

Notes:

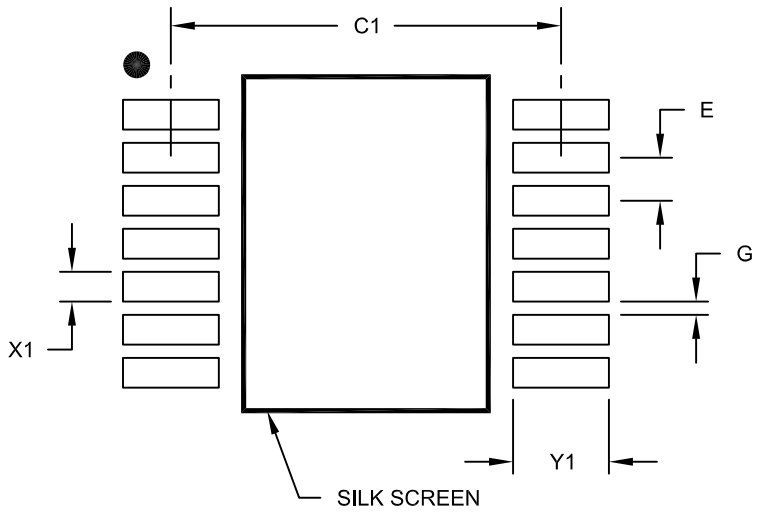
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-087C Sheet 2 of 2

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X14)	X1			0.45
Contact Pad Length (X14)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2087A

APPENDIX A: REVISION HISTORY

Revision B (August 2013)

The following is the list of modifications:

1. Added two new devices to the family: dual version MCP6422 (in 8L-MSOP and 8L-SOIC packages) and quad version MCP6424 (in 15L-SOIC and 14L-TSSOP packages). Added related information throughout the document.
2. Updated Package Types drawing with the new devices' pinouts.
3. Added ESD Protection on all pins (HBM; MM) (Dual and Quad) in the Section 1.1, Absolute Maximum Ratings †.
4. Added the new package temperatures in Table 1-3.
5. Updated Figures 2-2 and 2-37 in Section 2.0, Typical Performance Curves. Added new Figure 2-38.
6. Updated Section 3.0, Pin Descriptions with pin list and information.
7. Added new Section 4.5, Unused Op Amps.
8. Updated Section 6.0, Packaging Information with markings and package specification drawings.
9. Updated Product Identification System.

Revision A (March 2013)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-X	/XX
Device	Temperature Range	Package

Device:	MCP6421T:	Single Op Amp (Tape and Reel) (SC70, SOT-23)
	MCP6422:	Dual Op Amp (MSOP, SOIC)
	MCP6422T:	Dual Op Amp (Tape and Reel) (MSOP, SOIC)
	MCP6424:	Quad Op Amp (SOIC, TSSOP)
	MCP6424T:	Quad Op Amp (Tape and Reel) (SOIC, TSSOP)
Temperature Range:	E =	-40°C to +125°C (Extended)
Package:	LTY* =	Plastic Package (SC70), 5-lead
	MS =	Plastic Micro Small Outline Package (MSOP), 8-lead
	OT =	Plastic Small Outline Transistor (SOT-23), 5-lead
	SL =	Plastic Small Outline - Narrow, 3.90 mm Body, 14-lead
	SN =	Plastic Small Outline - Narrow, 3.90 mm Body, 8-lead
	ST =	Plastic Thin Shrink Small Outline - 4.4 mm Body, 14-lead

* Y = Nickel palladium gold manufacturing designator. Only available on the TDFN package.

Examples:

a)	MCP6421T-E/LTY:	Tape and Reel, Extended Temperature, 5LD SC-70 package
b)	MCP6421T-E/OT:	Tape and Reel, Extended Temperature, 5LD SOT-23 package
a)	MCP6422-E/MS:	Extended Temperature, 8LD MSOP package
b)	MCP6422T-E/MS:	Tape and Reel, Extended Temperature, 8LD MSOP package
c)	MCP6422-E/SN:	Extended Temperature, 8LD SOIC package
d)	MCP6422T-E/SN:	Tape and Reel, Extended Temperature, 8LD SOIC package
a)	MCP6424-E/SL:	Extended Temperature, 14LD SOIC package
b)	MCP6424T-E/SL:	Tape and Reel, Extended Temperature, 14LD SOIC package
c)	MCP6424-E/ST:	Extended Temperature, 14LD TSSOP package
d)	MCP6424T-E/ST:	Tape and Reel, Extended Temperature, 14LD TSSOP package

NOTES:

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