1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

$V_{DD} – V_{SS}$ 7.0V
Current at Input Pins .....±2 mA
Analog Inputs (V_{IN}+, V_{IN}-)†† ..... V_{SS} – 1.0V to V_{DD} + 1.0V
All Other Inputs and Outputs ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Difference Input Voltage ..... $|V_{DD} – V_{SS}|$
Output Short-Circuit Current .....continuous
Current at Output and Supply Pins .....±30 mA
Storage Temperature.....-65°C to +150°C
Maximum Junction Temperature (T_J) ..... +150°C
ESD Protection on All Pins (HBM; MM) ..... ≥ 4 kV; 400V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1.2 "Input Voltage and Current Limits"**.

DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated: V_{DD} = +1.8V to +5.5V, V_{SS} = GND, T_A = +25°C, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L and $\overline{CS}$ is tied low. (Refer to Figure 1-2 and Figure 1-3.)

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-150	—	+150	µV	V_{DD} = 3.0V, V_{CM} = V_{DD}/3
Input Offset Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	±3.0	—	µV/°C	T_A = -40°C to +125°C, V_{DD} = 3.0V, V_{CM} = V_{DD}/3
Power Supply Rejection Ratio	PSRR	70	88	—	dB	V_{CM} = V_{SS}
Input Bias Current and Impedance						
Input Bias Current	I_B	—	±1.0	100	pA	
	I_B	—	60	—	pA	T_A = +85°C
	I_B	—	2000	5000	pA	T_A = +125°C
Input Offset Current	I_{OS}	—	±1.0	—	pA	
Common-mode Input Impedance	Z_{CM}	—	10^{13}||6	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||6	—	Ω||pF	
Common-mode						
Common-mode Input Voltage Range	V_{CMR}	V_{SS} – 0.3	—	V_{DD} + 0.3	V	
Common-mode Rejection Ratio	CMRR	70	95	—	dB	V_{CM} = -0.3V to 2.1V, V_{DD} = 1.8V
		72	93	—	dB	V_{CM} = -0.3V to 5.8V, V_{DD} = 5.5V
		70	89	—	dB	V_{CM} = 2.75V to 5.8V, V_{DD} = 5.5V
		72	93	—	dB	V_{CM} = -0.3V to 2.75V, V_{DD} = 5.5V
Open-Loop Gain						
DC Open-Loop Gain (Large Signal)	A_{OL}	95	115	—	dB	0.2V < V_{OUT} < (V_{DD} – 0.2V), R_L = 50 kΩ to V_L

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DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise indicated: V_{DD} = +1.8V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, R_L = 1 MΩ to V_L and $\overline{CS}$ is tied low. (Refer to Figure 1-2 and Figure 1-3.)

Parameters	Sym	Min	Typ	Max	Units	Conditions
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 10	—	V_{DD} – 10	mV	R_L = 50 kΩ to V_L, 0.5V input overdrive
Output Short-Circuit Current	I_{SC}	—	±5	—	mA	V_{DD} = 1.8V
		—	±23	—	mA	V_{DD} = 5.5V
Power Supply						
Supply Voltage	V_{DD}	1.8	—	5.5	V	
Quiescent Current per Amplifier	I_Q	0.4	0.9	1.35	µA	I_O = 0, $V_{CM} = V_{DD}$, V_{DD} = 5.5V

AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated: T_A = +25°C, V_{DD} = +1.8 to +5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $V_L = V_{DD}/2$, C_L = 60 pF, R_L = 1 MΩ to V_L and $\overline{CS}$ is tied low. (Refer to Figure 1-2 and Figure 1-3.)

Parameters	Sym	Min	Typ	Max	Units	Conditions
AC Response						
Gain Bandwidth Product	GBWP	—	10	—	kHz	
Phase Margin	PM	—	65	—	°	G = +1 V/V
Slew Rate	SR	—	4.0	—	V/ms	
Noise						
Input Noise Voltage	E_{ni}	—	3.9	—	µVp-p	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	165	—	nV/√Hz	f = 1 kHz
Input Noise Current Density	i_{ni}	—	0.6	—	fA/√Hz	f = 1 kHz

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MCP6033 CHIP SELECT ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V, V_{SS} =GND, T_A = +25°C, V_{CM} = $V_{DD}/2$, V_{OUT} = $V_{DD}/2$, V_L = $V_{DD}/2$, C_L = 60 pF, R_L = 1 MΩ to V_L and $\overline{CS}$ is tied low (Refer to Figure 1-1).

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{CS}$ Low Specifications						
$\overline{CS}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	0.2 V_{DD}	V	
$\overline{CS}$ Input Current, Low	I_{CSL}	—	-10	—	pA	$\overline{CS}$ = V_{SS}
$\overline{CS}$ High Specifications						
$\overline{CS}$ Logic Threshold, High	V_{IH}	0.8 V_{DD}	—	V_{DD}	V	
$\overline{CS}$ Input Current, High	I_{CSH}	—	10	—	pA	$\overline{CS}$ = V_{DD}
GND Current	I_{SS}	—	-400	—	pA	$\overline{CS}$ = V_{DD}
Amplifier Output Leakage	$I_{O(LEAK)}$	—	10	—	pA	$\overline{CS}$ = V_{DD}
$\overline{CS}$ Dynamic Specifications						
$\overline{CS}$ Low to Amplifier Output Turn-on Time	t_{ON}	—	4	100	ms	$\overline{CS}$ ≤ 0.2 V_{DD} to V_{OUT} = 0.9 $V_{DD}/2$, G = +1 V/V, V_{IN} = $V_{DD}/2$, R_L = 50 kΩ to V_L = V_{SS}
$\overline{CS}$ High to Amplifier Output High-Z	t_{OFF}	—	10	—	µs	$\overline{CS}$ ≥ 0.8 V_{DD} to V_{OUT} = 0.1 $V_{DD}/2$, G = +1 V/V, V_{IN} = $V_{DD}/2$, R_L = 50 kΩ to V_L = V_{SS}
$\overline{CS}$ Hysteresis	V_{HYST}	—	0.3 V_{DD}	—	V	

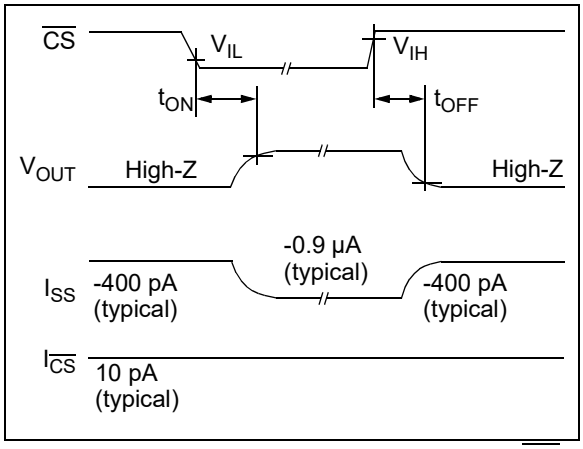

FIGURE 1-1: *Timing Diagram for the $\overline{CS}$ Pin on the MCP6033.*

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TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated: V_{DD} = +1.8V to +5.5V and V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5-Lead SOT-23	θ_{JA}	—	256	—	°C/W	
Thermal Resistance, 8-Lead DFN	θ_{JA}	—	84	—	°C/W	
Thermal Resistance, 8-Lead SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8-Lead MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 14-Lead SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14-Lead TSSOP	θ_{JA}	—	100	—	°C/W	

Note 1: The internal junction temperature (T_J) must not exceed the absolute maximum specification of +150°C.

1.1 Test Circuits

The test circuits used for the DC and AC tests are shown in Figure 1-2 and Figure 1-3. The bypass capacitors are laid out according to the rules discussed in **Section 4.6 "Supply Bypass"**.

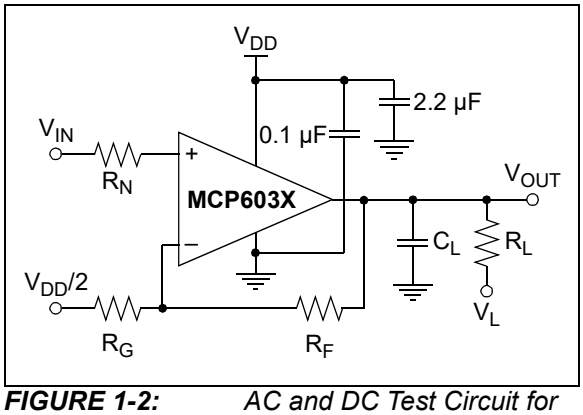

FIGURE 1-2: *AC and DC Test Circuit for Most Noninverting Gain Conditions.*

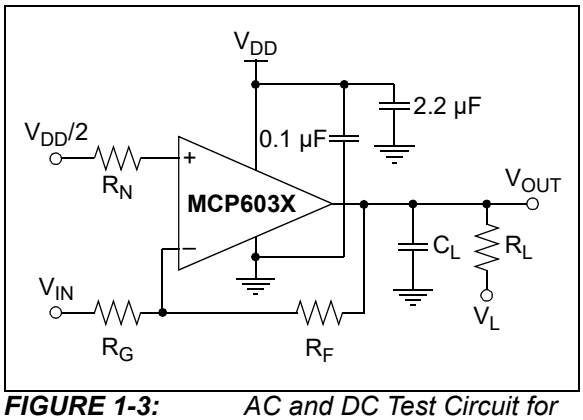

FIGURE 1-3: *AC and DC Test Circuit for Most Inverting Gain Conditions.*

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated: T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, $V_{OUT} \approx V_{DD}$/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L, C_L = 60 pF and CS is tied low.

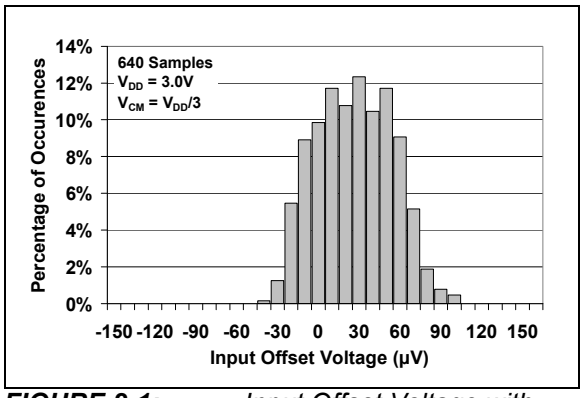

FIGURE 2-1: *Input Offset Voltage with V_{DD} = 3.0V.*

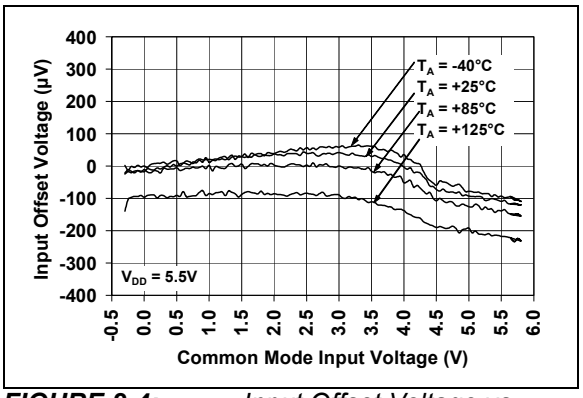

FIGURE 2-4: *Input Offset Voltage vs. Common-mode Input Voltage with V_{DD} = 5.5V.*

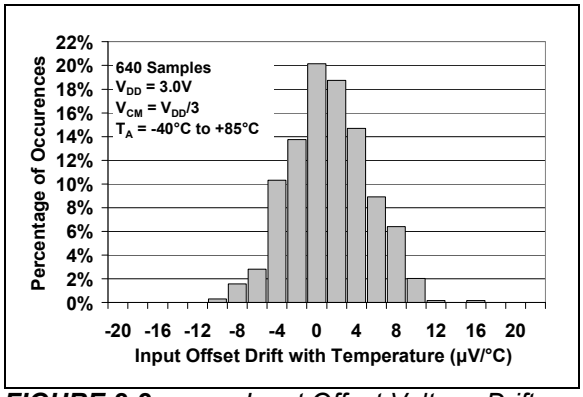

FIGURE 2-2: *Input Offset Voltage Drift with V_{DD} = 3.0V and $T_A \leq$ +85°C.*

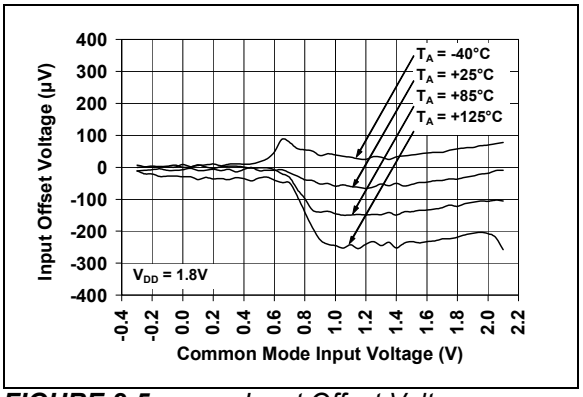

FIGURE 2-5: *Input Offset Voltage vs. Common-mode Input Voltage with V_{DD} = 1.8V.*

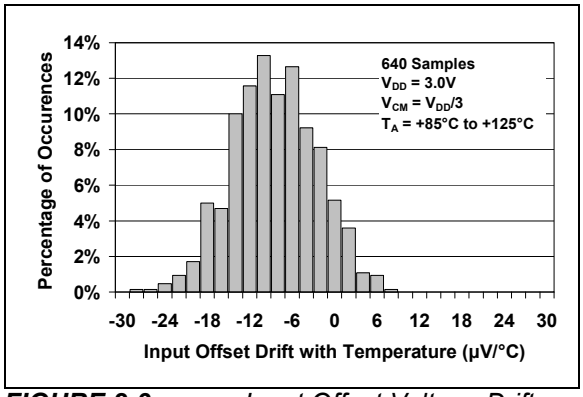

FIGURE 2-3: *Input Offset Voltage Drift with V_{DD} = 3.0V and $T_A \geq$ +85°C.*

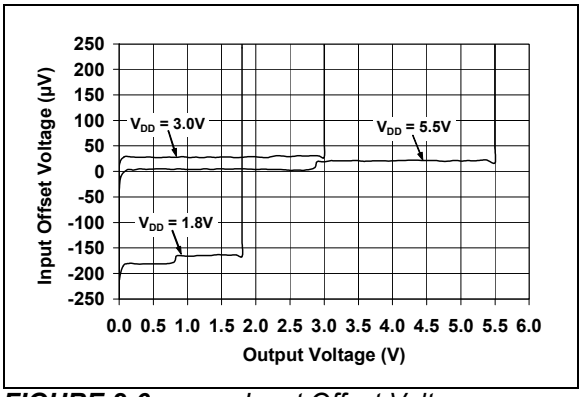

FIGURE 2-6: *Input Offset Voltage vs. Output Voltage.*

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Note: Unless otherwise indicated: T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L, C_L = 60 pF and $\overline{CS}$ is tied low.

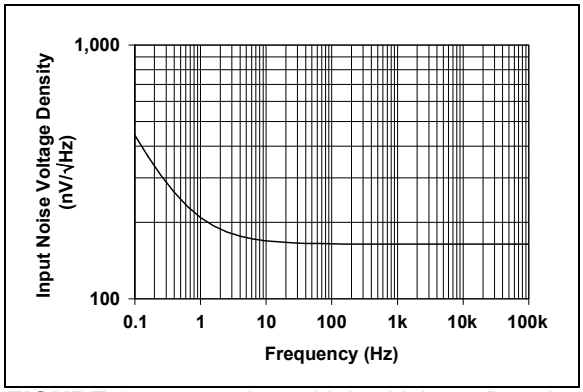

FIGURE 2-7: *Input Noise Voltage Density vs. Frequency.*

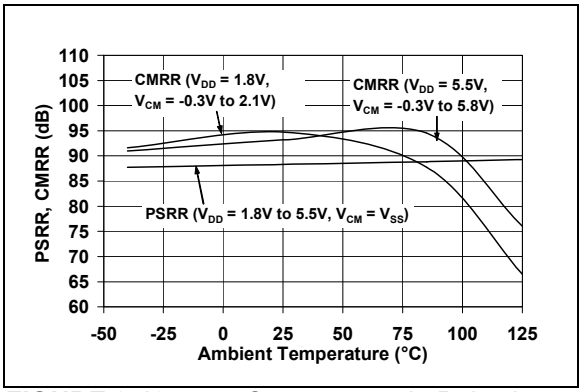

FIGURE 2-10: *Common-mode Rejection Ratio, Power Supply Rejection Ratio vs. Ambient Temperature.*

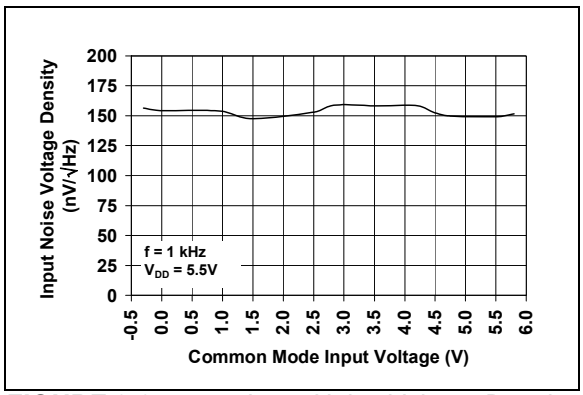

FIGURE 2-8: *Input Noise Voltage Density vs. Common-mode Input Voltage.*

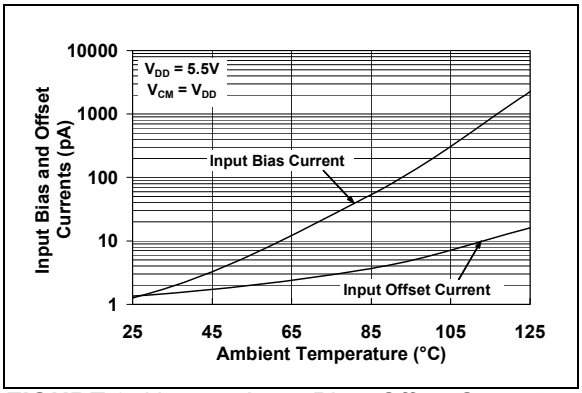

FIGURE 2-11: *Input Bias, Offset Currents vs. Ambient Temperature.*

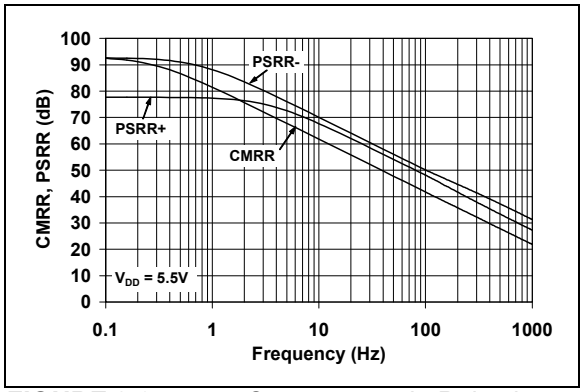

FIGURE 2-9: *Common-mode Rejection Ratio, Power Supply Rejection Ratio vs. Frequency.*

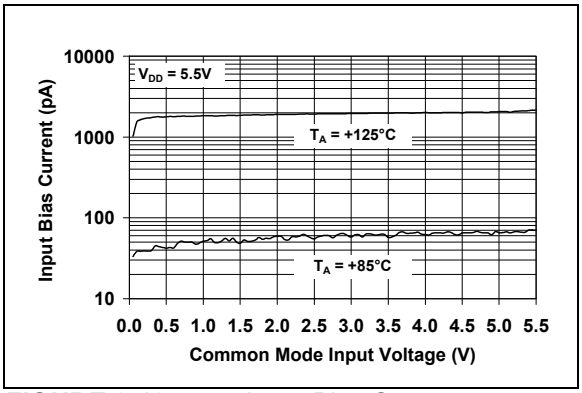

FIGURE 2-12: *Input Bias Current vs. Common-mode Input Voltage.*

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Note: Unless otherwise indicated: T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L, C_L = 60 pF and $\overline{CS}$ is tied low.

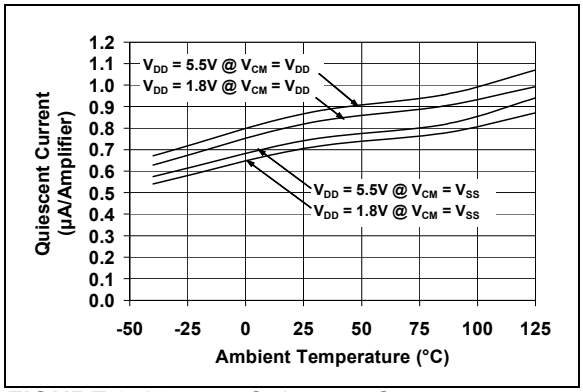

FIGURE 2-13: *Quiescent Current vs Ambient Temperature.*

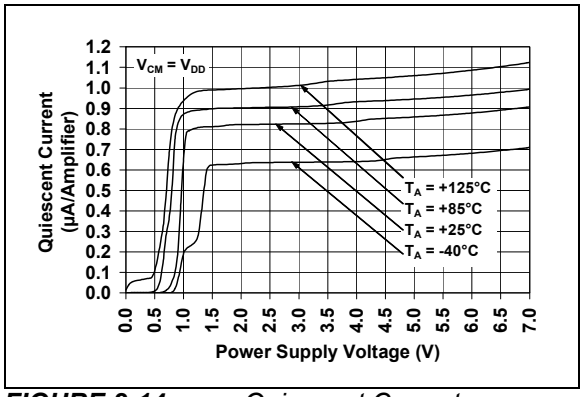

FIGURE 2-14: *Quiescent Current vs. Power Supply Voltage with V_{CM} = V_{DD}.*

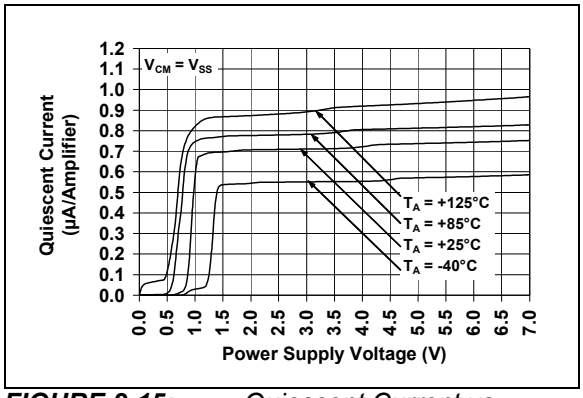

FIGURE 2-15: *Quiescent Current vs. Power Supply Voltage with V_{CM} = V_{SS}.*

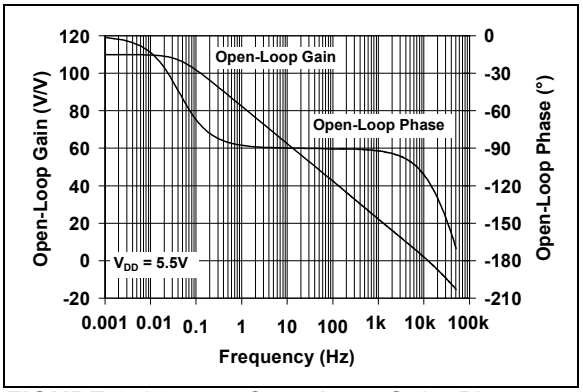

FIGURE 2-16: *Open-Loop Gain, Phase vs. Frequency.*

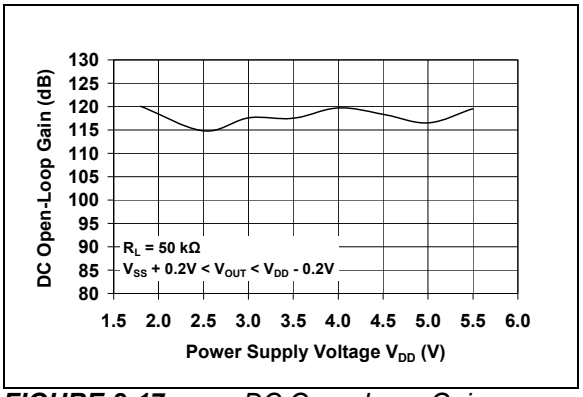

FIGURE 2-17: *DC Open-Loop Gain vs. Power Supply Voltage.*

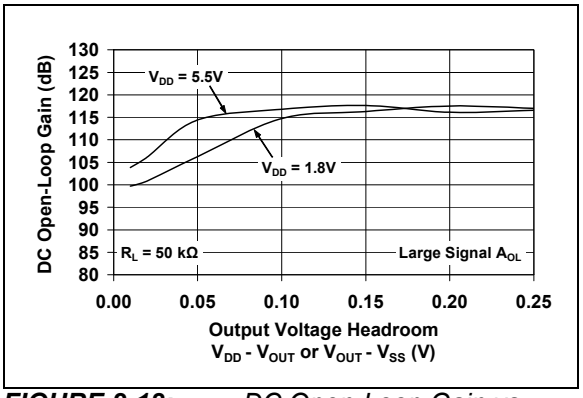

FIGURE 2-18: *DC Open-Loop Gain vs. Output Voltage Headroom.*

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Note: Unless otherwise indicated: T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L, C_L = 60 pF and $\overline{CS}$ is tied low.

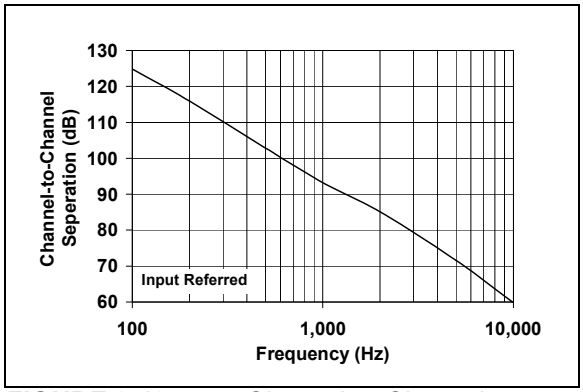

FIGURE 2-19: *Channel-to-Channel Separation vs. Frequency (MCP6032/4 only).*

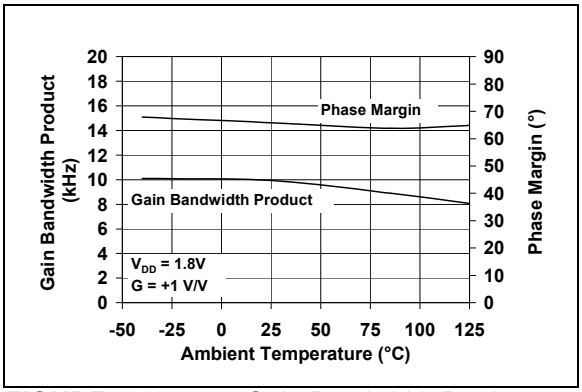

FIGURE 2-22: *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature.*

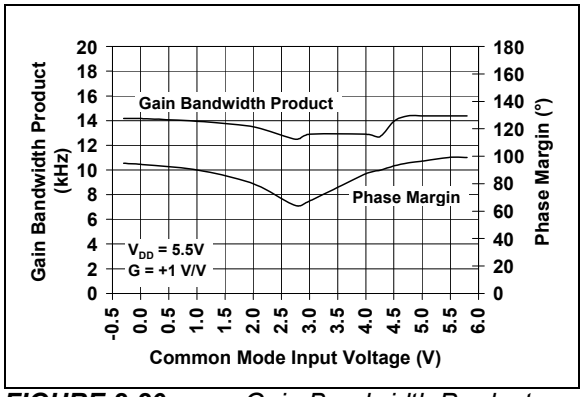

FIGURE 2-20: *Gain Bandwidth Product, Phase Margin vs. Common-mode Input Voltage.*

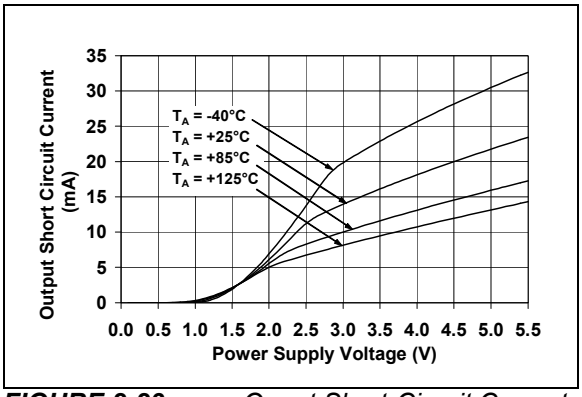

FIGURE 2-23: *Ouput Short-Circuit Current vs. Power Supply Voltage.*

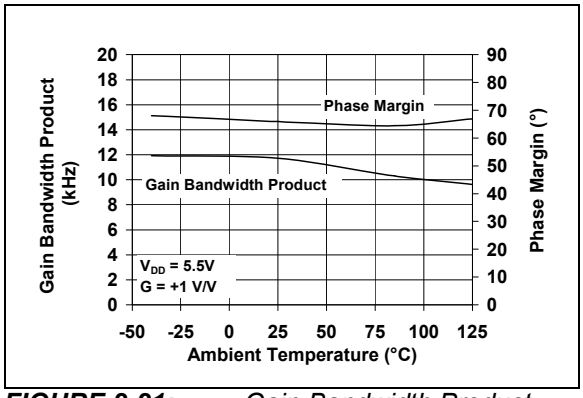

FIGURE 2-21: *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature.*

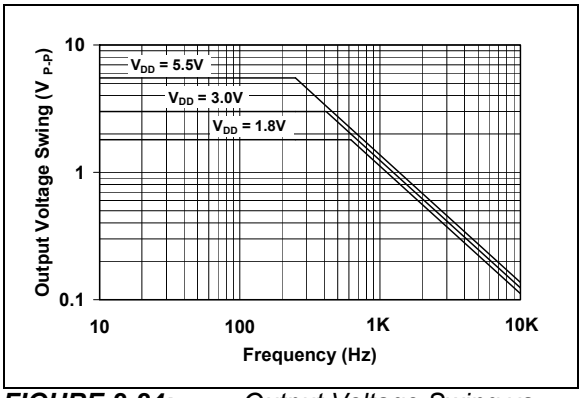

FIGURE 2-24: *Output Voltage Swing vs. Frequency.*

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Note: Unless otherwise indicated: T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L, C_L = 60 pF and $\overline{CS}$ is tied low.

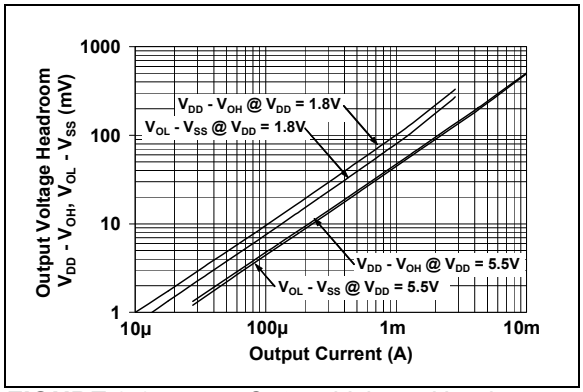

FIGURE 2-25: *Output Voltage Headroom vs. Output Current.*

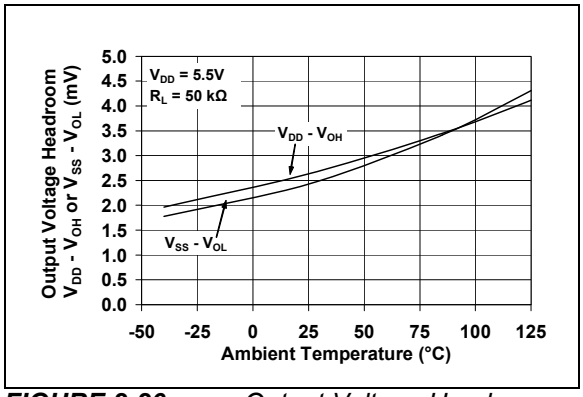

FIGURE 2-26: *Output Voltage Headroom vs. Ambient Temperature.*

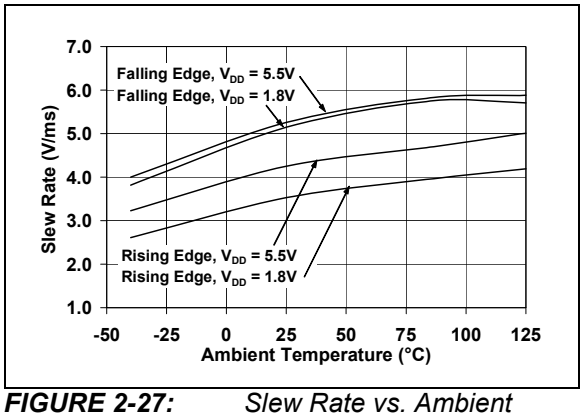

FIGURE 2-27: *Slew Rate vs. Ambient Temperature.*

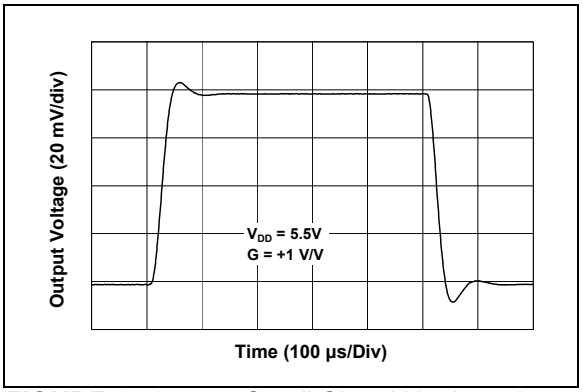

FIGURE 2-28: *Small-Signal Noninverting Pulse Response.*

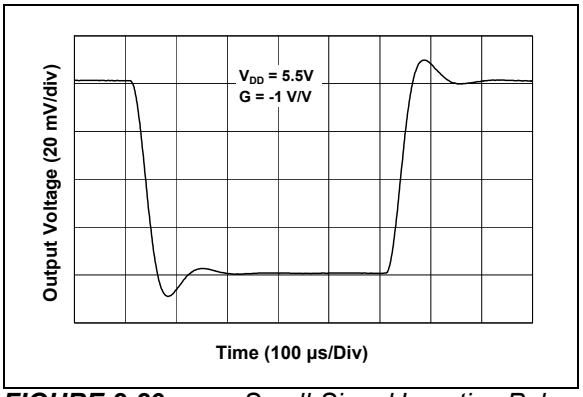

FIGURE 2-29: *Small-Signal Inverting Pulse Response.*

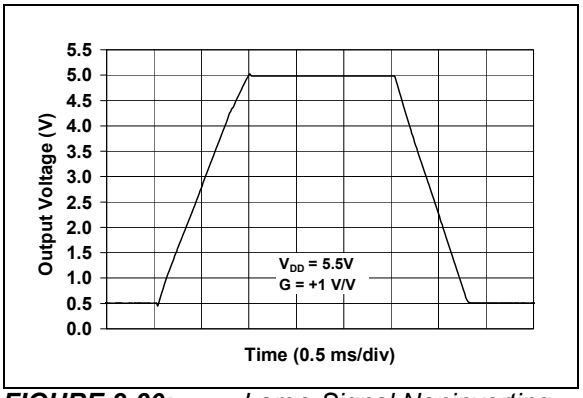

FIGURE 2-30: *Large-Signal Noninverting Pulse Response.*

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Note: Unless otherwise indicated: T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L, C_L = 60 pF and $\overline{CS}$ is tied low.

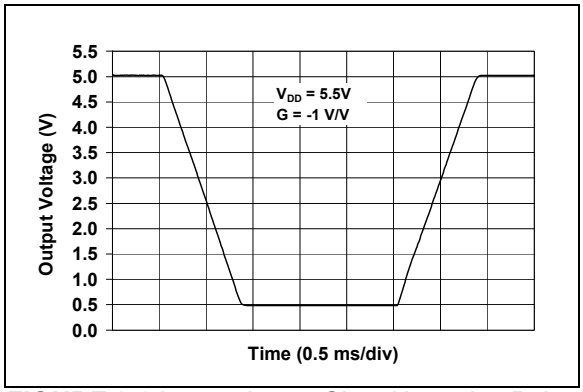

FIGURE 2-31: *Large-Signal Inverting Pulse Response.*

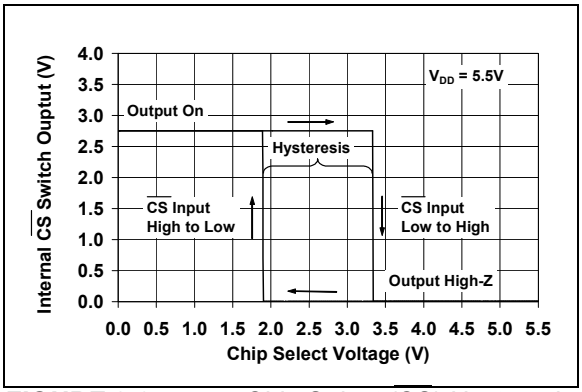

FIGURE 2-34: *Chip Select (CS) Hysteresis (MCP6033 only) with V_{DD} = 5.5V.*

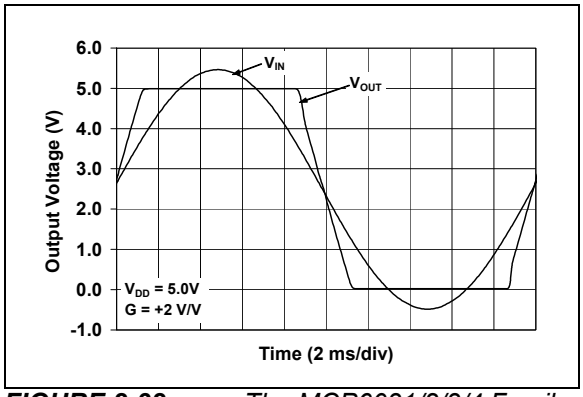

FIGURE 2-32: *The MCP6031/2/3/4 Family Shows No Phase Reversal.*

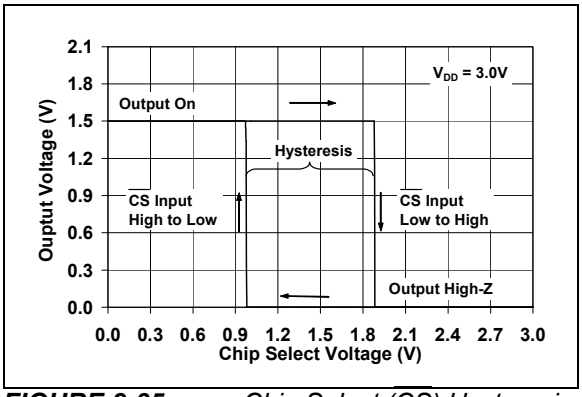

FIGURE 2-35: *Chip Select (CS) Hysteresis (MCP6033 only) with V_{DD} = 3.0V.*

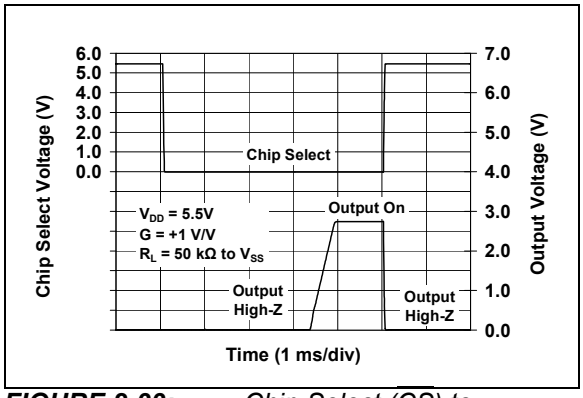

FIGURE 2-33: *Chip Select (CS) to Amplifier Output Response Time (MCP6033 only).*

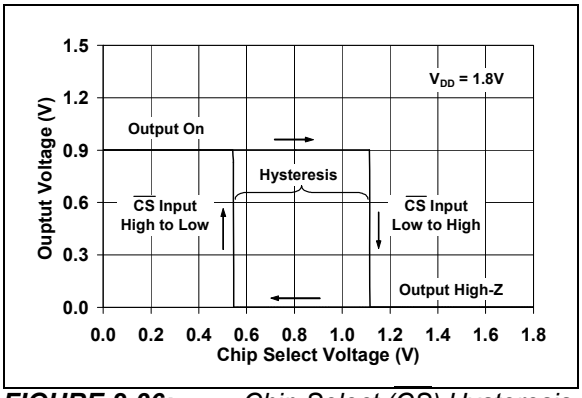

FIGURE 2-36: *Chip Select (CS) Hysteresis (MCP6033 only) with V_{DD} = 1.8V.*

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Note: Unless otherwise indicated: T_A = +25°C, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, V_L = V_{DD}/2, R_L = 1 MΩ to V_L, C_L = 60 pF and $\overline{CS}$ is tied low.

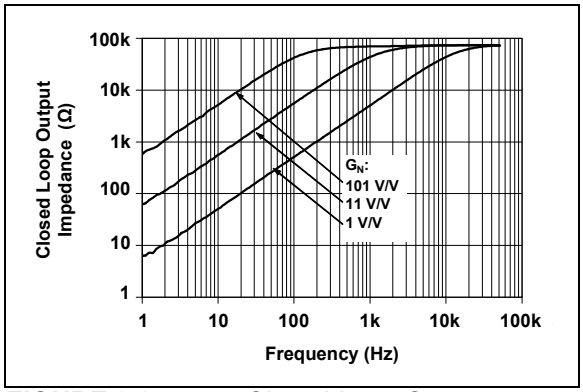

FIGURE 2-37: *Closed-Loop Output Impedance vs. Frequency.*

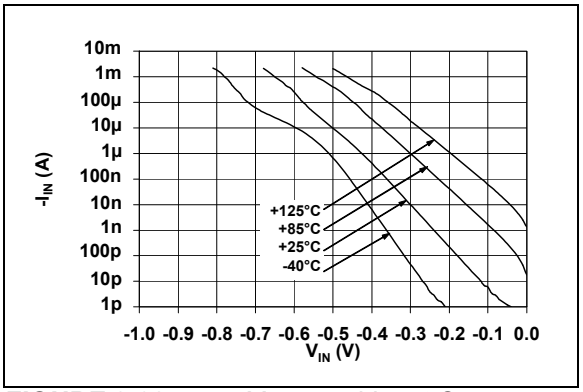

FIGURE 2-38: *Measured Input Current vs. Input Voltage (below V_{SS}).*

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3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP6031		MCP6032	MCP6033	MCP6034	Symbol	Description
SOT-23	DFN, MSOP, SOIC	MSOP, SOIC	DFN, MSOP, SOIC	SOIC, TSSOP		
1	6	1	6	1	V_{OUT}, V_{OUTA}	Analog Output (Op Amp A)
4	2	2	2	2	V_{IN}-, V_{INA}-	Inverting Input (Op Amp A)
3	3	3	3	3	V_{IN}+, V_{INA}+	Noninverting Input (Op Amp A)
5	7	8	7	4	V_{DD}	Positive Power Supply
—	—	5	—	5	V_{INB}+	Noninverting Input (Op Amp B)
—	—	6	—	6	V_{INB}-	Inverting Input (Op Amp B)
—	—	7	—	7	V_{OUTB}	Analog Output (Op Amp B)
—	—	—	—	8	V_{OUTC}	Analog Output (Op Amp C)
—	—	—	—	9	V_{INC}-	Inverting Input (Op Amp C)
—	—	—	—	10	V_{INC}+	Noninverting Input (Op Amp C)
2	4	4	4	11	V_{SS}	Negative Power Supply
—	—	—	—	12	V_{IND}+	Noninverting Input (Op Amp D)
—	—	—	—	13	V_{IND}-	Inverting Input (Op Amp D)
—	—	—	—	14	V_{OUTD}	Analog Output (Op Amp D)
—	—	—	8	—	$\overline{CS}$	Chip Select
—	1, 5, 8	—	1, 5	—	NC	No Internal Connection

3.1 Analog Outputs

The output pins are low-impedance voltage sources.

3.2 Analog Inputs

The noninverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.3 Chip Select Digital Input

This is a CMOS, Schmitt-trigerred input that places the device into a Low-Power mode of operation.

3.4 Power Supply Pins

The positive power supply (V_{DD}) is 1.8V to 5.5V higher than the negative power supply (V_{SS}). For normal operation, the other pins are at voltages between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need bypass capacitors.

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4.0 APPLICATION INFORMATION

The MCP6031/2/3/4 family of op amps is manufactured using Microchip's state-of-the-art CMOS process and is specifically designed for low-power, high-precision applications.

4.1 Rail-to-Rail Input

4.1.1 PHASE REVERASAL

The MCP6031/2/3/4 op amps are designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 2-32 shows the input voltage exceeding the supply voltage without any phase reversal.

4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors and to minimize input bias current (I_B). The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS}. They also clamp any voltage that goes too far above V_{DD}. Their breakdown voltage is high enough to allow normal operation and low enough to bypass ESD events within the specified limits.

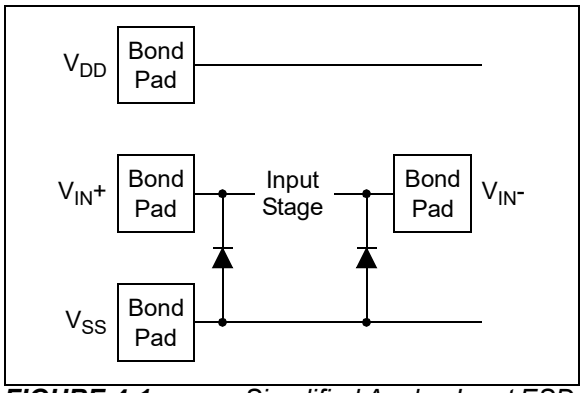

FIGURE 4-1: *Simplified Analog Input ESD Structures.*

In order to prevent damage and/or improper operation of these op amps, the circuit they are in must limit the voltages and currents at the V_{IN}+ and V_{IN}- pins (see **"Absolute Maximum Ratings†"** at the beginning of **Section 1.0 "Electrical Characteristics"**). Figure 4-2 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins (V_{IN}+ and V_{IN}-) from going too far below ground, and the resistors, R_1 and R_2, limit the possible current drawn out of the input pins. Diodes, D_1 and D_2, prevent the input pins (V_{IN}+ and V_{IN}-) from going too far above V_{DD}. When implemented as shown, resistors, R_1 and R_2, also limit the current through D_1 and D_2.

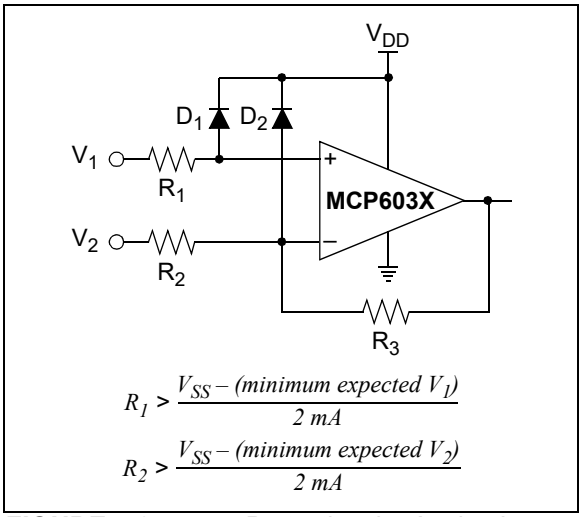

FIGURE 4-2: *Protecting the Analog Inputs.*

It is also possible to connect the diodes to the left of the resistors, R_1 and R_2. In this case, the currents through the diodes, D_1 and D_2, need to be limited by some other mechanism. The resistors then serve as inrush current limiters; the DC currents into the input pins (V_{IN}+ and V_{IN}-) should be very small. A significant amount of current can flow out of the inputs when the Common-mode voltage (V_{CM}) is below ground (V_{SS}).

4.1.3 NORMAL OPERATION

The input stage of the MCP6031/2/3/4 op amps uses two differential input stages in parallel. One operates at a low Common-mode input voltage (V_{CM}), while the other operates at a high V_{CM}. With this topology, the device operates with a V_{CM} up to 300 mV above V_{DD} and 300 mV below V_{SS}. The input offset voltage is measured at V_{CM} = V_{SS} – 0.3V and V_{DD} + 0.3V to ensure proper operation.

There are two transitions in input behavior as V_{CM} is changed. The first occurs, when V_{CM} is near V_{SS} + 0.4V, and the second occurs when V_{CM} is near V_{DD} – 0.5V. For the best distortion performance with noninverting gains, avoid these regions of operation.

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4.2 Rail-to-Rail Output

The output voltage range of the MCP6031/2/3/4 op amps is V_{SS} + 10 mV (minimum) and V_{DD} – 10 mV (maximum) when R_L = 50 kΩ is connected to $V_{DD}/2$ and V_{DD} = 5.5V. Refer to Figures 2-25 and 2-26 for more information.

4.3 Output Loads and Battery Life

The MCP6031/2/3/4 op amp family has outstanding quiescent current, which supports battery-powered applications. There is minimal quiescent current glitching when Chip Select ($\overline{CS}$) is raised or lowered. This prevents excessive current draw and reduced battery life when the part is turned off or on.

Heavy resistive loads at the output can cause excessive battery drain. Driving a DC voltage of 2.5V across a 100 kΩ load resistor will cause the supply current to increase by 25 µA, depleting the battery 28 times as fast as I_Q (0.9 µA, typical) alone.

High-frequency signals (fast edge rate) across capacitive loads will also significantly increase supply current. For instance, a 0.1 µF capacitor at the output presents an AC impedance of 15.9 kΩ (1/2πfC) to a 100 Hz sinewave. It can be shown that the average power drawn from the battery by a 5.0 V_{p-p} sinewave (1.77 V_{rms}) under these conditions is

EQUATION 4-1:

$$\begin{aligned} P_{Supply} &= (V_{DD} - V_{SS})\,(I_Q + V_{L(p-p)} f C_L) \\ &= (5V)(0.9\ \mu A + 5.0\ V_{p-p} \cdot 100\ Hz \cdot 0.1\ \mu F) \\ &= 4.5\ \mu W + 50\ \mu W \end{aligned}$$

This will drain the battery about 12 times as fast as I_Q alone.

4.4 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. While a unity gain buffer (G = +1) is the most sensitive to capacitive loads, all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., >100 pF when G = +1), a small series resistor at the output (R_{ISO} in Figure 4-3) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitance load.

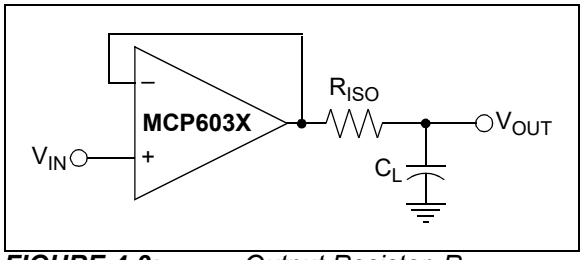

FIGURE 4-3: *Output Resistor, R_{ISO}, Stabilizes Large Capacitive Loads.*

Figure 4-4 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the circuit's noise gain. For noninverting gains, G_N and the Signal Gain are equal. For inverting gains, G_N is 1+|Signal Gain| (e.g., -1 V/V gives G_N = +2 V/V).

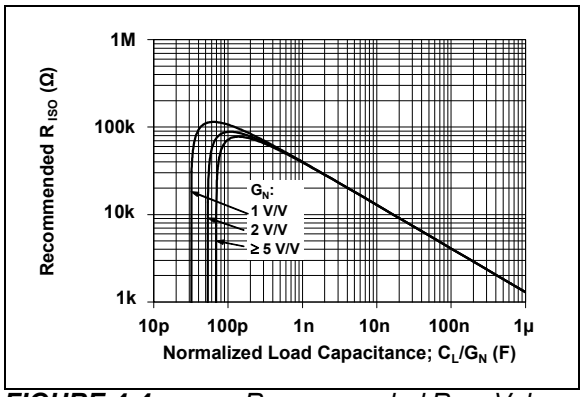

FIGURE 4-4: *Recommended R_{ISO} Values for Capacitive Loads.*

After selecting R_{ISO} for your circuit, double-check the resulting frequency response peaking and step response overshoot. Modify R_{ISO}'s value until the response is reasonable. Bench evaluation and simulations with the MCP6031/2/3/4 SPICE macro model are very helpful.

4.5 MCP6033 Chip Select

The MCP6033 is a single op amp with Chip Select ($\overline{CS}$). When $\overline{CS}$ is pulled high, the supply current drops to 0.4 nA (typical) and flows through the $\overline{CS}$ pin to V_{SS}. When this happens, the amplifier output is put into a high-impedance state. By pulling $\overline{CS}$ low, the amplifier is enabled. If the $\overline{CS}$ pin is left floating, the amplifier will not operate properly. Figure 1-1 shows the output voltage and supply current response to a $\overline{CS}$ pulse.

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4.6 Supply Bypass

With this family of operational amplifiers, the power supply pin (V_{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high-frequency performance. It can use a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

4.7 Unused Op Amps

An unused op amp in a quad package (MCP6034) should be configured as shown in Figure 4-5. These circuits prevent the output from toggling and causing crosstalk. Circuit A sets the op amp at its minimum noise gain. The resistor divider produces any desired reference voltage within the output voltage range of the op amp; the op amp buffers that reference voltage. Circuit B uses the minimum number of components and operates as a comparator, but it may draw more current.

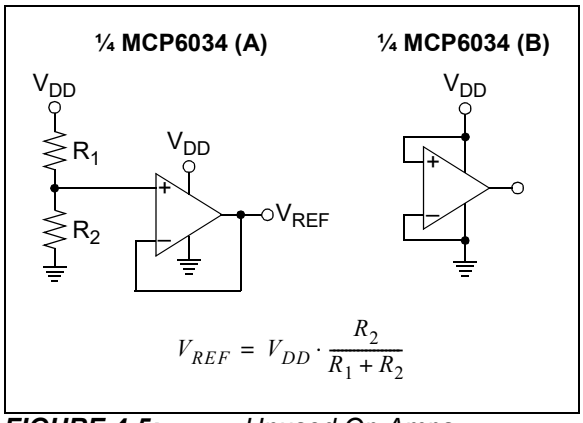

FIGURE 4-5: *Unused Op Amps.*

4.8 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow, which is greater than the MCP6031/2/3/4 family's bias current at +25°C (±1.0 pA, typical).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-6.

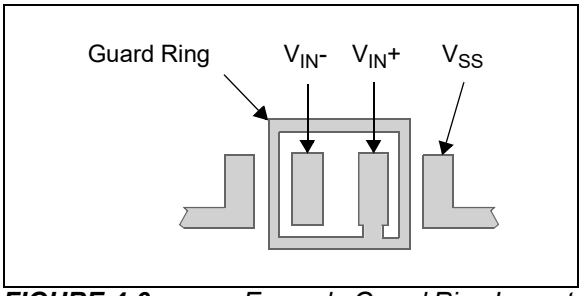

FIGURE 4-6: *Example Guard Ring Layout for Inverting Gain.*

1. Noninverting Gain and Unity Gain Buffer:
   a) Connect the noninverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
   b) Connect the guard ring to the inverting input pin (V_{IN}-). This biases the guard ring to the Common-mode input voltage.
2. Inverting Gain and Transimpedance Gain Amplifiers (convert current to voltage, such as photo detectors):
   a) Connect the guard ring to the noninverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the op amp (e.g., V_{DD}/2 or ground).
   b) Connect the inverting pin (V_{IN}-) to the input with a wire that does not touch the PCB surface.

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4.9 Application Circuits

4.9.1 BATTERY CURRENT SENSING

The MCP6031/2/3/4 op amps' Common-mode input range, which goes 0.3V beyond both supply rails, supports their use in high-side and low-side battery current sensing applications. The ultra-low quiescent current (0.9 µA, typical) helps prolong battery life and the rail-to-rail output supports detection of low currents.

Figure 4-7 shows a high-side battery current sensor circuit. The 10Ω resistor is sized to minimize power losses. The battery current (I_{DD}) through the 10Ω resistor causes its top terminal to be more negative than the bottom terminal. This keeps the Common-mode input voltage of the op amp below V_{DD}, which is within its allowed range. The output of the op amp will also be below V_{DD}, which is within its maximum output voltage swing specification.

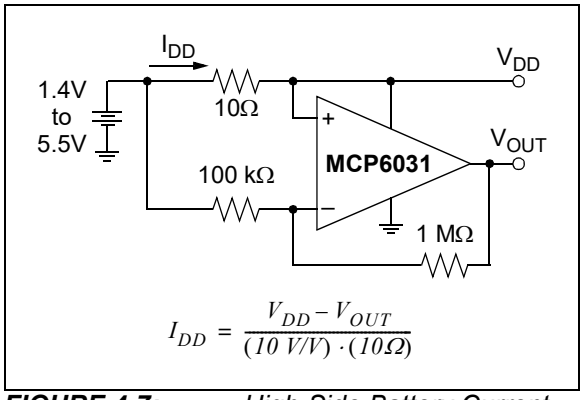

FIGURE 4-7: *High-Side Battery Current Sensor.*

4.9.2 PRECISION COMPARATOR

Use high gain before a comparator to improve the latter's input offset performance. Figure 4-8 shows a gain of 11 V/V placed before a comparator. The reference voltage, V_{REF}, can be any value between the supply rails.

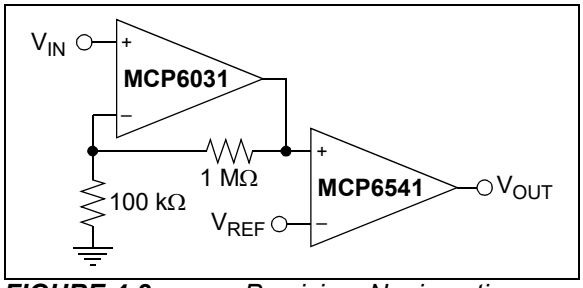

FIGURE 4-8: *Precision, Noninverting Comparator.*

4.9.3 DRIVING MCP3421 ΔΣ A/D CONVERTER

A R_{SH} and C_{SH} snubber reduces the output impedance of the MCP6031 op amp, which reduces the gain error caused by switching transients, which occur at the MCP3421 ADC's sampling rate. The snubber also maintains feedback stability, and avoids AC response peaking and step response overshoot and ringing (caused by the op amp's inductive output impedance resonating with the ADC's input capacitance). The cost for this improvement is low. Best of all, using an op amp with higher supply current is avoided (see Figure 4-9). This figure also includes a resistor to balance the impedance at the ADC's inputs (R_{BAL}) at the sampling frequency; it may not be needed in all designs.

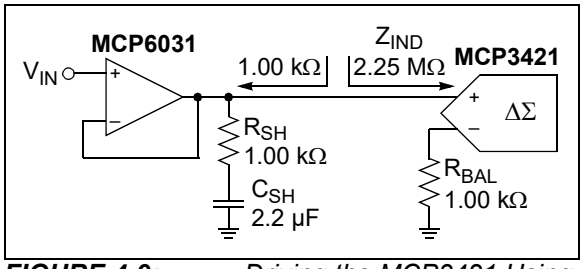

FIGURE 4-9: *Driving the MCP3421 Using an R-C Snubber.*

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5.0 DESIGN AIDS

Microchip provides the basic design tools needed for the MCP6031/2/3/4 family of op amps.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP6031/2/3/4 op amps is available on the Microchip website at www.microchip.com. This model is intended to be an initial design tool that works well in the op amp's linear region of operation over the temperature range. See the model file for information on its capabilities.

Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

5.2 FilterLab® Software

Microchip's FilterLab® software is an innovative software tool that simplifies analog active filter (using op amps) design. Available at no cost from the Microchip website at www.microchip.com/filterlab, the FilterLab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

5.3 Mindi™ Circuit Designer and Simulator

Microchip's Mindi™ Circuit Designer and Simulator aids in the design of various circuits useful for active filter, amplifier and power management applications. It is a free online circuit designer and simulator available from the Microchip website at www.microchip.com/mindi. This interactive circuit designer and simulator enables designers to quickly generate circuit diagrams and simulate circuits. Circuits developed using the Mindi Circuit Designer and Simulator can be downloaded to a personal computer or workstation.

5.4 MAPS (Microchip Advanced Part Selector)

MAPS is a software tool that helps semiconductor professionals efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip website at www.microchip.com/maps, the MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool you can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for Data Sheets, Purchase and Sampling of Microchip parts.

5.5 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip website at www.microchip.com/analogtools.

Two of our boards that are especially useful are:

- **P/N SOIC8EV:** *8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board*
- **P/N SOIC14EV:** *14-Pin SOIC/TSSOP/DIP Evaluation Board*

5.6 Application Notes

The following Microchip Analog Design Note and Application Notes are available on the Microchip website at www.microchip.com/appnotes and are recommended as supplemental reference resources.

ADN003: *"Select the Right Operational Amplifier for your Filtering Circuits",* DS21821

AN722: *"Operational Amplifier Topologies and DC Specifications",* DS00722

AN723: *"Operational Amplifier AC Specifications and Applications",* DS00723

AN884: *"Driving Capacitive Loads With Op Amps",* DS00884

AN990: *"Analog Sensor Conditioning Circuits – An Overview",* DS00990

These application notes and others are listed in the design guide:

"Signal Chain Design Guide", DS21825

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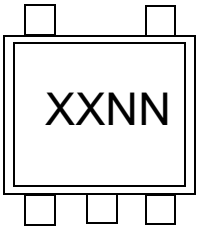
6.0 PACKAGING INFORMATION

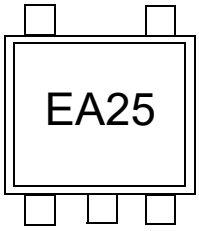
6.1 Package Marking Information

5-Lead SOT-23 **(MCP6031)**

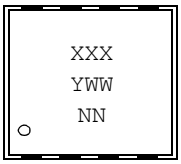


Device	E-Temp Code
MCP6031T-E/OT	EANN

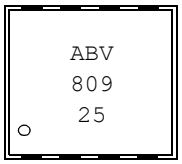
Example:



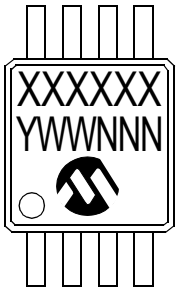
8-Lead 2x3 mm DFN **(MCP6031 and MCP6033)**



Example:

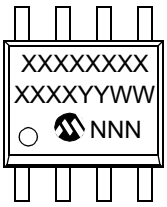


8-Lead MSOP

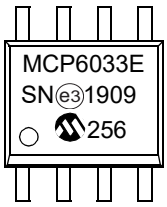


Example:

8-Lead SOIC (3.90 mm)



Example:



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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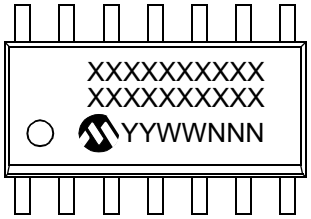
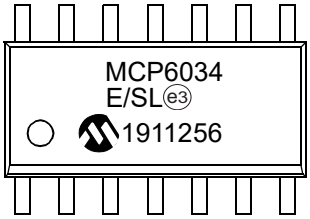
Package Marking Information (Continued)

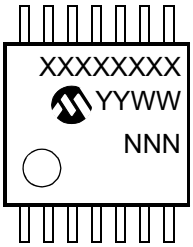
14-Lead SOIC (3.90 mm) **(MCP6034)**



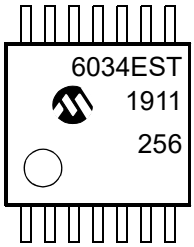
Example:



14-Lead TSSOP **(MCP6034)**



Example:



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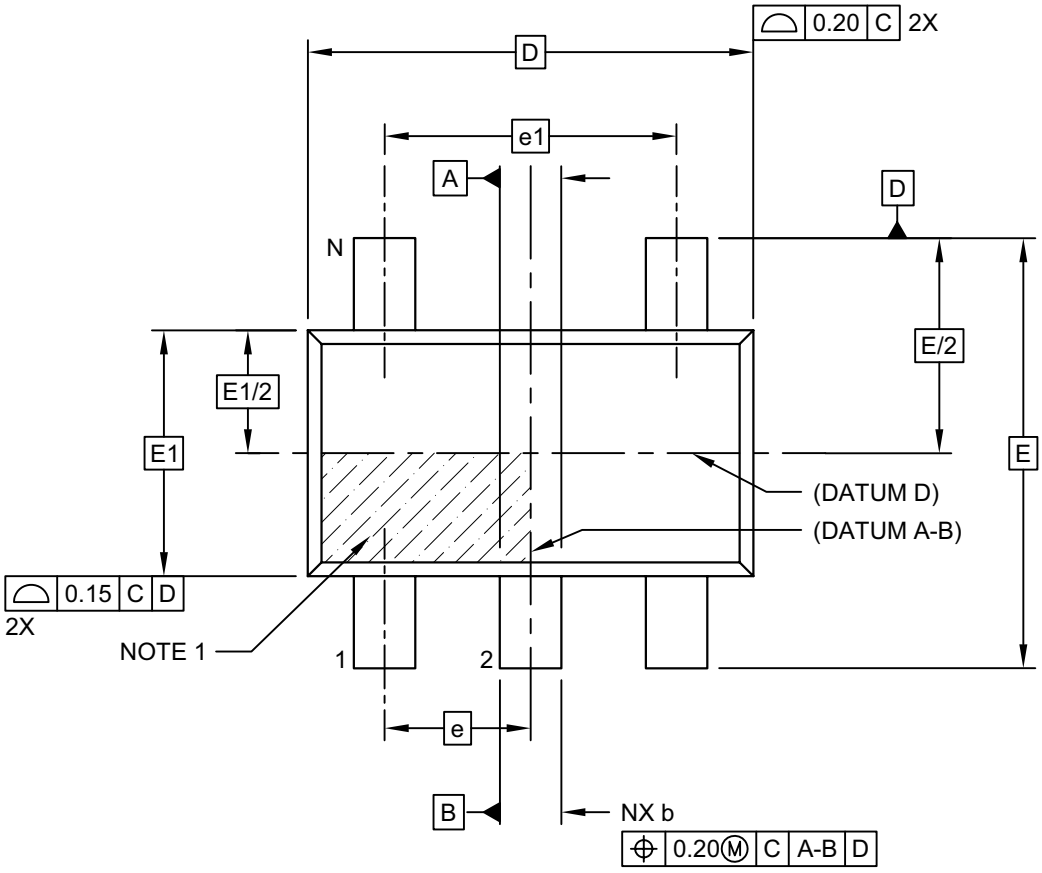
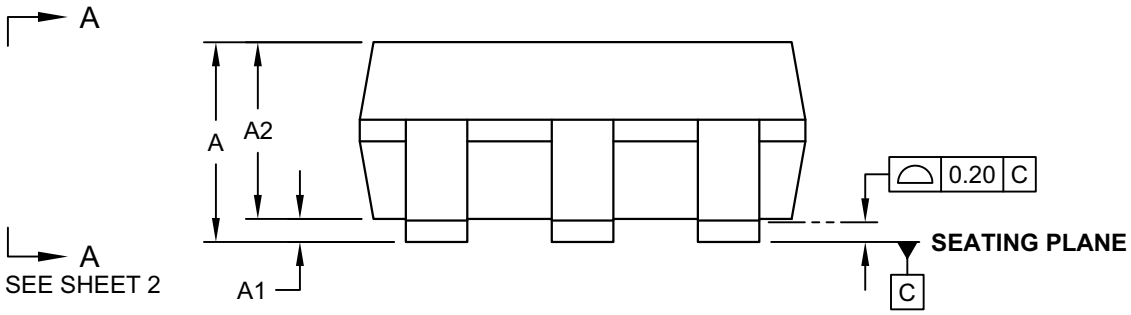
5-Lead Plastic Small Outline Transistor (OT) [SOT23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

Microchip Technology Drawing C04-091-OT Rev F Sheet 1 of 2

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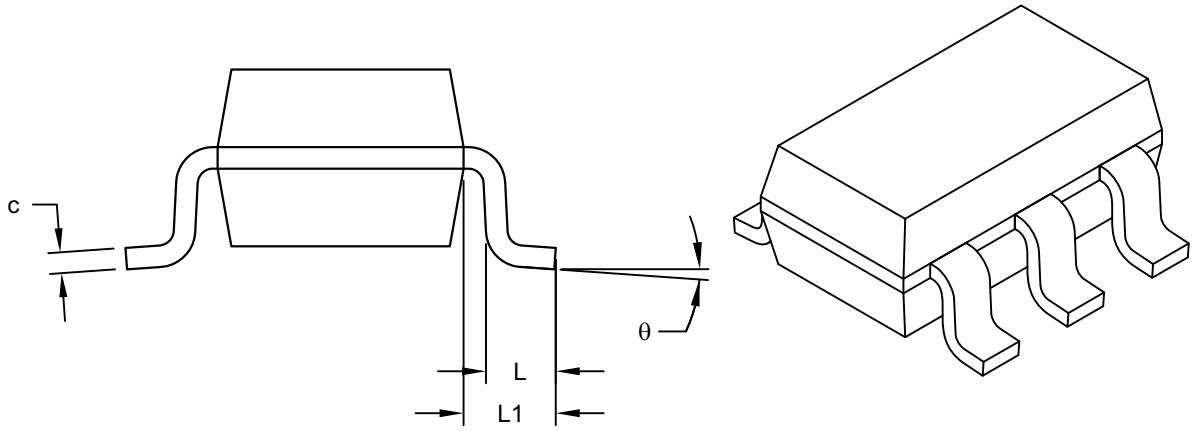
5-Lead Plastic Small Outline Transistor (OT) [SOT23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW A-A
SHEET 1

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	5		
Pitch	e	0.95 BSC		
Outside lead pitch	e1	1.90 BSC		
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	-	1.30
Standoff	A1	-	-	0.15
Overall Width	E	2.80 BSC		
Molded Package Width	E1	1.60 BSC		
Overall Length	D	2.90 BSC		
Foot Length	L	0.30	-	0.60
Footprint	L1	0.60 REF		
Foot Angle	ϕ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-091-OT Rev F Sheet 2 of 2

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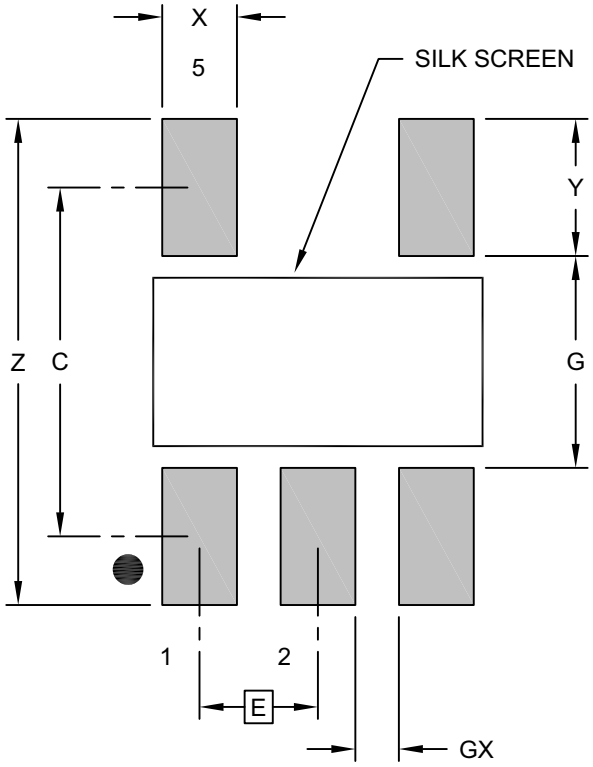
5-Lead Plastic Small Outline Transistor (OT) [SOT23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091-OT Rev F

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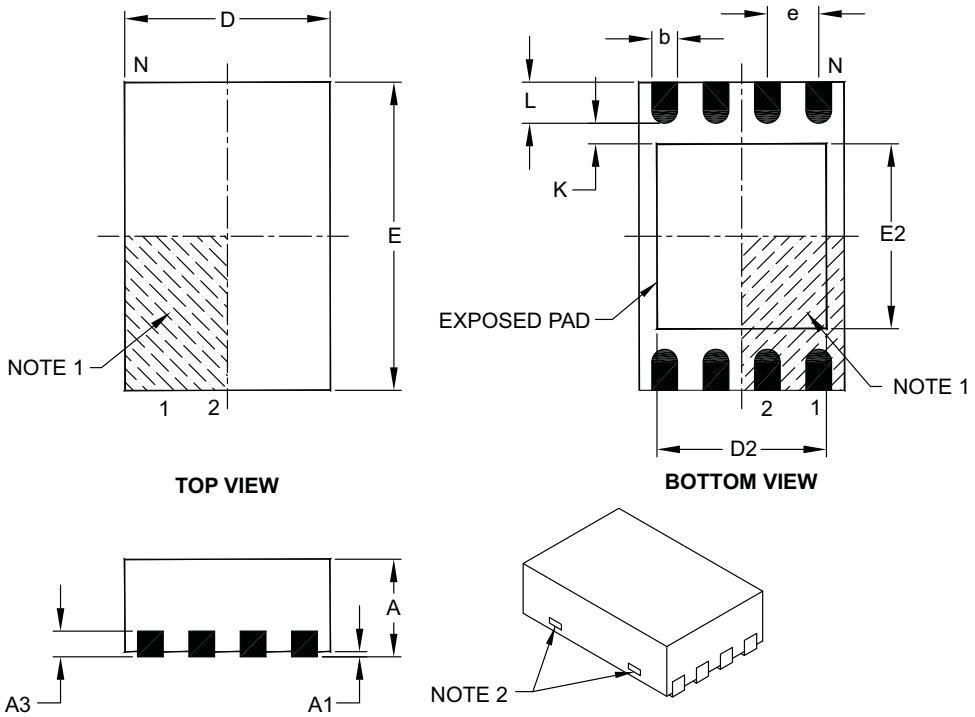
8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Length	D	2.00 BSC		
Overall Width	E	3.00 BSC		
Exposed Pad Length	D2	1.30	–	1.55
Exposed Pad Width	E2	1.50	–	1.75
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123C

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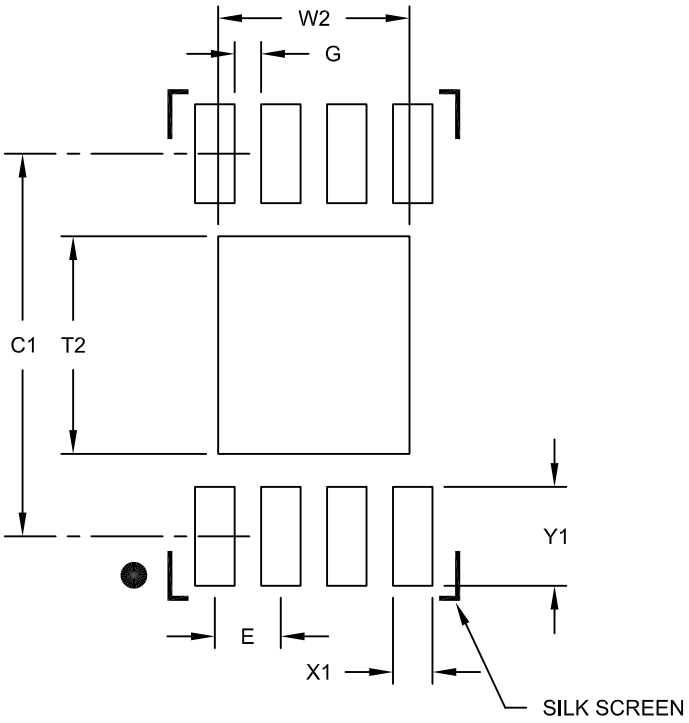
8-Lead Plastic Dual Flat, No Lead Package (MC) - 2x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			1.45
Optional Center Pad Length	T2			1.75
Contact Pad Spacing	C1		2.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2123B

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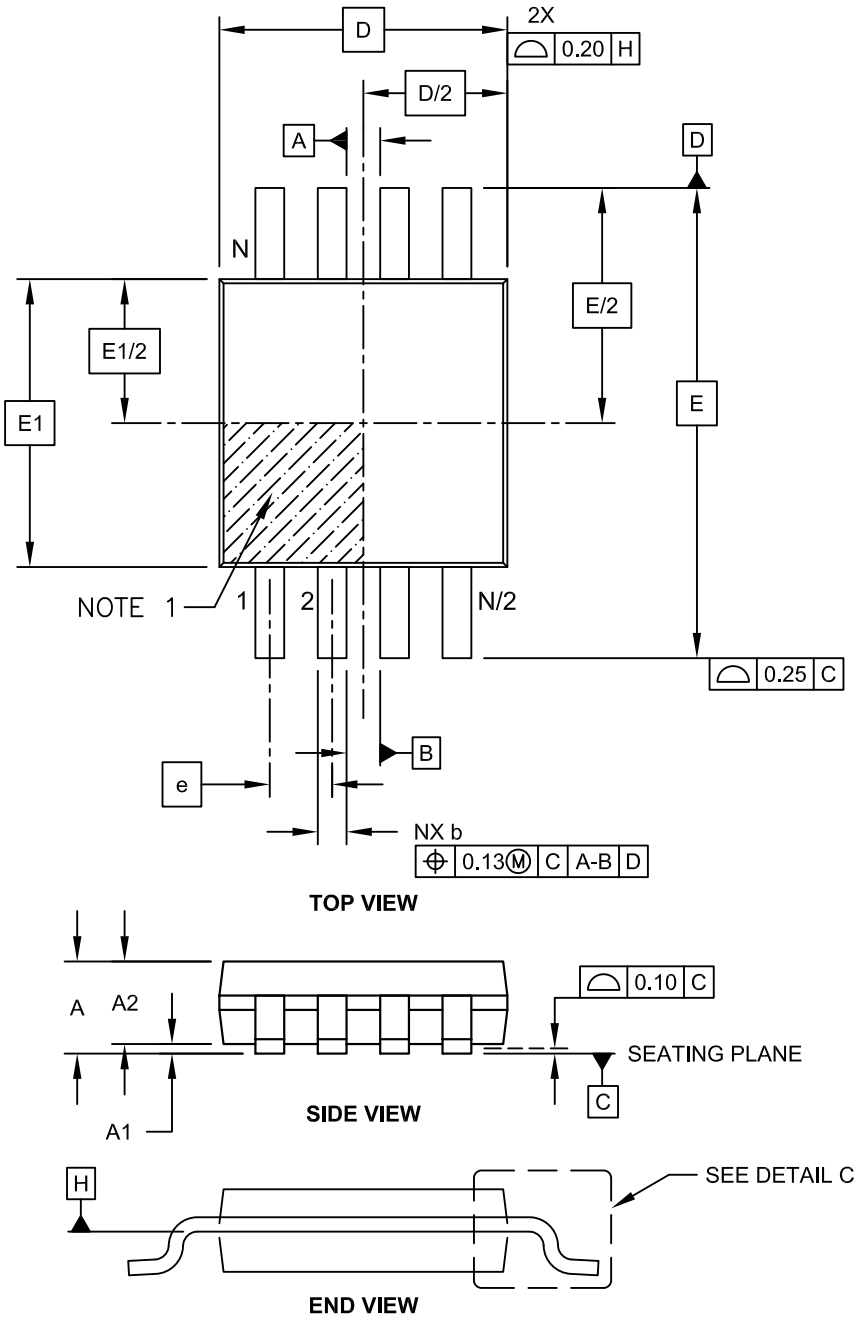
8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-111C Sheet 1 of 2

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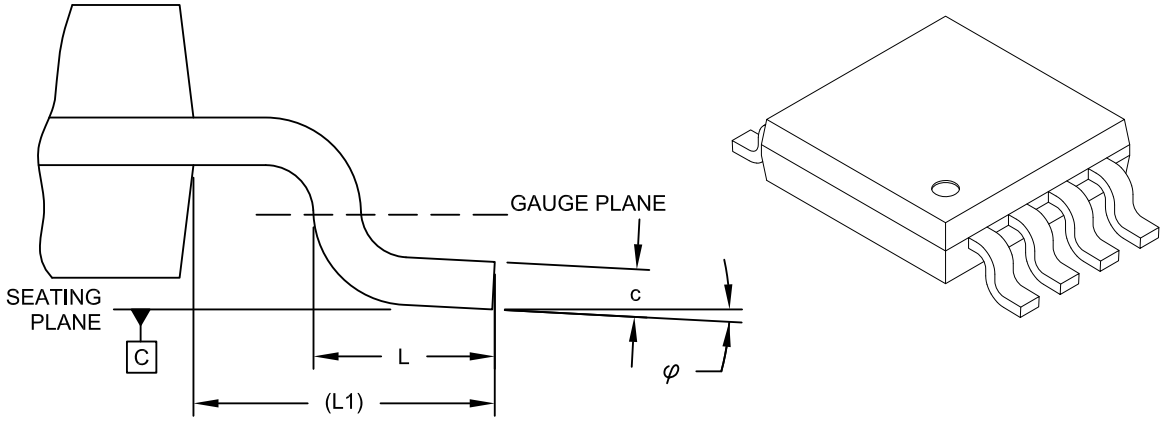
8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.22	-	0.40

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

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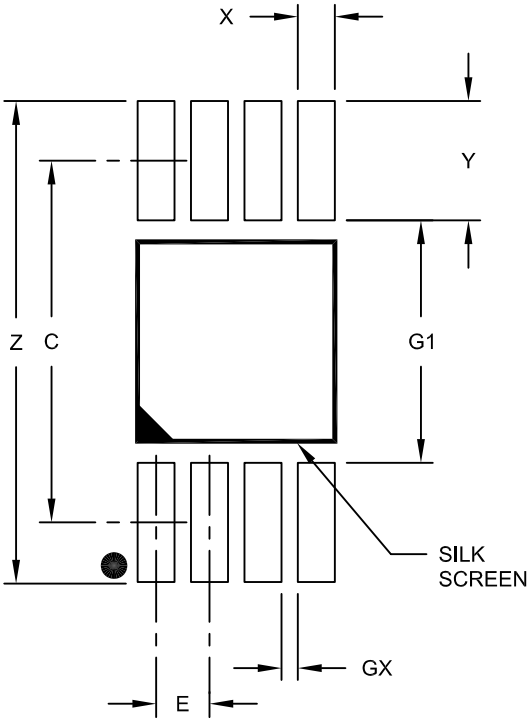
8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A

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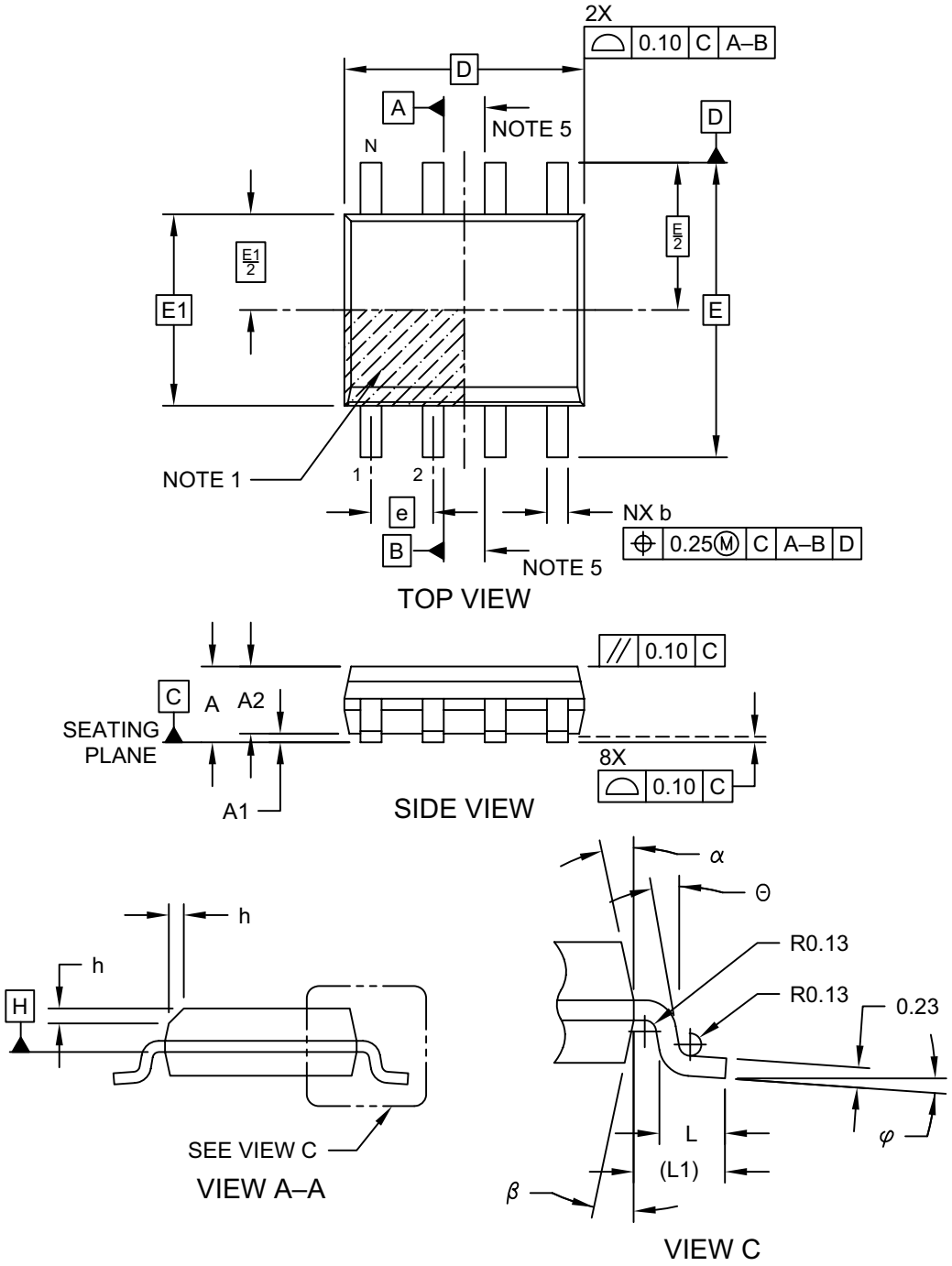
8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SN Rev E Sheet 1 of 2

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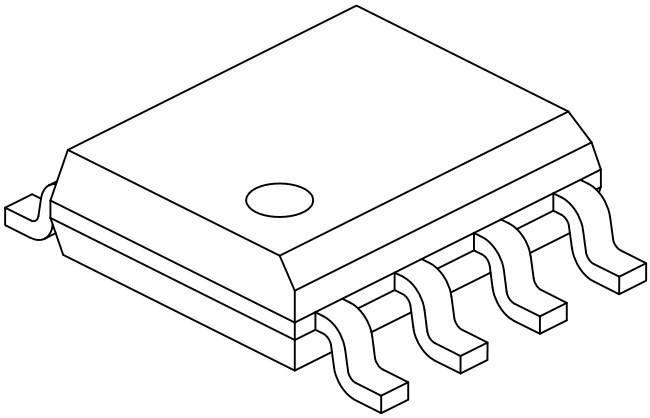
8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev E Sheet 2 of 2

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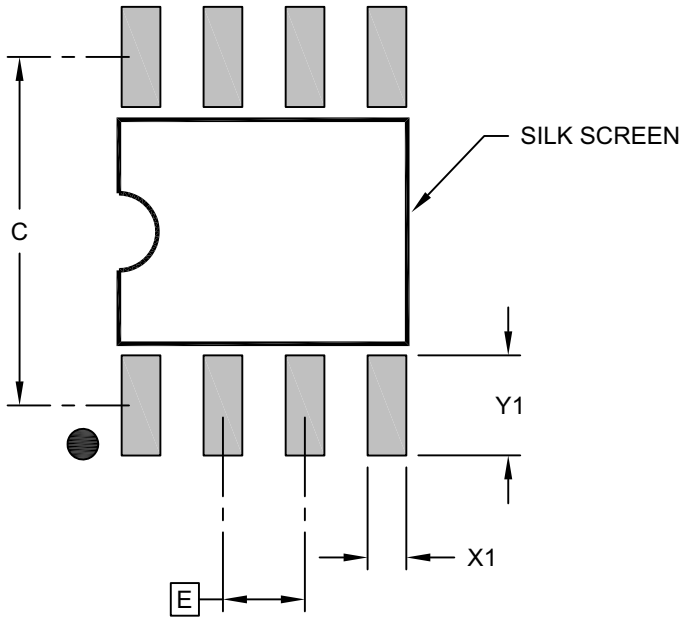
8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev E

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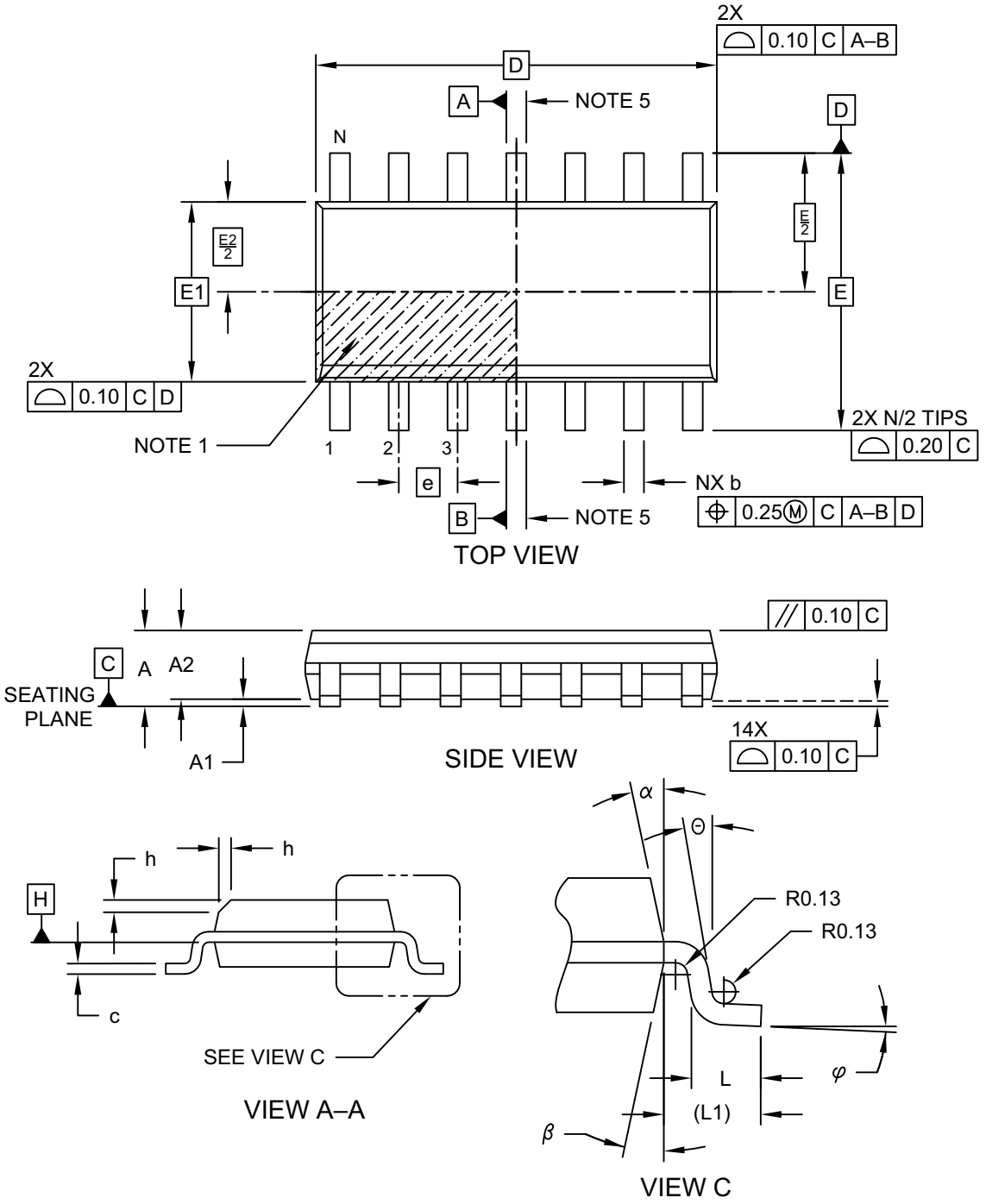
14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-065-SL Rev D Sheet 1 of 2

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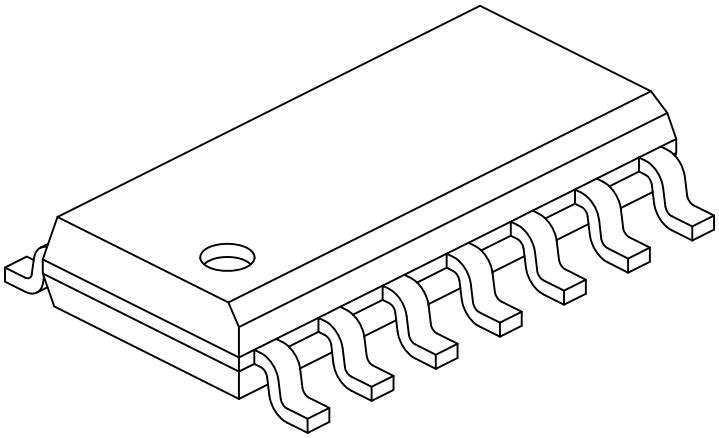
14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	8.65 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065-SL Rev D Sheet 2 of 2

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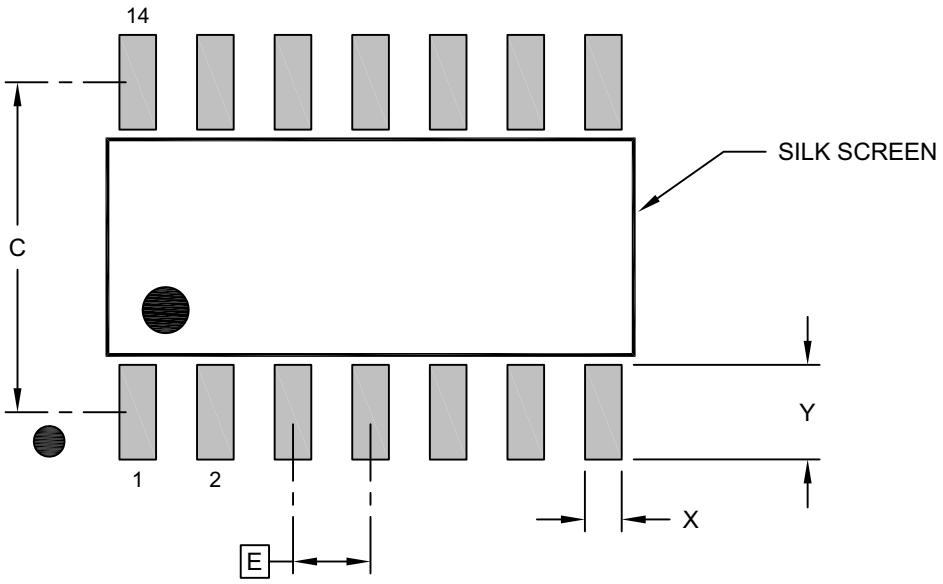
14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X14)	X			0.60
Contact Pad Length (X14)	Y			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065-SL Rev D

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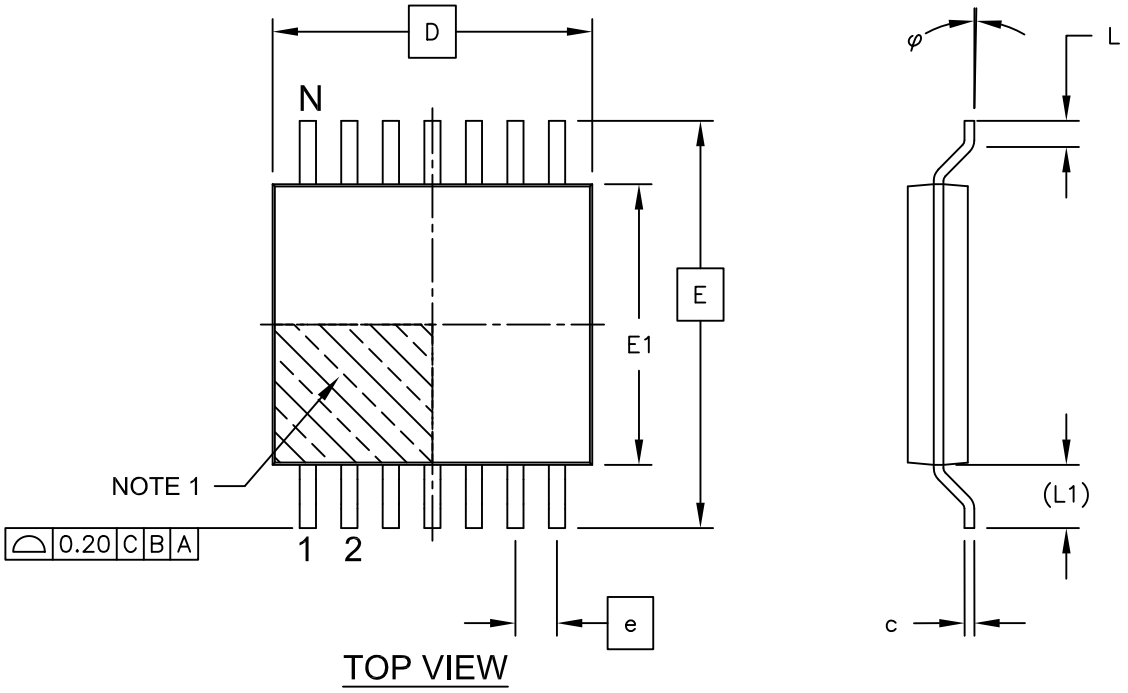
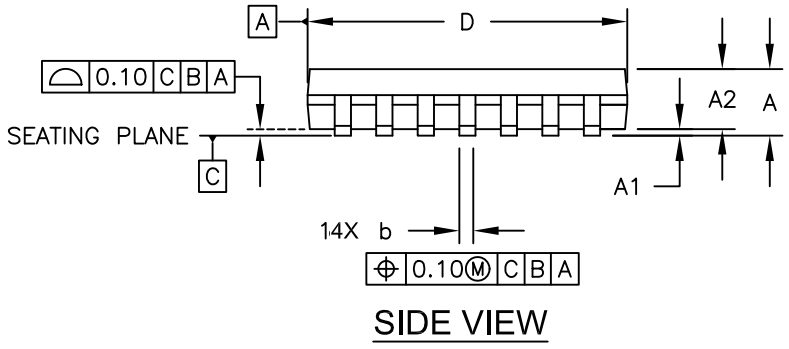
14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Microchip Technology Drawing C04-087C Sheet 1 of 2

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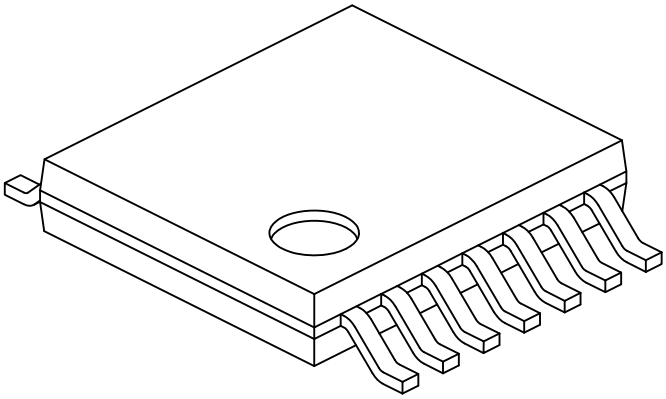
14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	0.65 BSC		
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	0.15
Overall Width	E	6.40 BSC		
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	(L1)	1.00 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.19	-	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-087C Sheet 2 of 2

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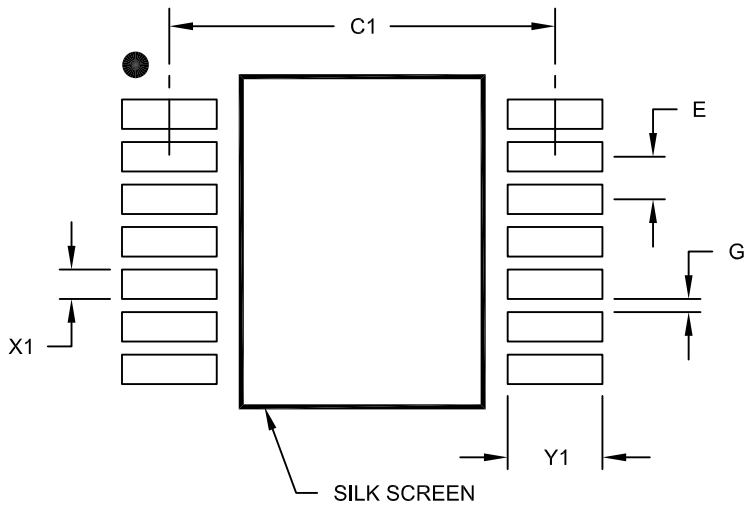
14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X14)	X1			0.45
Contact Pad Length (X14)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2087A

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APPENDIX A: REVISION HISTORY

Revision C (October 2019)

The following is the list of modifications:

1. Updated **Section 6.0 "Packaging Information"**.

Revision B (March 2008)

The following is the list of modifications:

1. Added SOT-23-5 and 2x3 DFN packages.
2. Added test circuits.
3. Corrected V_{OS} temperature drift information.
4. Added Section 4.9.3.
5. Updated Package Marking Information.
6. Updated all package outline drawings and added package outline drawings for SOT-23-5 and 2x3 DFN packages.
7. Added Landing Pattern drawings for 2x3 DFN and 8-lead SOIC packages.
8. Updated information in Product Identification System for SOT-23-5 and 2x3 DFN packages.

Revision A (March 2007)

- Original Release of this Document.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	MCP6031:	Single Op Amp
	MCP6031T:	Single Op Amp (Tape and Reel)
	MCP6032:	Dual Op Amp
	MCP6032T:	Dual Op Amp (Tape and Reel)
	MCP6033:	Single Op Amp with Chip Select
	MCP6033T:	Single Op Amp with Chip Select (Tape and Reel)
	MCP6034:	Quad Op Amp
	MCP6034T:	Quad Op Amp (Tape and Reel)
Temperature Range:	E = -40°C to +125°C	
Package:	MC = Plastic Dual Flat, No Lead, (2x3 mm DFN) 8-Lead**	
	MS = Plastic MSOP, 8-Lead	
	OT = Plastic Small Outline Transistor (SOT-23), 5-Lead*	
	SL = Plastic SOIC (3.90 mm Body), 14-Lead	
	SN = Plastic SOIC, (3.90 mm Body), 8-Lead	
	ST = Plastic TSSOP (4.4 mm Body), 14-Lead	

* This package is only available on the MCP6031 device.
** These packages are only available on the MCP6031 and MCP6033 devices.

Examples:

a) MCP6031-E/SN: 8-Lead SOIC Package.
b) MCP6031T-E/SN: Tape and Reel, 8-Lead SOIC Package.
c) MCP6031-E/MS: 8-Lead MSOP Package.
d) MCP6031T-E/MS: Tape and Reel, 8-Lead MSOP Package.
e) MCP6031-E/MC: 8-Lead DFN Package.
f) MCP6031T-E/MC: Tape and Reel, 8-Lead DFN Package.
g) MCP6031T-E/OT: Tape and Reel, 5-Lead SOT-23 Package.

a) MCP6032-E/SN: 8-Lead SOIC Package.
b) MCP6032T-E/SN: Tape and Reel, 8-Lead SOIC Package.
c) MCP6032-E/MS: 8-Lead MSOP Package.
d) MCP6032T-E/MS: Tape and Reel 8-Lead MSOP Package.

a) MCP6033-E/SN: 8-Lead SOIC Package.
b) MCP6033T-E/SN: Tape and Reel, 8-Lead SOIC Package.
c) MCP6033-E/MS: 8-Lead MSOP Package.
d) MCP6033T-E/MS: Tape and Reel, 8-Lead MSOP Package.
e) MCP6033-E/MC: 8-Lead DFN Package.
f) MCP6033T-E/MC: Tape and Reel, 8-Lead DFN Package.

a) MCP6034-E/SL: 14-Lead SOIC Package.
b) MCP6034T-E/SL: Tape and Reel, 14-Lead SOIC Package.
c) MCP6034-E/ST: 14-Lead TSSOP Package.
d) MCP6034T-E/ST: Tape and Reel, 14-Lead TSSOP Package.

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- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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