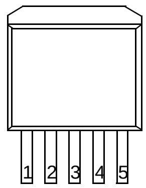
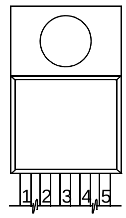
Package Types

MCP1825

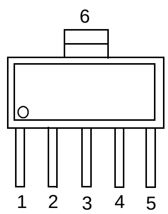
DDPAK-5 **TO-220-5**

Fixed/Adjustable





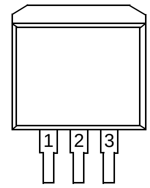
SOT-223-5

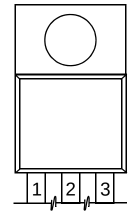


Pin	Fixed	Adjustable
1	$\overline{SHDN}$	$\overline{SHDN}$
2	V_{IN}	V_{IN}
3	GND (TAB)	GND (TAB)
4	V_{OUT}	V_{OUT}
5	PWRGD	ADJ
6	GND (TAB)	GND (TAB)

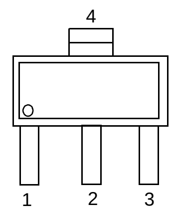
MCP1825S

DDPAK-3 **TO-220-3**





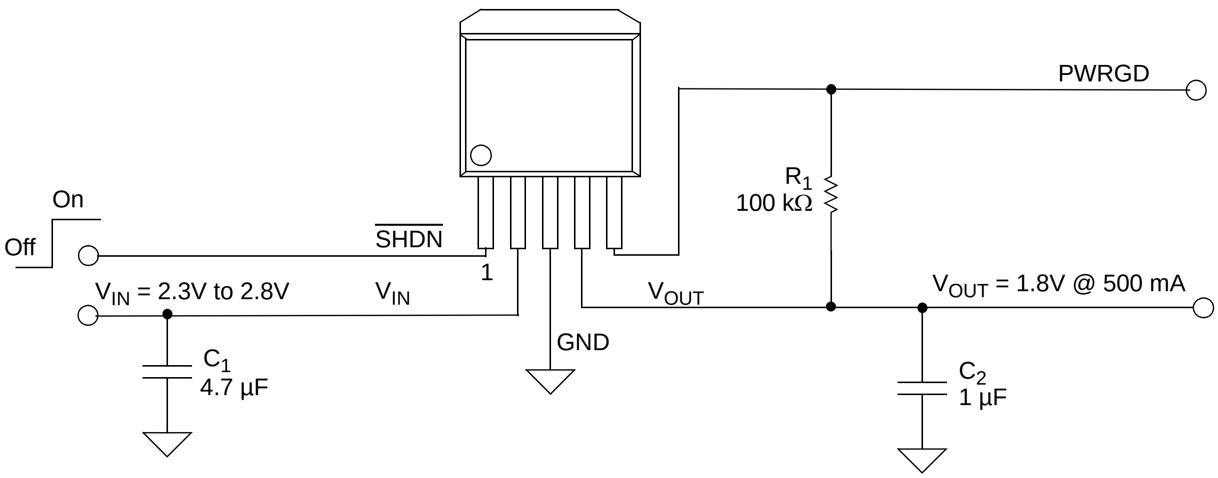
SOT-223-3



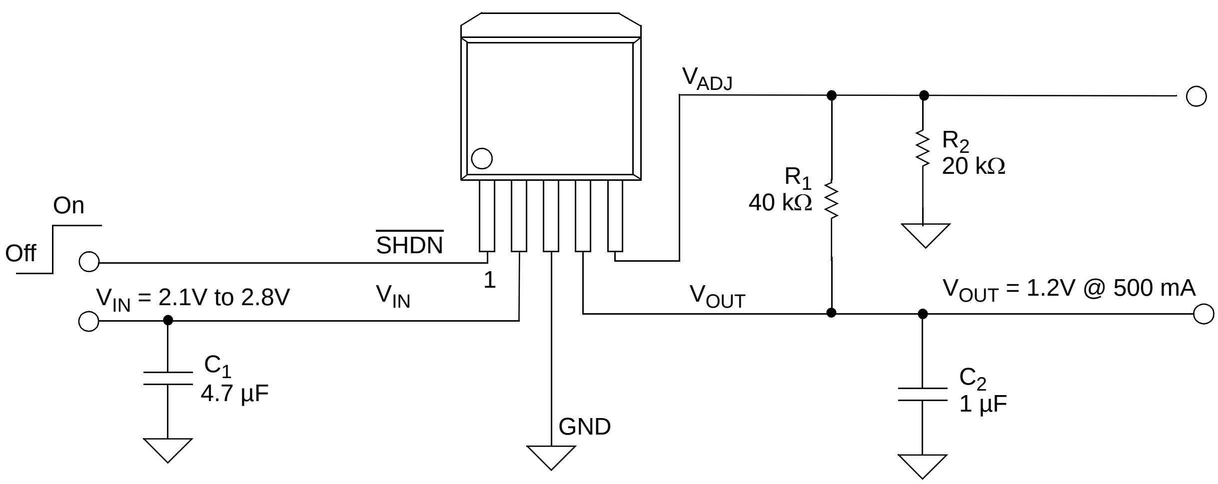
Pin	
1	V_{IN}
2	GND (TAB)
3	V_{OUT}
4	GND (TAB)

Typical Applications

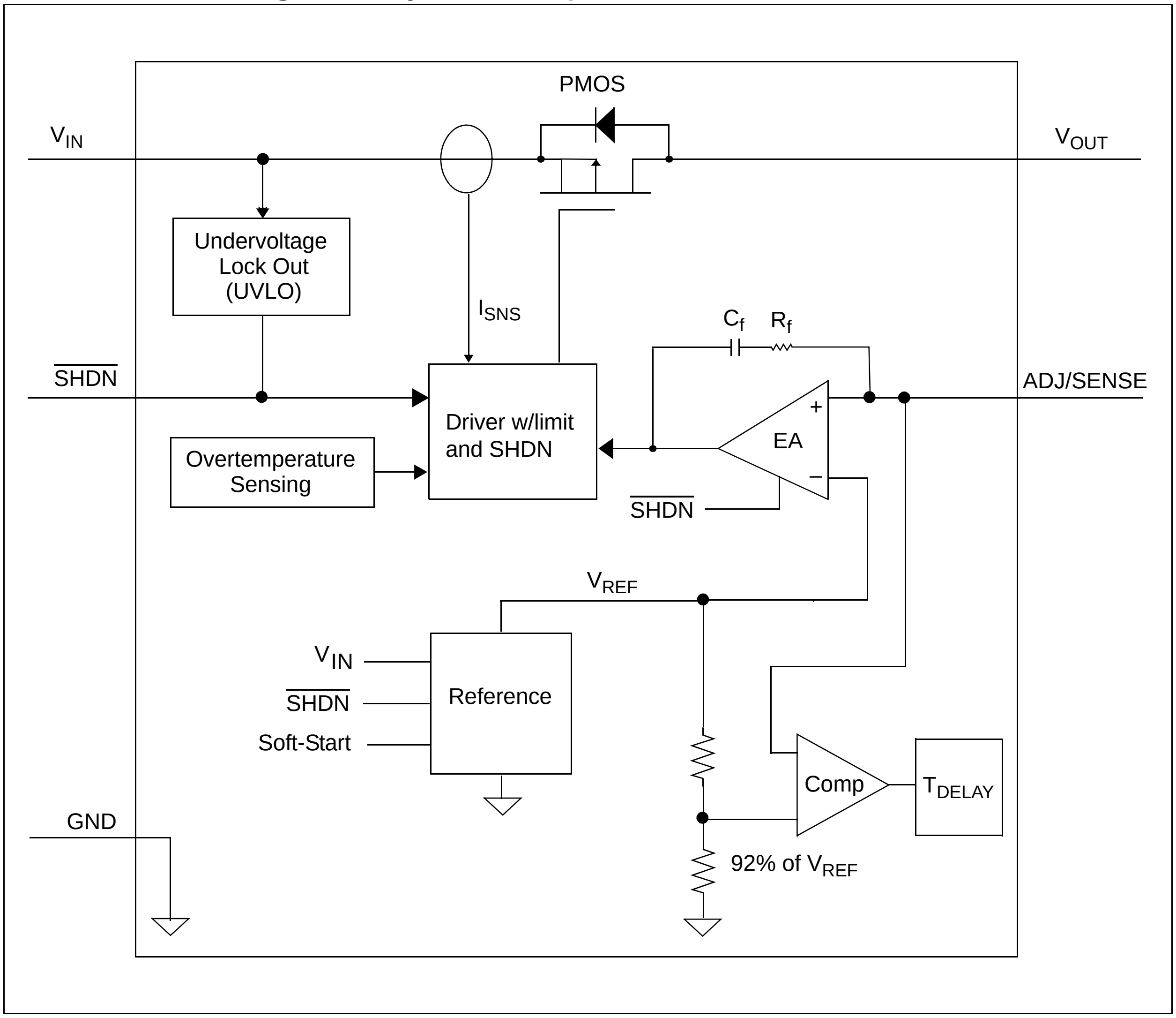
MCP1825 Fixed Output Voltage



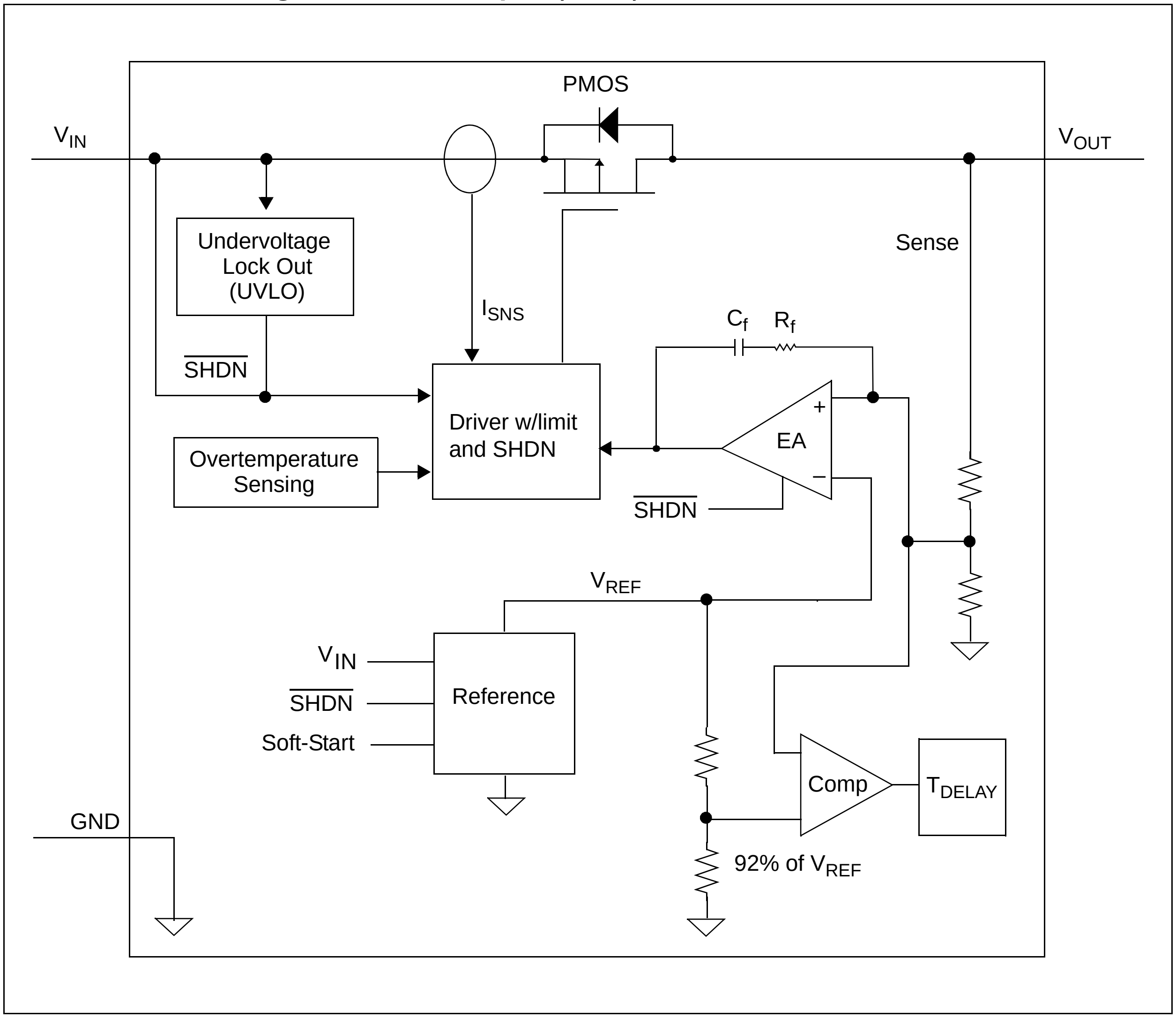
MCP1825 Adjustable Output Voltage



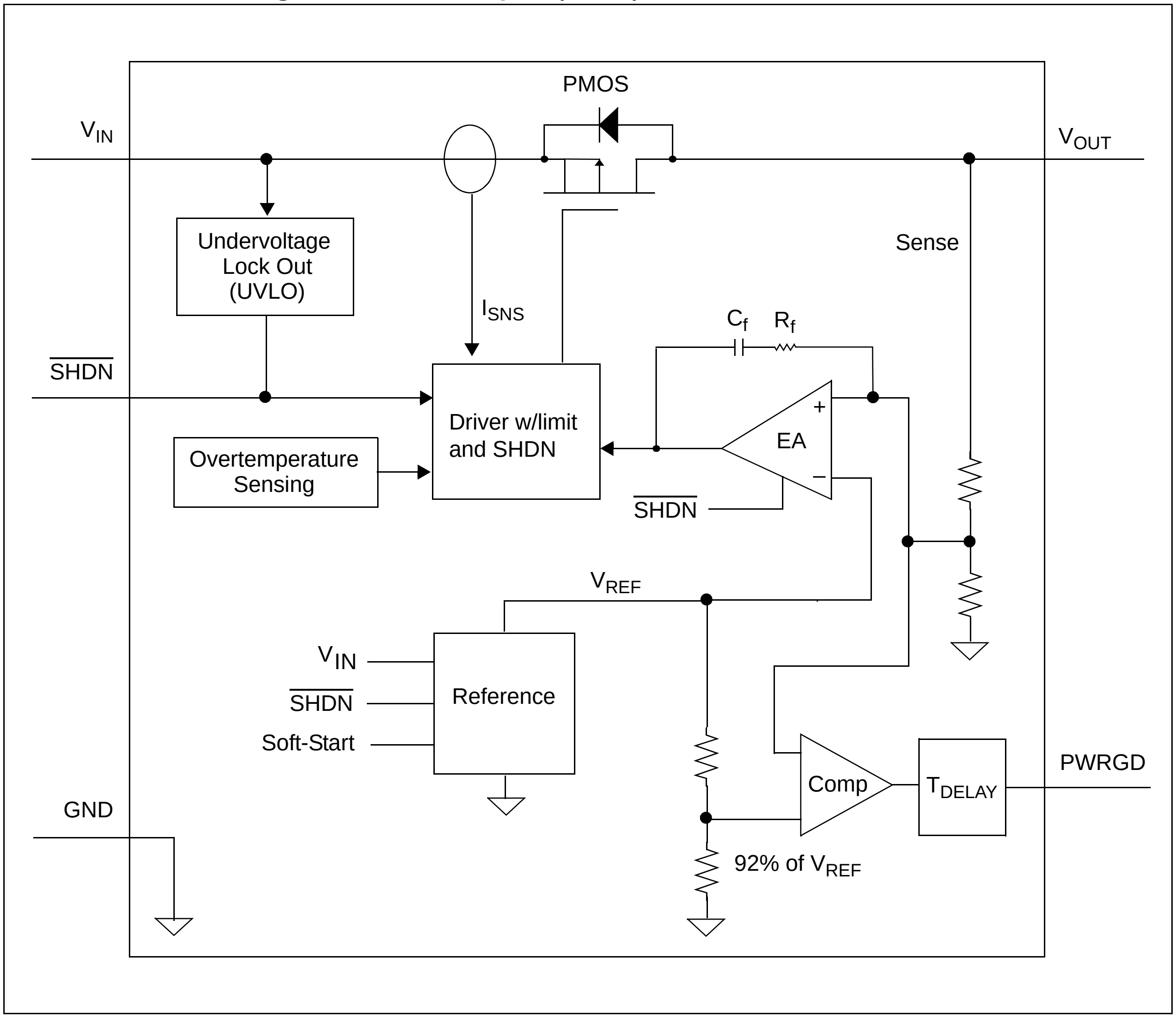
Functional Block Diagram - Adjustable Output



Functional Block Diagram - Fixed Output (3-Pin)



Functional Block Diagram - Fixed Output (5-Pin)



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{IN} 6.5V

Maximum Voltage on Any Pin .. (GND – 0.3V) to (V_{DD} + 0.3)V

Maximum Power Dissipation......... Internally-Limited (**Note 6**)

Output Short Circuit Duration ....Continuous

Storage temperature ....-65°C to +150°C

Maximum Junction Temperature, T_J ....+150°C

ESD protection on all pins (HBM/MM) .... ≥ 4 kV; ≥ 300V

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

AC/DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, $V_{IN} = V_{OUT(MAX)} + V_{DROPOUT(MAX)}$, **Note 1**, V_R = 1.8V for Adjustable Output, I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 4.7 µF (X7R Ceramic), T_A = +25°C.
Boldface type applies for junction temperatures, T_J (**Note 7**) of **-40°C to +125°C**

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Operating Voltage	V_{IN}	**2.1**		**6.0**	V	**Note 1**
Input Quiescent Current	I_q	—	120	**220**	µA	I_L = 0 mA, V_{OUT} = 0.8V to 5.0V
Input Quiescent Current for $\overline{SHDN}$ Mode	$I_{\overline{SHDN}}$	—	0.1	**3**	µA	$\overline{SHDN}$ = GND
Maximum Output Current	I_{OUT}	**500**	—	—	mA	V_{IN} = 2.1V to 6.0V V_R = 0.8V to 5.0V, **Note 1**
Line Regulation	$\Delta V_{OUT}/(V_{OUT} \times \Delta V_{IN})$	—	±0.05	±0.**16**	%/V	**(Note 1)** $\le V_{IN} \le$ 6V
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	**-1.0**	±0.5	**1.0**	%	I_{OUT} = 1 mA to 500 mA, (**Note 4**)
Output Short Circuit Current	I_{OUT_SC}	—	1.2	—	A	$R_{LOAD} < 0.1\Omega$, Peak Current
Adjust Pin Characteristics (Adjustable Output Only)						
Adjust Pin Reference Voltage	V_{ADJ}	**0.402**	0.410	**0.418**	V	V_{IN} = 2.1V to V_{IN} = 6.0V, I_{OUT} = 1 mA
Adjust Pin Leakage Current	I_{ADJ}	-10	±0.01	+10	nA	V_{IN} = 6.0V, V_{ADJ} = 0V to 6V
Adjust Temperature Coefficient	TCV_{OUT}	—	40	—	ppm/°C	**Note 3**
Fixed-Output Characteristics (Fixed Output Only)						
Voltage Regulation	V_{OUT}	**V_R - 2.5%**	V_R ±0.5%	**V_R + 2.5%**	V	**Note 2**

Note 1: The minimum V_{IN} must meet two conditions: $V_{IN} \ge$ 2.1V and $V_{IN} \ge V_{OUT(MAX)} + V_{DROPOUT(MAX)}$.

2: V_R is the nominal regulator output voltage for the fixed cases. V_R = 1.2V, 1.8V, etc. V_R is the desired set point output voltage for the adjustable cases. $V_R = V_{ADJ} * ((R_1/R_2)+1)$. Figure 4-1.

3: $TCV_{OUT} = (V_{OUT-HIGH} - V_{OUT-LOW}) *10^6 / (V_R * \Delta Temperature)$. $V_{OUT-HIGH}$ is the highest voltage measured over the temperature range. $V_{OUT-LOW}$ is the lowest voltage measured over the temperature range.

4: Load regulation is measured at a constant junction temperature using low duty-cycle pulse testing. Load regulation is tested over a load range from 1 mA to the maximum specified output current.

5: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value that was measured with an input voltage of $V_{IN} = V_{OUT(MAX)} + V_{DROPOUT(MAX)}$.

6: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above 150°C can impact device reliability.

7: The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in the junction temperature over the ambient temperature is not significant.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, $V_{IN} = V_{OUT(MAX)} + V_{DROPOUT(MAX)}$, **Note 1**, V_R = 1.8V for Adjustable Output, I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 4.7 µF (X7R Ceramic), T_A = +25°C.
Boldface type applies for junction temperatures, T_J (**Note 7**) of **-40°C to +125°C**

Parameters	Sym	Min	Typ	Max	Units	Conditions
Dropout Characteristics						
Dropout Voltage	$V_{DROPOUT}$	—	210	**350**	mV	**Note 5**, I_{OUT} = 500 mA, $V_{IN(MIN)}$ = 2.1V
Power Good Characteristics						
PWRGD Input Voltage Operating Range	V_{PWRGD_VIN}	1.0 **1.2**	— —	6.0 **6.0**	V	T_A = +25°C T_A = -40°C to +125°C For V_{IN} < 2.1V, I_{SINK} = 100 µA
PWRGD Threshold Voltage (Referenced to V_{OUT})	V_{PWRGD_TH}	 **89** **90**	 92 92	 **95** **94**	$\%V_{OUT}$	Falling Edge V_{OUT} < 2.5V Fixed, V_{OUT} = Adj. V_{OUT} >= 2.5V Fixed
PWRGD Threshold Hysteresis	V_{PWRGD_HYS}	**1.0**	2.0	**3.0**	$\%V_{OUT}$	
PWRGD Output Voltage Low	V_{PWRGD_L}	—	0.2	**0.4**	V	$I_{PWRGD\ SINK}$ = 1.2 mA, ADJ = 0V
PWRGD Leakage	P_{WRGD_LK}	—	1	—	nA	$V_{PWRGD} = V_{IN}$ = 6.0V
PWRGD Time Delay	T_{PG}	—	110	—	µs	Rising Edge R_{PULLUP} = 10 kΩ
Detect Threshold to PWRGD Active Time Delay	$T_{VDET\text{-}PWRGD}$	—	200	—	µs	$V_{OUT} = V_{PWRGD\_TH}$ + 20 mV to V_{PWRGD_TH} - 20 mV
Shutdown Input						
Logic High Input	$V_{SHDN\text{-}HIGH}$	**45**	—	—	$\%V_{IN}$	V_{IN} = 2.1V to 6.0V
Logic Low Input	$V_{SHDN\text{-}LOW}$	—	—	**15**	$\%V_{IN}$	V_{IN} = 2.1V to 6.0V
$\overline{SHDN}$ Input Leakage Current	$\overline{SHDN}_{ILK}$	**-0.1**	±0.001	**+0.1**	µA	V_{IN} = 6V, $\overline{SHDN} = V_{IN}$, $\overline{SHDN}$ = GND
AC Performance						
Output Delay From $\overline{SHDN}$	T_{OR}	—	100	—	µs	$\overline{SHDN}$ = GND to V_{IN}, V_{OUT} = GND to 95% V_R
Output Noise	e_N	—	2.0	—	µV/√Hz	I_{OUT} = 200 mA, f = 1 kHz, C_{OUT} = 10 µF (X7R Ceramic), V_{OUT} = 2.5V

Note 1: The minimum V_{IN} must meet two conditions: $V_{IN} \geq 2.1V$ and $V_{IN} \geq V_{OUT(MAX)} + V_{DROPOUT(MAX)}$.

2: V_R is the nominal regulator output voltage for the fixed cases. V_R = 1.2V, 1.8V, etc. V_R is the desired set point output voltage for the adjustable cases. $V_R = V_{ADJ} * ((R_1/R_2)+1)$. Figure 4-1.

3: $TCV_{OUT} = (V_{OUT\text{-}HIGH} - V_{OUT\text{-}LOW}) * 10^6 / (V_R * \Delta Temperature)$. $V_{OUT\text{-}HIGH}$ is the highest voltage measured over the temperature range. $V_{OUT\text{-}LOW}$ is the lowest voltage measured over the temperature range.

4: Load regulation is measured at a constant junction temperature using low duty-cycle pulse testing. Load regulation is tested over a load range from 1 mA to the maximum specified output current.

5: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value that was measured with an input voltage of $V_{IN} = V_{OUT(MAX)} + V_{DROPOUT(MAX)}$.

6: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above 150°C can impact device reliability.

7: The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in the junction temperature over the ambient temperature is not significant.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, $V_{IN} = V_{OUT(MAX)} + V_{DROPOUT(MAX)}$, **Note 1**, V_R = 1.8V for Adjustable Output, I_{OUT} = 1 mA, $C_{IN} = C_{OUT}$ = 4.7 µF (X7R Ceramic), T_A = +25°C.
Boldface type applies for junction temperatures, T_J (**Note 7**) of **-40°C to +125°C**

Parameters	Sym	Min	Typ	Max	Units	Conditions
Power Supply Ripple Rejection Ratio	PSRR	—	60	—	dB	f = 100 Hz, C_{OUT} = 4.7 µF, I_{OUT} = 100 µA, V_{INAC} = 100 mV pk-pk, C_{IN} = 0 µF
Thermal Shutdown Temperature	T_{SD}	—	150	—	°C	I_{OUT} = 100 µA, V_{OUT} = 1.8V, V_{IN} = 2.8V
Thermal Shutdown Hysteresis	ΔT_{SD}	—	10	—	°C	I_{OUT} = 100 µA, V_{OUT} = 1.8V, V_{IN} = 2.8V

Note 1: The minimum V_{IN} must meet two conditions: $V_{IN} \geq 2.1V$ and $V_{IN} \geq V_{OUT(MAX)} + V_{DROPOUT(MAX)}$.

2: V_R is the nominal regulator output voltage for the fixed cases. V_R = 1.2V, 1.8V, etc. V_R is the desired set point output voltage for the adjustable cases. $V_R = V_{ADJ} * ((R_1/R_2)+1)$. Figure 4-1.

3: $TCV_{OUT} = (V_{OUT-HIGH} - V_{OUT-LOW}) *10^6 / (V_R * \Delta Temperature)$. $V_{OUT-HIGH}$ is the highest voltage measured over the temperature range. $V_{OUT-LOW}$ is the lowest voltage measured over the temperature range.

4: Load regulation is measured at a constant junction temperature using low duty-cycle pulse testing. Load regulation is tested over a load range from 1 mA to the maximum specified output current.

5: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value that was measured with an input voltage of $V_{IN} = V_{OUT(MAX)} + V_{DROPOUT(MAX)}$.

6: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above 150°C can impact device reliability.

7: The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in the junction temperature over the ambient temperature is not significant.

TEMPERATURE SPECIFICATIONS

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Operating Junction Temperature Range	T_J	-40	—	+125	°C	Steady State
Maximum Junction Temperature	T_J	—	—	+150	°C	Transient
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 3LD DDPAK	θ_{JA}	—	31.4	—	°C/W	4-Layer JC51 Standard Board
	θ_{JC}	—	3.0	—		
Thermal Resistance, 3LD TO-220	θ_{JA}	—	29.4	—	°C/W	4-Layer JC51 Standard Board
	θ_{JC}	—	2.0	—		
Thermal Resistance, 3LD SOT-223	θ_{JA}	—	62	—	°C/W	EIA/JEDEC JESD51-751-7 4 Layer Board
	θ_{JC}	—	15.0	—		
Thermal Resistance, 5LD DDPAK	θ_{JA}	—	31.2	—	°C/W	4-Layer JC51 Standard Board
	θ_{JC}	—	3.0	—		
Thermal Resistance, 5LD TO-220	θ_{JA}	—	29.3	—	°C/W	4-Layer JC51 Standard Board
	θ_{JC}	—	2.0	—		
Thermal Resistance, 5LD SOT-223	θ_{JA}	—	62	—	°C/W	EIA/JEDEC JESD51-751-7 4 Layer Board
	θ_{JC}	—	15.0	—		

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, C_{OUT} = 4.7 µF Ceramic (X7R), C_{IN} = 4.7 µF Ceramic (X7R), I_{OUT} = 1 mA, Temperature = +25°C, V_{IN} = V_{OUT} + 0.5V, Fixed output.

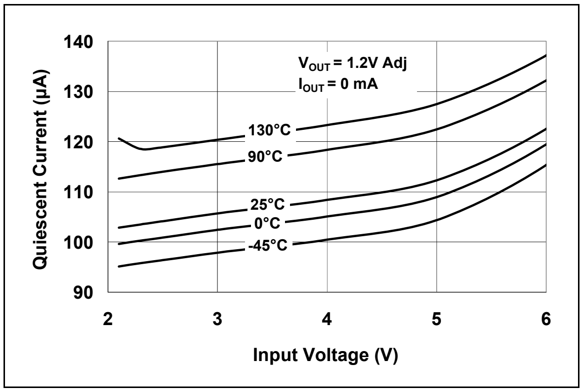


FIGURE 2-1: Quiescent Current vs. Input Voltage (Adjustable Version).

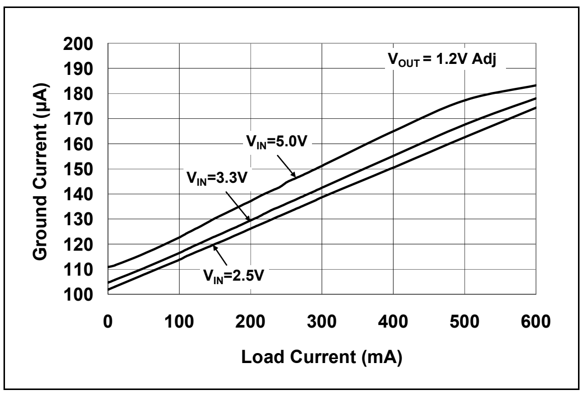


FIGURE 2-2: Ground Current vs. Load Current (Adjustable Version).

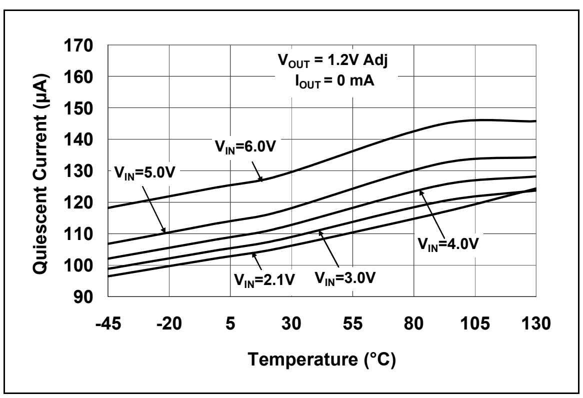


FIGURE 2-3: Quiescent Current vs. Junction Temperature (Adjustable Version).

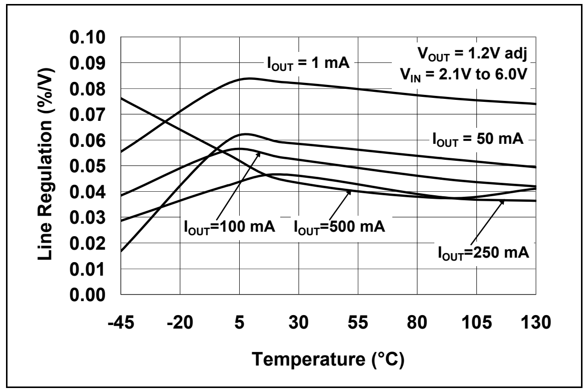


FIGURE 2-4: Line Regulation vs. Temperature (Adjustable Version).

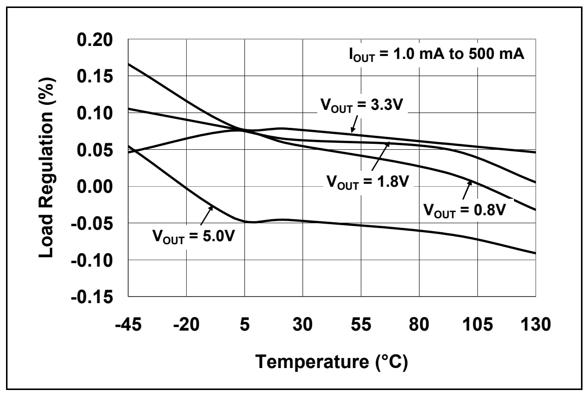


FIGURE 2-5: Load Regulation vs. Temperature (Adjustable Version).

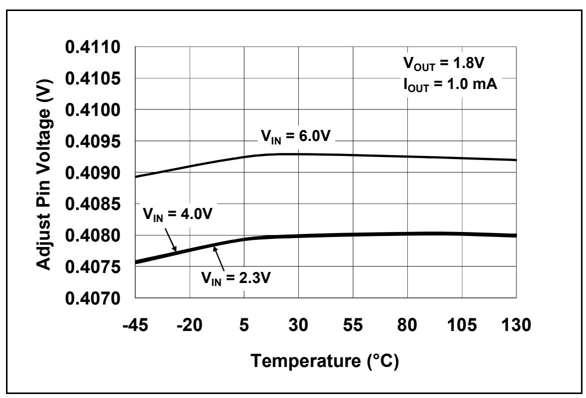


FIGURE 2-6: Adjust Pin Voltage vs. Temperature (Adjustable Version).

Note: Unless otherwise indicated, C_{OUT} = 4.7 µF Ceramic (X7R), C_{IN} = 4.7 µF Ceramic (X7R), I_{OUT} = 1 mA, Temperature = +25°C, V_{IN} = V_{OUT} + 0.5V, Fixed output.

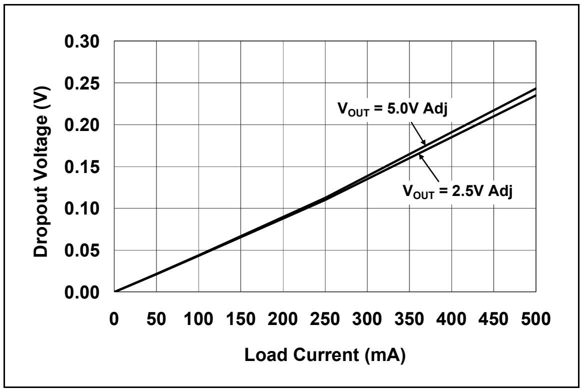


FIGURE 2-7: Dropout Voltage vs. Load Current (Adjustable Version).

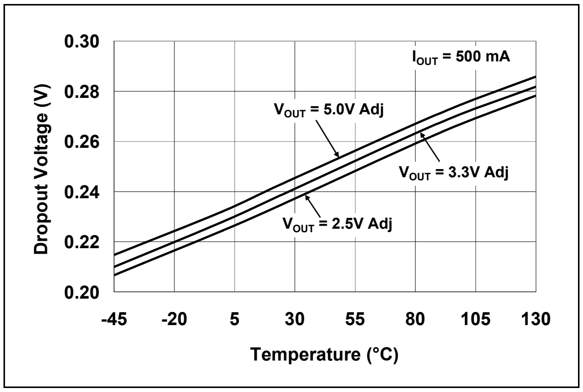


FIGURE 2-8: Dropout Voltage vs. Temperature (Adjustable Version).

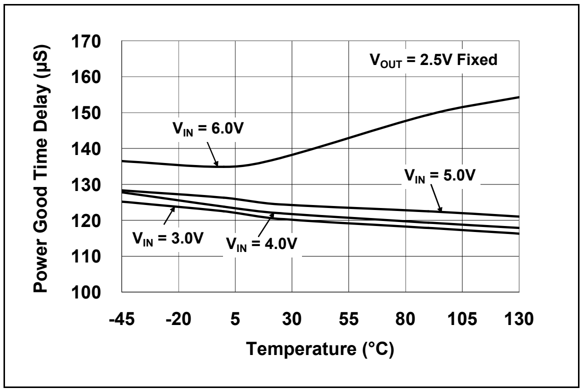


FIGURE 2-9: Power Good (PWRGD) Time Delay vs. Temperature.

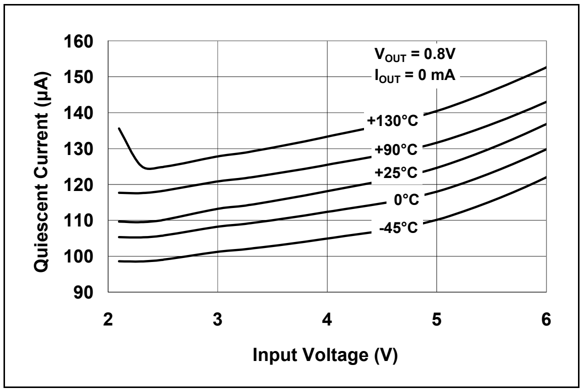


FIGURE 2-10: Quiescent Current vs. Input Voltage.

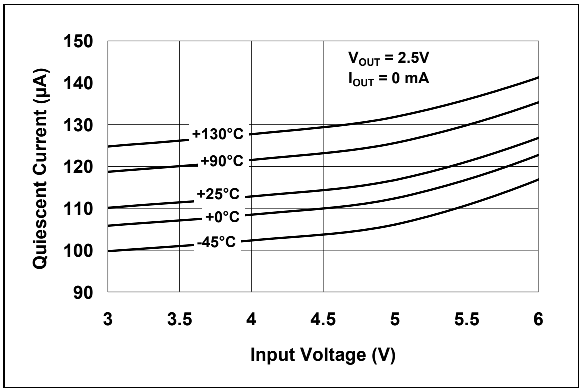


FIGURE 2-11: Quiescent Current vs. Input Voltage.

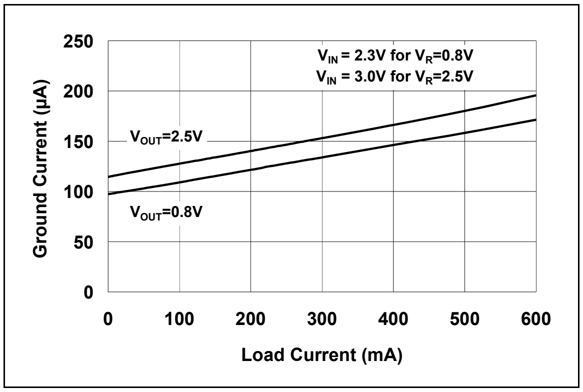


FIGURE 2-12: Ground Current vs. Load Current.

Note: Unless otherwise indicated, C_{OUT} = 4.7 µF Ceramic (X7R), C_{IN} = 4.7 µF Ceramic (X7R), I_{OUT} = 1 mA, Temperature = +25°C, V_{IN} = V_{OUT} + 0.5V, Fixed output.

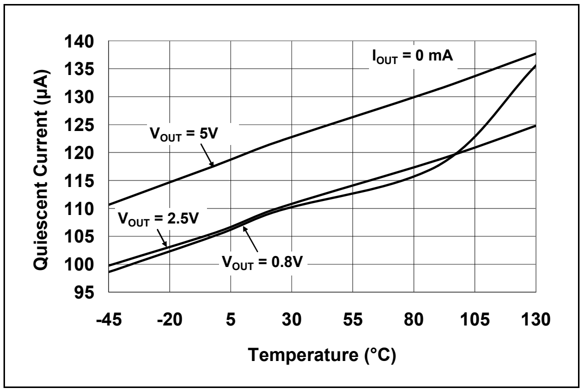


FIGURE 2-13: Quiescent Current vs. Temperature.

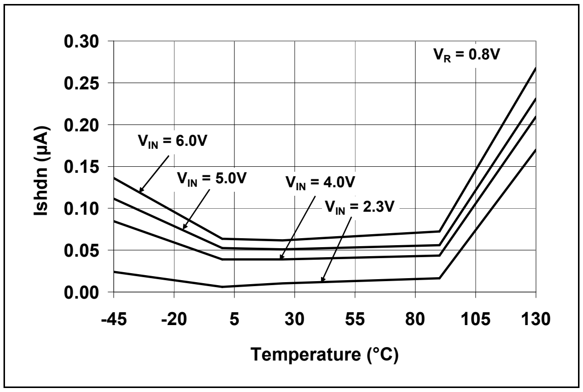


FIGURE 2-14: $I_{\overline{SHDN}}$ vs. Temperature.

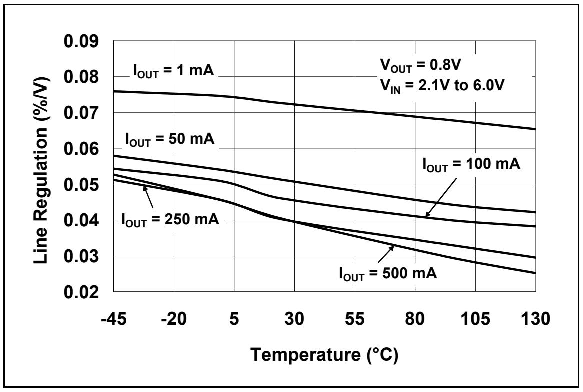


FIGURE 2-15: Line Regulation vs. Temperature.

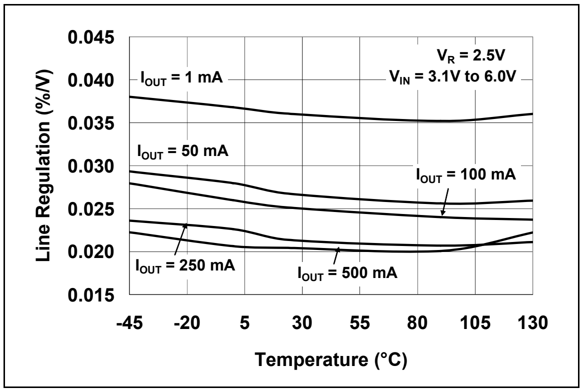


FIGURE 2-16: Line Regulation vs. Temperature.

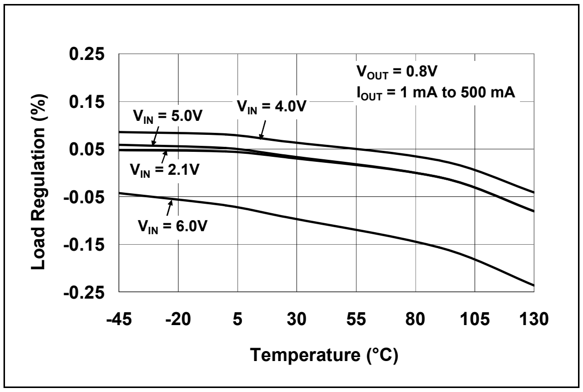


FIGURE 2-17: Load Regulation vs. Temperature (V_{OUT} < 2.5V Fixed).

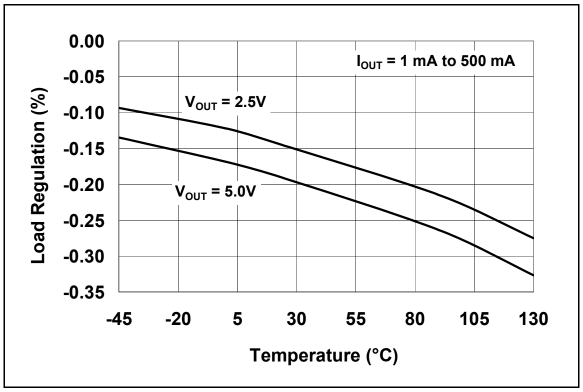


FIGURE 2-18: Load Regulation vs. Temperature ($V_{OUT} \geq$ 2.5V Fixed).

Note: Unless otherwise indicated, C_{OUT} = 4.7 µF Ceramic (X7R), C_{IN} = 4.7 µF Ceramic (X7R), I_{OUT} = 1 mA, Temperature = +25°C, V_{IN} = V_{OUT} + 0.5V, Fixed output.

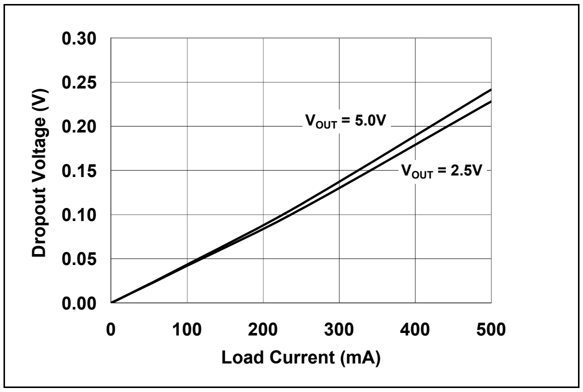


FIGURE 2-19: Dropout Voltage vs. Load Current.

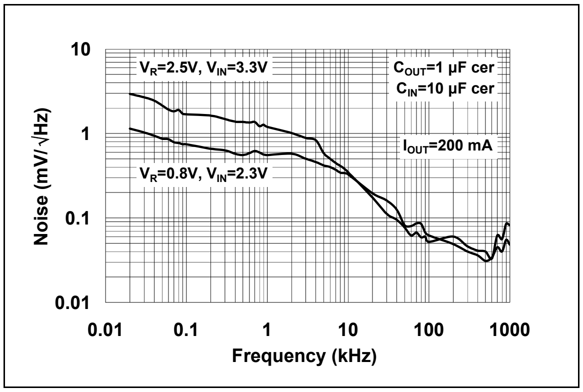


FIGURE 2-22: Output Noise Voltage Density vs. Frequency.

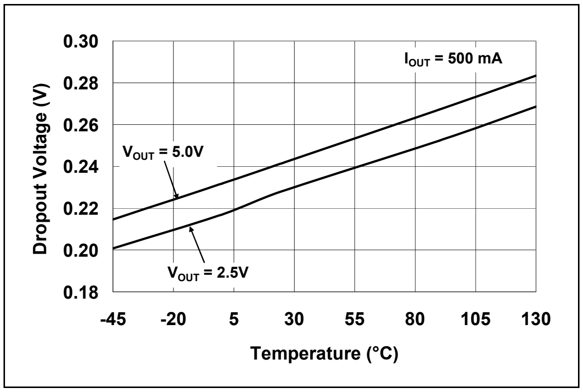


FIGURE 2-20: Dropout Voltage vs. Temperature.

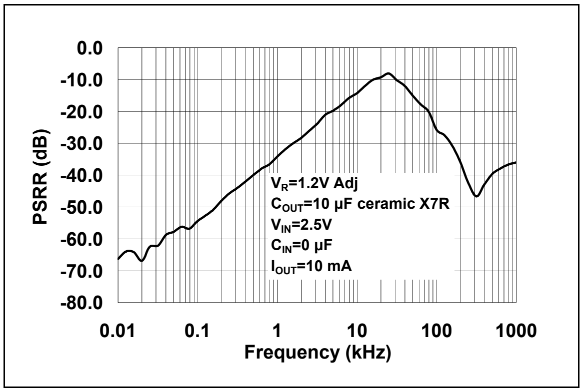


FIGURE 2-23: Power Supply Ripple Rejection (PSRR) vs. Frequency (Adj.).

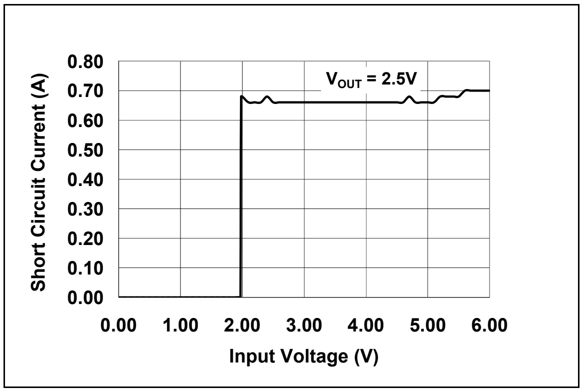


FIGURE 2-21: Short Circuit Current vs. Input Voltage.

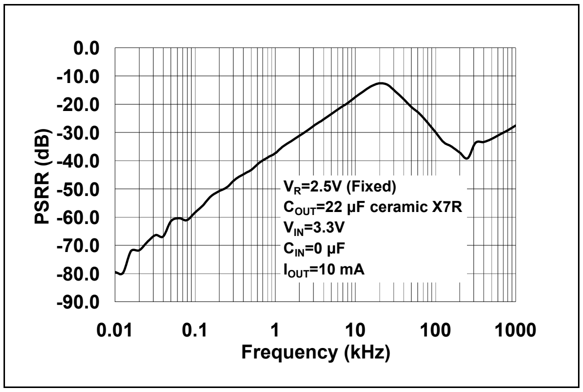


FIGURE 2-24: Power Supply Ripple Rejection (PSRR) vs. Frequency.

Note: Unless otherwise indicated, C_{OUT} = 4.7 µF Ceramic (X7R), C_{IN} = 4.7 µF Ceramic (X7R), I_{OUT} = 1 mA, Temperature = +25°C, V_{IN} = V_{OUT} + 0.5V, Fixed output.

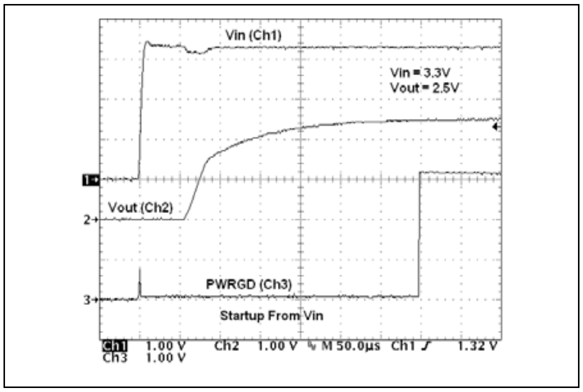


FIGURE 2-25: *2.5V (Adj.) Startup from V_{IN}.*

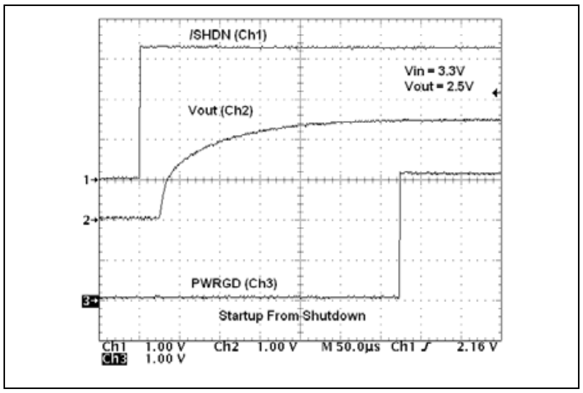


FIGURE 2-26: *2.5V (Adj.) Startup from Shutdown.*

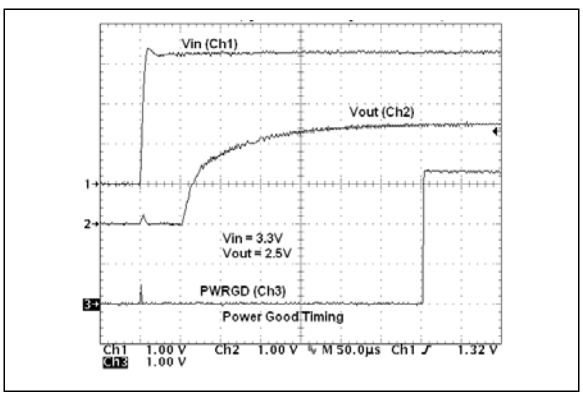


FIGURE 2-27: *Power Good (PWRGD) Timing.*

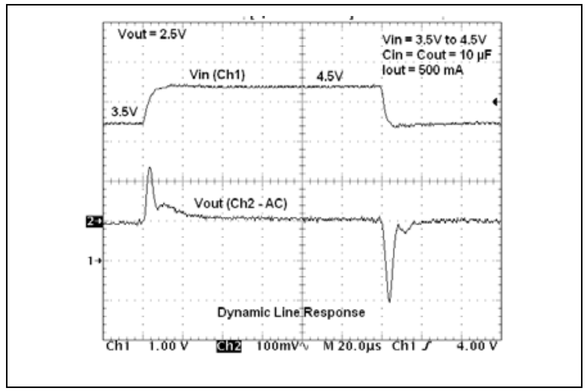


FIGURE 2-28: *Dynamic Line Response.*

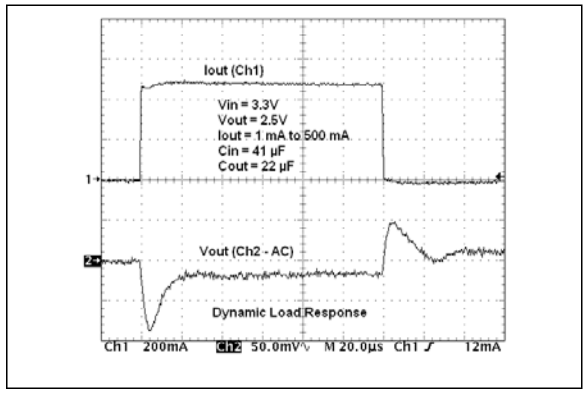


FIGURE 2-29: *Dynamic Load Response (1 mA to 500 mA).*

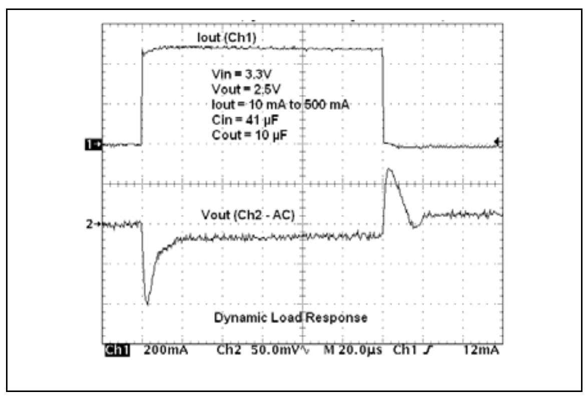


FIGURE 2-30: *Dynamic Load Response (10 mA to 500 mA).*

3.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

3-Pin Fixed Output	5-Pin Fixed Output	Adjustable Output	Name	Description
—	1	1	$\overline{\text{SHDN}}$	Shutdown Control Input (active-low)
1	2	2	V_{IN}	Input Voltage Supply
2	3	3	GND	Ground
3	4	4	V_{OUT}	Regulated Output Voltage
—	5	—	PWRGD	Power Good Output
—	—	5	ADJ	Voltage Adjust/Sense Input
Exposed Pad	Exposed Pad	Exposed Pad	EP	Exposed Pad of the Package (ground potential)

3.1 Shutdown Control Input ($\overline{\text{SHDN}}$)

The $\overline{\text{SHDN}}$ input is used to turn the LDO output voltage on and off. When the $\overline{\text{SHDN}}$ input is at a logic-high level, the LDO output voltage is enabled. When the $\overline{\text{SHDN}}$ input is pulled to a logic-low level, the LDO output voltage is disabled. When the $\overline{\text{SHDN}}$ input is pulled low, the PWRGD output also goes low and the LDO enters a low quiescent current shutdown state where the typical quiescent current is 0.1 µA.

3.2 Input Voltage Supply (V_{IN})

Connect the unregulated or regulated input voltage source to V_{IN}. If the input voltage source is located several inches away from the LDO, or the input source is a battery, it is recommended that an input capacitor be used. A typical input capacitance value of 1 µF to 10 µF should be sufficient for most applications.

3.3 Ground (GND)

Connect the GND pin of the LDO to a quiet circuit ground. This will help the LDO power supply rejection ratio and noise performance. The ground pin of the LDO only conducts the quiescent current of the LDO (typically 120 µA), so a heavy trace is not required. For applications that have switching or noisy inputs, tie the GND pin to the return of the output capacitor. Ground planes help lower inductance and voltage spikes caused by fast transient load currents and are recommended for applications that are subjected to fast load transients.

3.4 Regulated Output Voltage (V_{OUT})

The V_{OUT} pin is the regulated output voltage of the LDO. A minimum output capacitance of 1.0 µF is required for LDO stability. The MCP1825/MCP1825S is stable with ceramic, tantalum and aluminum-electrolytic capacitors. See **Section 4.3 "Output Capacitor"** for output capacitor selection guidance.

3.5 Power Good Output (PWRGD)

The PWRGD output is an open-drain output used to indicate when the LDO output voltage is within 92% (typically) of its nominal regulation value. The PWRGD threshold has a typical hysteresis value of 2%. The PWRGD output is delayed by 110 µs (typical) from the time the LDO output is within 92% + 3% (maximum hysteresis) of the regulated output value on power-up. This delay time is internally fixed.

3.6 Output Voltage Adjust Input (ADJ)

For adjustable applications, the output voltage is connected to the ADJ input through a resistor divider that sets the output voltage regulation value. This provides the user the capability to set the output voltage to any value they desire within the 0.8V to 5.0V range of the device.

3.7 Exposed Pad (EP)

The DDPAK and TO-220 package have an exposed tab on the package. A heat sink may may be mount to the tab to aid in the removal of heat from the package during operation. The exposed tab is at the ground potential of the LDO.

4.0 DEVICE OVERVIEW

The MCP1825/MCP1825S is a high output current, Low Dropout (LDO) voltage regulator. The low dropout voltage of 210 mV typical at 500 mA of current makes it ideal for battery-powered applications. Unlike other high output current LDOs, the MCP1825/MCP1825S only draws a maximum of 220 µA of quiescent current. The MCP1825 has a shutdown control input and a power good output.

4.1 LDO Output Voltage

The 5-pin MCP1825 LDO is available with either a fixed output voltage or an adjustable output voltage. The output voltage range is 0.8V to 5.0V for both versions. The 3-pin MCP1825S LDO is available as a fixed voltage device.

4.1.1 ADJUST INPUT

The adjustable version of the MCP1825 uses the ADJ pin (pin 5) to get the output voltage feedback for output voltage regulation. This allows the user to set the output voltage of the device with two external resistors. The nominal voltage for ADJ is 0.41V.

Figure 4-1 shows the adjustable version of the MCP1825. Resistors R_1 and R_2 form the resistor divider network necessary to set the output voltage. With this configuration, the equation for setting V_{OUT} is:

EQUATION 4-1:

$$V_{OUT} = V_{ADJ}\left(\frac{R_1 + R_2}{R_2}\right)$$

Where:

V_{OUT}	=	LDO Output Voltage
V_{ADJ}	=	ADJ Pin Voltage (typically 0.41V)

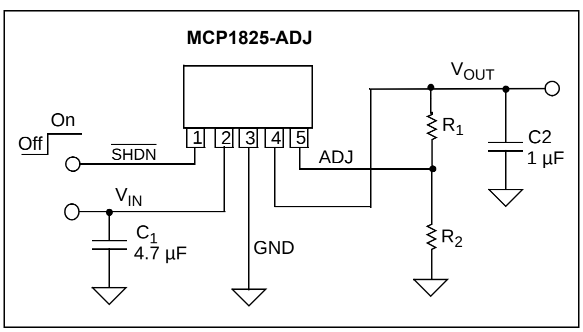


FIGURE 4-1: *Typical adjustable output voltage application circuit.*

The allowable resistance value range for resistor R_2 is from 10 kΩ to 200 kΩ. Solving the equation for R_1 yields the following equation:

EQUATION 4-2:

$$R_1 = R_2\left(\frac{V_{OUT} - V_{ADJ}}{V_{ADJ}}\right)$$

Where:

V_{OUT}	=	LDO Output Voltage
V_{ADJ}	=	ADJ Pin Voltage (typically 0.41V)

4.2 Output Current and Current Limiting

The MCP1825/MCP1825S LDO is tested and ensured to supply a minimum of 500 mA of output current. The MCP1825/MCP1825S has no minimum output load, so the output load current can go to 0 mA and the LDO will continue to regulate the output voltage to within tolerance.

The MCP1825/MCP1825S also incorporates an output current limit. If the output voltage falls below 0.7V due to an overload condition (usually represents a shorted load condition), the output current is limited to 1.2A (typical). If the overload condition is a soft overload, the MCP1825/MCP1825S will supply higher load currents of up to 1.5A. The MCP1825/MCP1825S should not be operated in this condition continuously as it may result in failure of the device. However, this does allow for device usage in applications that have higher pulsed load currents having an average output current value of 500 mA or less.

Output overload conditions may also result in an over-temperature shutdown of the device. If the junction temperature rises above 150°C, the LDO will shut down the output voltage. See **Section 4.8 "Overtemperature Protection"** for more information on overtemperature shutdown.

4.3 Output Capacitor

The MCP1825/MCP1825S requires a minimum output capacitance of 1 µF for output voltage stability. Ceramic capacitors are recommended because of their size, cost and environmental robustness qualities.

Aluminum-electrolytic and tantalum capacitors can be used on the LDO output as well. The Equivalent Series Resistance (ESR) of the electrolytic output capacitor must be no greater than 1 ohm. The output capacitor should be located as close to the LDO output as is practical. Ceramic materials X7R and X5R have low temperature coefficients and are well within the acceptable ESR range required. A typical 1 µF X7R 0805 capacitor has an ESR of 50 milli-ohms.

Larger LDO output capacitors can be used with the MCP1825/MCP1825S to improve dynamic performance and power supply ripple rejection performance. A maximum of 22 µF is recommended. Aluminum-electrolytic capacitors are not recommended for low temperature applications of < -25°C.

4.4 Input Capacitor

Low input source impedance is necessary for the LDO output to operate properly. When operating from batteries, or in applications with long lead length (> 10 inches) between the input source and the LDO, some input capacitance is recommended. A minimum of 1.0 µF to 4.7 µF is recommended for most applications.

For applications that have output step load requirements, the input capacitance of the LDO is very important. The input capacitance provides the LDO with a good local low-impedance source to pull the transient currents from in order to respond quickly to the output load step. For good step response performance, the input capacitor should be of equivalent (or higher) value than the output capacitor. The capacitor should be placed as close to the input of the LDO as is practical. Larger input capacitors will also help reduce any high-frequency noise on the input and output of the LDO and reduce the effects of any inductance that exists between the input source voltage and the input capacitance of the LDO.

4.5 Power Good Output (PWRGD)

The PWRGD output is used to indicate when the output voltage of the LDO is within 92% (typical value, see **Section 1.0 "Electrical Characteristics"** for Minimum and Maximum specifications) of its nominal regulation value.

As the output voltage of the LDO rises, the PWRGD output will be held low until the output voltage has exceeded the power good threshold plus the hysteresis value. Once this threshold has been exceeded, the power good time delay is started (shown as T_{PG} in the Electrical Characteristics table). The power good time delay is fixed at 110 µs (typical). After the time delay period, the PWRGD output will go high, indicating that the output voltage is stable and within regulation limits.

If the output voltage of the LDO falls below the power good threshold, the power good output will transition low. The power good circuitry has a 170 µs delay when detecting a falling output voltage, which helps to increase noise immunity of the power good output and avoid false triggering of the power good output during fast output transients. See Figure 4-2 for power good timing characteristics.

When the LDO is put into Shutdown mode using the $\overline{SHDN}$ input, the power good output is pulled low immediately, indicating that the output voltage will be out of regulation. The timing diagram for the power good output when using the shutdown input is shown in Figure 4-3.

The power good output is an open-drain output that can be pulled up to any voltage that is equal to or less than the LDO input voltage. This output is capable of sinking 1.2 mA (V_{PWRGD} < 0.4V maximum).

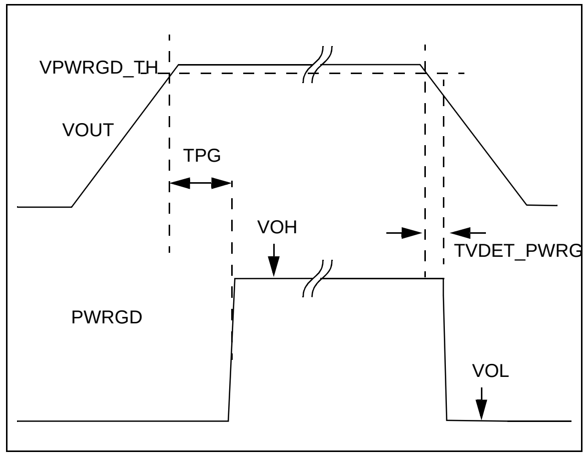


FIGURE 4-2: *Power Good Timing.*

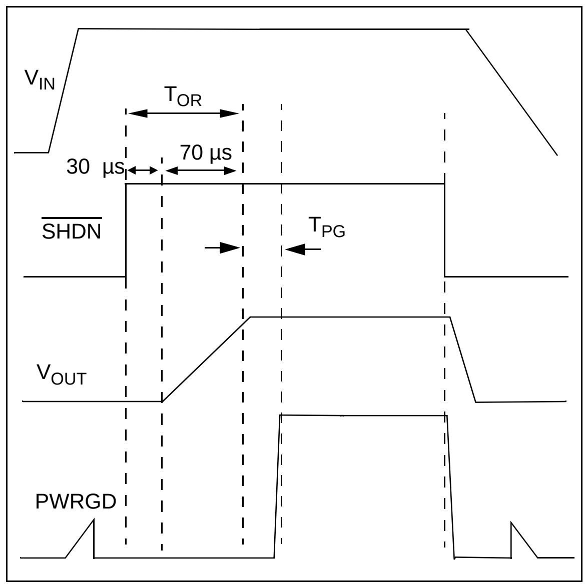


FIGURE 4-3: *Power Good Timing from Shutdown.*

4.6 Shutdown Input ($\overline{SHDN}$)

The $\overline{SHDN}$ input is an active-low input signal that turns the LDO on and off. The $\overline{SHDN}$ threshold is a percentage of the input voltage. The typical value of this shutdown threshold is 30% of V_{IN}, with minimum and maximum limits over the entire operating temperature range of 45% and 15%, respectively.

The $\overline{SHDN}$ input will ignore low-going pulses (pulses meant to shut down the LDO) that are up to 400 ns in pulse width. If the shutdown input is pulled low for more than 400 ns, the LDO will enter Shutdown mode. This small bit of filtering helps to reject any system noise spikes on the shutdown input signal.

On the rising edge of the $\overline{SHDN}$ input, the shutdown circuitry has a 30 µs delay before allowing the LDO output to turn on. This delay helps to reject any false turn-on signals or noise on the $\overline{SHDN}$ input signal. After the 30 µs delay, the LDO output enters its soft-start period as it rises from 0V to its final regulation value. If the $\overline{SHDN}$ input signal is pulled low during the 30 µs delay period, the timer will be reset and the delay time will start over again on the next rising edge of the $\overline{SHDN}$ input. The total time from the $\overline{SHDN}$ input going high (turn-on) to the LDO output being in regulation is typically 100 µs. See Figure 4-4 for a timing diagram of the $\overline{SHDN}$ input.

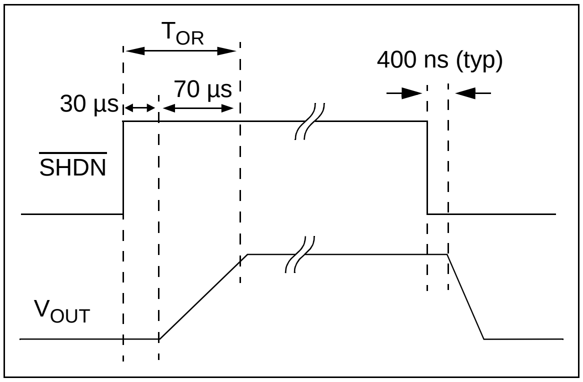


FIGURE 4-4: *Shutdown Input Timing Diagram.*

4.7 Dropout Voltage and Undervoltage Lockout

Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below the nominal value that was measured with a V_R + 0.5V differential applied. The MCP1825/MCP1825S LDO has a very low dropout voltage specification of 210 mV (typical) at 500 mA of output current. See **Section 1.0 "Electrical Characteristics"** for maximum dropout voltage specifications.

The MCP1825/MCP1825S LDO operates across an input voltage range of 2.1V to 6.0V and incorporates input Undervoltage Lockout (UVLO) circuitry that keeps the LDO output voltage off until the input voltage reaches a minimum of 2.00V (typical) on the rising edge of the input voltage. As the input voltage falls, the LDO output will remain on until the input voltage level reaches 1.82V (typical).

Since the MCP1825/MCP1825S LDO undervoltage lockout activates at 1.82V as the input voltage is falling, the dropout voltage specification does not apply for output voltages that are less than 1.8V.

For high-current applications, voltage drops across the PCB traces must be taken into account. The trace resistances can cause significant voltage drops between the input voltage source and the LDO. For applications with input voltages near 2.1V, these PCB trace voltage drops can sometimes lower the input voltage enough to trigger a shutdown due to undervoltage lockout.

4.8 Overtemperature Protection

The MCP1825/MCP1825S LDO has temperature-sensing circuitry to prevent the junction temperature from exceeding approximately 150°C. If the LDO junction temperature does reach 150°C, the LDO output will be turned off until the junction temperature cools to approximately 140°C, at which point the LDO output will automatically resume normal operation. If the internal power dissipation continues to be excessive, the device will again shut off. The junction temperature of the die is a function of power dissipation, ambient temperature and package thermal resistance. See **Section 5.0 "Application Circuits/ Issues"** for more information on LDO power dissipation and junction temperature.

5.0 APPLICATION CIRCUITS/ ISSUES

5.1 Typical Application

The MCP1825/MCP1825S is used for applications that require high LDO output current and a power good output.

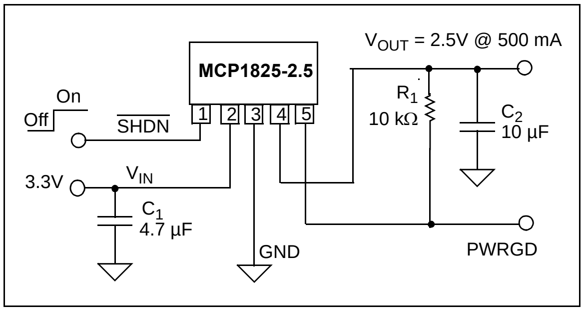


FIGURE 5-1: *Typical Application Circuit.*

5.1.1 APPLICATION CONDITIONS

Package Type	=	TO-220-5
Input Voltage Range	=	3.3V ± 5%
V_{IN} maximum	=	3.465V
V_{IN} minimum	=	3.135V
$V_{DROPOUT\ (max)}$	=	0.350V
V_{OUT} (typical)	=	2.5V
I_{OUT}	=	500 mA maximum
P_{DISS} (typical)	=	0.483W
Temperature Rise	=	14.2°C

5.2 Power Calculations

5.2.1 POWER DISSIPATION

The internal power dissipation within the MCP1825/MCP1825S is a function of input voltage, output voltage, output current and quiescent current. Equation 5-1 can be used to calculate the internal power dissipation for the LDO.

EQUATION 5-1:

$$P_{LDO} = (V_{IN(MAX))} - V_{OUT(MIN)}) \times I_{OUT(MAX))}$$

Where:

P_{LDO}	=	LDO Pass device internal power dissipation
$V_{IN(MAX)}$	=	Maximum input voltage
$V_{OUT(MIN)}$	=	LDO minimum output voltage

In addition to the LDO pass element power dissipation, there is power dissipation within the MCP1825/ MCP1825S as a result of quiescent or ground current. The power dissipation as a result of the ground current can be calculated using the following equation:

EQUATION 5-2:

$$P_{I(GND)} = V_{IN(MAX)} \times I_{VIN}$$

Where:

$P_{I(GND}$	=	Power dissipation due to the quiescent current of the LDO
$V_{IN(MAX)}$	=	Maximum input voltage
I_{VIN}	=	Current flowing in the V_{IN} pin with no LDO output current (LDO quiescent current)

The total power dissipated within the MCP1825/ MCP1825S is the sum of the power dissipated in the LDO pass device and the P(I_{GND}) term. Because of the CMOS construction, the typical I_{GND} for the MCP1825/ MCP1825S is 120 µA. Operating at a maximum V_{IN} of 3.465V results in a power dissipation of 0.12 milli-Watts for a 2.5V output. For most applications, this is small compared to the LDO pass device power dissipation and can be neglected.

The maximum continuous operating junction temperature specified for the MCP1825/MCP1825S is +125°C. To estimate the internal junction temperature of the MCP1825/MCP1825S, the total internal power dissipation is multiplied by the thermal resistance from junction to ambient ($R\theta_{JA}$) of the device. The thermal resistance from junction to ambient for the TO-220-5 package is estimated at 29.3°C/W.

EQUATION 5-3:

$$T_{J(MAX)} = P_{TOTAL} \times R\theta_{JA} + T_{AMAX}$$

$T_{J(MAX)}$	=	Maximum continuous junction temperature
P_{TOTAL}	=	Total device power dissipation
$R\theta_{JA}$	=	Thermal resistance from junction to ambient
T_{AMAX}	=	Maximum ambient temperature

The maximum power dissipation capability for a package can be calculated given the junction-to-ambient thermal resistance and the maximum ambient temperature for the application. Equation 5-4 can be used to determine the package maximum internal power dissipation.

EQUATION 5-4:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{R\theta_{JA}}$$

$P_{D(MAX)}$ = Maximum device power dissipation
$T_{J(MAX)}$ = maximum continuous junction temperature
$T_{A(MAX)}$ = maximum ambient temperature
$R\theta_{JA}$ = Thermal resistance from junction-to-ambient

EQUATION 5-5:

$$T_{J(RISE)} = P_{D(MAX)} \times R\theta_{JA}$$

$T_{J(RISE)}$ = Rise in device junction temperature over the ambient temperature
$P_{D(MAX)}$ = Maximum device power dissipation
$R\theta_{JA}$ = Thermal resistance from junction-to-ambient

EQUATION 5-6:

$$T_J = T_{J(RISE)} + T_A$$

T_J = Junction temperature
$T_{J(RISE)}$ = Rise in device junction temperature over the ambient temperature
T_A = Ambient temperature

5.3 Typical Application

Internal power dissipation, junction temperature rise, junction temperature and maximum power dissipation is calculated in the following example. The power dissipation as a result of ground current is small enough to be neglected.

5.3.1 POWER DISSIPATION EXAMPLE

Package

Package Type = TO-220-5

Input Voltage

V_{IN} = 3.3V ± 5%

LDO Output Voltage and Current

V_{OUT} = 2.5V
I_{OUT} = 500 mA

Maximum Ambient Temperature

$T_{A(MAX)}$ = 60°C

Internal Power Dissipation

$P_{LDO(MAX)} = (V_{IN(MAX)} - V_{OUT(MIN)}) \times I_{OUT(MAX)}$
P_{LDO} = ((3.3V x 1.05) – (2.5V x 0.975)) x 500 mA
P_{LDO} = 0.514 Watts

5.3.1.1 Device Junction Temperature Rise

The internal junction temperature rise is a function of internal power dissipation and the thermal resistance from junction-to-ambient for the application. The thermal resistance from junction-to-ambient ($R\theta_{JA}$) is derived from EIA/JEDEC standards for measuring thermal resistance. The EIA/JEDEC specification is JESD51. The standard describes the test method and board specifications for measuring the thermal resistance from junction to ambient. The actual thermal resistance for a particular application can vary depending on many factors such as copper area and thickness. Refer to AN792, *"A Method to Determine How Much Power a SOT23 Can Dissipate in an Application"* (DS00792), for more information regarding this subject.

$T_{J(RISE)} = P_{TOTAL} \times R\theta_{JA}$
T_{JRISE} = 0.514 W x 29.3° C/W
T_{JRISE} = 15.06°C

5.3.1.2 Junction Temperature Estimate

To estimate the internal junction temperature, the calculated temperature rise is added to the ambient or offset temperature. For this example, the worst-case junction temperature is estimated below:

$$T_J = T_{JRISE} + T_{A(MAX)}$$
$$T_J = 15.06°C + 60.0°C$$
$$T_J = 75.06°C$$

5.3.1.3 Maximum Package Power Dissipation at 60°C Ambient Temperature

TO-220-5 (29.3°C/W Rθ_{JA}):

$$P_{D(MAX)} = (125°C – 60°C) / 29.3°C/W$$
$$P_{D(MAX)} = 2.218W$$

DDPAK-5 (31.2°C/Watt Rθ_{JA}):

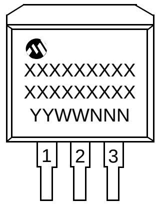
$$P_{D(MAX)} = (125°C – 60°C)/ 31.2°C/W$$
$$P_{D(MAX)} = 2.083W$$

From this table, you can see the difference in maximum allowable power dissipation between the TO-220-5 package and the DDPAK-5 package.

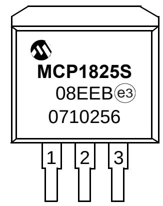
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

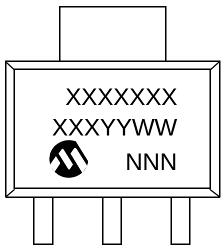
3-Lead DDPAK (MCP1825S)



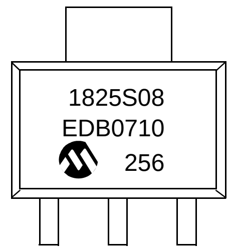
Example:



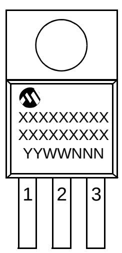
3-Lead SOT-223 (MCP1825S)



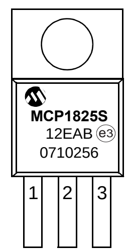
Example:



3-Lead TO-220 (MCP1825S)



Example:

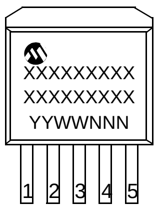


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

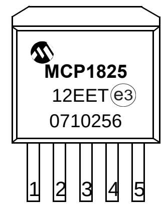
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Package Marking Information (Continued)

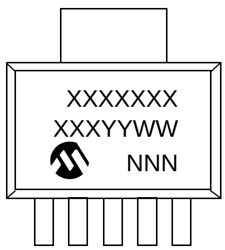
5-Lead DDPAK (MCP1825)



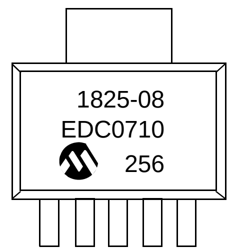
Example:



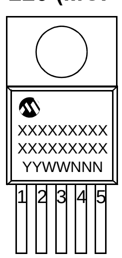
5-Lead SOT-223 (MCP1825)



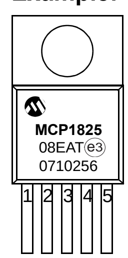
Example:



5-Lead TO-220 (MCP1825)



Example:

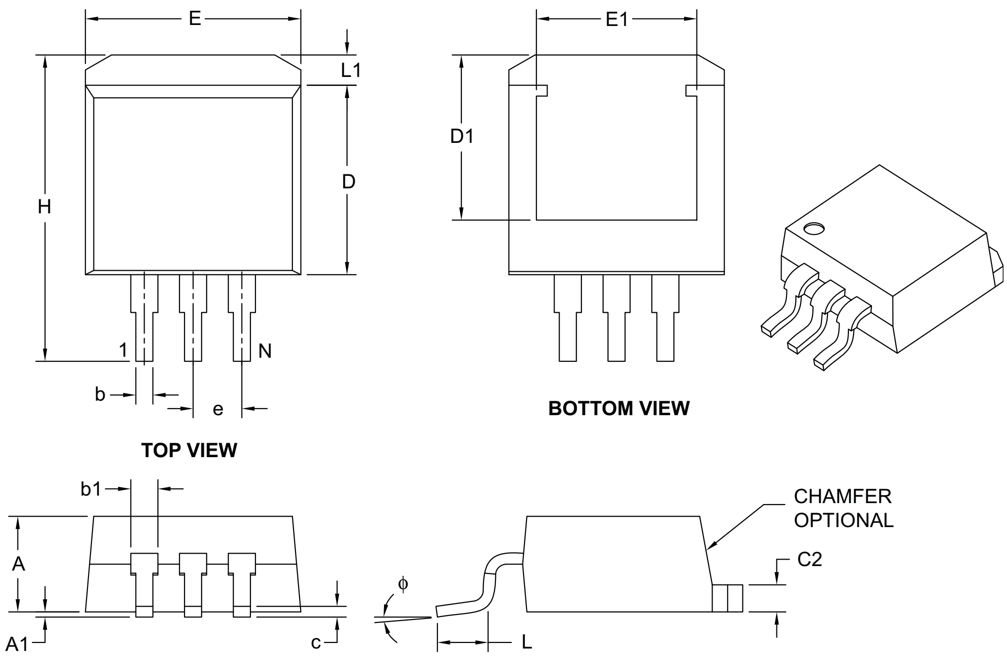


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

3-Lead Plastic (EB) [DDPAK]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	INCHES		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	3		
Pitch	e	.100 BSC		
Overall Height	A	.160	–	.190
Standoff §	A1	.000	–	.010
Overall Width	E	.380	–	.420
Exposed Pad Width	E1	.245	–	–
Molded Package Length	D	.330	–	.380
Overall Length	H	.549	–	.625
Exposed Pad Length	D1	.270	–	–
Lead Thickness	c	.014	–	.029
Pad Thickness	C2	.045	–	.065
Lower Lead Width	b	.020	–	.039
Upper Lead Width	b1	.045	–	.070
Foot Length	L	.068	–	.110
Pad Length	L1	–	–	.067
Foot Angle	ϕ	0°	–	8°

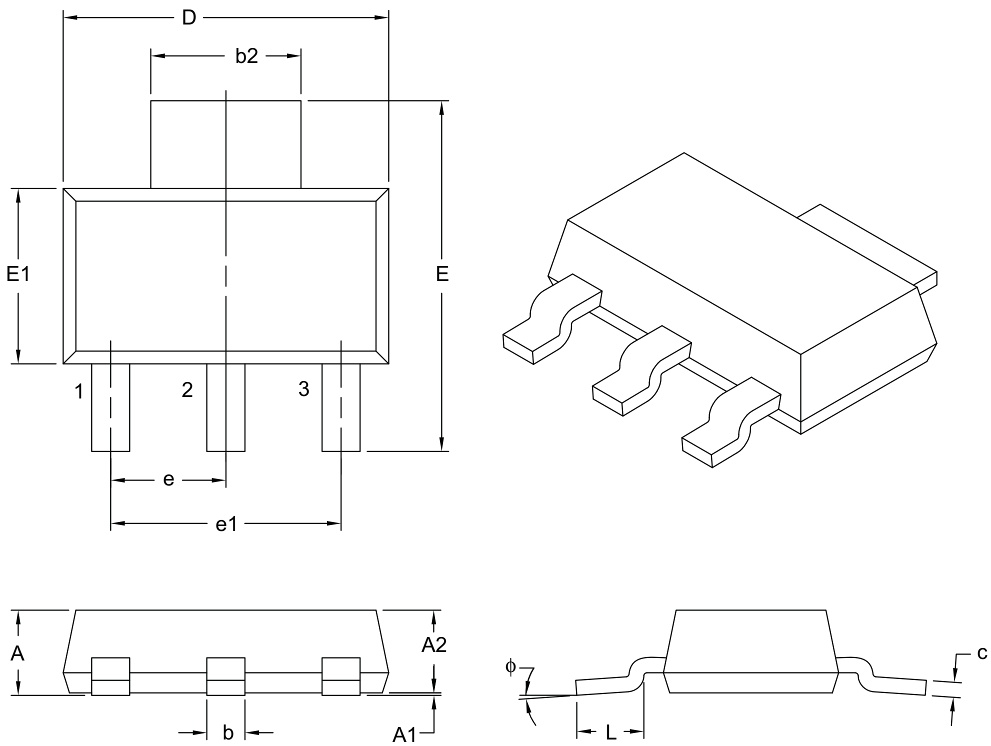
Notes:
1. § Significant Characteristic.
2. Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-011B

3-Lead Plastic Small Outline Transistor (DB) [SOT-223]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		3	
Lead Pitch	e		2.30 BSC	
Outside Lead Pitch	e1		4.60 BSC	
Overall Height	A	–	–	1.80
Standoff	A1	0.02	–	0.10
Molded Package Height	A2	1.50	1.60	1.70
Overall Width	E	6.70	7.00	7.30
Molded Package Width	E1	3.30	3.50	3.70
Overall Length	D	6.30	6.50	6.70
Lead Thickness	c	0.23	0.30	0.35
Lead Width	b	0.60	0.76	0.84
Tab Lead Width	b2	2.90	3.00	3.10
Foot Length	L	0.75	–	–
Lead Angle	φ	0°	–	10°

Notes:

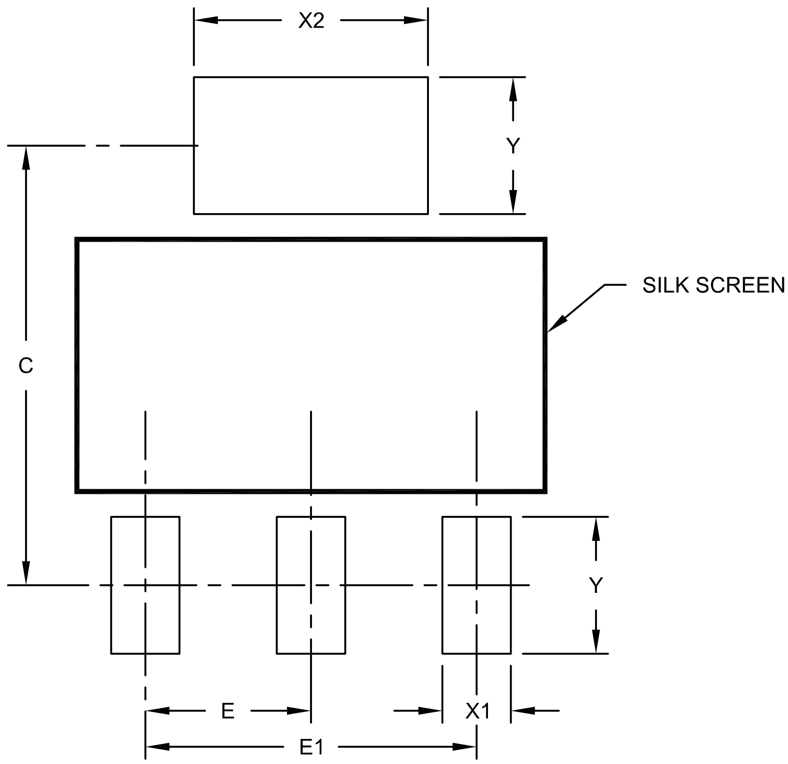
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-032B

3-Lead Plastic Small Outline Transistor (DB) [SOT-223]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	2.30 BSC		
Overall Pitch	E1	4.60 BSC		
Contact Pad Spacing	C		6.10	
Contact Pad Width	X1			0.95
Contact Pad Width	X2			3.25
Contact Pad Length	Y			1.90

Notes:

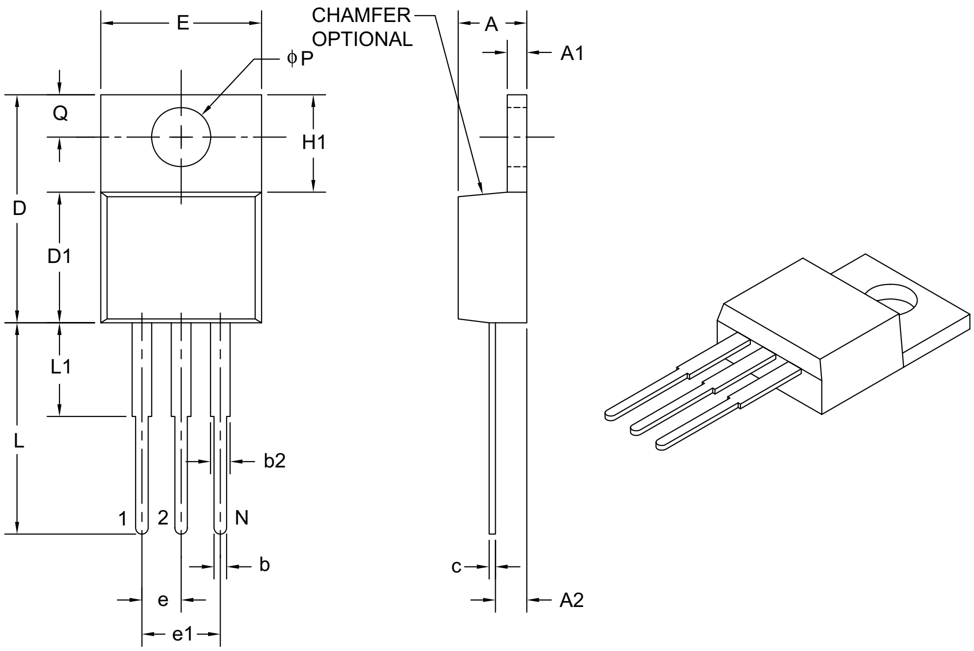
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2032A

3-Lead Plastic Transistor Outline (AB) [TO-220]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		3	
Pitch	e		.100 BSC	
Overall Pin Pitch	e1		.200 BSC	
Overall Height	A	.140	–	.190
Tab Thickness	A1	.020	–	.055
Base to Lead	A2	.080	–	.115
Overall Width	E	.357	–	.420
Mounting Hole Center	Q	.100	–	.120
Overall Length	D	.560	–	.650
Molded Package Length	D1	.330	–	.355
Tab Length	H1	.230	–	.270
Mounting Hole Diameter	ϕP	.139	–	.156
Lead Length	L	.500	–	.580
Lead Shoulder	L1	–	–	.250
Lead Thickness	c	.012	–	.024
Lead Width	b	.015	.027	.040
Shoulder Width	b2	.045	.057	.070

Notes:

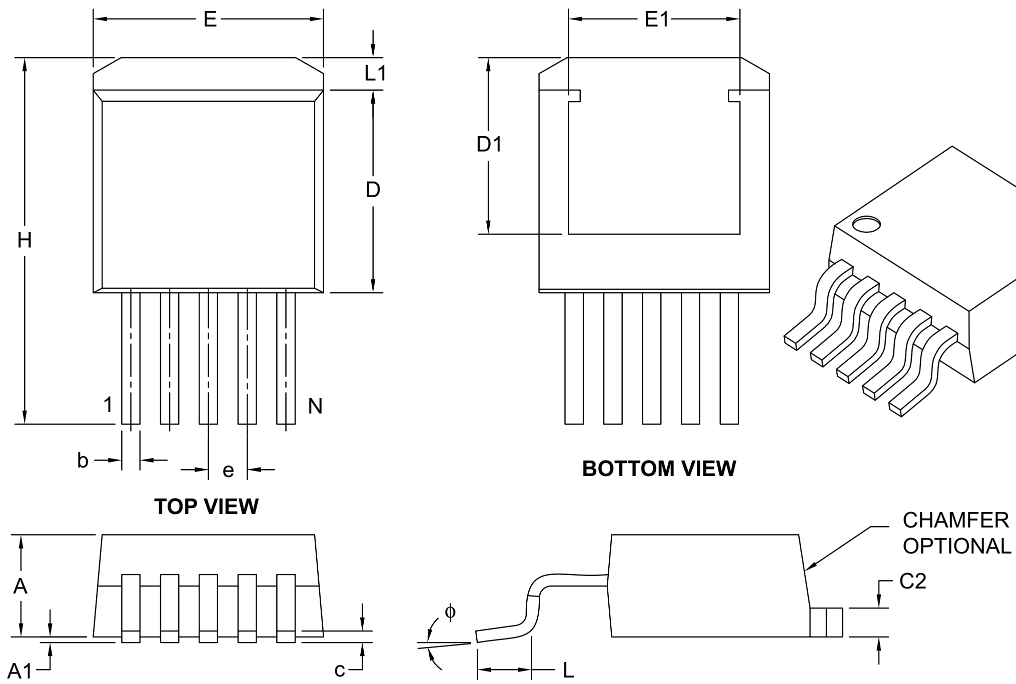
1. Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-034B

5-Lead Plastic (ET) [DDPAK]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	5		
Pitch	e	.067 BSC		
Overall Height	A	.160	–	.190
Standoff §	A1	.000	–	.010
Overall Width	E	.380	–	.420
Exposed Pad Width	E1	.245	–	–
Molded Package Length	D	.330	–	.380
Overall Length	H	.549	–	.625
Exposed Pad Length	D1	.270	–	–
Lead Thickness	c	.014	–	.029
Pad Thickness	C2	.045	–	.065
Lead Width	b	.020	–	.039
Foot Length	L	.068	–	.110
Pad Length	L1	–	–	.067
Foot Angle	ϕ	0°	–	8°

Notes:

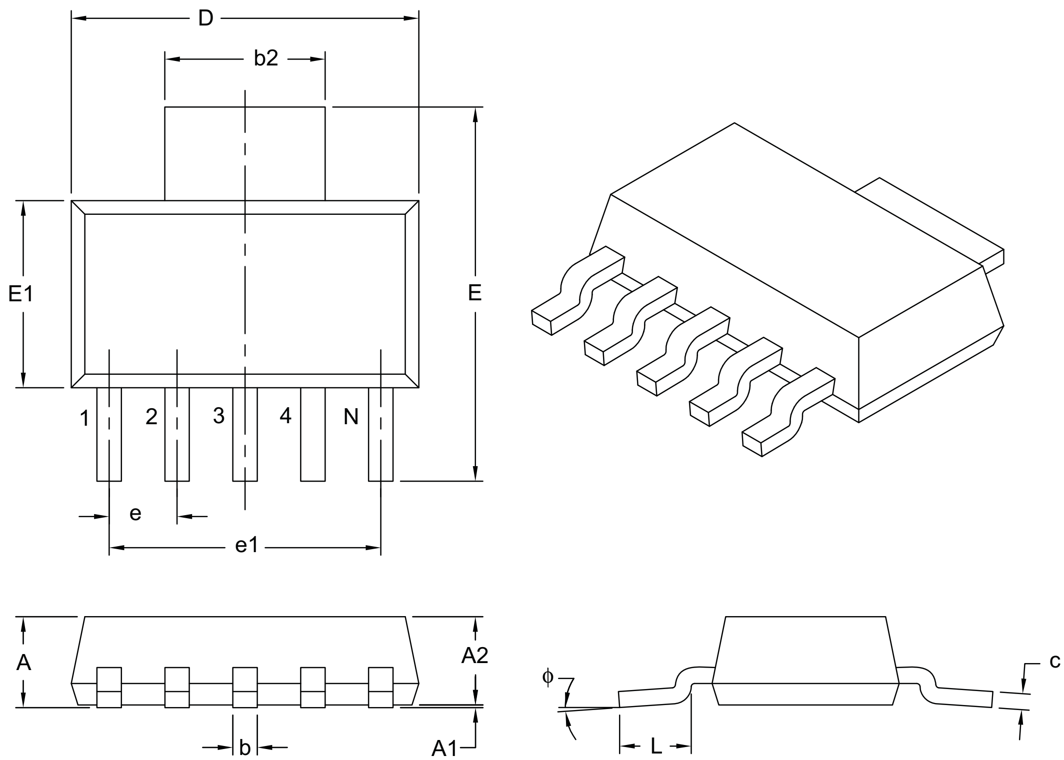
1. § Significant Characteristic.
2. Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-012B

5-Lead Plastic Small Outline Transistor (DC) [SOT-223]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



		Units	MILLIMETERS		
		Dimension Limits	MIN	NOM	MAX
Number of Leads	N			5	
Lead Pitch	e			1.27 BSC	
Outside Lead Pitch	e1			5.08 BSC	
Overall Height	A		–	–	1.80
Standoff	A1		0.02	0.06	0.10
Molded Package Height	A2		1.55	1.60	1.65
Overall Width	E		6.86	7.00	7.26
Molded Package Width	E1		3.45	3.50	3.55
Overall Length	D		6.45	6.50	6.55
Lead Thickness	c		0.24	0.28	0.32
Lead Width	b		0.41	0.457	0.51
Tab Lead Width	b2		2.95	3.00	3.05
Foot Length	L		0.91	–	1.14
Lead Angle	ϕ		0°	4°	8°

Notes:

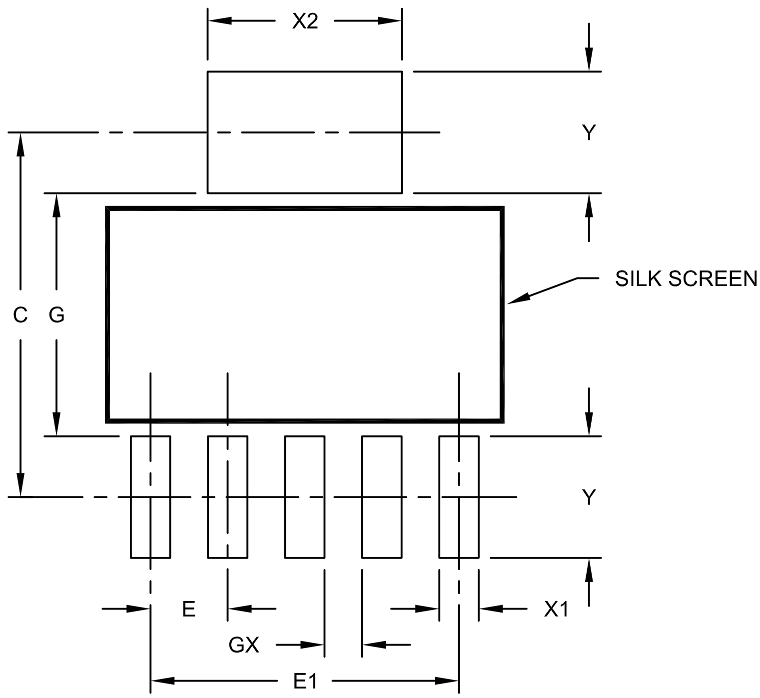
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-137B

5-Lead Plastic Small Outline Transistor (DC) [SOT-223]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Pad Pitch	E	1.27 BSC		
Overall Pad Pitch	E1	5.08 BSC		
Pad Spacing	C		6.00	
Pad Width	X1			0.65
Pad Width	X2			3.20
Pad Length	Y			2.00
Distance Between Pads	G	4.00		
Distance Between Pads	GX	0.62		

Notes:

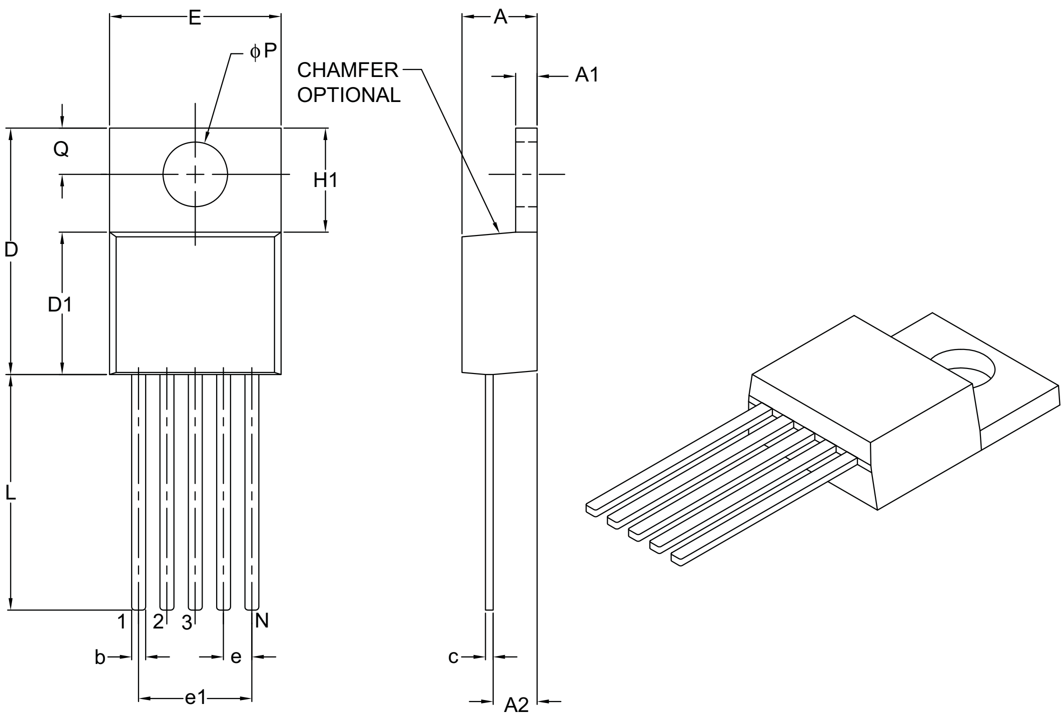
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2137A

5-Lead Plastic Transistor Outline (AT) [TO-220]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		.067 BSC	
Overall Pin Pitch	e1		.268 BSC	
Overall Height	A	.140	–	.190
Overall Width	E	.380	–	.420
Overall Length	D	.560	–	.650
Molded Package Length	D1	.330	–	.355
Tab Length	H1	.204	–	.293
Tab Thickness	A1	.020	–	.055
Mounting Hole Center	Q	.100	–	.120
Mounting Hole Diameter	φP	.139	–	.156
Lead Length	L	.482	–	.590
Base to Bottom of Lead	A2	.080	–	.115
Lead Thickness	c	.012	–	.025
Lead Width	b	.015	.027	.040

Notes:
1. Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" per side.
2. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-036B

APPENDIX A: REVISION HISTORY

Revision B (February 2008)

The following is the list of modifications

1. Updated Figure 2-4, Figure 2-5, Figure 2-16, Figure 2-29, and Figure 2-30.
2. Updated package outline drawings and landing pattern drawings to **Section 6.0 “Packaging Information”**.
3. Updated **Appendix A: “Revision History”**.

Revision A (August 2007)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	X	X	X/	XX
Device	Output Voltage	Feature Code	Tolerance	Temp.	Package

Device:	MCP1825:	500 mA Low Dropout Regulator
	MCP1825T:	500 mA Low Dropout Regulator Tape and Reel
	MCP1825S:	500 mA Low Dropout Regulator
	MCP1825ST:	500 mA Low Dropout Regulator Tape and Reel
Output Voltage *:	08 =	0.8V "Standard"
	12 =	1.2V "Standard"
	18 =	1.8V "Standard"
	25 =	2.5V "Standard"
	30 =	3.0V "Standard"
	33 =	3.3V "Standard"
	50 =	5.0V "Standard"
	ADJ =	Adjustable Output Voltage ** (MCP1825 Only)

*Contact factory for other output voltage options
** When ADJ is used, the "extra feature code" and "tolerance" columns do not apply. Refer to examples.

Extra Feature Code:	0 =	Fixed
Tolerance:	2 =	2.5% (Standard)
Temperature:	E =	-40°C to +125°C
Package Type:	AB =	Plastic Transistor Outline, TO-220, 3-lead
	AT =	Plastic Transistor Outline, TO-220, 5-lead
	EB =	Plastic, DDPAK, 3-lead
	ET =	Plastic, DDPAK, 5-lead
	DB =	Plastic Small Transistor Outline, SOT-223, 3-lead
	DC =	Plastic Small Transistor Outline, SOT-223, 5-lead

Note: ADJ (Adjustable) only available in 5-lead version.

Examples:

a) MCP1825-0802E/XX: 0.8V LDO Regulator
b) MCP1825-1202E/XX: 1.2V LDO Regulator
c) MCP1825-1802E/XX: 1.8V LDO Regulator
d) MCP1825-2502E/XX: 2.5V LDO Regulator
e) MCP1825-3002E/XX: 3.0V LDO Regulator
f) MCP1825-3302E/XX: 3.3V LDO Regulator
g) MCP1825-5002E/XX: 5.0V LDO Regulator
h) MCP1825-ADJE/XX: ADJ LDO Regulator

a) MCP1825S-0802E/YY: 0.8V LDO Regulator
b) MCP1825S-1202E/YY: 1.2V LDO Regulator
c) MCP1825S-1802E/YY: 1.8V LDO Regulator
d) MCP1825S-2502E/YY: 2.5V LDO Regulator
e) MCP1825S-2502E/YY: 3.0V LDO Regulator
f) MCP1825S-3302E/YY: 3.3V LDO Regulator
g) MCP1825S-5002E/YY: 5.0V LDO Regulator

XX = AT for 5LD TO-220 package
= DC for 5LD SOT-223 package
= ET for 5LD DDPAK package

YY = AB for 3LD TO-220 package
= DB for 3LD SOT-223 package
= EB for 3LD DDPAK package

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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