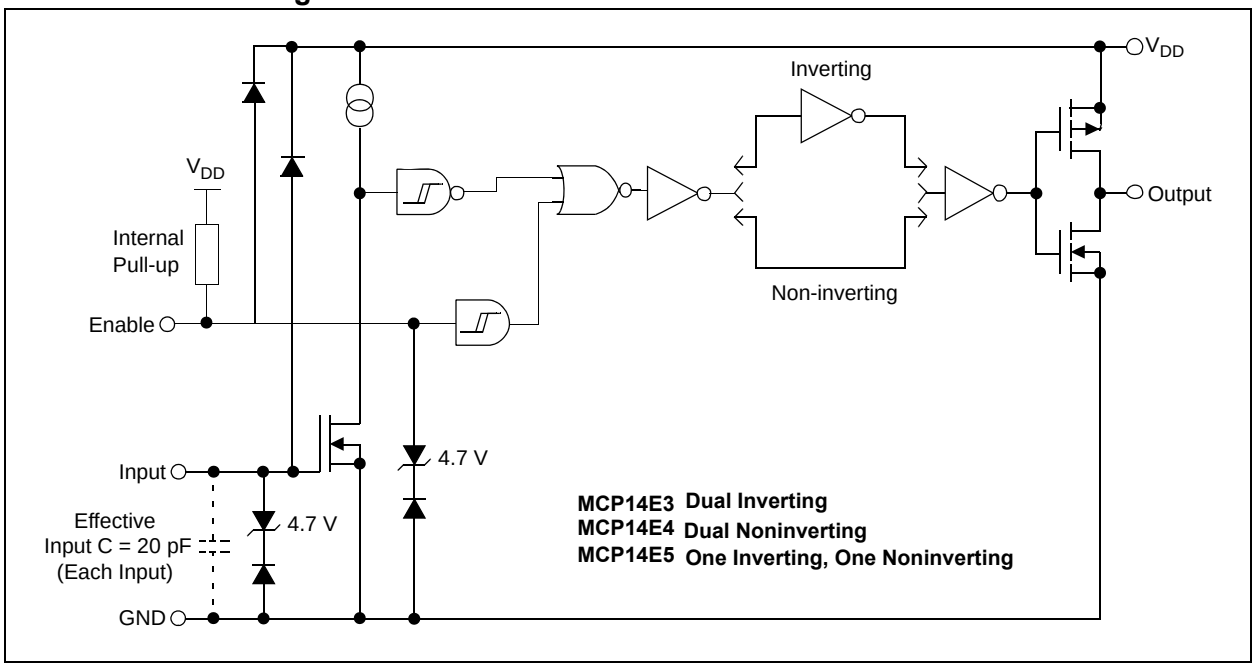
## Functional Block Diagram



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

Supply Voltage .....+20V
Input Voltage .....($V_{DD}$ + 0.3V) to (GND – 5V)
Enable Voltage .....($V_{DD}$ + 0.3V) to (GND - 5V)
Input Current ($V_{IN}$>$V_{DD}$).....50 mA
Package Power Dissipation ($T_A$ = 50°C)
8L-DFN ..... **Note 3**
8L-PDIP .....1.10W
8L-SOIC .....665 mW

† **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

## DC CHARACTERISTICS (NOTE 2)

**Electrical Specifications:** Unless otherwise indicated, $T_A$ = +25°C, with 4.5V ≤ $V_{DD}$ ≤ 18V.

| Parameters | Sym | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **Input** | | | | | | |
| Logic '1', High Input Voltage | $V_{IH}$ | 2.4 | 1.5 | — | V | |
| Logic '0', Low Input Voltage | $V_{IL}$ | — | 1.3 | 0.8 | V | |
| Input Current | $I_{IN}$ | –1 | — | 1 | µA | 0V ≤ $V_{IN}$ ≤ $V_{DD}$ |
| Input Voltage | $V_{IN}$ | -5 | — | $V_{DD}$+0.3 | V | |
| **Output** | | | | | | |
| High Output Voltage | $V_{OH}$ | $V_{DD}$ – 0.025 | — | — | V | DC Test |
| Low Output Voltage | $V_{OL}$ | — | — | 0.025 | V | DC Test |
| Output Resistance, High | $R_{OH}$ | — | 2.5 | 3.5 | Ω | $I_{OUT}$ = 10 mA, $V_{DD}$ = 18V |
| Output Resistance, Low | $R_{OL}$ | — | 2.5 | 3.0 | Ω | $I_{OUT}$ = 10 mA, $V_{DD}$ = 18V |
| Peak Output Current | $I_{PK}$ | — | 4.0 | — | A | $V_{DD}$ = 18V **(Note 2)** |
| Latch-Up Protection With-stand Reverse Current | $I_{REV}$ | — | >1.5 | — | A | Duty cycle ≤ 2%, t ≤ 300 µs |
| **Switching Time (Note 1)** | | | | | | |
| Rise Time | $t_R$ | — | 15 | 30 | ns | **Figure 4-1, Figure 4-2** $C_L$ = 2200 pF |
| Fall Time | $t_F$ | — | 18 | 30 | ns | **Figure 4-1, Figure 4-2** $C_L$ = 2200 pF |
| Propagation Delay Time | $t_{D1}$ | — | 46 | 55 | ns | **Figure 4-1, Figure 4-2** |
| Propagation Delay Time | $t_{D2}$ | — | 50 | 55 | ns | **Figure 4-1, Figure 4-2** |
| **Enable Function (ENB_A, ENB_B)** | | | | | | |
| High-Level Input Voltage | $V_{EN\_H}$ | 1.60 | 1.90 | 2.90 | V | $V_{DD}$ = 12V, LO to HI Transition |
| Low-Level Input Voltage | $V_{EN\_L}$ | 1.30 | 2.20 | 2.40 | V | $V_{DD}$ = 12V, HI to LO Transition |
| Hysteresis | $V_{HYST}$ | 0.10 | 0.30 | 0.60 | V | |
| Enable Leakage Current | $I_{ENBL}$ | 40 | 85 | 115 | µA | $V_{DD}$ = 12V, ENB_A = ENB_B = GND |
| Propagation Delay Time | $t_{D3}$ | — | 60 | — | ns | Figure 4-3 **(Note 1)** |
| Propagation Delay Time | $t_{D4}$ | — | 50 | — | ns | Figure 4-3 **(Note 1)** |

**Note 1:** Switching times ensured by design.
**2:** Tested during characterization, not production tested.
**3:** Package power dissipation is dependent on the copper pad area on the PCB.

## DC CHARACTERISTICS (NOTE 2) (CONTINUED)

**Electrical Specifications:** Unless otherwise indicated, $T_A$ = +25°C, with 4.5V ≤ $V_{DD}$ ≤ 18V.

| Parameters | Sym | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| Supply Voltage | $V_{DD}$ | 4.5 | — | 18.0 | V | |
| Supply Current | $I_{DD}$ | — | 1.60 | 2.00 | mA | $V_{IN\_A}$ = 3V, $V_{IN\_B}$ = 3V, $\overline{ENB\_A}$ = $\overline{ENB\_B}$ = High |
| | $I_{DD}$ | — | 0.60 | 0.90 | mA | $V_{IN\_A}$ = 0V, $V_{IN\_B}$ = 0V, $\overline{ENB\_A}$ = $\overline{ENB\_B}$ = High |
| | $I_{DD}$ | — | 1.20 | 1.40 | mA | $V_{IN\_A}$ = 3V, $V_{IN\_B}$ = 0V, $\overline{ENB\_A}$ = $\overline{ENB\_B}$ = High |
| | $I_{DD}$ | — | 1.20 | 1.40 | mA | $V_{IN\_A}$ = 0V, $V_{IN\_B}$ = 3V, $\overline{ENB\_A}$ = $\overline{ENB\_B}$ = High |
| | $I_{DD}$ | — | 1.40 | 1.80 | mA | $V_{IN\_A}$ = 3V, $V_{IN\_B}$ = 3V, $\overline{ENB\_A}$ = $\overline{ENB\_B}$ = Low |
| | $I_{DD}$ | — | 0.55 | 0.75 | mA | $V_{IN\_A}$ = 0V, $V_{IN\_B}$ = 0V, $\overline{ENB\_A}$ = $\overline{ENB\_B}$ = Low |
| | $I_{DD}$ | — | 1.00 | 1.20 | mA | $V_{IN\_A}$ = 3V, $V_{IN\_B}$ = 0V, $\overline{ENB\_A}$ = $\overline{ENB\_B}$ = Low |
| | $I_{DD}$ | — | 1.00 | 1.20 | mA | $V_{IN\_A}$ = 0V, $V_{IN\_B}$ = 3V, $\overline{ENB\_A}$ = $\overline{ENB\_B}$ = Low |

**Note 1:** Switching times ensured by design.

**2:** Tested during characterization, not production tested.

**3:** Package power dissipation is dependent on the copper pad area on the PCB.

## DC CHARACTERISTICS (OVER OPERATING TEMPERATURE RANGE)

**Electrical Specifications:** Unless otherwise indicated, operating temperature range with 4.5V ≤ $V_{DD}$ ≤ 18V.

| Parameters | Sym | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **Input** | | | | | | |
| Logic '1', High Input Voltage | $V_{IH}$ | 2.4 | — | — | V | |
| Logic '0', Low Input Voltage | $V_{IL}$ | — | — | 0.8 | V | |
| Input Current | $I_{IN}$ | –10 | — | +10 | µA | 0V ≤ $V_{IN}$ ≤ $V_{DD}$ |
| **Output** | | | | | | |
| High Output Voltage | $V_{OH}$ | $V_{DD}$ – 0.025 | — | — | V | DC TEST |
| Low Output Voltage | $V_{OL}$ | — | — | 0.025 | V | DC TEST |
| Output Resistance, High | $R_{OH}$ | — | 3.0 | 6.0 | Ω | $I_{OUT}$ = 10 mA, $V_{DD}$ = 18V |
| Output Resistance, Low | $R_{OL}$ | — | 3.0 | 5.0 | Ω | $I_{OUT}$ = 10 mA, $V_{DD}$ = 18V |
| **Switching Time (Note 1)** | | | | | | |
| Rise Time | $t_R$ | — | 25 | 40 | ns | **Figure 4-1**, **Figure 4-2** $C_L$ = 2200 pF |
| Fall Time | $t_F$ | — | 28 | 40 | ns | **Figure 4-1**, **Figure 4-2** $C_L$ = 2200 pF |
| Delay Time | $t_{D1}$ | — | 50 | 70 | ns | **Figure 4-1**, **Figure 4-2** |
| Delay Time | $t_{D2}$ | — | 50 | 70 | ns | **Figure 4-1**, **Figure 4-2** |
| **Enable Function (ENB_A, ENB_B)** | | | | | | |
| High-Level Input Voltage | $V_{EN\_H}$ | 1.60 | 2.20 | 2.90 | V | $V_{DD}$ = 12V, LO to HI Transition |
| Low-Level Input Voltage | $V_{EN\_L}$ | 1.30 | 1.80 | 2.40 | V | $V_{DD}$ = 12V, HI to LO Transition |
| Hysteresis | $V_{HYST}$ | — | 0.40 | — | V | |
| Enable Leakage Current | $I_{ENBL}$ | 40 | 87 | 115 | µA | $V_{DD}$ = 12V, ENB_A = ENB_B = GND |
| Propagation Delay Time | $t_{D3}$ | — | 50 | — | ns | Figure 4-3 |
| Propagation Delay Time | $t_{D4}$ | — | 60 | — | ns | Figure 4-3 |
| **Power Supply** | | | | | | |
| Supply Voltage | $V_{DD}$ | 4.5 | — | 18.0 | V | |
| Supply Current | $I_{DD}$ | — | 2.0 | 3.0 | mA | $V_{IN\_A}$ = 3V, $V_{IN\_B}$ = 3V, ENB_A = ENB_B = High |
| | $I_{DD}$ | — | 0.8 | 1.1 | mA | $V_{IN\_A}$ = 0V, $V_{IN\_B}$ = 0V, ENB_A = ENB_B = High |
| | $I_{DD}$ | — | 1.5 | 2.0 | mA | $V_{IN\_A}$ = 3V, $V_{IN\_B}$ = 0V, ENB_A = ENB_B = High |
| | $I_{DD}$ | — | 1.5 | 2.0 | mA | $V_{IN\_A}$ = 0V, $V_{IN\_B}$ = 3V, ENB_A = ENB_B = High |
| | $I_{DD}$ | — | 1.8 | 2.8 | mA | $V_{IN\_A}$ = 3V, $V_{IN\_B}$ = 3V, ENB_A = ENB_B = Low |
| | $I_{DD}$ | — | 0.6 | 0.8 | mA | $V_{IN\_A}$ = 0V, $V_{IN\_B}$ = 0V, ENB_A = ENB_B = Low |
| | $I_{DD}$ | — | 1.1 | 1.8 | mA | $V_{IN\_A}$ = 3V, $V_{IN\_B}$ = 0V, ENB_A = ENB_B = Low |
| | $I_{DD}$ | — | 1.1 | 1.8 | mA | $V_{IN\_A}$ = 0V, $V_{IN\_B}$ = 3V, ENB_A = ENB_B = Low |

**Note 1:** Switching times ensured by design.

## TEMPERATURE CHARACTERISTICS

| **Electrical Specifications:** Unless otherwise noted, all parameters apply with 4.5V ≤ $V_{DD}$ ≤ 18V. | | | | | | |
|---|---|---|---|---|---|---|
| **Parameters** | **Sym** | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| **Temperature Ranges** | | | | | | |
| Specified Temperature Range | $T_A$ | –40 | — | +125 | °C | |
| Maximum Junction Temperature | $T_J$ | — | — | +150 | °C | |
| Storage Temperature Range | $T_A$ | –65 | — | +150 | °C | |
| **Package Thermal Resistances** | | | | | | |
| Thermal Resistance, 8L-6x5 DFN | $\theta_{JA}$ | — | 35.7 | — | °C/W | Typical four-layer board with vias to ground plane |
| Thermal Resistance, 8L-PDIP | $\theta_{JA}$ | — | 89.3 | — | °C/W | |
| Thermal Resistance, 8L-SOIC | $\theta_{JA}$ | — | 149.5 | — | °C/W | |

## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

**Note:** Unless otherwise indicated, $T_A$ = +25°C with 4.5V ≤ $V_{DD}$ ≤ 18V.

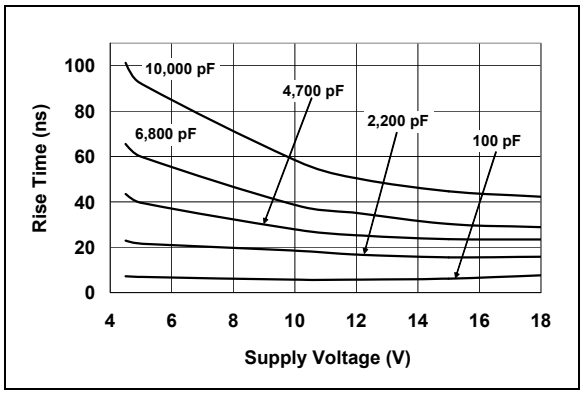



***FIGURE 2-1:*** *Rise Time vs. Supply Voltage.*

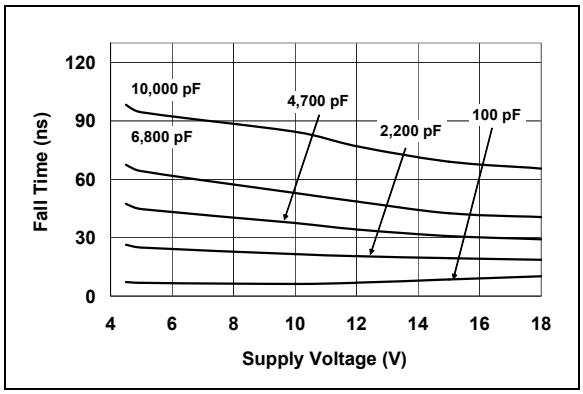



***FIGURE 2-4:*** *Fall Time vs. Supply Voltage.*

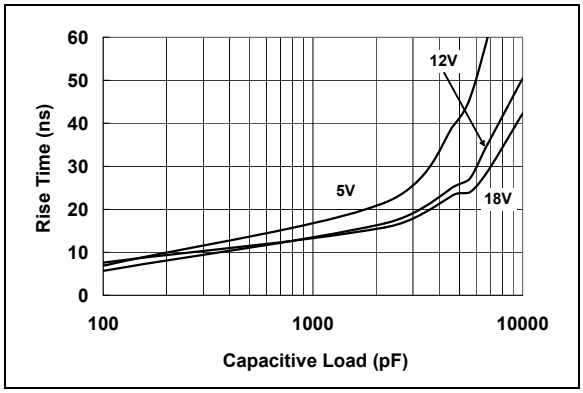



***FIGURE 2-2:*** *Rise Time vs. Capacitive Load.*

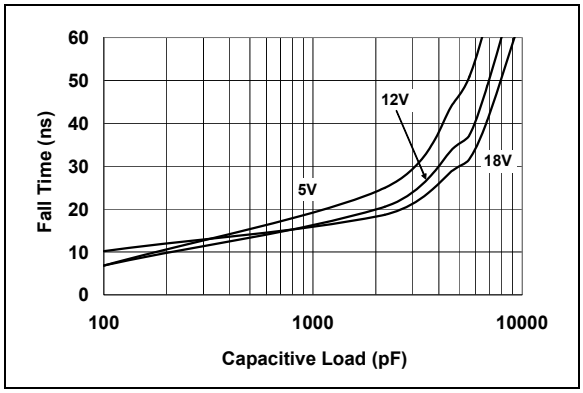



***FIGURE 2-5:*** *Fall Time vs. Capacitive Load.*

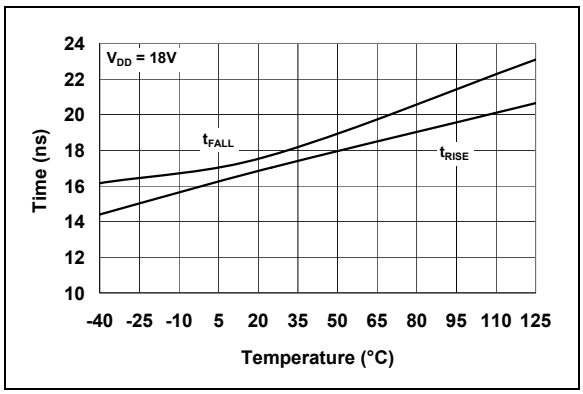



***FIGURE 2-3:*** *Rise and Fall Times vs. Temperature.*

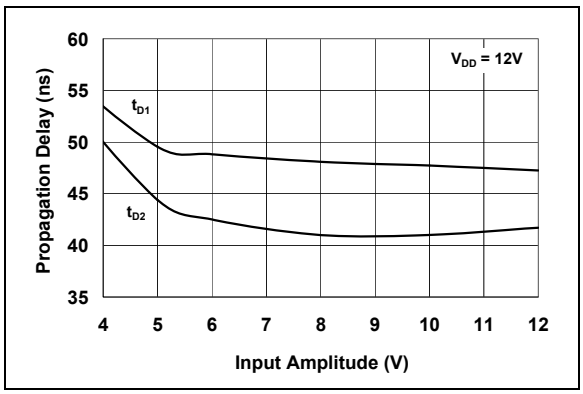



***FIGURE 2-6:*** *Propagation Delay vs. Input Amplitude.*

## Typical Performance Curves (Continued)

**Note:** Unless otherwise indicated, $T_A$ = +25°C with 4.5V ≤ $V_{DD}$ ≤ 18V.

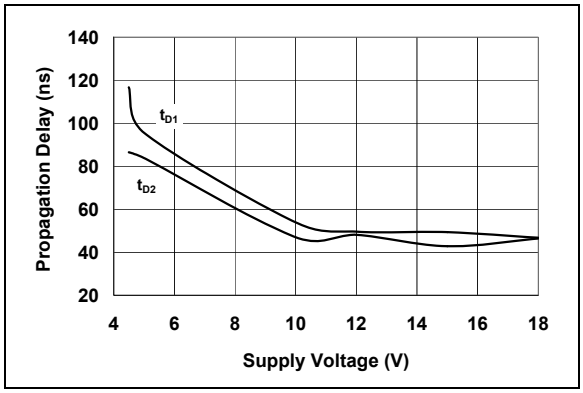



***FIGURE 2-7:*** *Propagation Delay Time vs. Supply Voltage.*

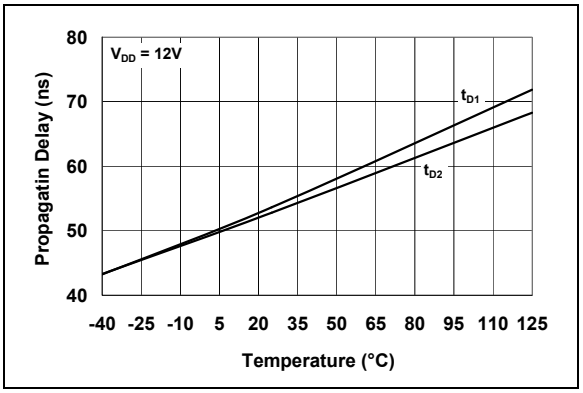



***FIGURE 2-10:*** *Propagation Delay Time vs. Temperature.*

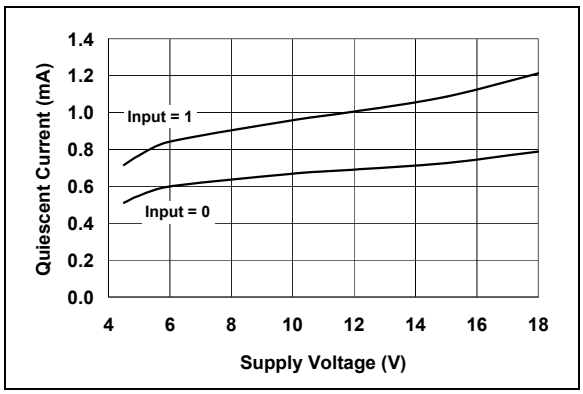



***FIGURE 2-8:*** *Quiescent Current vs. Supply Voltage.*

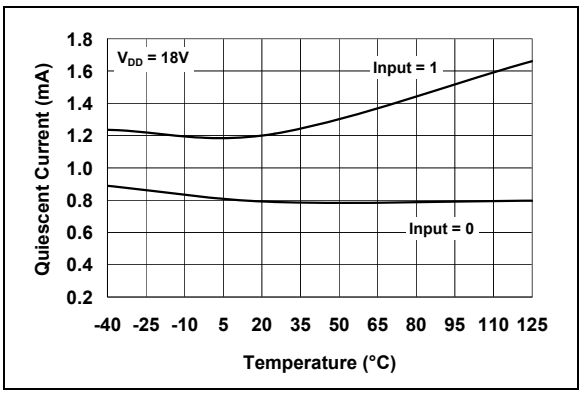



***FIGURE 2-11:*** *Quiescent Current vs. Temperature.*

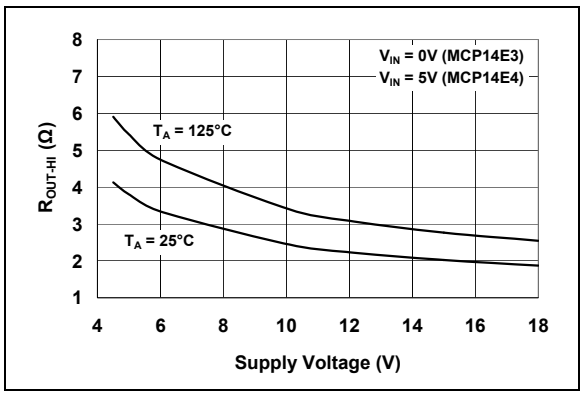



***FIGURE 2-9:*** *Output Resistance (Output High) vs. Supply Voltage.*

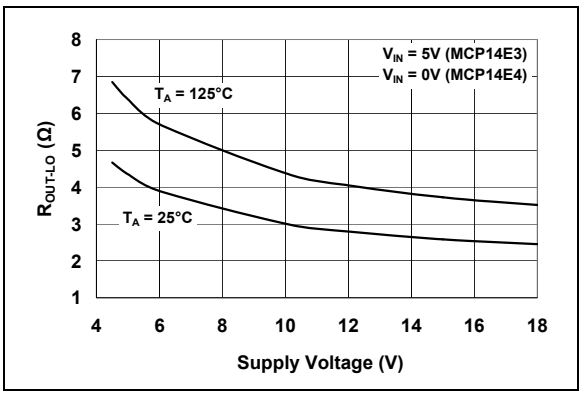



***FIGURE 2-12:*** *Output Resistance (Output Low) vs. Supply Voltage.*

## Typical Performance Curves (Continued)

**Note:** Unless otherwise indicated, $T_A$ = +25°C with 4.5V ≤ $V_{DD}$ ≤ 18V.

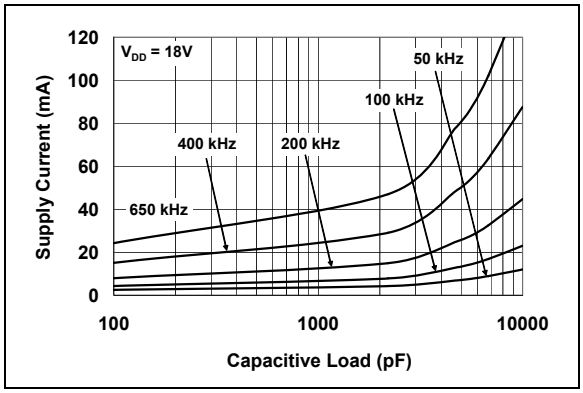



***FIGURE 2-13:*** *Supply Current vs. Capacitive Load.*

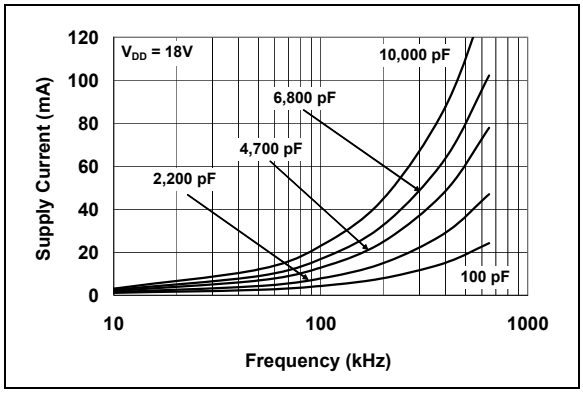



***FIGURE 2-16:*** *Supply Current vs. Frequency.*

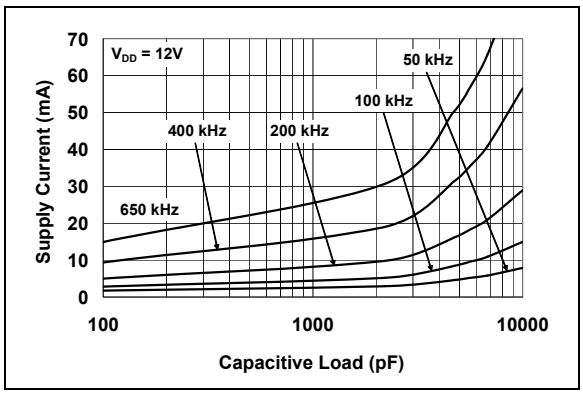



***FIGURE 2-14:*** *Supply Current vs. Capacitive Load.*

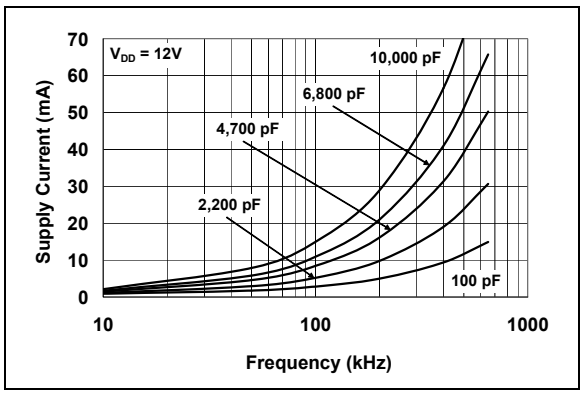



***FIGURE 2-17:*** *Supply Current vs. Frequency.*

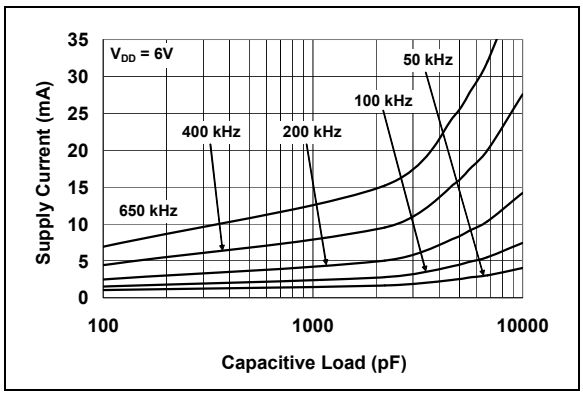



***FIGURE 2-15:*** *Supply Current vs. Capacitive Load.*

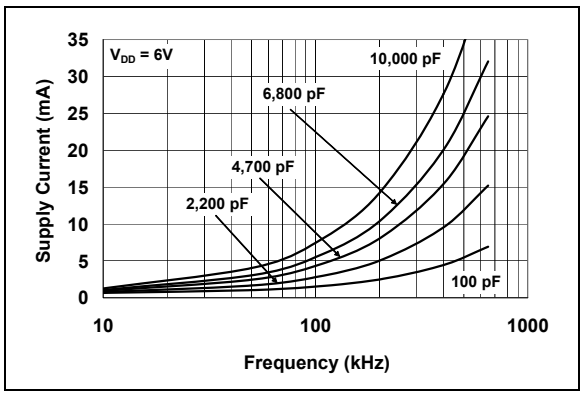



***FIGURE 2-18:*** *Supply Current vs. Frequency.*

## Typical Performance Curves (Continued)

**Note:** Unless otherwise indicated, $T_A$ = +25°C with 4.5V ≤ $V_{DD}$ ≤ 18V.

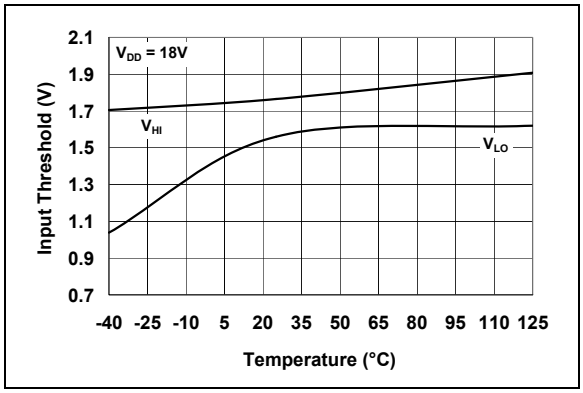



***FIGURE 2-19:*** *Input Threshold vs. Temperature.*

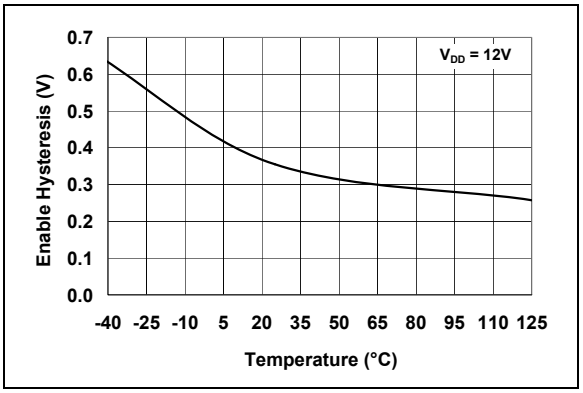



***FIGURE 2-22:*** *Enable Hysteresis vs. Temperature.*

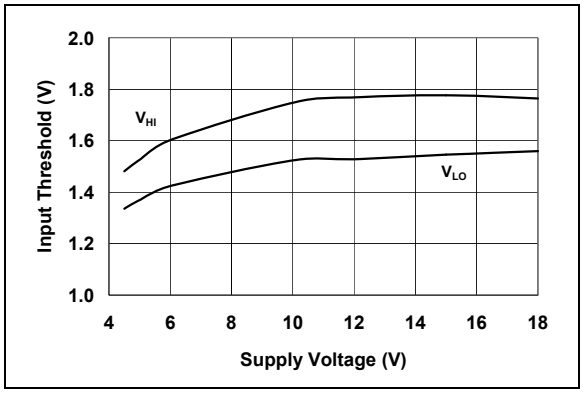



***FIGURE 2-20:*** *Input Threshold vs. Supply Voltage.*

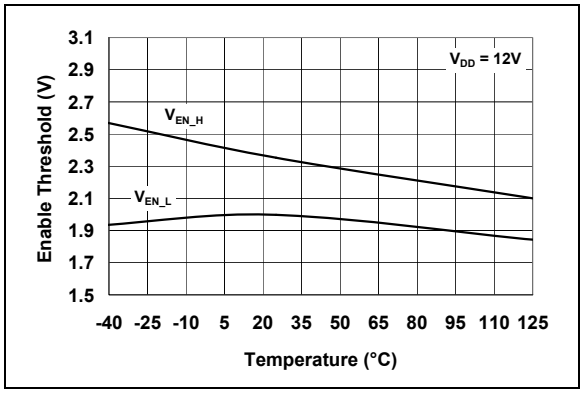
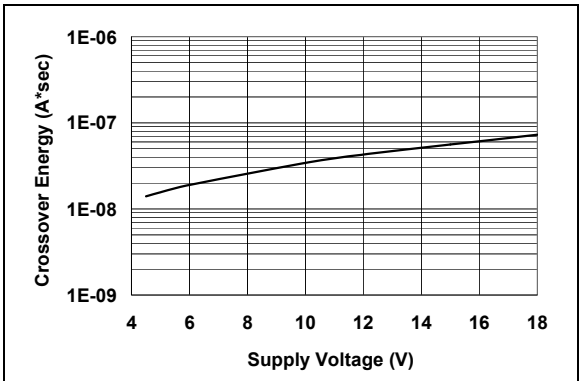



***FIGURE 2-21:*** *Enable Threshold vs. Temperature.*




**Note:** The values on this graph represent the loss seen by both drivers in a package during one complete cycle.
For a single driver, divide the stated value by 2.
For a signal transition of a single driver, divide the state value by 4.

***FIGURE 2-23:*** *Crossover Energy vs. Supply Voltage.*

## 3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

**TABLE 3-1: PIN FUNCTION TABLE**

| 8-Pin PDIP, SOIC | 8-Pin 6x5 DFN | Symbol | Description |
|---|---|---|---|
| 1 | 1 | ENB_A | Output A Enable |
| 2 | 2 | IN A | Input A |
| 3 | 3 | GND | Ground |
| 4 | 4 | IN B | Input B |
| 5 | 5 | OUT B | Output B |
| 6 | 6 | $V_{DD}$ | Supply Input |
| 7 | 7 | OUT A | Output A |
| 8 | 8 | ENB_B | Output B Enable |
| — | PAD | NC | Exposed Metal Pad |

**Note:** Duplicate pins must be connected for proper operation.

### 3.1 Control Inputs A and B

The MOSFET driver inputs are a high-impedance TTL/CMOS compatible input. The inputs also have hysteresis between the high and low input levels, allowing them to be driven from slow rising and falling signals and to provide noise immunity.

### 3.2 Outputs A and B

Outputs A and B are CMOS push-pull outputs that are capable of sourcing and sinking 4.0A of peak current ($V_{DD}$ = 18V). The low output impedance ensures the gate of the MOSFET will stay in the intended state even during large transients. These outputs also have a reverse latch-up rating of 1.5A.

### 3.3 Supply Input ($V_{DD}$)

$V_{DD}$ is the bias supply input for the MOSFET driver and has a voltage range of 4.5V to 18V. This input must be decoupled to ground with a local ceramic capacitor. This bypass capacitor provides a localized low-impedance path for the peak currents that are to be provided to the load.

### 3.4 Ground (GND)

Ground is the device return pin. The ground pin(s) should have a low impedance connection to the bias supply source return. High peak currents will flow out the ground pin(s) when the capacitive load is being discharged.

### 3.5 Enable A (ENB_A)

The ENB_A pin is the enable control for Output A. This enable pin is internally pulled up to $V_{DD}$ for active high operation and can be left floating for standard operation. When the ENB_A pin is pulled below the enable pin Low Level Input Voltage ($V_{EN\_L}$), Output A will be in the off state regardless of the input pin state.

### 3.6 Enable B (ENB_B)

The ENB_B pin is the enable control for Output B. This enable pin is internally pulled up to $V_{DD}$ for active high operation and can be left floating for standard operation. When the ENB_B pin is pulled below the enable pin Low-Level Input Voltage ($V_{EN\_L}$), Output B will be in the off state regardless of the input pin state.

### 3.7 DFN Exposed Pad

The exposed metal pad of the DFN package is not internally connected to any potential. Therefore, this pad can be connected to a ground plane or other copper plane on a printed circuit board to aid in heat removal from the package.

# 4.0 APPLICATION INFORMATION

## 4.1 General Information

MOSFET drivers are high-speed, high current devices which are intended to source/sink high peak currents to charge/discharge the gate capacitance of external MOSFETs or IGBTs. In high frequency switching power supplies, the PWM controller may not have the drive capability to directly drive the power MOSFET. A MOSFET driver like the MCP14E3/MCP14E4/MCP14E5 family can be used to provide additional source/sink current capability.

An additional degree of control has been added to the MCP14E3/MCP14E4/MCP14E5 family. There are separate enable functions for each driver that allow for the immediate termination of the output pulse regardless of the state of the input signal.

## 4.2 MOSFET Driver Timing

The ability of a MOSFET driver to transition from a fully off state to a fully on state are characterized by the drivers rise time ($t_R$), fall time ($t_F$), and propagation delays ($t_{D1}$ and $t_{D2}$). The MCP14E3/MCP14E4/MCP14E5 family of drivers can typically charge and discharge a 2200 pF load capacitance in 15 ns along with a typical matched propagation delay of 50 ns. Figure 4-1 and Figure 4-2 show the test circuit and timing waveform used to verify the MCP14E3/MCP14E4/MCP14E5 timing.

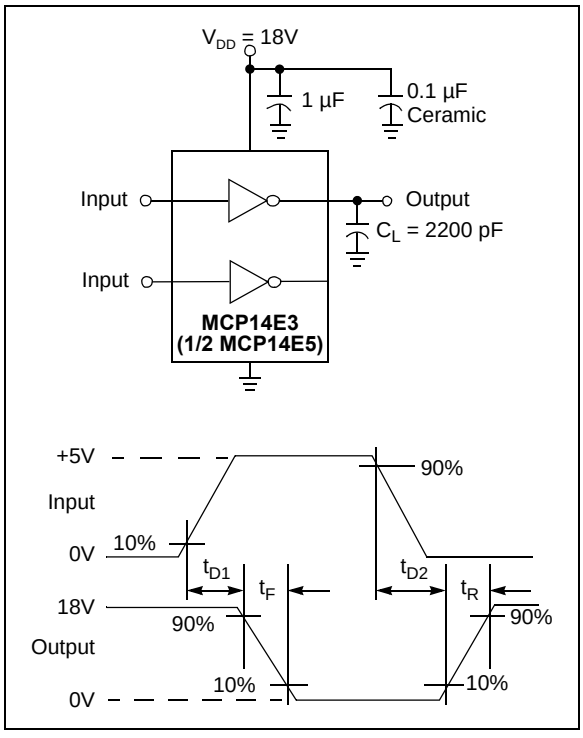



***FIGURE 4-1:*** *Inverting Driver Timing Waveform.*

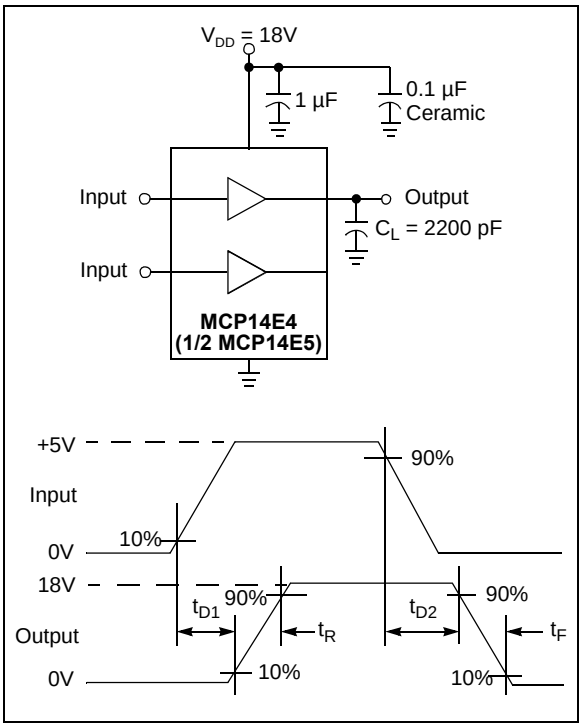



***FIGURE 4-2:*** *Non-Inverting Driver Timing Waveform.*

## 4.3 Enable Function

The ENB_A and ENB_B enable pins allow for independent control of OUT A and OUT B respectively. They are active high and are internally pulled up to $V_{DD}$ so that the default state is to enable the driver. These pins can be left floating for normal operation.

When an enable pin voltage is above the enable pin high threshold voltage, $V_{EN\_H}$ (2.4V typical), that driver output is enabled and allowed to react to changes in the INPUT pin voltage state. Likewise, when the enable pin voltage falls below the enable pin low threshold voltage, $V_{EN\_L}$ (2.0V typical), that driver output is disabled and does not respond the changes in the INPUT pin voltage state. When the driver is disabled, the output goes to a low state. Refer to Table 4-1 for enable pin logic. The threshold voltages of the enable function are compatible with logic levels. Hysteresis is provided to help increase the noise immunity of the enable function, avoiding false triggers of the enable signal during driver switching. For robust designs, it is recommended that the slew rate of the enable pin signal be greater than 1 V/ns.

There are propagation delays associated with the driver receiving an enable signal and the output reacting. These propagation delays, $t_{D3}$ and $t_{D4}$, are graphically represented in Figure 4-3.

**TABLE 4-1: ENABLE PIN LOGIC**

| | | | | MCP14E3 | | MCP14E4 | | MCP14E5 | |
|---|---|---|---|---|---|---|---|---|---|
| ENB_A | ENB_B | IN A | IN B | OUT A | OUT B | OUT A | OUT B | OUT A | OUT B |
| H | H | H | H | L | L | H | H | L | H |
| H | H | H | L | L | H | H | L | L | L |
| H | H | L | H | H | L | L | H | H | H |
| H | H | L | L | H | H | L | L | H | L |
| L | L | X | X | L | L | L | L | L | L |

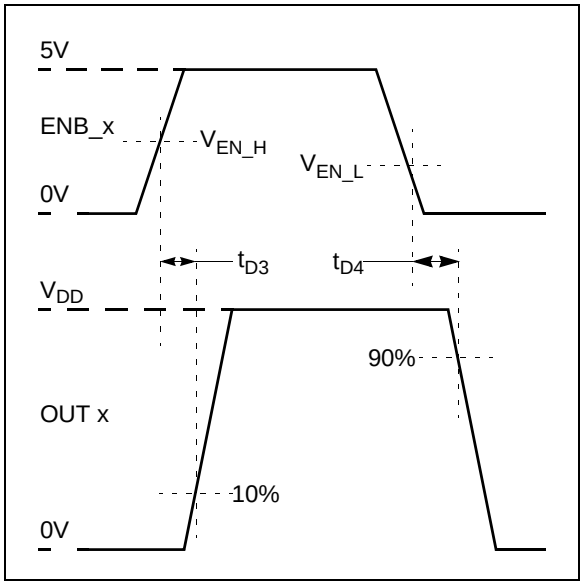



***FIGURE 4-3:*** *Enable Timing Waveform.*

## 4.4 Decoupling Capacitors

Careful layout and decoupling capacitors are highly recommended when using MOSFET drivers. Large currents are required to charge and discharge capacitive loads quickly. For example, 2.5A are needed to charge a 2200 pF load with 18V in 16 ns.

To operate the MOSFET driver over a wide frequency range with low supply impedance, a ceramic and low ESR film capacitor are recommended to be placed in parallel between the driver $V_{DD}$ and GND. A 1.0 µF low ESR film capacitor and a 0.1 µF ceramic capacitor should be used. These capacitors should be placed close to the driver to minimized circuit board parasitics and provide a local source for the required current.

## 4.5 PCB Layout Considerations

Proper PCB layout is important in a high current, fast switching circuit to provide proper device operation and robustness of design. PCB trace loop area and inductance should be minimized by the use of ground planes or trace under MOSFET gate drive signals, separate analog and power grounds, and local driver decoupling.

Placing a ground plane beneath the MCP14E3/MCP14E4/MCP14E5 will help as a radiated noise shield as well as providing some heat sinking for power dissipated within the device.

## 4.6 Power Dissipation

The total internal power dissipation in a MOSFET driver is the summation of three separate power dissipation elements.

**EQUATION 4-1:**

$$P_T = P_L + P_Q + P_{CC}$$

Where:

| | | |
|---|---|---|
| $P_T$ | = | Total power dissipation |
| $P_L$ | = | Load power dissipation |
| $P_Q$ | = | Quiescent power dissipation |
| $P_{CC}$ | = | Operating power dissipation |

### 4.6.1 CAPACITIVE LOAD DISSIPATION

The power dissipation caused by a capacitive load is a direct function of frequency, total capacitive load, and supply voltage. The power lost in the MOSFET driver for a complete charging and discharging cycle of a MOSFET is:

**EQUATION 4-2:**

$$P_L = f \times C_T \times V_{DD}^2$$

Where:

| | | |
|---|---|---|
| f | = | Switching frequency |
| $C_T$ | = | Total load capacitance |
| $V_{DD}$ | = | MOSFET driver supply voltage |

### 4.6.2 QUIESCENT POWER DISSIPATION

The power dissipation associated with the quiescent current draw of the MCP14E3/MCP14E4/MCP14E5 depends upon the state of the input and enable pins. Refer to the DC Characteristic table for the quiescent current draw for specific combinations of input and enable pin states. The quiescent power dissipation is:

**EQUATION 4-3:**

$$P_Q = (I_{QH} \times D + I_{QL} \times (1 - D)) \times V_{DD}$$

Where:

| | | |
|---|---|---|
| $I_{QH}$ | = | Quiescent current in the high state |
| D | = | Duty cycle |
| $I_{QL}$ | = | Quiescent current in the low state |
| $V_{DD}$ | = | MOSFET driver supply voltage |

### 4.6.3 OPERATING POWER DISSIPATION

The operating power dissipation occurs each time the MOSFET driver output transitions because for a very short period of time both MOSFETs in the output stage are on simultaneously. This cross-conduction current leads to a power dissipation describes as:

**EQUATION 4-4:**

$$P_{CC} = CC \times f \times V_{DD}$$

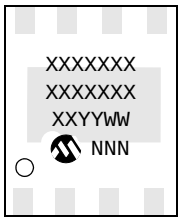
Where:

| | | |
|---|---|---|
| CC | = | Cross-conduction constant (A*sec) |
| f | = | Switching frequency |
| $V_{DD}$ | = | MOSFET driver supply voltage |

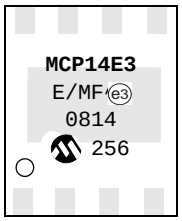
## 5.0 PACKAGING INFORMATION

### 5.1 Package Marking Information (Not to Scale)

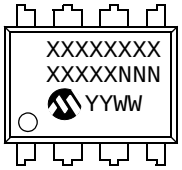
8-Lead DFN-S (6x5)



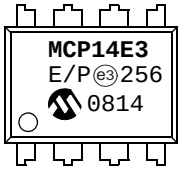

Example:



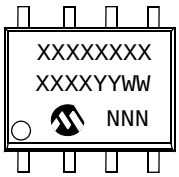

8-Lead PDIP (300 mil)



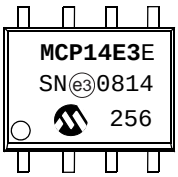

Example:




8-Lead SOIC (150 mil)




Example:

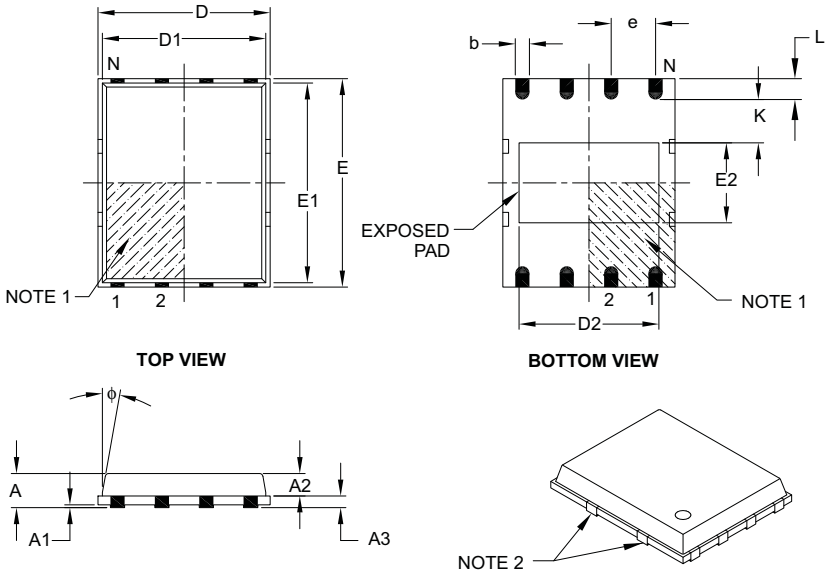



| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

## 8-Lead Plastic Dual Flat, No Lead Package (MF) – 6x5 mm Body [DFN-S] PUNCH SINGULATED

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | – | 0.85 | 1.00 |
| Molded Package Thickness | A2 | – | 0.65 | 0.80 |
| Standoff | A1 | 0.00 | 0.01 | 0.05 |
| Base Thickness | A3 | | 0.20 REF | |
| Overall Length | D | | 4.92 BSC | |
| Molded Package Length | D1 | | 4.67 BSC | |
| Exposed Pad Length | D2 | 3.85 | 4.00 | 4.15 |
| Overall Width | E | | 5.99 BSC | |
| Molded Package Width | E1 | | 5.74 BSC | |
| Exposed Pad Width | E2 | 2.16 | 2.31 | 2.46 |
| Contact Width | b | 0.35 | 0.40 | 0.47 |
| Contact Length | L | 0.50 | 0.60 | 0.75 |
| Contact-to-Exposed Pad | K | 0.20 | – | – |
| Model Draft Angle Top | ϕ | – | – | 12° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Dimensioning and tolerancing per ASME Y14.5M.

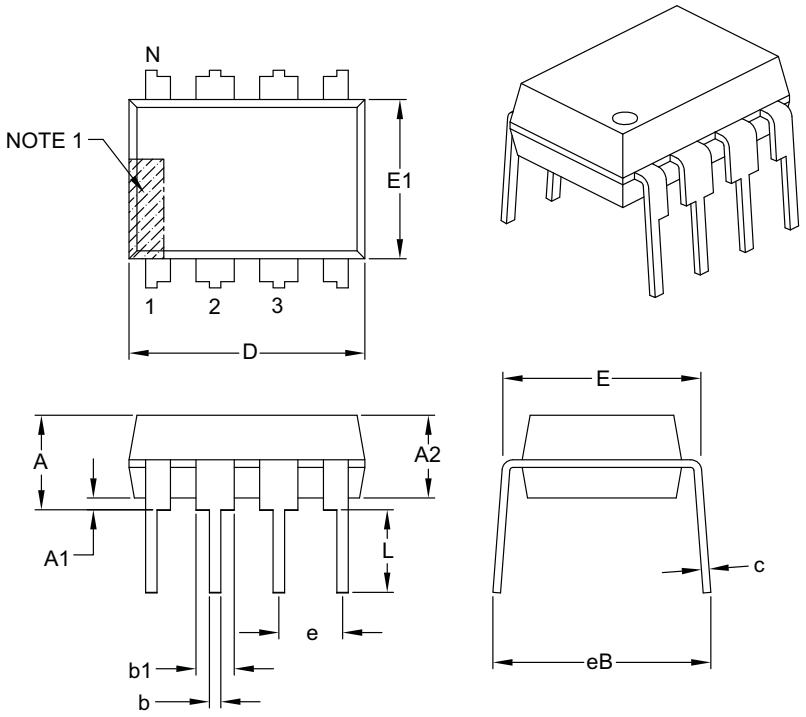
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-113B

## 8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | .100 BSC | |
| Top to Seating Plane | A | – | – | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 |
| Base to Seating Plane | A1 | .015 | – | – |
| Shoulder to Shoulder Width | E | .290 | .310 | .325 |
| Molded Package Width | E1 | .240 | .250 | .280 |
| Overall Length | D | .348 | .365 | .400 |
| Tip to Seating Plane | L | .115 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .060 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | – | – | .430 |

**Notes:**

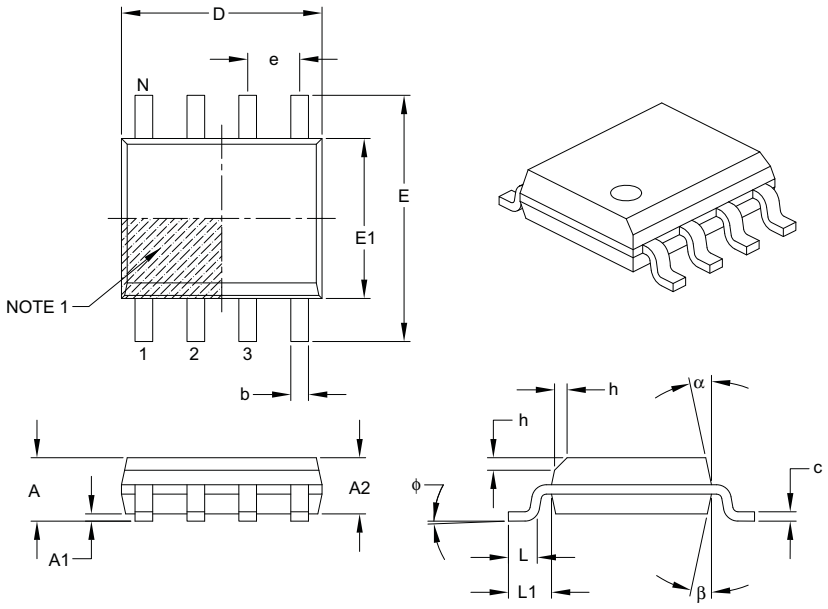
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

## 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | – | – | 1.75 |
| Molded Package Thickness | A2 | 1.25 | – | – |
| Standoff § | A1 | 0.10 | – | 0.25 |
| Overall Width | E | | 6.00 BSC | |
| Molded Package Width | E1 | | 3.90 BSC | |
| Overall Length | D | | 4.90 BSC | |
| Chamfer (optional) | h | 0.25 | – | 0.50 |
| Foot Length | L | 0.40 | – | 1.27 |
| Footprint | L1 | | 1.04 REF | |
| Foot Angle | φ | 0° | – | 8° |
| Lead Thickness | c | 0.17 | – | 0.25 |
| Lead Width | b | 0.31 | – | 0.51 |
| Mold Draft Angle Top | α | 5° | – | 15° |
| Mold Draft Angle Bottom | β | 5° | – | 15° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

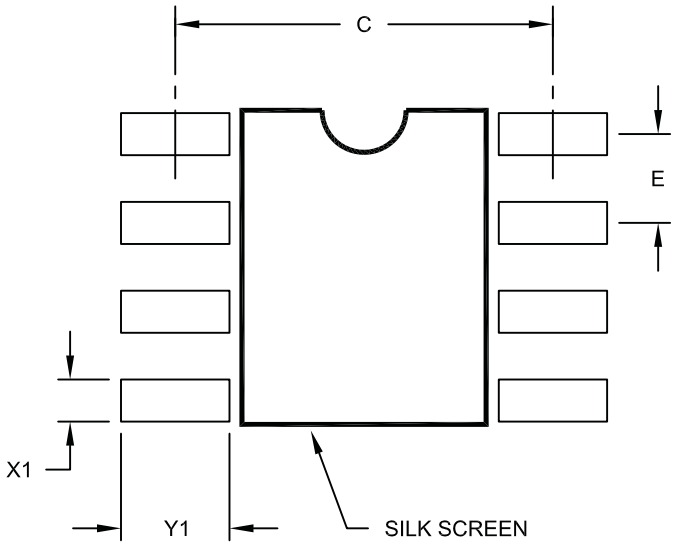
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

## 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.27 BSC | |
| Contact Pad Spacing | C | | 5.40 | |
| Contact Pad Width (X8) | X1 | | | 0.60 |
| Contact Pad Length (X8) | Y1 | | | 1.55 |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

**NOTES:**

# APPENDIX A: REVISION HISTORY

## Revision B (April 2008)

The following is the list of modifications:

1. Correct examples in Product identification System page.

## Revision A (September 2007)

- Original Release of this Document.

**NOTES:**

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | X | XX |
|---|---|---|
| Device | Temperature Range | Package |

| | | |
|---|---|---|
| Device: | MCP14E3: | 4.0A Dual MOSFET Driver, Inverting |
| | MCP14E3T: | 4.0A Dual MOSFET Driver, Inverting Tape and Reel |
| | MCP14E4: | 4.0A Dual MOSFET Driver, Non-Inverting |
| | MCP14E4T: | 4.0A Dual MOSFET Driver, Non-Inverting Tape and Reel |
| | MCP14E5: | 4.0A Dual MOSFET Driver, Complementary |
| | MCP14E5T: | 4.0A Dual MOSFET Driver, Complementary Tape and Reel |
| Temperature Range: | E = | -40°C to +125°C |
| Package: * | MF = | Dual, Flat, No-Lead (6x5 mm Body), 8-lead |
| | P = | Plastic DIP, (300 mil body), 8-lead |
| | SN = | Plastic SOIC (150 mil Body), 8-Lead |

* All package offerings are Pb Free (Lead Free)

**Examples:**

a) MCP14E3-E/MF: 4.0A Dual Inverting MOSFET Driver, 8LD DFN package.

b) MCP14E3-E/P: 4.0A Dual Inverting MOSFET Driver, 8LD PDIP package.

c) MCP14E3-E/SN: 4.0A Dual Inverting MOSFET Driver, 8LD SOIC package.

a) MCP14E4-E/MF: 4.0A Dual Non-Inverting MOSFET Driver, 8LD DFN package.

b) MCP14E4-E/P: 4.0A Dual Non-Inverting MOSFET Driver, 8LD PDIP package.

c) MCP14E4T-E/SN: Tape and Reel, 4.0A Dual Non-Inverting MOSFET Driver, 8LD SOIC package.

a) MCP14E5T-E/MF: Tape and Reel, 4.0A Dual Complementary MOSFET Driver, 8LD DFN package.

b) MCP14E5-E/P: 4.0A Dual Complementary MOSFET Driver, 8LD PDIP package.

c) MCP14E5-E/SN: 4.0A Dual Complementary MOSFET Driver, 8LD SOIC package.

**NOTES:**

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