Stereo 3.1W Class D Amplifier

ABSOLUTE MAXIMUM RATINGS

PVDD to PGND..-0.3V to +6V
OUT_+, OUT_- to PGND.......................-0.3V to (V_{PVDD} + 0.3V)
All Other Pins to PGND..-0.3V to +6V
Continuous Current for PVDD, PGND,
OUTL_, OUTR_ .... ±1600mA
Continuous Input Current (all other pins)........................ ±20mA
Duration of Short Circuit Between
OUTL_, OUTR_ to PVDD or PGND........................Continuous
OUTL+ to OUTL-, OUTR+ to OUTR- ....Continuous

Continuous Power Dissipation for Multilayer Board (T_A = +70°C)
16-Bump WLP (derate 17.2mW/°C above +70°C)........1.38W
θ_{JA} (Note 1)...58°C/W
θ_{JC} (Note 1) ....15°C/W
Junction Temperature ....+150°C
Operating Temperature Range.......................... -40°C to +85°C
Storage Temperature Range............................ -65°C to +150°C
Soldering Temperature (reflow) ....+260°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{PVDD} = $V_{\overline{SHDN}}$ = 3.7V, V_{PGND} = 0V, A_V = 12dB (GAIN = PVDD), R_L = ∞, R_L connected between OUT_+ to OUT_-, 20Hz to 22kHz AC measurement bandwidth, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{PVDD}	Inferred from PSRR test	2.6		5.5	V
Undervoltage Lockout	UVLO				2.3	V
Quiescent Supply Current	I_{DD}			2.0	3.1	mA
		V_{PVDD} = 5.0V		2.7		
Shutdown Supply Current	$I_{\overline{SHDN}}$	$V_{\overline{SHDN}}$ = 0V, T_A = +25°C		≤ 0.1	10	µA
Turn-On Time	t_{ON}			3.4	10	ms
Bias Voltage	V_{BIAS}			1.3		V
Voltage Gain	A_V	Connect GAIN to PGND	17.5	18	18.5	dB
		Connect GAIN to PGND through 100kΩ ±5% resistor	14.5	15	15.5	
		Connect GAIN to PVDD	11.5	12	12.5	
		Connect GAIN to PVDD through 100kΩ ±5% resistor	8.5	9	9.5	
		GAIN unconnected	5.5	6	6.5	
Channel-to-Channel Gain Tracking				±0.1		%
Input Resistance	R_{IN}	A_V = 18dB	15	20	29	kΩ
		A_V = 15dB	15	20	29	
		A_V = 12dB	15	20	29	
		A_V = 9dB	20	28	40	
		A_V = 6dB	30	40	58	
Output Offset Voltage	V_{OS}	T_A = +25°C (Note 4)		±0.3	±3	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{PVDD} = $V_{\overline{SHDN}}$ = 3.7V, V_{PGND} = 0V, A_V = 12dB (GAIN = PVDD), R_L = ∞, R_L connected between OUT_+ to OUT_-, 20Hz to 22kHz AC measurement bandwidth, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Click and Pop	K_{CP}	Peak voltage, A-weighted, 32 samples per second, R_L = 8Ω + 68µH (Notes 4, 5)	Into shutdown		-74		dBV
			Out of shutdown		-59		
Common-Mode Rejection Ratio	CMRR	f_{IN} = 1kHz, input referred	A_V = 18dB		67		dB
			A_V = 15dB		72		
			A_V = 12dB		67		
			A_V = 9dB		65		
			A_V = 6dB		62		
Crosstalk		P_{OUT} = 300mW, R_L = 8Ω + 68µH	f = 1kHz		100		dB
			f = 10kHz		95		
Power-Supply Rejection Ratio (Note 4)	PSRR	V_{PVDD} = 2.6V to 5.5V, T_A = +25°C		51	78		dB
		V_{RIPPLE} = 200mV_{P-P}, R_L = 8Ω + 68µH	f = 217Hz		66		
			f = 1kHz		66		
			f = 10kHz		63		
Output Power	P_{OUT}	THD+N = 10%, f = 1kHz, R_L = 4Ω + 33µH	V_{PVDD} = 5.0V		3.1		W
			V_{PVDD} = 4.2V		2.2		
			V_{PVDD} = 3.7V		1.7		
		THD+N = 1%, f = 1kHz, R_L = 4Ω + 33µH	V_{PVDD} = 5.0V		2.5		
			V_{PVDD} = 4.2V		1.7		
			V_{PVDD} = 3.7V		1.3		
		THD+N = 10%, f = 1kHz, R_L = 8Ω + 68µH	V_{PVDD} = 5.0V		1.8		
			V_{PVDD} = 4.2V		1.2		
			V_{PVDD} = 3.7V		1.0		
		THD+N = 1%, f = 1kHz, R_L = 8Ω + 68µH	V_{PVDD} = 5.0V		1.4		
			V_{PVDD} = 4.2V		1.0		
			V_{PVDD} = 3.7V		0.7		
Total Harmonic Distortion Plus Noise	THD+N	f_{IN} = 1kHz	R_L = 4Ω + 33µH, P_{OUT} = 1W		0.047		%
			R_L = 8Ω + 68µH, P_{OUT} = 0.5W		0.04		
Oscillator Frequency	f_{OSC}				300		kHz
Spread-Spectrum Bandwidth					±15		kHz
Efficiency	η	THD+N = 10%, f = 1kHz, R_L = 8Ω + 68µH			93		%
Output Noise	V_N	A_V = 6dB, A weighted (Note 4)			37		µV_{RMS}
Signal-to-Noise Ratio	SNR	P_{OUT} = 3.1W, V_{PVDD} = 5.0V, A_V = 6dB			99.6		dB

ELECTRICAL CHARACTERISTICS (continued)

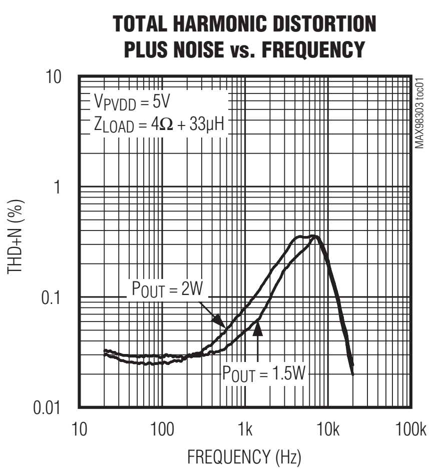
(V_{PVDD} = $V_{\overline{SHDN}}$ = 3.7V, V_{PGND} = 0V, A_V = 12dB (GAIN = PVDD), R_L = ∞, R_L connected between OUT_+ to OUT_-, 20Hz to 22kHz AC measurement bandwidth, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 3)

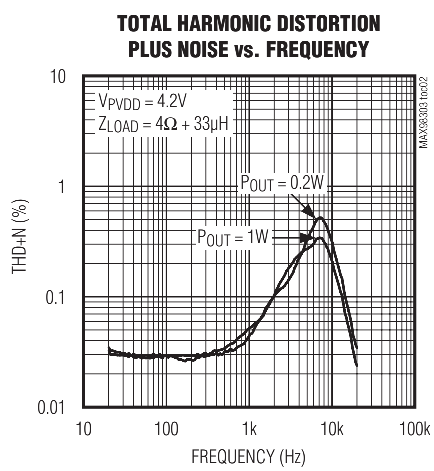
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Current Limit	I_{LIM}			2		A
Thermal Shutdown Level				145		°C
Thermal Shutdown Hysteresis				15		°C
DIGITAL INPUT ($\overline{SHDN}$)						
Input Voltage High	V_{INH}	V_{PVDD} = 2.5V to 5.5V	1.4			V
Input Voltage Low	V_{INL}	V_{PVDD} = 2.5V to 5.5V			0.4	V
Input Leakage Current		T_A = +25°C			±1	µA

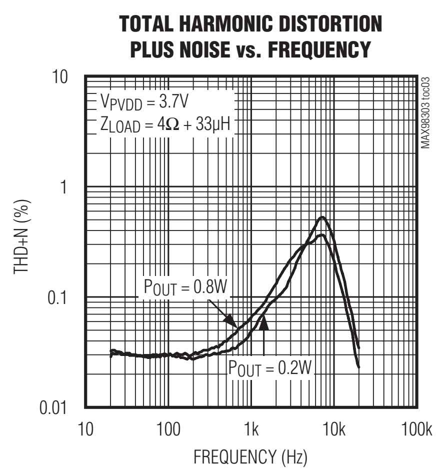
Note 2: This device is 100% production tested at T_A = +25°C. All temperature limits are guaranteed by design.
Note 3: Testing performed with a resistive load in series with an inductor to simulate an actual speaker load. For R_L = 4Ω, L = 33µH. For R_L = 8Ω, L = 68µH.
Note 4: Amplifier inputs AC-coupled to ground.
Note 5: Mode transitions controlled by $\overline{SHDN}$.

Typical Operating Characteristics

(V_{PVDD} = $V_{\overline{SHDN}}$ = 5.0V, V_{PGND} = 0V, A_V = 12dB, R_L = ∞, R_L connected between OUT_+ to OUT_-, 20Hz to 22kHz AC measurement bandwidth, T_A = +25°C, unless otherwise noted.)



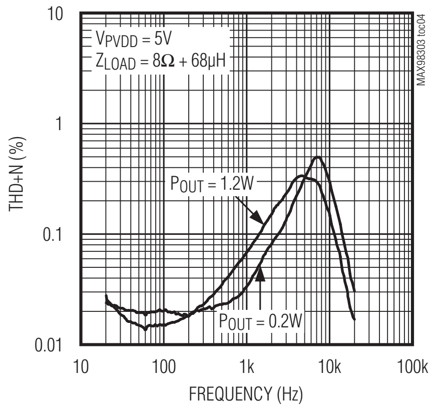




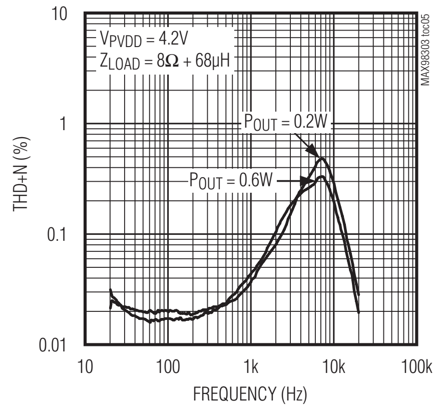
Typical Operating Characteristics (continued)

(V_{PVDD} = $V_{\overline{SHDN}}$ = 5.0V, V_{PGND} = 0V, A_V = 12dB, R_L = ∞, R_L connected between OUT_+ to OUT_-, 20Hz to 22kHz AC measurement bandwidth, T_A = +25°C, unless otherwise noted.)

TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



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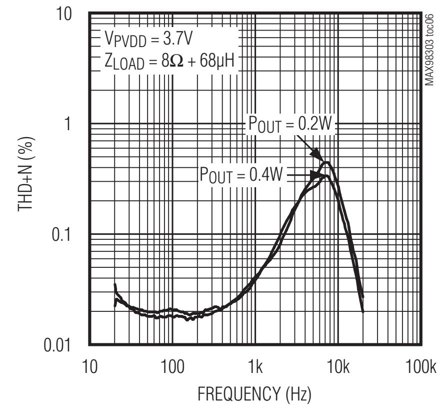
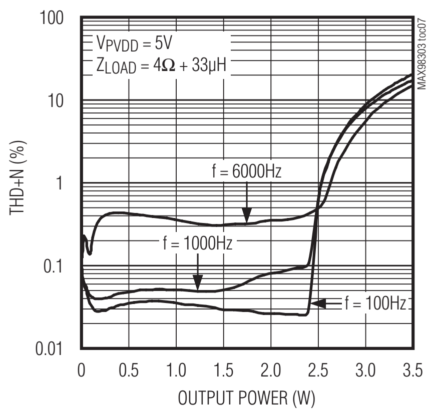


TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



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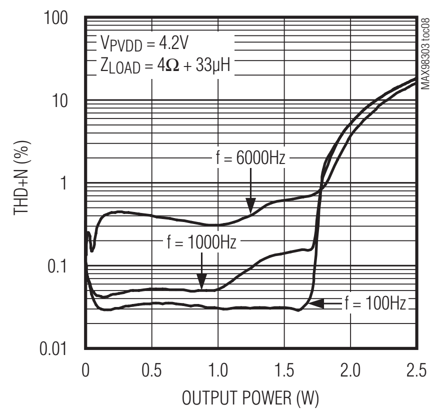
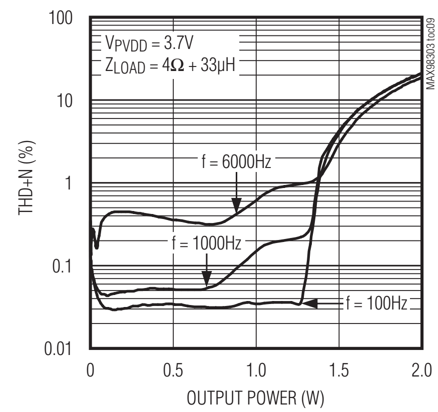
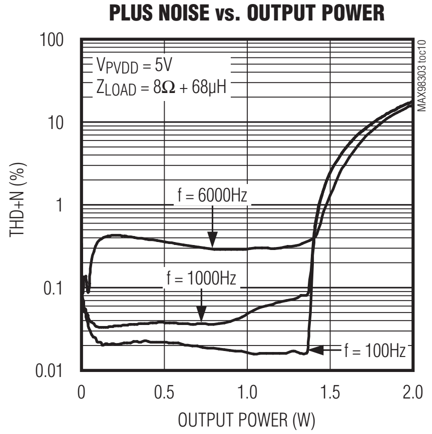


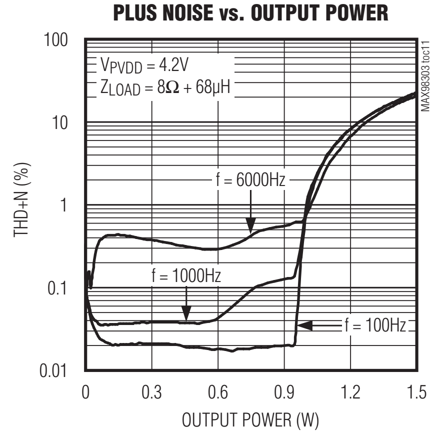
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



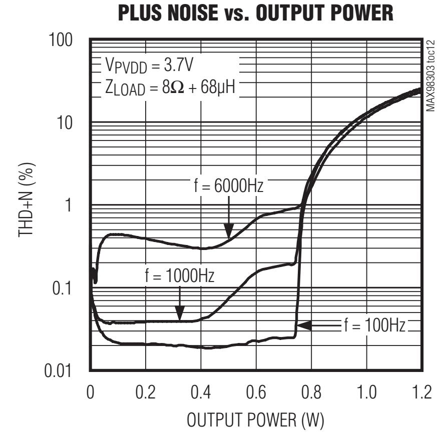
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



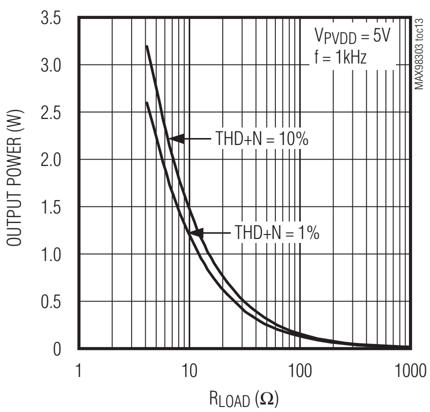
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



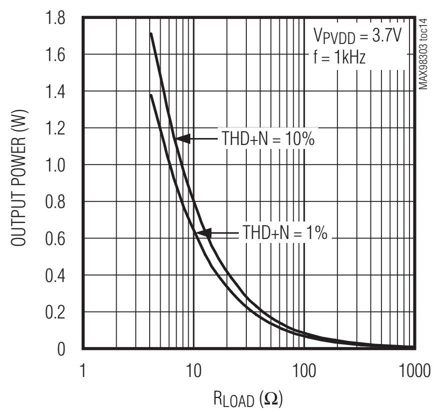
Typical Operating Characteristics (continued)

($V_{PVDD} = V_{\overline{SHDN}} = 5.0V$, $V_{PGND} = 0V$, $A_V = 12dB$, $R_L = \infty$, R_L connected between OUT_+ to OUT_-, 20Hz to 22kHz AC measurement bandwidth, $T_A = +25°C$, unless otherwise noted.)

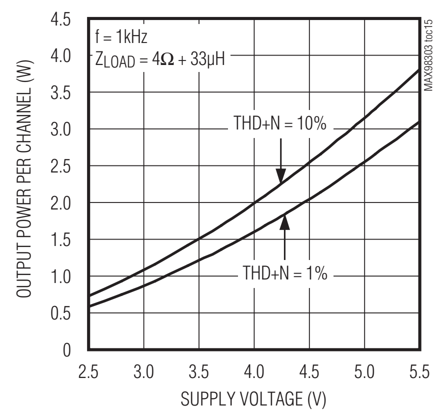
OUTPUT POWER vs. LOAD RESISTANCE



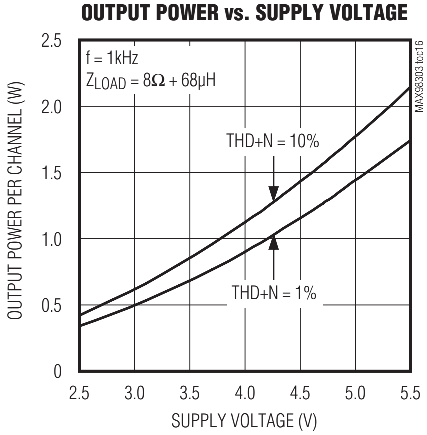
OUTPUT POWER vs. LOAD RESISTANCE



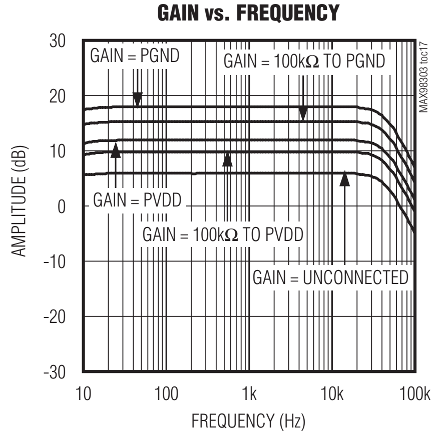
OUTPUT POWER vs. SUPPLY VOLTAGE



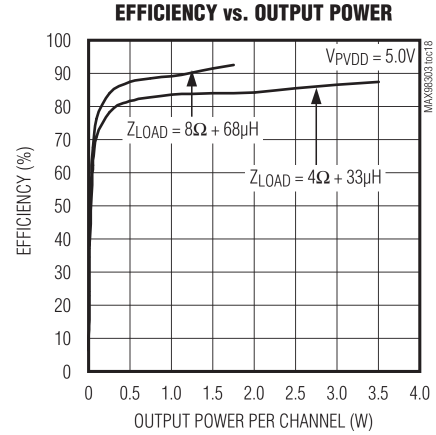
OUTPUT POWER vs. SUPPLY VOLTAGE



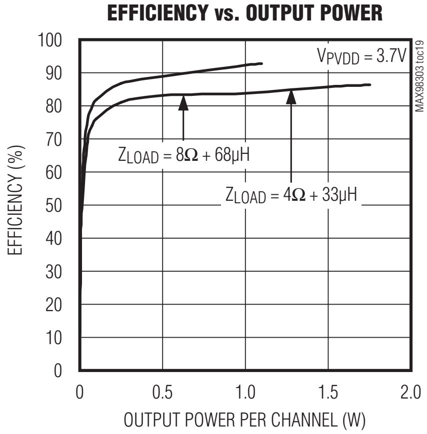
GAIN vs. FREQUENCY



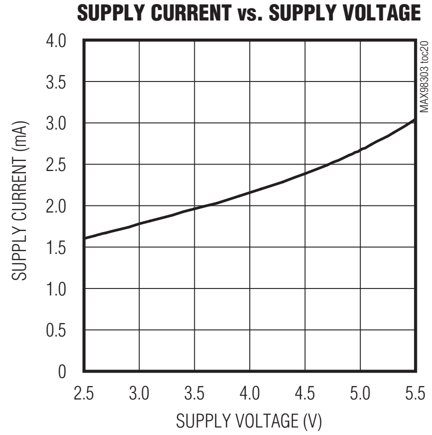
EFFICIENCY vs. OUTPUT POWER



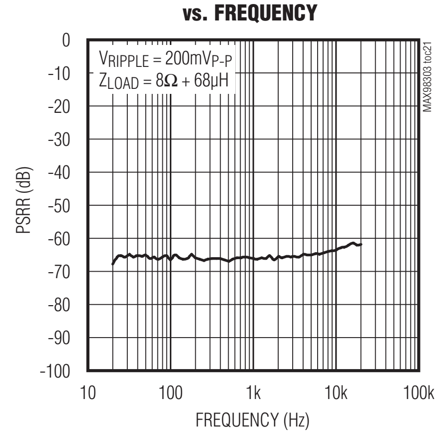
EFFICIENCY vs. OUTPUT POWER



SUPPLY CURRENT vs. SUPPLY VOLTAGE



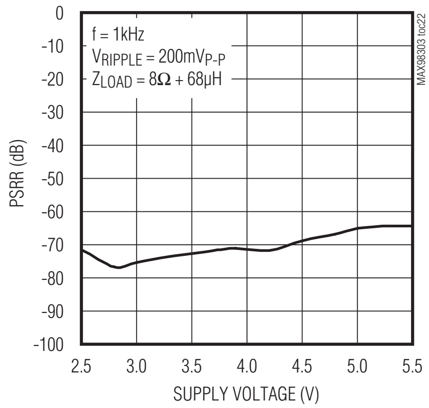
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



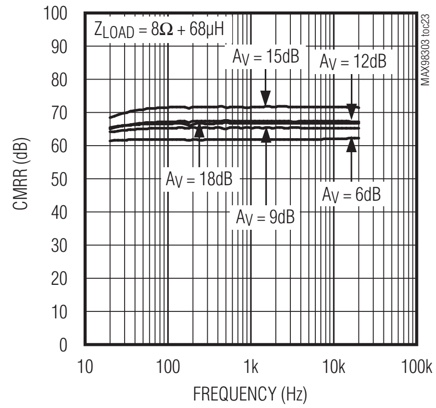
Typical Operating Characteristics (continued)

($V_{PVDD} = V_{\overline{SHDN}}$ = 5.0V, V_{PGND} = 0V, A_V = 12dB, R_L = ∞, R_L connected between OUT_+ to OUT_-, 20Hz to 22kHz AC measurement bandwidth, T_A = +25°C, unless otherwise noted.)

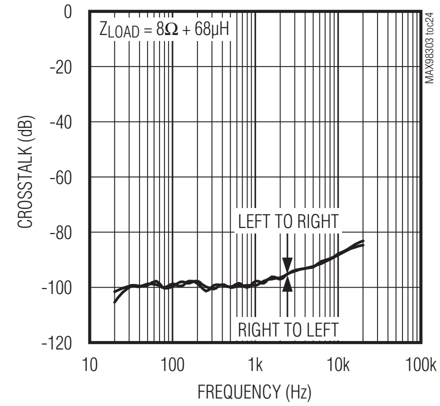
POWER-SUPPLY REJECTION RATIO vs. SUPPLY VOLTAGE



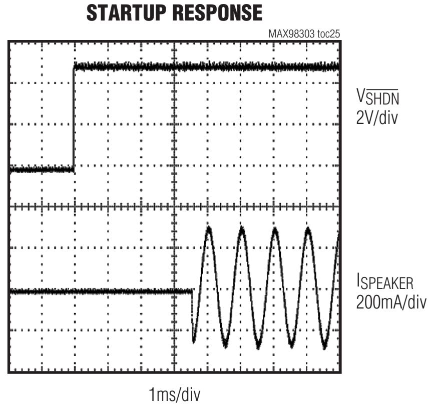
COMMON-MODE REJECTION RATIO vs. FREQUENCY



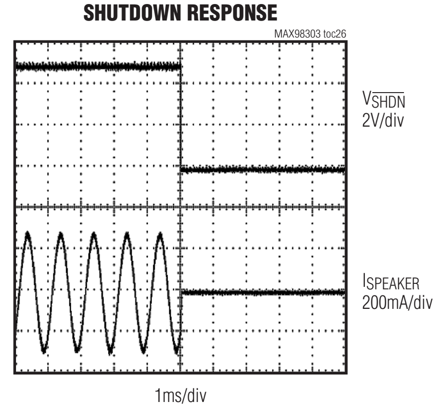
CROSSTALK vs. FREQUENCY



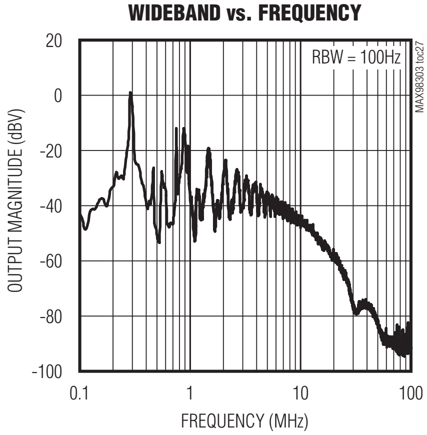
STARTUP RESPONSE



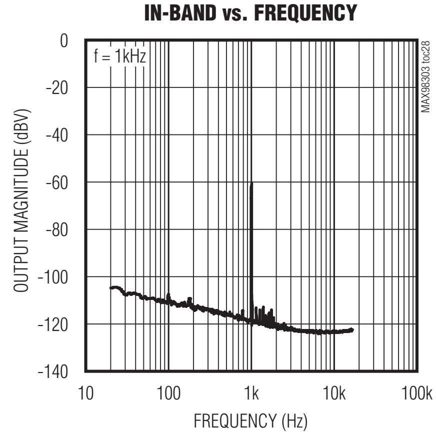
SHUTDOWN RESPONSE



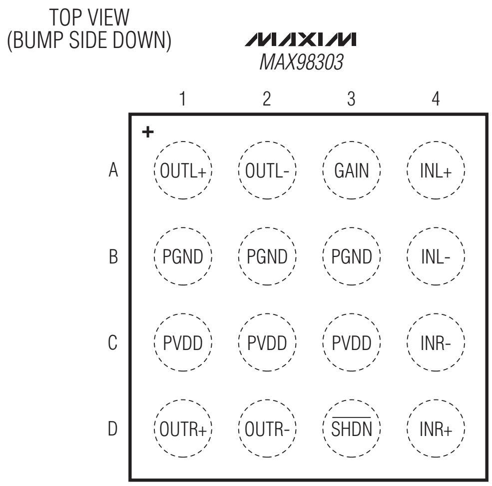
WIDEBAND vs. FREQUENCY



IN-BAND vs. FREQUENCY



Bump Configuration



WLP
(1.68mm x 1.68mm x 0.64mm, 0.4mm PITCH)

Bump Description

BUMP	NAME	FUNCTION
A1	OUTL+	Positive Left Speaker Output
A2	OUTL-	Negative Left Speaker Output
A3	GAIN	Gain Select. See Table 1 for Gain Settings.
A4	INL+	Noninverting Audio Left Input
B1, B2, B3	PGND	Ground
B4	INL-	Inverting Audio Left Input
C1, C2, C3	PVDD	Power Supply. Bypass PVDD to PGND with 0.1µF and 10µF capacitors.
C4	INR-	Inverting Audio Right Input
D1	OUTR+	Positive Right Speaker Output
D2	OUTR-	Negative Right Speaker Output
D3	$\overline{\text{SHDN}}$	Active-Low Shutdown Input. Drive $\overline{\text{SHDN}}$ low to place the device in shutdown.
D4	INR+	Noninverting Audio Right Input

Detailed Description

The MAX98303 features low quiescent current, a low-power shutdown mode, comprehensive click-and-pop suppression, and excellent RF immunity.

The IC offers Class AB audio performance with Class D efficiency in a minimal board-space solution.

The Class D amplifier features spread-spectrum modulation, edge-rate, and overshoot control circuitry that offers significant improvements to switch-mode amplifier radiated emissions.

The amplifier features click-and-pop suppression that reduces audible transients on startup and shutdown. The amplifier includes thermal-overload and short-circuit protection.

Class D Speaker Amplifier

The filterless Class D amplifier offers much higher efficiency than Class AB amplifiers. The high efficiency of a Class D amplifier is due to the switching operation of the output stage transistors. Any power loss associated with the Class D output stage is mostly due to the I^2R loss of the MOSFET on-resistance and quiescent current overhead.

Ultra-Low-EMI Filterless Output Stage

Traditional Class D amplifiers require the use of external LC filters, or shielding, to meet EN55022B electromagnetic-interference (EMI) regulation standards. Maxim's active emissions limiting edge-rate control circuitry and spread-spectrum modulation reduce EMI emissions, while maintaining up to 93% efficiency.

Maxim's spread-spectrum modulation mode flattens wideband spectral components, while proprietary techniques ensure that the cycle-to-cycle variation of the switching period does not degrade audio reproduction or efficiency. The IC's spread-spectrum modulator randomly varies the switching frequency by ±15kHz around the center frequency (300kHz). Above 10MHz, the wideband spectrum looks like noise for EMI purposes (Figure 1).

Speaker Current Limit

If the output current of the speaker amplifier exceeds the current limit (2A typ), the IC disables the outputs for approximately 100µs. At the end of 100µs, the outputs are reenabled. If the fault condition still exists, the IC continues to disable and reenable the outputs until the fault condition is removed.

Selectable Gain

The IC offers five programmable gains selected using the GAIN input.

Table 1. Gain Control Configuration

GAIN PIN	MAXIMUM GAIN (dB)
Connect to PGND	18
Connect to PGND through 100kΩ ±5% resistor	15
Connect to PVDD	12
Connect to PVDD through 100kΩ ±5% resistor	9
Unconnected	6

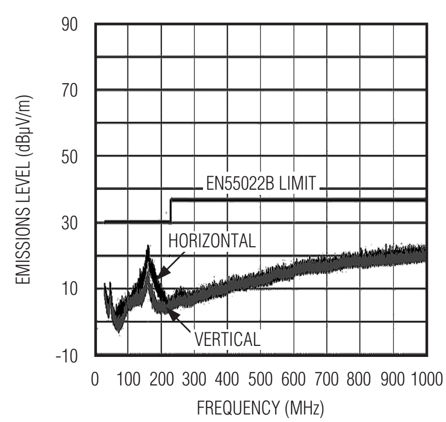


Figure 1. EMI with 30cm of Speaker Cable and No Output Filter

Shutdown

The IC features a low-power shutdown mode, drawing ≤ 0.1µA (typ) of supply current. Drive $\overline{SHDN}$ low to place the MAX98303 into shutdown.

Click-and-Pop Suppression

The IC speaker amplifier features Maxim's comprehensive click-and-pop suppression. During startup, the click-and-pop suppression circuitry reduces any audible transient sources internal to the device. When entering shutdown, the differential speaker outputs ramp down to PGND quickly and simultaneously.

Applications Information

Filterless Class D Operation

Traditional Class D amplifiers require an output filter. The filter adds cost and size and decreases THD performance. The IC's filterless modulation scheme does not require an output filter.

Because the switching frequency of the IC is well beyond the bandwidth of most speakers, voice coil movement due to the switching frequency is very small. Use a speaker with a series inductance > 10µH. Typical 8Ω speakers exhibit series inductances in the 20µH to 100µH range.

Component Selection

Power-Supply Input (PVDD)

PVDD powers the speaker amplifier. PVDD ranges from 2.6V to 5.5V. Bypass PVDD with 0.1µF and 10µF capacitors to PGND. Apply additional bulk capacitance at the device if long input traces between PVDD and the power source are used.

Input Filtering

The input-coupling capacitor (C_{IN}), in conjunction with the amplifier's internal input resistance (R_{IN}), forms a highpass filter that removes the DC bias from the incoming signal. These capacitors allow the amplifier to bias the signal to an optimum DC level.

Assuming zero source impedance with a gain setting of 12dB, 15dB, or 18dB, C_{IN} is:

$$C_{IN} = \frac{8}{f_{-3dB}}[\mu F]$$

with a gain setting of 9dB, C_{IN} is:

$$C_{IN} = \frac{5.7}{f_{-3dB}}[\mu F]$$

with a gain setting of 6dB, C_{IN} is:

$$C_{IN} = \frac{4}{f_{-3dB}}[\mu F]$$

where f_{-3dB} is the -3dB corner frequency. Use capacitors with adequately low-voltage coefficients for best low-frequency THD performance.

Layout and Grounding

Proper layout and grounding are essential for optimum performance. Good grounding improves audio performance and prevents switching noise from coupling into the audio signal.

Use wide, low-resistance output traces. As the load impedance decreases, the current drawn from the device increases. At higher current, the resistance of the output traces decrease the power delivered to the load. For example, if 2W is delivered from the device output to a 4Ω load through 100mΩ of total speaker trace, 1.904W is delivered to the speaker. If power is delivered through 10mΩ of total speaker trace, 1.99W is delivered to the speaker. Wide output, supply, and ground traces also improve the power dissipation of the device.

The IC is inherently designed for excellent RF immunity. For best performance, add ground fills around all signal traces on top or bottom PCB planes.

WLP Applications Information

For the latest application details on WLP construction, dimensions, tape carrier information, PCB techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to Application Note 1891: *Wafer level packaging (WLP) and its applications*. Figure 2 shows the dimensions of the WLP balls used on the IC.

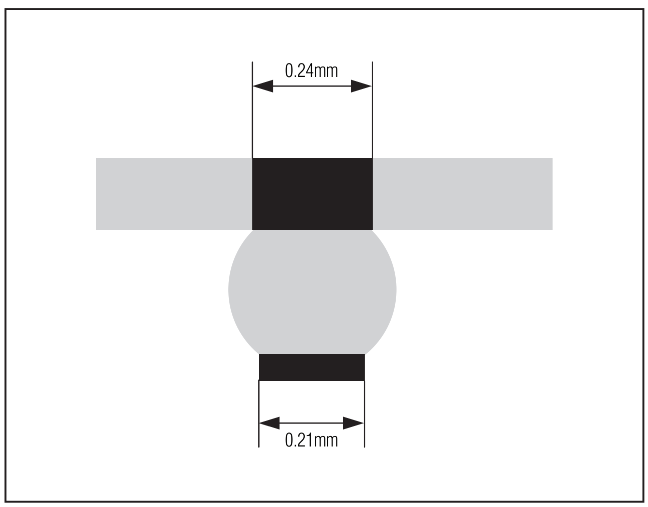
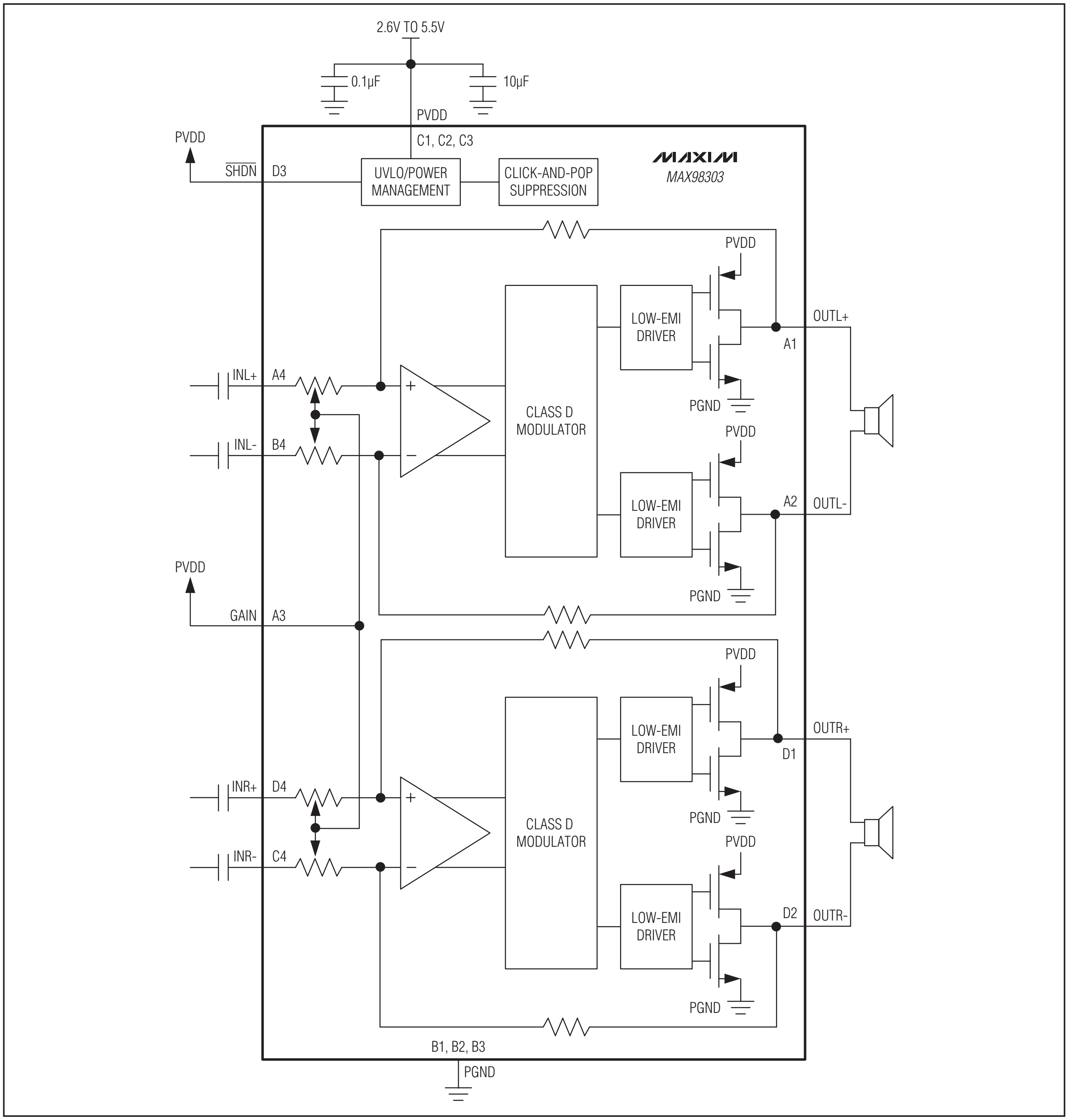


Figure 2. MAX98303 WLP Ball Dimensions

Block Diagram



Chip Information

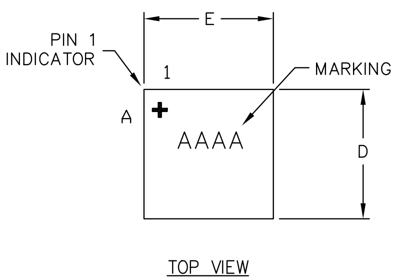
PROCESS: CMOS

Stereo 3.1W Class D Amplifier

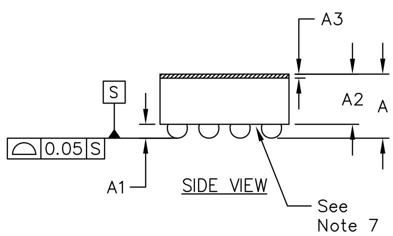
Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 WLP	W161B1+1	21-0491	—



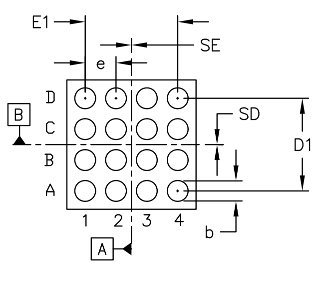
TOP VIEW



SIDE VIEW

COMMON DIMENSIONS	
A	0.64±0.05
A1	0.19±0.03
A2	0.45 REF
A3	0.025 BASIC
b	ø0.27±0.03
D1	1.20 BASIC
E1	1.20 BASIC
e	0.40 BASIC
SD	0.20 BASIC
SE	0.20 BASIC

PKG. CODE	E MIN	E MAX	D MIN	D MAX	DEPOPULATED BUMPS
W161B1+1	1.64	1.68	1.64	1.68	NONE



BOTTOM VIEW

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeters.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02mm unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front-side finish can be either Black or Clear.

MAXIM

TITLE: PACKAGE OUTLINE
16 BUMPS, WLP PKG. 0.4mm PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0491	A	1/1

–DRAWING NOT TO SCALE–

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/10	Initial release	—