Absolute Maximum Ratings

Voltage Range on V_{DD} Relative to GND .....-0.3V to +4V
Voltage Range on IN+, IN- Relative to GND.....-0.3V to +16V
Voltage Range on All Other Pins
Relative to GND... -0.3V to (V_{DD} + 0.3V) (not to exceed +4V)
Differential Input Voltage, IN+ to IN- .....±16V

Continuous Power Dissipation (T_A = +70°C)
16-Pin TQFN (derate 25mW/°C above +70°C).....2000mW
Operating Temperature Range..... -40°C to +85°C
Storage Temperature Range..... -55°C to +125°C
Soldering Temperature (reflow).....+260°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics(Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}).....40°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....6°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Recommended DC Operating Conditions

(T_A = -40°C to +85°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Operating Voltage Range	V_{DD}		2.7		3.6	V
Input Logic 1: ENA Pin	V_{IH1}		V_{DD} x 0.7		V_{DD} + 0.3	V
Input Logic 0: ENA Pin	V_{IL1}		-0.3		+0.3 x V_{DD}	V
Input Logic 1: SCL/SDA Pins	V_{IH2}		2.1		V_{DD} + 0.3	V
Input Logic 0: SCL/SDA Pins	V_{IL2}		-0.3		+0.8	V

Electrical Characteristics

(V_{IN+} = V_{IN-} = 12V, V_{SENSE} = 0V, V_{DD} = 2.7V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{DD}	SMBus idle		830		µA
Current-Sense Common-Mode Input Range			2.5		13.2	V
Input Bias Current (IN+/IN-)		Common-mode voltage = 13.2V, IN input differential = 12.25mV		2		µA
ADC Resolution			8			Bits
Per-Channel Current Sample Rate				1		ksps
IN Input Full Scale			12.00	12.25	12.50	mV
ADC INL				±0.5	±2	LSB
ADC DNL				±0.5	±2	LSB
IN Input Offset				±0.5	±4	LSB

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Electrical Characteristics (continued)

(V_{IN+} = V_{IN-} = 12V, V_{SENSE} = 0V, V_{DD} = 2.7V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Logic Low (SHTDN, $\overline{ALERT}$)	V_{OL}	I_{OL} = 4mA			0.4	V
Output Leakage (SHTDN, $\overline{ALERT}$)					±1	µA
SCL, SDA Leakage		V_{DD} = 0V or float			±5	µA
ENA Leakage					±1	µA
Digital Comparator Resolution			8			Bits
Delay Time from V_{DD} Applied Until SMBus Active (Figure 1)	t_{SMBD}			500		µs
Delay Time from Common-Mode Voltage Applied Until Current Monitoring Active (Figure 1)	t_{CSAD}			10		ms

AC Electrical Characteristics: I²C/SMBus Interface

(V_{DD} = 2.7V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = 3.3V, T_A = +25°C.) (Notes 3, 4) (Figure 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}		10		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$		0.6			µs
Low Period of SCL	t_{LOW}		1.3			µs
High Period of SCL	t_{HIGH}		0.6			µs
Data Hold Time	$t_{HD:DAT}$	Receive	0			ns
		Transmit	300			
Data Setup Time	$t_{SU:DAT}$		100			ns
Start Setup Time	$t_{SU:STA}$		0.6			µs
SDA and SCL Rise Time	t_R				300	ns
SDA and SCL Fall Time	t_F				300	ns
Stop Setup Time	$t_{SU:STO}$		0.6			µs
Clock Low Timeout	t_{TO}		25		35	ms

Note 2: All voltages are referenced to ground. Current entering the device are specified as positive and currents exiting the device are negative.

Note 3: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 4: All timing specifications are guaranteed by design.

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Timing Diagrams

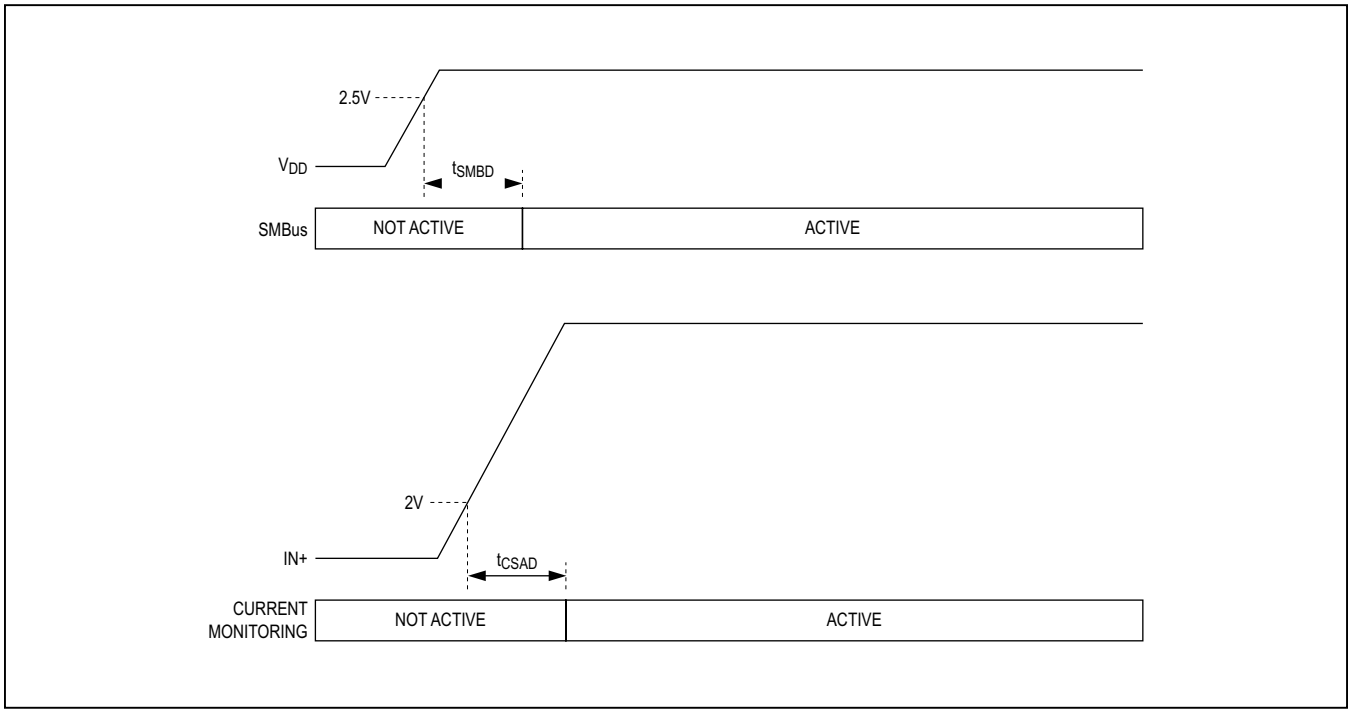

Figure 1. Delay Timing

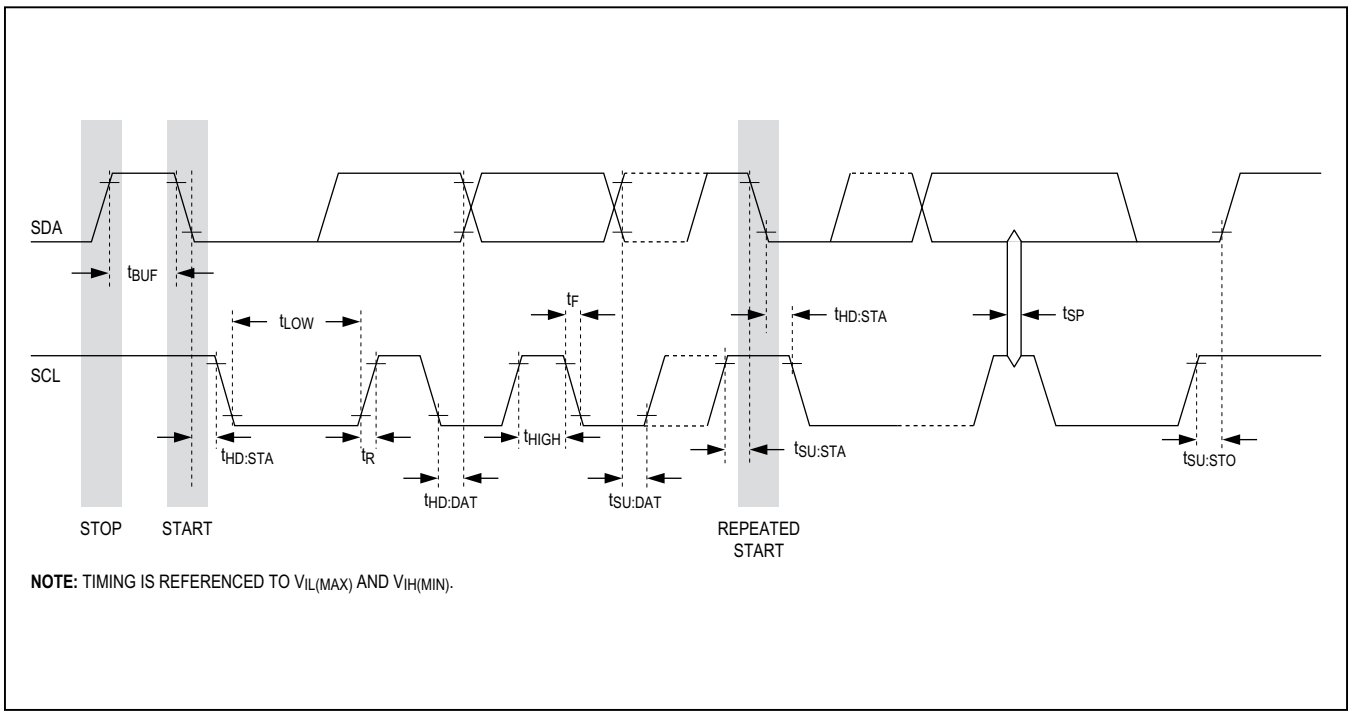

Figure 2. I^2C/SMBus Timing

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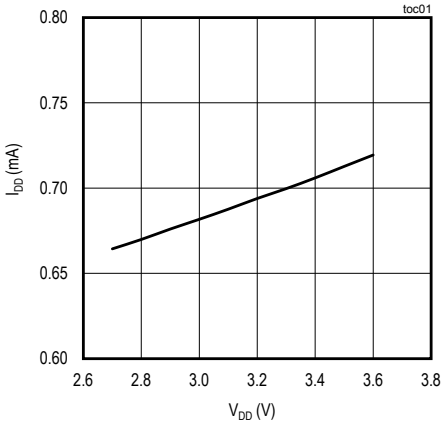
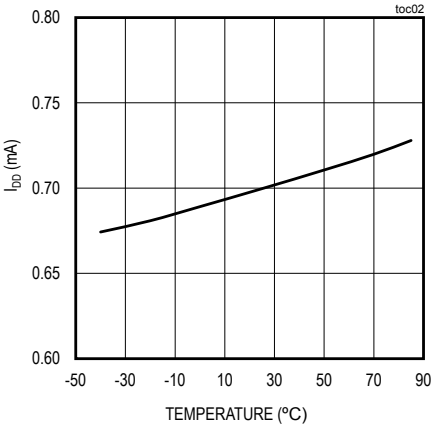
Typical Operating Characteristics

(V_{DD} = 3.3V and T_A = +25°C, common-mode voltage = 12.0V, unless otherwise noted.)

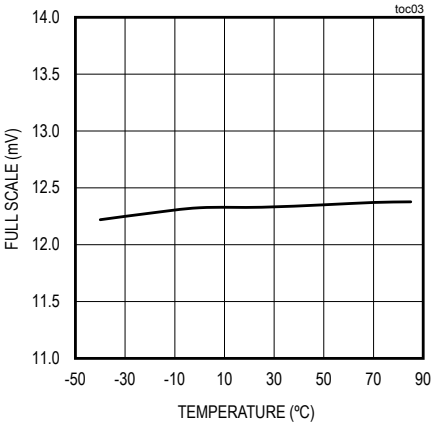
SUPPLY CURRENT vs. SUPPLY VOLTAGE



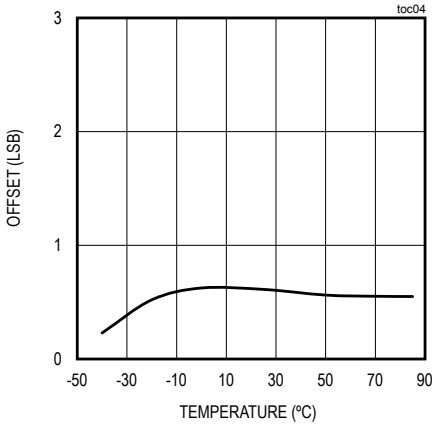
SUPPLY CURRENT vs. TEMPERATURE



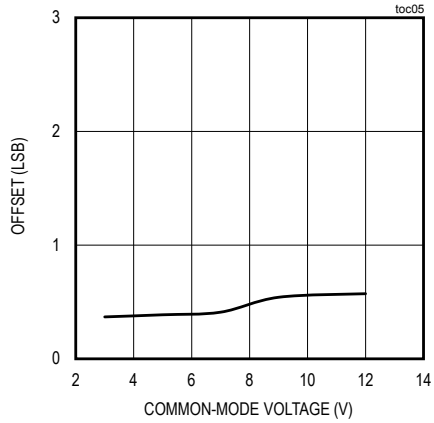
IN INPUT FULL SCALE vs. TEMPERATURE



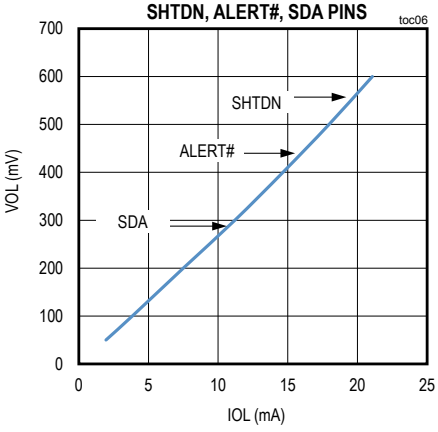
IN INPUT OFFSET vs. TEMPERATURE



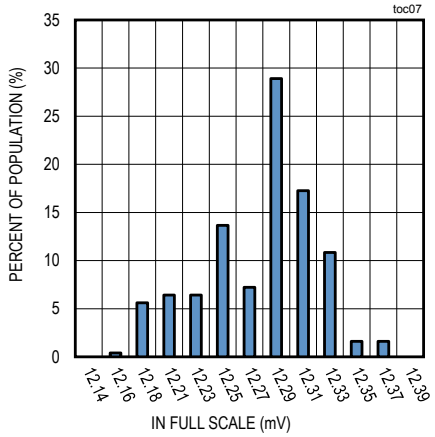
IN INPUT OFFSET vs. COMMON-MODE VOLTAGE



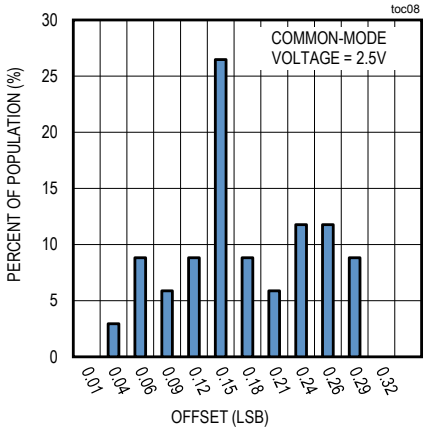
VOL vs. IOL SHTDN, ALERT#, SDA PINS



PERCENT OF POPULATION vs. IN FULL SCALE



PERCENT OF POPULATION vs. IN INPUT OFFSET



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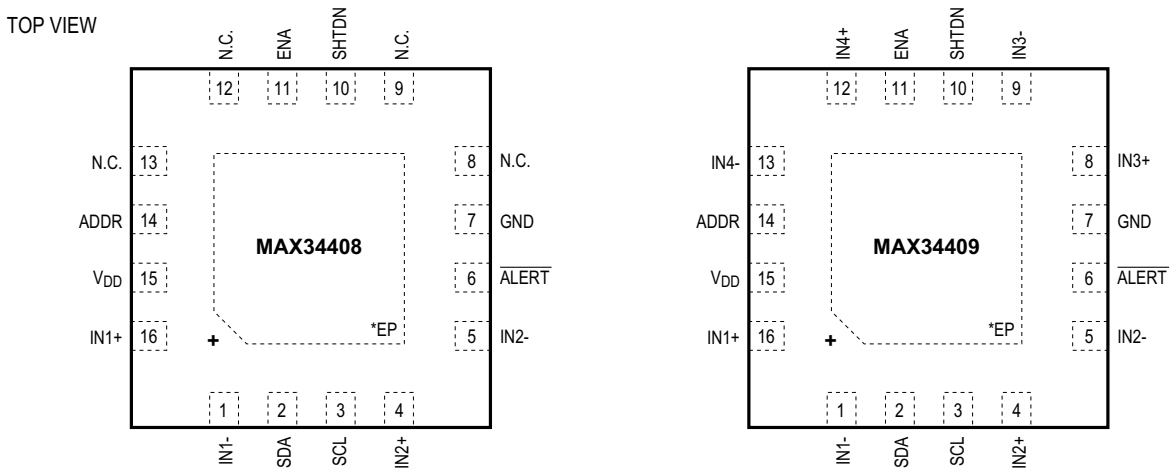
Pin Configurations



16 TQFN
(4mm x 4mm x 0.75mm)

*EXPOSED BACKSIDE PAD (EP)

Pin Description

PIN		NAME	FUNCTION
MAX34408	MAX34409		
1	1	IN1-	External Sense Resistor Load-Side Connection for Amplifier 1. This pin should be left open circuit if not needed.
2	2	SDA	I²C/SMBus-Compatible Data Input/Output. Output is open drain.
3	3	SCL	I²C/SMBus-Compatible Clock Input
4	4	IN2+	External Sense Resistor Power-Side Connection for Amplifier 2. This pin should be left open circuit if not needed.
5	5	IN2-	External Sense Resistor Load-Side Connection for Amplifier 2. This pin should be left open circuit if not needed.
6	6	$\overline{\text{ALERT}}$	I²C/SMBus Interrupt. Open-drain output.
7	7	GND	Ground Connection
8, 9, 12, 13	—	N.C.	No Connection. Do not connect any signal to this pin.
10	10	SHTDN	Shutdown Output. Open-drain output. This output transitions to high impedance when any of the digital comparator thresholds are exceeded as long as the ENA pin is high.
11	11	ENA	SHTDN Enable Input. CMOS digital input. Connect to GND to clear the latch and unconditionally deassert (force low) the SHTDN output and reset the shutdown delay. Connect to V_{DD} to enable normal latch operation of the SHTDN output.
14	14	ADDR	I²C/SMBus Address Select. On device power-up, the device samples a resistor to ground to determine the 7-bit serial bus address. See the *Addressing* section for details on which resistor values select which SMBus address.

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Pin Description (continued)

PIN		NAME	FUNCTION
MAX34408	MAX34409		
15	15	V_{DD}	Supply Voltage for Comparators and Logic. A +2.7V to +3.6V supply. This pin should be decoupled to GND with a 100nF ceramic capacitor.
16	16	IN1+	External Sense Resistor Power-Side Connection for Amplifier 1. This pin should be left open circuit if not needed.
—	8	IN3+	External Sense Resistor Power-Side Connection for Amplifier 3. This pin should be left open circuit if not needed.
—	9	IN3-	External Sense Resistor Load-Side Connection for Amplifier 3. This pin should be left open circuit if not needed.
—	12	IN4+	External Sense Resistor Power-Side Connection for Amplifier 4. This pin should be left open circuit if not needed.
—	13	IN4-	External Sense Resistor Load-Side Connection for Amplifier 4. This pin should be left open circuit if not needed.
—	—	EP	Exposed Pad. No internal electrical connection. Can be left open circuit.

Detailed Description

The MAX34408 and MAX34409 are two- and four-channel current monitors that are configured and monitored with a standard I²C/SMBus serial interface. Each unidirectional current sensor offers precision high-side operation with a low full-scale sense voltage. The devices automatically sequence through two or four channels and collect the current-sense samples and average them to reduce the effect of impulse noise. The raw ADC samples are compared to user-programmable digital thresholds to indicate overcurrent conditions. Overcurrent conditions trigger a hardware output to provide an immediate indication to shut down any necessary external circuitry.

The devices provide an $\overline{\text{ALERT}}$ output signal. Host communications are conducted through a SMBus-compatible communications port.

SMBus Operation

The devices use the SMBus command/response format as described in the System Management Bus Specification Version 2.0. The structure of the data flow between the host and the slave is shown for several different types of transactions. Data is sent MSB first. The fixed slave address of the MAX34408 or MAX34409 is determined on device power-up by sampling the resistor connected to the ADDR pin. See the *Addressing* section for details. On device power-up, the device defaults to the STATUS command code (00h). If the host sends an invalid command code, the device NACKs (not acknowledge) the command code. If the host attempts to read the device with an invalid command code, all ones (FFh) are returned in the data byte.

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Table 1. Read Byte Format

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Slave Address	W	A	Command Code	A	SR	Slave Address	R	A	Data Byte	NA	P

Table 2. Write Byte Format

1	7	1	1	8	1	8	1	1
S	Slave Address	W	A	Command Code	A	Data Byte	A	P

Key:

S = Start

SR = Repeated Start

P = Stop

W = Write Bit (0)

R = Read Bit (1)

A = Acknowledge (ACK) (0)

NA = Not Acknowledge (NACK) (1)

Shaded Block = Slave Transaction

Addressing

The devices respond to receiving the fixed slave address by asserting an ACK on the bus. The fixed slave address of the MAX34408 or MAX34409 is determined on device power-up by sampling the resistor connected to the ADDR pin. See Table 4 for more details. The devices do not respond to a General Call address, only when it receives its fixed slave address or the Alert Response Address (ARA). See the ALERT description for more details.

ALERT and Alert Response Address (ARA)

If the $\overline{\text{ALERT}}$ output is enabled (ALERT bit = 1 in CONTROL), when an overcurrent condition is detected, the devices assert the $\overline{\text{ALERT}}$ signal and then wait for the host to send the Alert Response Address (ARA) as shown in Table 5.

When the ARA is received and the devices are asserting $\overline{\text{ALERT}}$, the devices attempt to place the fixed slave address on the bus by arbitrating the bus since another device may also try to respond to the ARA. The rules of arbitration state that the lowest address device wins. If the devices win the arbitration, they deassert $\overline{\text{ALERT}}$. If the devices lose arbitration, they keep $\overline{\text{ALERT}}$ asserted and wait for the host to once again send the ARA.

Table 3. Receive Byte Format (reads data from the last transacted command code)

1	7	1	1	8	1	1
S	Slave Address	R	A	Data Byte	NA	P

Table 4. SMBus Slave Address Select

R_{ADDR} (±1%)	SLAVE ADDRESS	R_{ADDR} (±1%)	SLAVE ADDRESS
Open	0011 110 (3Ch)	3.01kΩ	0010 110 (2Ch)
9.31kΩ	0011 100 (38h)	1.69kΩ	0010 100 (28h)
6.81kΩ	0011 010 (34h)	750Ω	0010 010 (24h)
4.75kΩ	0011 000 (30h)	0 (connect to GND)	0010 000 (20h)

Table 5. Alert Response Address (ARA) Byte Format

1	7	1	1	8	1	1
S	ARA 0001100	R	A	Device Slave Address with LSB = 1	NA	P

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SMBus Commands

A summary of the SMBus commands supported by the devices are described in the following sections, see Table 6.

Table 6. Command Codes

COMMAND CODE	NAME	DETAILED DESCRIPTION	TYPE	POR (Note 1)
00h	STATUS	Overcurrent Alarm	R/W Byte	00h
01h	CONTROL	Device Configuration	R/W Byte	0Ch
02h	OCDELAY	Overcurrent Detection Delay Configuration	R/W Byte	04h
03h	SDDELAY	SHTDN Pin Delay Configuration	R/W Byte	14h
04h	ADC1	Averaged ADC Reading from Current Sensor 1	Read Byte	—
05h	ADC2	Averaged ADC Reading from Current Sensor 2	Read Byte	—
06h	ADC3	Averaged ADC Reading from Current Sensor 3 (Note 2)	Read Byte	—
07h	ADC4	Averaged ADC Reading from Current Sensor 4 (Note 2)	Read Byte	—
08h	OCT1	Overcurrent Threshold for Current Sensor 1	R/W Byte	D1h
09h	OCT2	Overcurrent Threshold for Current Sensor 2	R/W Byte	D1h
0Ah	OCT3	Overcurrent Threshold for Current Sensor 3 (Note 3)	R/W Byte	D1h
0Bh	OCT4	Overcurrent Threshold for Current Sensor 4 (Note 3)	R/W Byte	D1h
0Ch	DID	Device ID & Revision	Read Byte	Factory Set
0Dh	DCYY	Date Code Year	Read Byte	Factory Set
0Eh	DCWW	Date Code Work Week	Read Byte	Factory Set

Note 1: POR = Power-on reset, and this is the default value when power is applied to the device.
Note 2: In the MAX34408, ADC3 and ADC4 always report 00h when read.
Note 3: In the MAX34408, OCT3 and OCT4 can be written to and read from, but they have no affect on the device.

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STATUS (00h)

The STATUS command returns 1 byte of information with a summary of the fault conditions along with the real-time status of the ENA and SHTDN pins. The STATUS byte message content is described in Table 7. See Figure 3 for STATUS bits 3:0 organization.

Table 7. STATUS (00h)—R/W Byte

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	NA	NA	ENA	SHTDN	OC4	OC3	OC2	OC1
POR	0	0	0	0	0	0	0	0

Note: Bit positions marked as NA are Not Assigned and have no meaning. These bits can be either 0 or 1 when read.

BIT	NAME	DESCRIPTION
5	ENA	This bit reports the real-time status of the ENA input pin. The ENA pin is sampled when SMBus communication is initiated. This bit has no affect on the $\overline{\text{ALERT}}$ output. Writing a 0 or 1 to this bit position has no affect on the device.
4	SHTDN	This bit reports the real-time status of the SHTDN output pin. The shutdown latch is sampled when SMBus communication is initiated. This bit has no affect on the $\overline{\text{ALERT}}$ output. Writing a 0 or 1 to this bit position has no affect on the device.
3:0	OC4/OC3/ OC2/OC1 (MAX34409)	These bits reflect the latched status of the overcurrent thresholds for each current sensor. The OCD0 to OCD3 bits configured with the OCDELAY command determine the number of consecutive overcurrent threshold excursion samples that are required to set these bits. Once set, these bits remain set until written with a 0. Once they are cleared, they are not set again until the sensed current has exceeded the threshold for the programmed delay time. The setting of any of these bits asserts the $\overline{\text{ALERT}}$ pin if the ALERT bit in the CONTROL command is set to a one. Reading or writing the STATUS command deasserts the $\overline{\text{ALERT}}$ pin if it is asserted. In the MAX34408, bit positions OC3 and OC4 are inactive.
1:0	OC2/OC1 (MAX34408)	

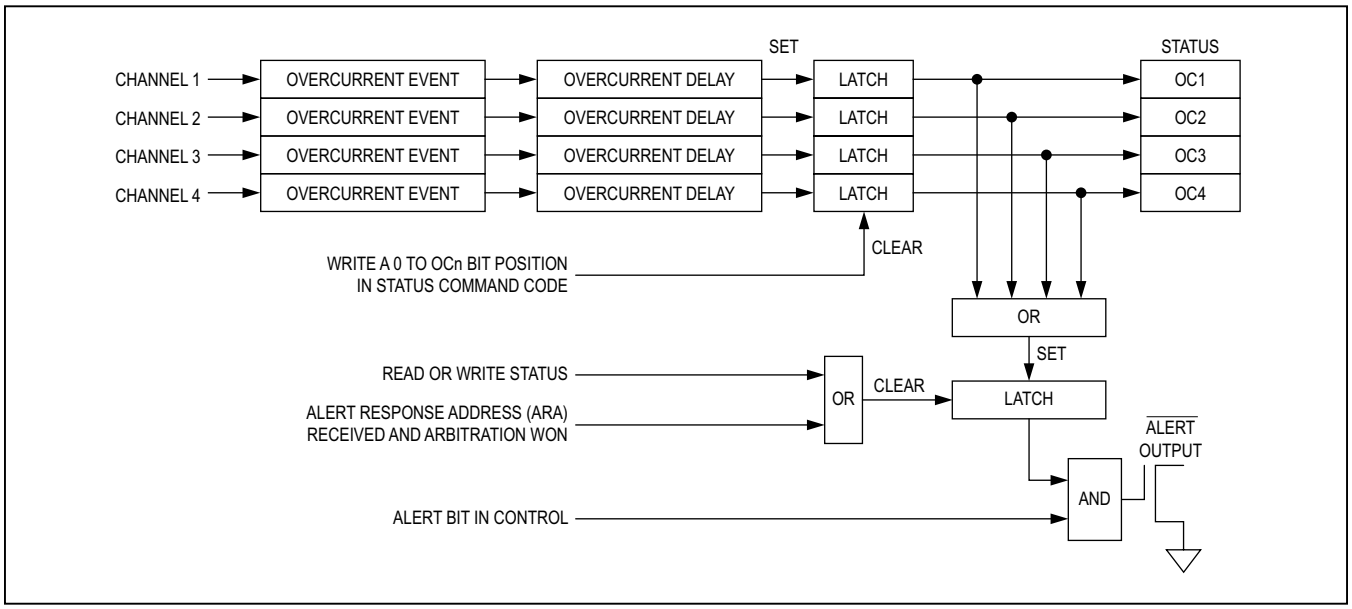

Figure 3. OCn Status Bits Set/Clear Functionality and $\overline{\text{ALERT}}$ Assertion

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CONTROL (01h)

The CONTROL command configures the digital current-sensing averaging function. The CONTROL command also defines if the devices respond to the Alert Response Address. The CONTROL byte command is described in Table 8.

Table 8. CONTROL (01h)—R/W Byte

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	NA	NA	NA	NA	ALERT	AVG2	AVG1	AVG0
POR	0	0	0	0	1	1	0	0

Note: Bit positions marked as NA are Not Assigned and have no meaning. These bits can be either 0 or 1 when read.

BIT	NAME	DESCRIPTION			
3	ALERT	If this bit is cleared, the $\overline{\text{ALERT}}$ output is disabled and the devices do not respond to the Alert Response Address. If this bit is set, the $\overline{\text{ALERT}}$ function is enabled and the devices respond to the Alert Response Address.			
2:0	AVG2/ AVG1/AVG0	These bits configure the digital current-sensing averaging function as shown below.			
		AVG2	AVG1	AVG0	SELECTED AVERAGING
		0	0	0	1 Sample (no averaging)
		0	0	1	2 Samples
		0	1	0	4 Samples
		0	1	1	8 Samples
		1	0	0	16 Samples (default)
		1	0	1	32 Samples
		1	1	0	64 Samples
		1	1	1	128 Samples

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OVER_CURRENT_DELAY (02h)

The OVER_CURRENT_DELAY command configures and resets the overcurrent delay counters. The OVER_CURRENT_DELAY byte command is described in Table 9. See Figure 4 for delay counter timing.

Table 9. OVER_CURRENT_DELAY (02h)—R/W Byte

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	RESET	OCD6	OCD5	OCD4	OCD3	OCD2	OCD1	OCD0
POR	0	0	0	0	0	1	0	0

BIT	NAME	DESCRIPTION		
7	RESET	If this bit is cleared, the OCD0 to OCD6 bits are used to set the overcurrent delay for all channels. If this is set, all of the overcurrent delay counters are reset and the devices do not trigger any overcurrent events and the OC status bits are cleared.		
6:0	OCD6 to OCD0	These bits configure the overcurrent delay as shown below. For each channel, the digital overcurrent threshold must be continuously breached in consecutive samples for the delay listed below before the respective OC bit in the STATUS register is set and the $\overline{\text{ALERT}}$ output is asserted (if enabled with the ALERT bit in the CONTROL command). For example, if the delay is set to 0ms, then the OC bit and the $\overline{\text{ALERT}}$ output are asserted on the first sample that breaches the threshold. If delay is set to 4ms, then the OC bit and the $\overline{\text{ALERT}}$ output are not asserted until the overcurrent threshold is exceeded in five consecutive samples.		
		OCD[6:0]	**OVERCURRENT DELAY**	
		00h	0ms	1 Event
		01h	1ms	2 Consecutive Events
		02h	2ms	3 Consecutive Events
		03h	3ms	4 Consecutive Events
		04h	4ms (default)	5 Consecutive Events
		14h	20ms	21 Consecutive Events
		15h	21ms	22 Consecutive Events
		7Eh	126ms	127 Consecutive Events
		7Fh	127ms	128 Consecutive Events

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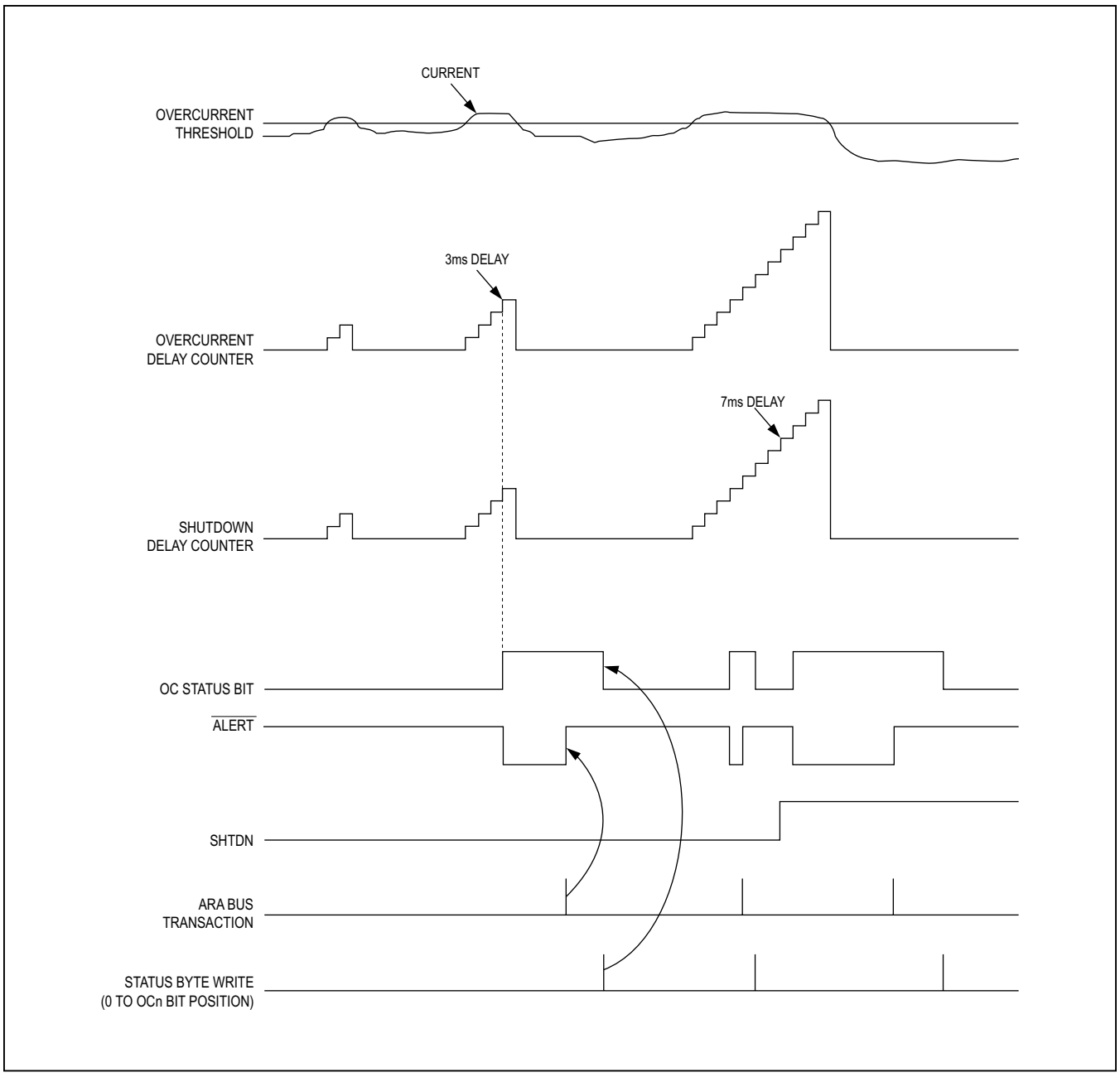

Figure 4. Delay Timing

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SHUTDOWN_DELAY (03h)

The SHUTDOWN_DELAY command configures and resets the shutdown delay counters. The SHUTDOWN_DELAY byte command is described in Table 10.

Table 10. SHUTDOWN_DELAY (03h)—R/W Byte

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	RESET	SHD6	SHD5	SHD4	SHD3	SHD2	SHD1	SHD0
POR	0	0	0	1	0	1	0	0

BIT	NAME	DESCRIPTION		
7	RESET	If this bit is cleared, the SHD0 to SHD6 bits are used to set the shutdown delay that is used to control the SHTDN pin. If this is set, the shutdown delay counter is reset and the SHTDN pin is forced inactive (low).		
6:0	SHD6 to SHD0	These bits configure the shutdown latch delay as shown below. For each channel, the digital overcurrent threshold must be continuously breached in consecutive samples for the delay listed below before the shutdown latch (and hence the SHTDN pin) is asserted. For example, if the delay is set to 0ms, then the SHTDN output is asserted on the first sample that breaches the threshold. If delay is set to 20ms, then the SHTDN output is not asserted until the overcurrent threshold is exceeded in 21 consecutive samples.		
		SHD[6:0]	SHUTDOWN DELAY	
		00h	0ms	1 Event
		01h	1ms	2 Consecutive Events
		02h	2ms	3 Consecutive Events
		03h	3ms	4 Consecutive Events
		13h	19ms	20 Consecutive Events
		14h	20ms (default)	21 Consecutive Events
		15h	21ms	22 Consecutive Events
		7Eh	126ms	127 Consecutive Events
		7Fh	127ms	128 Consecutive Events

ADC1/2/3/4 (04h/05h/06h/07h)

The ADC1/2/3/4 command returns the associated latest measured current reading. The ADC1/2/3/4 byte command is described in Table 11.

Table 11. ADC1/2/3/4 (04h/05h/06h/07h)—Read Byte

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	C7	C6	C5	C4	C3	C2	C1	C0
POR	X	X	X	X	X	X	X	X

BIT	NAME	DESCRIPTION
7:0	C7 to C0	These bits report the latest current reading from the ADC. The reported results are averaged according to the averaging function as configured with the AVG0 to AVG2 bits in the CONTROL command. Reading the ADC results faster than they are sampled and averaged results in the previous values being reported. In the MAX34408, ADC3 and ADC4 always report 00h when read.

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OVER_CURRENT_THRESHOLD_1/2/3/4 (08h/09h/0Ah/0Bh)

The OVER_CURRENT_THRESHOLD_1/2/3/4 command sets the overcurrent threshold for each channel. The OVER_CURRENT_THRESHOLD_1/2/3/4 byte command is described in Table 12. See Table 13 for the configuration formula and Table 14 for an example.

Table 12. OVER_CURRENT_THRESHOLD_1/2/3/4 (08h/09h/0Ah/0Bh)—R/W Byte

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	OCT7	OCT6	OCT5	OCT4	OCT3	OCT2	OCT1	OCT0
POR	1	1	0	1	0	0	0	1

Note: In the MAX34408, OCT3 and OCT4 can be written to and read from but they have no affect on the device.

BIT	NAME	DESCRIPTION
7:0	OCT7 to OCT0	These bits select the digital overcurrent threshold for each channel. The formula for selecting the threshold is as shown in Table 13. If the threshold is set to FFh, the digital comparator is disabled and the output of the comparator is unconditionally deasserted.

Table 13. Overcurrent Threshold Register Configuration Formula

Overcurrent Threshold Analog Voltage at the IN+/IN- Pins	÷	0.01225	=	Ratio to Full Scale	x	256	=	Rounded Decimal Value	=	Overcurrent Threshold Register Setting

Table 14. Overcurrent Threshold Register Example

10mV	÷	0.01225	=	0.816	x	256	=	209	=	D1h

DEVICE_ID_&_REVISION (0Ch)

The DEVICE_ID_&_REVISION command returns a fixed device ID and a factory programmed revision. The DEVICE_ID_&_REVISION byte command is described in Table 15.

Table 15. DEVICE_ID_&_REVISION (0Ch)—Read Byte

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	ID4	ID3	ID2	ID1	ID0	REV2	REV1	REV0
POR	0	0	0	0	1	Factory set		

BIT	NAME	DESCRIPTION
7:3	ID4 to ID0	These bits report the device identification (ID). The ID is fixed at 01h.
2:0	REV2 to REV0	These bits report the device revision. The device revision is factory set.

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DATE_CODE_YEAR (0Dh)

The DATE_CODE_YEAR command returns a factory programmed date code. The DATE_CODE_YEAR byte command is described in Table 16.

Table 16. DATE_CODE_YEAR (0Dh)—Read Byte

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	0	0	YY5	YY4	YY3	YY2	YY1	YY0
POR	Factory Set							

BIT	NAME	DESCRIPTION	
5:0	YY5 to YY0	These bits report the last two decimal digits of the calendar year in which the device was tested. The year is reported as a binary decimal. Some examples are listed below. The range is valid until the year 2063.	
		YY[5:0]	YEAR
		0Ch	2012
		0Dh	2013
		14h	2020

DATE_CODE_WORK_WEEK (0Eh)

The DATE_CODE_WORK_WEEK command returns a factory-programmed date code. The DATE_CODE_WORK_WEEK byte command is described in Table 17.

Table 17. DATE_CODE_WORK_WEEK (0Eh)—Read Byte

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	0	0	WW5	WW4	WW3	WW2	WW1	WW0
POR	Factory Set							

BIT	NAME	DESCRIPTION	
5:0	WW5 to WW0	These bits report the calendar work week in which the device was tested. The work week is reported as a binary decimal. Some examples are listed below. 00h (0 decimal) and 36h (54 decimal) through 3Fh (63) are not valid.	
		WW[5:0]	WORK WEEK
		06h	6
		0Dh	13
		2Bh	43

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Applications Information

Sense Resistor, R_{SENSE}

Adjust the R_{SENSE} value to monitor higher or lower current levels. Select R_{SENSE} based on the following criteria:

Resistor Value: Select an R_{SENSE} resistor value in which the largest expected current results in a 10mV full-scale current-sense voltage. Select R_{SENSE} in accordance to the following equation and see Table 18 for examples:

$$R_{SENSE} = 10mV/(Max\ Current)$$

Power Dissipation: Select a sense resistor that is rated for the max expected current and power dissipation (wattage). The sense resistor's value might drift if it is allowed to heat up excessively.

Accuracy

Current measurement accuracy increases the closer the measured current readings are to the 12.25mV full-scale current-sense voltage. This is because offsets become less significant when the sense voltage is larger. For best performance, select R_{SENSE} to provide approximately 10mV of sense voltage for the full-scale current in each application. Figure 5 shows the error contributed by the input offset vs. reading percentage of full scale.

Table 18. R_{SENSE} Example Values

R_{SENSE} (mΩ)	MAX CURRENT (A)
0.25	40
0.5	20
1	10
5	2
10	1
50	0.2
100	0.1
200	0.05
500	0.02

Kelvin Connections

Because of the high currents that flow through R_{SENSE}, take care to eliminate parasitic trace resistance from causing errors in the sense voltage. Use Kelvin (force and sense) PCB layout techniques as shown in Figure 6.

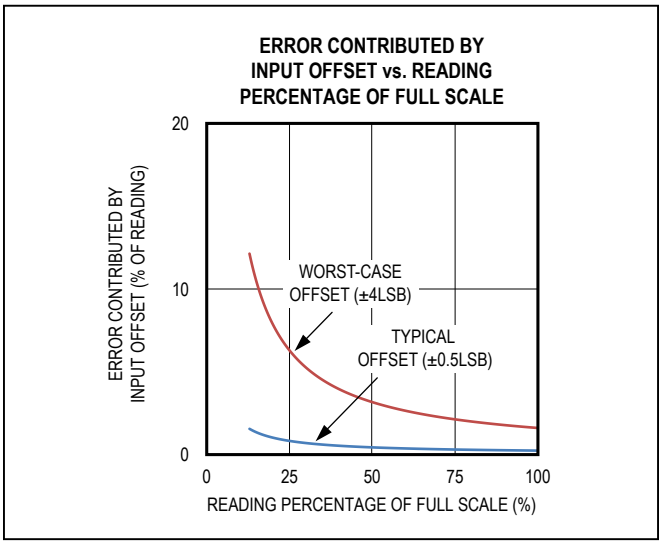

Figure 5. Input Offset Error

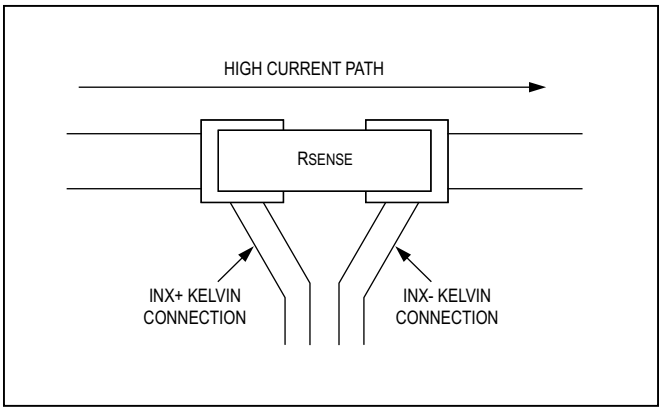

Figure 6. Kelvin Connection Layout Example

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Optional Filter Network

For noisy environments, a simple lowpass filter can be placed at the devices' amplifier inputs as shown in Figure 7. The 100Ω resistor and 1µF capacitor provide a 1.6kHz rolloff frequency. To achieve the most effective results, use the filter in conjunction with the device's digital averaging as described in the *CONTROL (01h)* section.

Layout Considerations

For noisy digital environments, the use of a multilayer PCB with separate ground and power-supply planes is recommended. Keep digital signals far away from the sensitive analog inputs. Unshielded long traces at the input terminals of the amplifier can degrade performance due to noise pickup. The analog differential current-sense traces should be routed close together to maximize common-mode rejection.

Power-Supply Decoupling

To achieve the best results when using these devices, decouple the V_{DD} power supply with a 0.1µF capacitor. Use a high-quality, ceramic, surface-mount capacitor if possible. Surface-mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high-frequency response for decoupling applications.

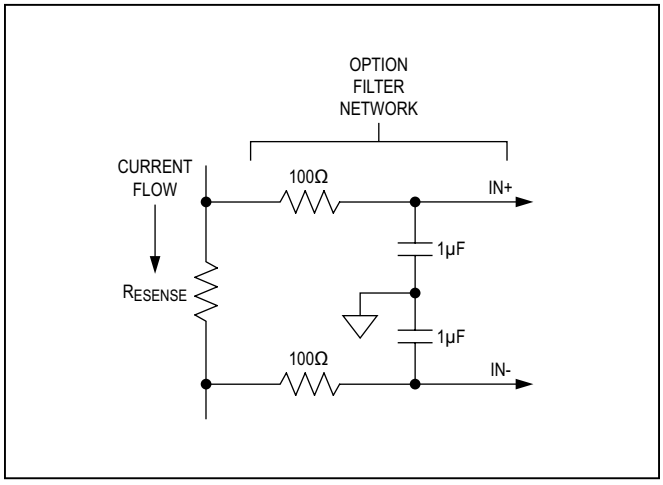

Figure 7. Filter Network

Ordering Information

PART	CONFIGURATION	PIN-PACKAGE
MAX34408ETE+	Dual	16 TQFN-EP*
MAX34409ETE+	Quad	16 TQFN-EP*

+Denotes a lead (Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TQFN-EP	T1644+4	**21-0139**	**90-0070**

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/13	Initial release	—
1	1/15	Updated *Benefits and Features* section	1

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