

±15kV ESD-Protected USB Transceivers in UCSP with USB Detect

ABSOLUTE MAXIMUM RATINGS

(All voltages refer to GND, unless otherwise noted.)
 Supply Voltage (V_{CC}) -0.3V to +6V
 Output of Internal Regulator (V_{TRM}) -0.3V to ($V_{CC} + 0.3V$)
 Input Voltage (D+, D-) -0.3V to +6V
 System Supply Voltage (V_L) -0.3V to +6V
 RCV, SUSP, VMO, MODE, VPO, $\overline{OE}$, VMI,
 VPI, USB_DET, ENUM -0.3V to ($V_L + 0.3V$)
 Short-Circuit Current (D+, D-) to V_{CC} or
 GND (Note 1) Continuous

Maximum Continuous Current (all other pins) ±15mA
 Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)
 16-Pin TSSOP (derate 9.4mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) ... 754mW (U16-2)
 4 × 4 UCSP (derate 8.2mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) ... 659mW (B16-1)
 Operating Temperature Range -40°C to $+85^\circ\text{C}$
 Junction Temperature $+150^\circ\text{C}$
 Storage Temperature Range -65°C to $+150^\circ\text{C}$
 Lead Temperature (soldering, 10s) $+300^\circ\text{C}$
 Bump Temperature (soldering) Reflow $+235^\circ\text{C}$

Note 1: External 23.7Ω resistors connected to D+ and D-.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{CC} = 4V$ to $5.5V$ bypassed with $1\mu F$ to GND, GND = 0, $V_L = 1.65V$ to $3.6V$, ENUM = V_L , $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_{CC} = 5V$, $V_L = 2.5V$, $T_A = +25^\circ\text{C}$.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY INPUTS (V_{CC}, V_{TRM}, V_L)						
Regulated Supply Voltage Output	V_{TRM}	Internal regulator	3.0	3.3	3.6	V
V_{CC} Input Range	V_{CC}		4.0		5.5	V
V_L Input Range	V_L		1.65		3.60	V
Operating V_{CC} Supply Current	I_{VCC}	Full-speed transmitting/receiving at 12Mbps, $C_L = 50pF$ on D+ and D-			10	mA
Operating V_L Supply Current	I_{VL}	Full-speed transmitting/receiving at 12Mbps			8	mA
Full-Speed Idle and SE0 Supply Current	$I_{VCC(IDLE)}$	Full-speed idle: $V_{D+} > 2.7V$, $V_{D-} < 0.3V$		340	450	μA
		SE0: $V_{D+} < 0.3V$, $V_{D-} < 0.3V$		390	500	
Static V_L Supply Current	$I_{VL(STATIC)}$	Full-speed idle, SE0, or suspend mode			12.5	μA
Suspend Supply Current	$I_{VCC(SUSP)}$	SUSP = $\overline{OE}$ = high			40	μA
Disable-Mode Supply Current	$I_{VCC(DIS)}$	$V_L = \text{GND}$ or open			20	μA
D+/D- Disable-Mode Load Current	$I_{D(DIS)}$	$V_L = \text{GND}$ or open, $V_{D-} = 0$ or $+5.5V$			5	μA
Sharing-Mode V_L Supply Current	$I_{VL(SHARING)}$	$V_{CC} = \text{GND}$ or open, $\overline{OE} = \text{low}$, SUSP = high			20	μA
D+/D- Sharing-Mode Load Current	$I_{D(SHARING)}$	$V_{CC} = \text{GND}$ or open, $V_{D-} = 0$ or $+5.5V$			20	μA
LOGIC-SIDE I/O						
Input High Voltage	V_{IH}	SUSP, MODE, ENUM, $\overline{OE}$, VMO, VPO	$2/3 \times V_L$			V
Input Low Voltage	V_{IL}	SUSP, MODE, ENUM, $\overline{OE}$, VMO, VPO			0.4	V
Output-Voltage High	V_{OH}	VPI, VMI, RCV, USB_DET; $I_{SOURCE} = 2mA$	$V_L - 0.4$			V
Output-Voltage Low	V_{OL}	VPI, VMI, RCV, USB_DET; $I_{SINK} = -2mA$			0.4	V

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MAX3344E/MAX3345E

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4V to 5.5V bypassed with 1μF to GND, GND = 0, V_L = 1.65V to 3.6V, ENUM = V_L, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 5V, V_L = 2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current		SUSP, MODE, ENUM, $\overline{OE}$, VMO, VPO = 0 or V _L			±1	μA
USB-SIDE I/O						
Output-Voltage Low	V _{OL}	R _L = 1.5kΩ from D+ or D- to 3.6V			0.3	V
Output-Voltage High	V _{OH}	R _L = 15kΩ from D+ and D- to GND	2.8		3.6	V
Input Impedance	Z _{IN}	Three-state driver, ENUM = 0, V _{D-} = 0 or +3.6V	1			MΩ
Single-Ended Input-Voltage High	V _{IH}		2.0			V
Single-Ended Input-Voltage Low	V _{IL}				0.8	V
Receiver Single-Ended Hysteresis	V _{HYS}			200		mV
Differential Input Sensitivity	V _{DIFF}		200			mV
Input Common-Mode Voltage Range	V _{CM}		0.8		2.5	V
Driver Output Impedance	R _{OUT}		4.6		16.0	Ω
Internal Pullup Resistor	R _{PU}		1.410	1.500	1.540	kΩ
USB_DET Threshold	V _{USBLH1}	MAX3344E			4.0	V
	V _{USBHL1}	MAX3344E	3.6			
	V _{USBLH2}	MAX3345E			2.8	
	V _{USBHL2}	MAX3345E	1			
USB_DET Hysteresis	V _{USBHYS}	MAX3344E		25		mV
LINEAR REGULATOR						
External Capacitor	C _{OUT}	Compensation of linear regulator	1			μF
ESD PROTECTION (V_{CC}, D+, D-)						
Human Body Model				±15		kV
IEC1000-4-2 Air-Gap Discharge				±10		kV
IEC1000-4-2 Contact Discharge				±8		kV

TIMING CHARACTERISTICS

(V_{CC} = 4V to 5.5V, GND = 0, V_L = 1.65V to 3.6V, ENUM = V_L, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 5V, V_L = 2.5V, T_A = +25°C.) (Figures 2–6) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMITTER						
$\overline{OE}$ to Transmit Delay Enable Time	t _{pZD}	Figures 2 and 6c			20	ns
$\overline{OE}$ to Driver Three-State Delay Driver Disable Time	t _{pDZ}	Figures 2 and 6c			20	ns
VPO/VMO to D+/D- Propagation Delay	t _{PLH1} (drv)	MODE = high, Figures 4 and 6b		10	18	ns
	t _{PHL1} (drv)	MODE = high, Figures 4 and 6b		10	18	
VPO/VMO D+/D- Propagation Delay	t _{PLH0} (drv)	MODE = low, Figures 3 and 6c		11	20	ns
	t _{PHL0} (drv)	MODE = low, Figures 3 and 6c		11	20	

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TIMING CHARACTERISTICS (continued)

($V_{CC} = 4V$ to $5.5V$, $GND = 0$, $V_L = 1.65V$ to $3.6V$, $ENUM = V_L$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_{CC} = 5V$, $V_L = 2.5V$, $T_A = +25^\circ C$.) (Figures 2–6) (Note 2)

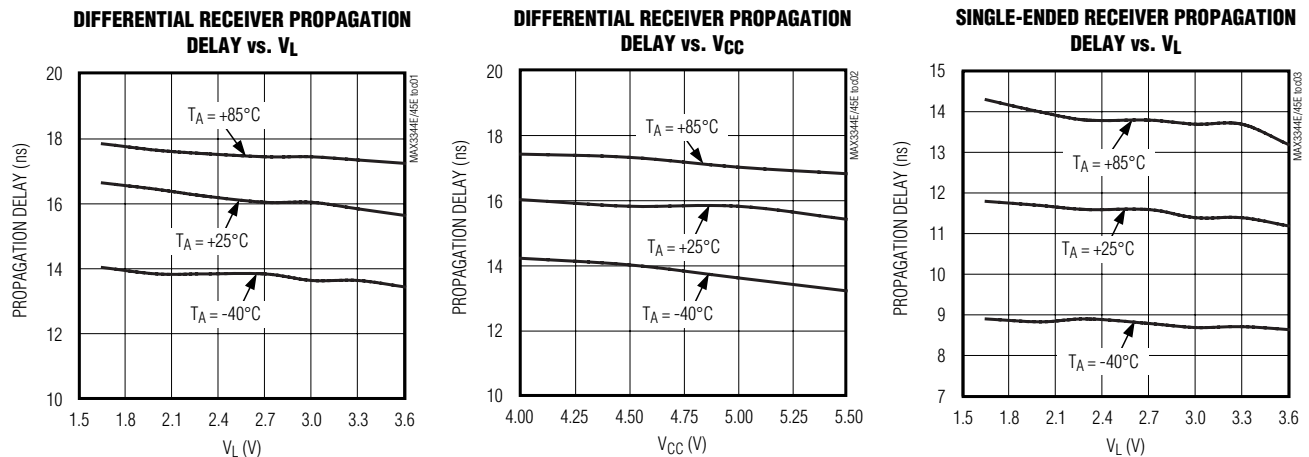
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time D+/D-	t_{R1}	$C_L = 50pF$, 10% to 90% of $ V_{OH} - V_{OL} $	4		20	ns
Fall Time D+/D-	t_{F1}	$C_L = 50pF$, 90% to 10% of $ V_{OH} - V_{OL} $	4		20	ns
Rise- and Fall-Time Matching	t_{R1}/t_{F1}	(Note 3)	90		111	%
Output Signal Crossover	V_{CRS}	(Note 3)	1.3		2.0	V
DIFFERENTIAL RECEIVER (Figures 5 and 6a)						
D+/D- to RCV Propagation Delay	$t_{PLH}(RCV)$				18	ns
	$t_{PHL}(RCV)$				18	ns
SINGLE-ENDED RECEIVERS (Figures 5 and 6a)						
D+/D- to VPI or VMI Propagation Delay	$t_{PLH}(SE)$				18	ns
	$t_{PHL}(SE)$				18	ns

Note 2: Parameters are 100% production tested at $25^\circ C$, limits over temperature are guaranteed by design.

Note 3: Guaranteed by design, not production tested.

Typical Operating Characteristics

($V_{CC} = 5V$, $V_L = 3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)



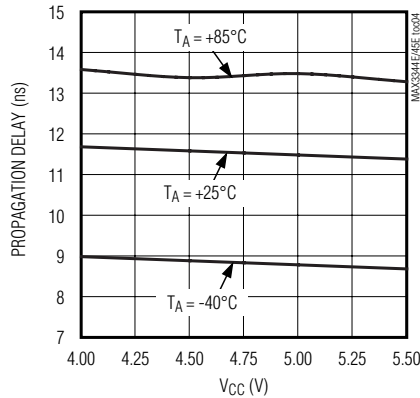
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Typical Operating Characteristics (continued)

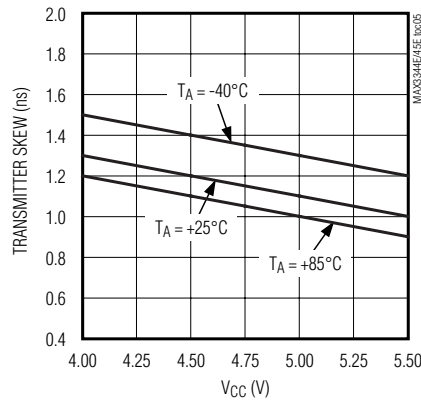
($V_{CC} = 5V$, $V_L = 3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)

MAX3344E/MAX3345E

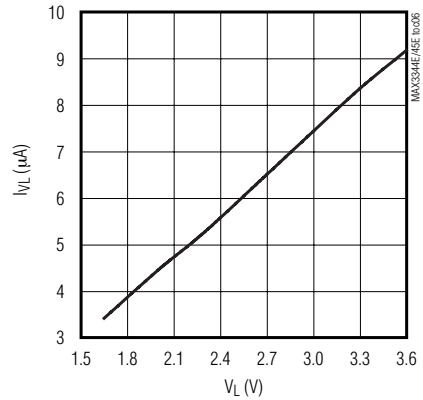
**SINGLE-ENDED RECEIVER PROPAGATION
DELAY vs. V_{CC}**



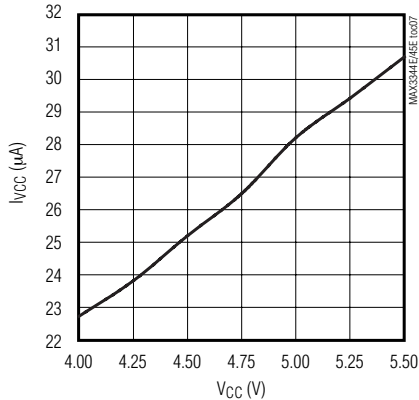
TRANSMITTER SKEW vs. V_{CC}



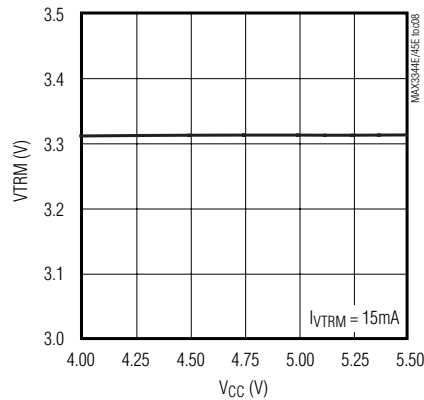
**LOGIC CURRENT CONSUMPTION IN
SUSPEND MODE**



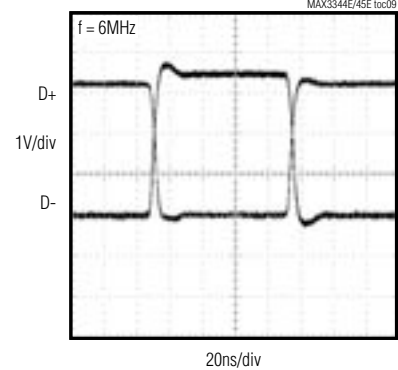
**V_{CC} CURRENT CONSUMPTION IN
SUSPEND MODE**



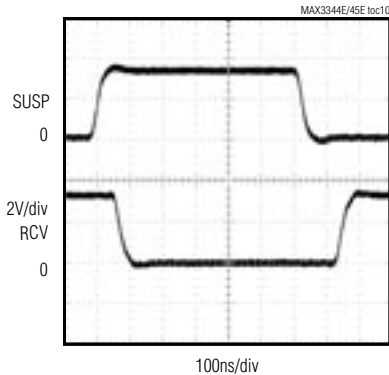
VTRM vs. V_{CC}



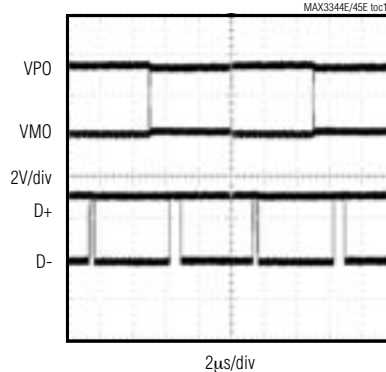
RISE- AND FALL-TIME MATCHING



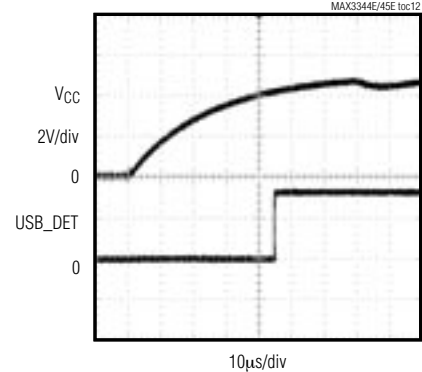
SUSPEND RESPONSE



**TRANSMISSION IN SUSPEND MODE
(SUSP = 1)**



USB_DET RESPONSE



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Pin Description

PIN		NAME	INPUT/ OUTPUT	FUNCTION
TSSOP	UCSP			
1	D2	RCV	Output	Receiver Output. Single-ended CMOS output. RCV responds to the differential input on D+ and D-.
2	D1	VPO	Input	Logic-Level Data Input. VPO is level translated to D+.
3	C2	MODE	Input	Mode-Control Input. Selects differential (mode 1) or single-ended (mode 0) input for the system side when converting logic-level signals to USB level signals. Force MODE high to select mode 1. Force MODE low to select mode 0.
4	C1	VMO	Input	Logic-Level Data Input. VMO is level translated to D-.
5	B1	$\overline{\text{OE}}$	Input	Output Enable. Drive $\overline{\text{OE}}$ low to enable data transmission on D+ and D-. Drive $\overline{\text{OE}}$ high to disable data transmission or to receive data.
6	B2	SUSP	Input	Suspend Input. Drive SUSP low for normal operation. Drive SUSP high for low-power state. In low-power state, RCV is low and VPI/VMI are active.
7	A1	VPI	Output	Logic-Level Data Output. VPI is the level-translated value of D+.
8	A2	VMI	Output	Logic-Level Data Output. VMI is the level-translated value of D-.
9	B3	ENUM	Input	Enumerate. Drive ENUM high to connect the internal 1.5k Ω resistor from D+ to 3.3V. Drive ENUM low to disconnect the internal 1.5k Ω resistor.
10	A3	VCC	Power	USB-Side Power-Supply Input. Connect VCC to the incoming USB power supply. Bypass VCC to GND with a 1 μ F ceramic capacitor.
11	A4	GND	Power	Ground
12	B4	D-	Input/ Output	Negative USB Differential Data Input/Output. Connect to the USB's D- signal through a 23.7 Ω $\pm$ 1% resistor.
13	C4	D+	Input/ Output	Positive USB Differential Data Input/Output. Connect to the USB's D+ signal through a 23.7 Ω $\pm$ 1% resistor.
14	D4	VTRM	Power	Regulated Output Voltage. VTRM provides a 3.3V output derived from VCC. Bypass VTRM to GND with a 1 μ F (min) low-ESR capacitor, such as ceramic or plastic film types.
15	D3	VL	Power	System-Side Power-Supply Input. Connect to the system's logic-level power supply, 1.65V to 3.6V.
16	C3	USB_DET	Output	USB Detector Output. A high at USB_DET signals to the ASIC that VCC is present. A low at USB_DET indicates that VCC is not present. The MAX3344E USB_DET threshold is between 3.6V (min) and 4V (max), while the MAX3345E USB_DET threshold is between 1V (min) and 2.8V (max).

Detailed Description

The MAX3344E/MAX3345E are bidirectional transceivers that convert single-ended or differential logic-level signals to differential USB signals, and convert differential USB signals to single-ended or differential logic-level signals. The MAX3344E/MAX3345E are operational from VCC = 5.5V to VCC = 3V (electrical specifications are not guaranteed for VCC < 4V). Both devices include an internal 1.5k Ω pullup resistor that connects and disconnects D+ to VTRM (see the *Functional Diagram*).

The MAX3344E/MAX3345E are tolerant to power sequencing with either VCC > VL or VL > VCC. Additionally,

the USB I/O, D+ and D-, and VCC are ESD protected to $\pm$ 15kV. The MAX3344E/MAX3345E can receive USB power (VCC) directly from the USB connection and operate with logic supplies (VL) down to 1.65V, while still meeting the USB physical layer specifications. The MAX3344E/MAX3345E support full-speed (12Mbps) USB specification 2.0 operation.

The MAX3344E/MAX3345E have an enumerate feature that functions when power is applied. Driving ENUM low disconnects the internal 1.5k Ω pullup resistor from D+ enumerating the USB. This is useful if changes in communication protocol are required while power is applied, and while the USB cable is connected.

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Power-Supply Configurations

Normal Operating Mode

Connect V_L and V_{CC} to system power supplies (Table 1). Connect V_L to a +1.65V to +3.6V supply. Connect V_{CC} to a +4.0V to +5.5V supply. Alternatively, the MAX3344E/MAX3345E can derive power from a single Li+ battery. Connect the battery to V_{CC} . V_{TRM} remains above +3.0V for V_{CC} as low as +3.1V.

Additionally, the MAX3344E/MAX3345E can derive power from a 3.3V ±10% voltage regulator. Connect V_{CC} and V_{TRM} to an external +3.3V voltage regulator.

Disable Mode

Connect V_{CC} to a system power supply and leave V_L unconnected or connect to GND. D+ and D- enter a tri-state mode and V_{CC} consumes less than 20µA of supply current. D+ and D- withstand external signals up to +5.5V in disable mode (Table 2).

Sharing Mode

Connect V_L to a system power supply and leave V_{CC} (or V_{CC} and V_{TRM}) unconnected or connect to GND. D+ and D- enter a tri-state mode, allowing other circuitry to share the USB D+ and D- lines, and V_L consumes less than 20µA of supply current. D+ and D- withstand external signals up to +5.5V in sharing mode (Table 2).

Device Control

D+ and D-

D+ and D- are the USB-side transmitter I/O connections, and are ESD protected to ±15kV using the Human Body Model, ±10kV using IEC 1000-4-2 Air-Gap Discharge, and ±8kV using IEC 1000-4-2 Contact Discharge, making the MAX3344E/MAX3345E ideal for applications where a robust transmitter is required. A 23.7Ω resistor is required on D+ and D- for normal operation (see the *External Resistors* section).

ENUM

USB specification 2.0 requires a 1.5kΩ pullup resistor on D+ for full-speed (12Mbps) operation. Controlled by enumerate (ENUM), the MAX3344E/MAX3345E provide this internal 1.5kΩ resistor. Drive ENUM high to connect the pullup resistor from D+ to V_{TRM} . Drive ENUM low to disconnect the pullup resistor from D+ to V_{TRM} .

VPO/VMO, VPI/VMI, and $\overline{OE}$

The MAX3344E/MAX3345E system-side inputs are VPO and VMO. Data comes into the MAX3344E/MAX3345E through VPO and VMO. VPO and VMO operate either differentially with VPO as the positive terminal and VMO as the negative terminal, or single ended with VPO as the data input (see the *MODE* section).

Table 1. Power-Supply Configurations

V_{CC} (V)	V_{TRM} (V)	V_L (V)	CONFIGURATION	NOTES
+4.0 to +5.5	+3.3 Output	+1.65 to +3.6	Normal mode	—
+3.1 to +4.5	+3.3 Output	+1.65 to +3.6	Battery supply	—
+3.0 to +3.6	+3.0 to +3.6 Input	+1.65 to +3.6	Voltage regulator supply	—
GND or floating	Output	+1.65 to +3.6	Sharing mode	Table 2
+3.0 to +5.5	Output	GND or floating	Disable mode	Table 2

Table 2. Disable-Mode and Sharing-Mode Configurations

INPUTS/OUTPUTS	DISABLE MODE	SHARING MODE
V_{CC}/V_{TRM}	+5V input/+3.3V output +3.3V input/+3.3V input +3.7V input/+3.3V output	- Floating or connected to GND < +3.6V (MAX3344E) < +1.0V (MAX3345E)
V_L	Floating or connected to GND	+1.65V to +3.6V input
D+ and D-	High impedance	High impedance
VPI and VMI	Invalid*	High impedance for $\overline{OE}$ = Low High for $\overline{OE}$ = High
RCV	Invalid*	Undefined**
SPEED, SUSP, $\overline{OE}$, ENUM	High impedance	High impedance

*High Impedance or low.

**High or low.

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The MAX3344E/MAX3345E system-side outputs are VPI, VMI, and RCV. The MAX3344E/MAX3345E send data through VPI, VMI, and RCV. VPI and VMI are outputs to the single-ended receivers and RCV is the output of the differential receiver.

Output enable ($\overline{OE}$) controls data transmission. Drive $\overline{OE}$ low to enable data transmission on D+ and D-. Drive $\overline{OE}$ high to disable data transmission or receive data.

MODE

MODE is a control input that selects whether differential or single-ended logic signals are recognized by the system side of the MAX3344E/MAX3345E. Drive MODE high to select differential mode with VPO as the positive terminal and VMO as the negative terminal. Drive MODE low to select single-ended mode with VPO as the data input (Table 3).

VTRM

VTRM is the 3.3V output of the internal linear voltage regulator. VTRM powers the internal circuitry of the USB side of the MAX3344E/MAX3345E. Connect a 1 μ F (min) low-ESR ceramic or plastic capacitor from VTRM to GND, as close to VTRM as possible. Do not use VTRM to power external circuitry.

VCC

Bypass VCC to GND with a 1 μ F ceramic capacitor as close to the device as possible. If VCC drops below the USB detect threshold, supply current drops below 20 μ A avoiding excessive VCC current consumption, and D+/D- enter a high-impedance state allowing other devices to drive the lines.

USB Detect

USB detect output (USB_DET) signals that VCC is present. A high at USB_DET indicates that VCC is present, while a low at USB_DET indicates that VCC is not present. The MAX3344E USB_DET threshold is between 3.6V (min) and 4V (max), while the MAX3345E USB_DET threshold is between 1V (min) and 2.8V (max).

SUSP

Suspend (SUSP) is a control input. Force SUSP high to place the MAX3344E/MAX3345E in a low-power state. In this state, the quiescent supply current into VCC is less than 40 μ A and RCV goes low.

In suspend mode, VPI and VMI remain active as receive outputs and VTRM stays on. The MAX3344E/MAX3345E continue to receive data from the USB, allowing the μ P to sense activity on the D+/D- lines and wake up the MAX3344E/MAX3345E.

The MAX3344E/MAX3345E can also transmit data to D+ and D- while in suspend mode. This function is

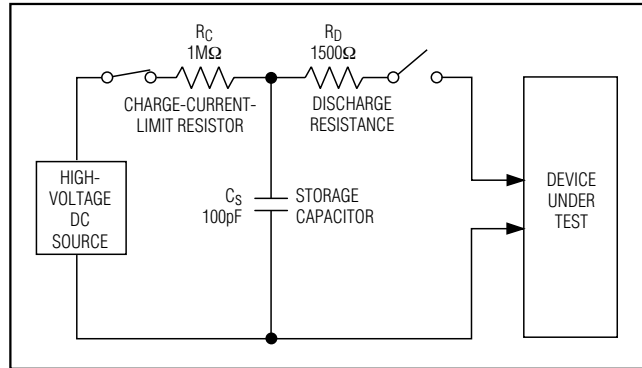


Figure 1a. Human Body ESD Test Models

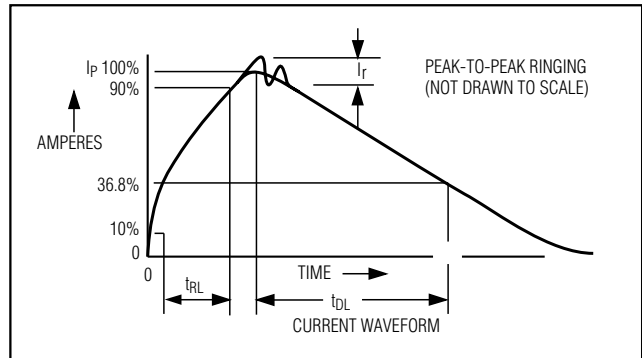


Figure 1b. Human Body Model Current Waveform

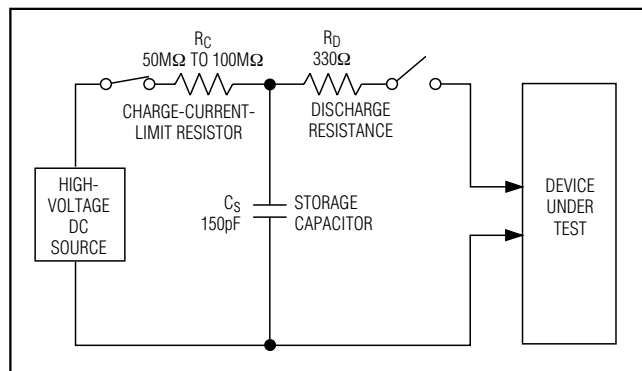


Figure 1c. IEC 1000-4-2 ESD Test Model

used to signal a remote wake-up by driving a signal on D+ and D- for a period of 1ms to 15ms. In suspend mode, data can only be transmitted with full-speed slope control.

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Data Transfer

Receiving Data from the USB

Data received from the USB are output to VPI/VMI in either of two ways, differentially or single ended. To receive data from the USB, force $\overline{OE}$ high and SUSP low. Differential data arriving at D+/D- appear as differential logic signals at VPI/VMI, and as a single-ended logic signal at RCV. If both D+ and D- are low, then VPI and VMI are low, signaling a single-ended zero condition on the bus; RCV remains in the last known state (Table 3).

Transmitting Data to the USB

The MAX3344E/MAX3345E output data to the USB differentially on D+ and D-. The logic driving signals can be either differential or single ended. For sending differential logic, force MODE high, force $\overline{OE}$ and SUSP low, and apply data to VPO and VMO. D+ then follows VPO, and D- follows VMO. To send single-ended logic signals, force MODE, SUSP, and $\overline{OE}$ low, and apply data to VPO/VMO.

ESD Protection

To protect the MAX3344E/MAX3345E against ESD, D+ and D- have extra protection against static electricity to protect the device up to ±15kV. The ESD structures withstand high ESD in all states—normal operation, suspend, and powered down. For the 15kV ESD structures to work correctly, a 1μF or greater capacitor must be connected from VTRM to GND.

ESD protection can be tested in various ways; the D+ and D- input/output pins are characterized for protection to the following limits:

- 1) ±15kV using the Human Body Model
- 2) ±8kV using the IEC 1000-4-2 Contact Discharge Method
- 3) ±10kV using the IEC 1000-4-2 Air-Gap Method

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 1a shows the Human Body Model, and Figure 1b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

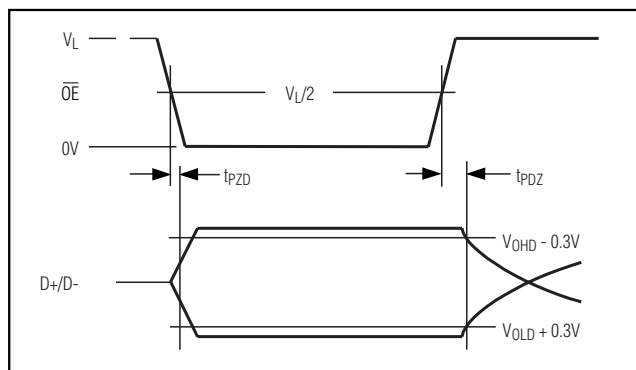


Figure 2. Enable and Disable Timing, Transmitter

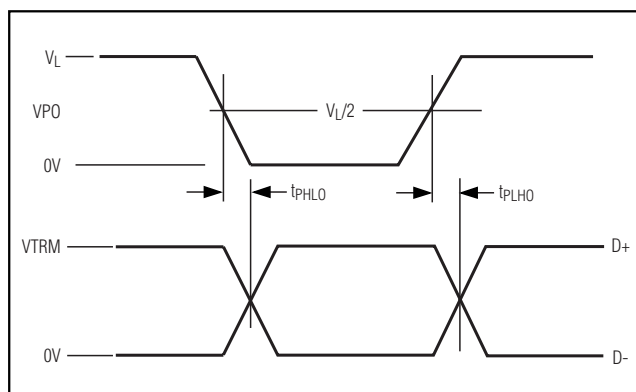


Figure 3. Mode 0 Timing

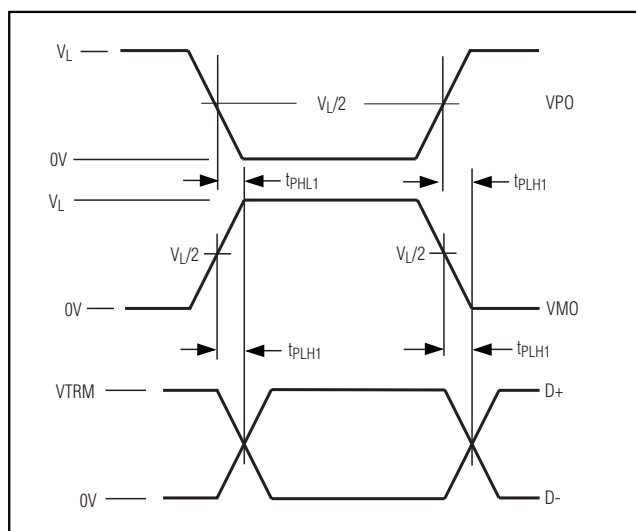


Figure 4. Mode 1 Timing

±15kV ESD-Protected USB Transceivers in UCSP with USB Detect

Table 3a. Truth Table Transmit (SUSP = 0, $\overline{OE}$ = 0, ENUM = X)

INPUT			OUTPUT					
MODE	VPO	VMO	D+	D-	RCV	VPI	VMI	RESULT
0	0	0	0	1	0	0	1	LOGIC 0
0	0	1	0	0	RCV*	0	0	SE0
0	1	0	1	0	1	1	0	LOGIC 1
0	1	1	0	0	RCV*	0	0	SE0
1	0	0	0	0	RCV*	0	0	SE0
1	0	1	0	1	0	0	1	LOGIC 0
1	1	0	1	0	1	1	0	LOGIC 1
1	1	1	1	1	X	1	1	UNDEFINED

*RCV denotes the signal level on output RCV just before SE0 state occurs. This level is stable during the SE0 period.

Table 3b. Truth Table Receive (SUSP = 0, $\overline{OE}$ = 1, ENUM = X)

INPUT		OUTPUT			
D+	D-	RCV	VPI	VMI	RESULT
0	0	RCV*	0	0	SE0
0	1	0	0	1	LOGIC 0
1	0	1	1	0	LOGIC 1
1	1	X	1	1	UNDEFINED

*RCV denotes the signal level on output RCV just before SE0 state occurs. This level is stable during the SE0 period.

Table 3c. Truth Table Transmit in Suspend* (SUSP = 1, $\overline{OE}$ = 0, ENUM = X)

INPUT			OUTPUT					
MODE	VPO	VMO	D+	D-	RCV	VPI	VMI	RESULT
0	0	0	0	1	0	0	1	LOGIC 0
0	0	1	0	0	0	0	0	SE0
0	1	0	1	0	0	1	0	LOGIC 1
0	1	1	0	0	0	0	0	SE0
1	0	0	0	0	0	0	0	SE0
1	0	1	0	1	0	0	1	LOGIC 0
1	1	0	1	0	0	1	0	LOGIC 1
1	1	1	1	1	0	1	1	UNDEFINED

*Timing specifications are not guaranteed for D+ and D-.

Table 3d. Truth Table Receive in Suspend* (SUSP = 1, $\overline{OE}$ = 1, MODE = X, VPO/VMO = X, ENUM = X)

INPUT		OUTPUT			
D+	D-	RCV	VPI	VMI	RESULT
0	0	0	0	0	VPI/VMI ACTIVE
0	1	0	0	1	VPI/VMI ACTIVE
1	0	0	1	0	VPI/VMI ACTIVE
1	1	0	1	1	VPI/VMI ACTIVE

*Timing specifications are not guaranteed for D+ and D-.

$\pm 15\text{kV}$ ESD-Protected USB Transceivers in UCSP with USB Detect

IEC 1000-4-2

The IEC 1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX3344E/MAX3345E help the user design equipment that meets level 4 of IEC 1000-4-2, without the need for additional ESD-protection components.

The major difference between tests done using the Human Body Model and IEC 1000-4-2 is a higher peak current in IEC 1000-4-2, because series resistance is lower in the IEC 1000-4-2 model. Hence, the ESD withstand voltage measured to IEC 1000-4-2 is generally lower than that measured using the Human Body Model. Figure 1c shows the IEC 1000-4-2 model.

The Air-Gap Discharge Method involves approaching the device with a charged probe. The Contact Discharge Method connects the probe to the device before the probe is energized.

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing. All pins require this protection during manufacturing. Therefore, after PC board assembly, the Machine Model is less relevant to I/O ports.

Applications Information

External Components

External Resistors

Two external $23.7\Omega \pm 1\%$ to $27.4\Omega \pm 1\%$, 1/2W resistors are required for USB connection. Place the resistors in between the MAX3344E/MAX3345E and the USB connector on the D+ and D- lines (see the *Typical Operating Circuit*).

External Capacitors

Use three external capacitors for proper operation. Use a 0.1 μF ceramic for decoupling V_L , a 1 μF ceramic for decoupling V_{CC} , and a 1.0 μF (min) ceramic or plastic filter capacitor on VTRM. Return all capacitors to GND.

UCSP Applications Information

For the latest application details on UCSP construction, dimensions, tape carrier information, printed circuit board techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to the Application Note *UCSP—A Wafer-Level Chip-Scale Package* available on Maxim's website at www.maxim-ic.com/ucsp.

Chip Information

TRANSISTOR COUNT: 2162

PROCESS: BiCMOS

MAX3344E/MAX3345E

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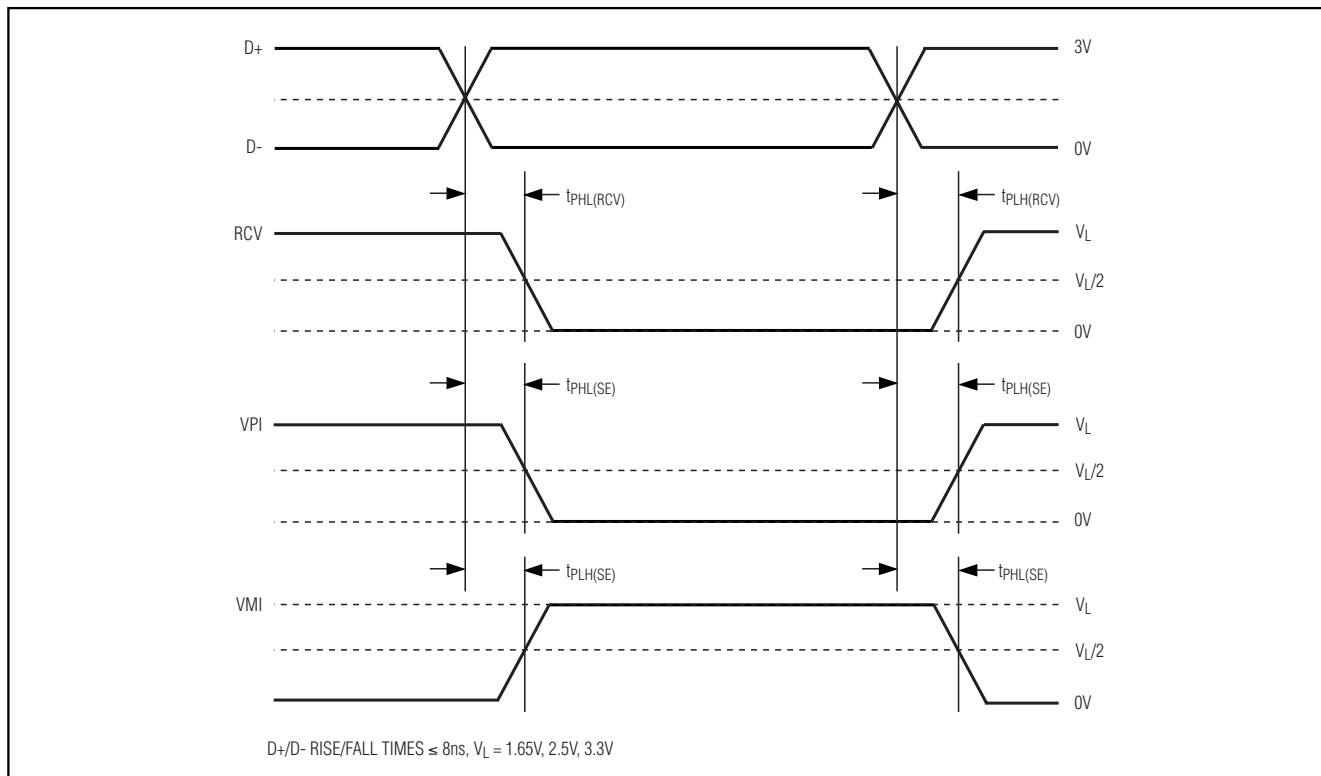


Figure 5. D+/D- to RCV, VPI, VMI Propagation Delays

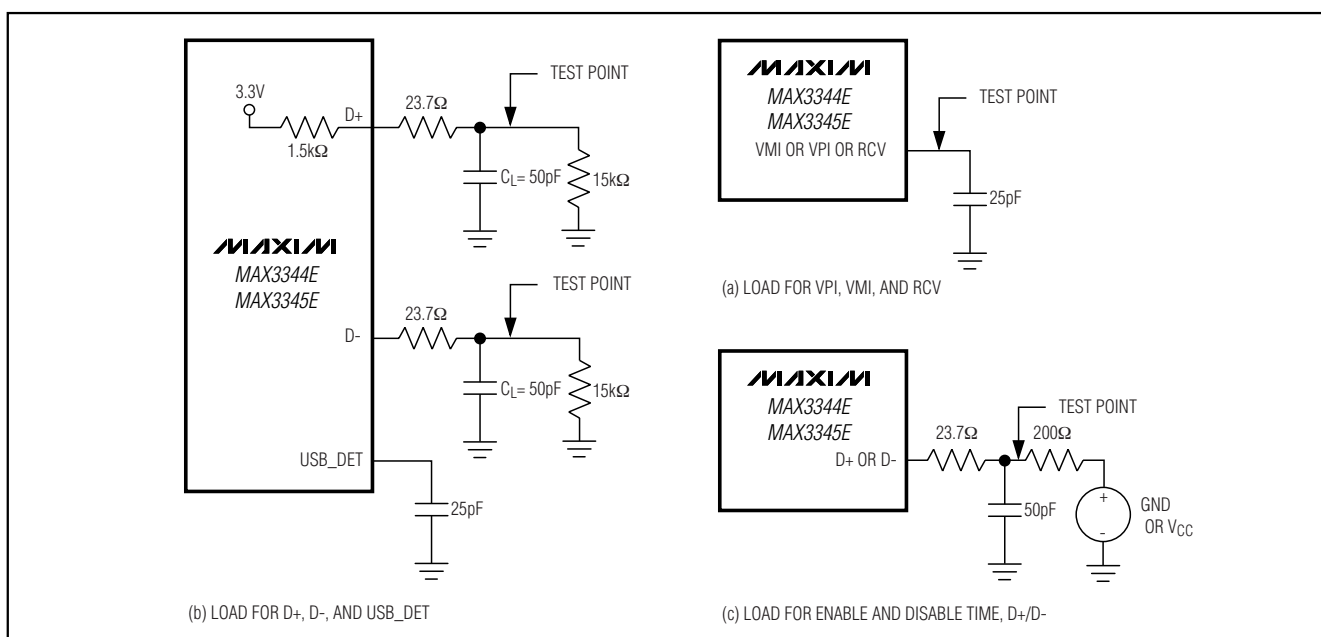


Figure 6. Test Circuits

MAX3344E/MAX3345E

The schematic diagram illustrates the internal and external components of the MAX3344E/MAX3345E USB interface circuit. The circuit is divided into three main sections by dashed lines: INTERNAL CIRCUITS, EXTERNAL RESISTORS, and a section for the USB DET signal.

INTERNAL CIRCUITS: This section contains the MAX3344E/MAX3345E chip. It includes a LINEAR REGULATOR, a BANDGAP, a RECEIVER, a TRANSMITTER, and SINGLE-ENDED RECEIVERS. The chip is connected to various pins: V_L, VTRM, RCV, GND, SUSP, VMO, MODE, VPO, OE, VMI, and VPI. The chip is also connected to a USB SUPPLY (VCC) and a USB DET signal.

EXTERNAL RESISTORS: This section contains external resistors connected to the D- and D+ lines. The D- and D+ lines are connected to a 23.7kΩ resistor. The USB DET signal is connected to a 1.5kΩ resistor.

USB DET: This section contains the USB DET signal, which is connected to a 1.5kΩ resistor and a USB DET pin.

The diagram is labeled with "MAXIM MAX3344E MAX3345E".

The image shows two pin configuration diagrams for the MAX3344E/MAX3345E. The left diagram is the TOP VIEW for the TSSOP package, showing pins 1 through 8 on the left and pins 16 through 9 on the right. The right diagram is the BOTTOM VIEW for the UCSP package, showing pins 1 through 4 at the top and pins 16 through 9 at the bottom. The MAX3344E/MAX3345E logo is present in both views.

TOP VIEW (TSSOP)

Pin	Signal
1	RCV
2	VPO
3	MODE
4	VMO
5	OE
6	SUSP
7	VPI
8	VMI
9	ENUM
10	VCC
11	GND
12	D-
13	D+
14	VTRM
15	VL
16	USB_DET

UCSP

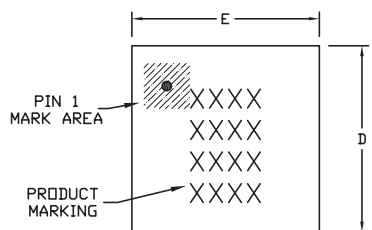
BOTTOM VIEW (UCSP)

Pin	Signal
1	VPO
2	RCV
3	VL
4	VTRM
5	VMO
6	MODE
7	USB_DET
8	D+
9	D-
10	OE
11	SUSP
12	ENUM
13	VPI
14	VMI
15	VCC
16	GND

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Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



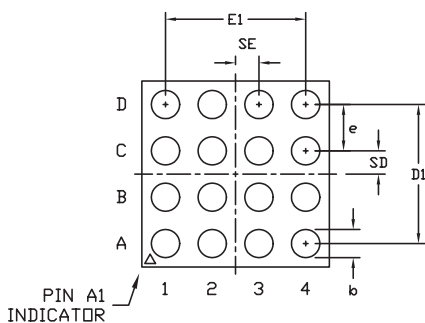
TOP VIEW

COMMON DIMENSIONS	
A	0.62±0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	∅0.35±0.03
D1	1.50 BASIC
E1	1.50 BASIC
e	0.50 BASIC
SD	0.25 BASIC
SE	0.25 BASIC

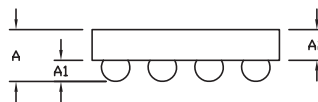
PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B16-1	2.02±0.05	2.02±0.05	NONE
B16-2	2.02±0.05	2.02±0.05	B3, C3
B16-3	2.02±0.05	2.02±0.05	B3, C2
B16-4	2.02±0.05	2.02±0.05	B2, C3
B16-5	2.02±0.05	2.02±0.05	B2, B3, C2, C3
B16-6	2.02±0.05	2.02±0.05	C3

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



BOTTOM VIEW



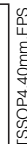
SIDE VIEW

 DALLAS SEMICONDUCTOR			
PROPRIETARY INFORMATION			
TITLE: PACKAGE OUTLINE, 4x4 UCSP			
APPROVAL	DOCUMENT CONTROL NO. 21-0101	REV. H	1/1

16LUCSP.EPS

MAX3344E/MAX3345E

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



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