Absolute Maximum Ratings

PV to PGND .....-0.3V to +6V
AV to GND .....-0.3V to +6V
$\overline{\text{RESET}}$, OUT to GND.....-0.3V to +6V
SYNC, EN, SSEN to GND .....-0.3V to PV +0.3V
GND to PGND .....-0.3V to +0.3V
LX Continuous RMS Current 4A
LX to PGND (Note 1) .....-0.3V to PV + 0.3V

Output Short-Circuit Duration .....Continuous
Continuous Power Dissipation (T_A = +70°C)
10-pin TDFN-EP (derate 24.4mW/°C > 70°C)..... 1951mW
Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -40°C to +150°C
Lead Temperature Range.....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

Junction-to-Ambient Thermal Resistance (θ_{JA}).....41°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....9°C/W

Note 1: Self-protected from transient voltages exceeding these limits in circuit under normal operation.
Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{AV} = V_{PV} = 5.0V, V_{EN} = 5.0V, V_{SSEN} = 0V, . T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage Range	V_{IN}		2.7		5.5	V
Supply Current	I_{SHDN}	V_{EN} = 0V		3	10	µA
Supply Current	I_{IN}	V_{EN} = 5V, V_{SYNC} = 0V, no load		40	93	µA
Undervoltage Lockout	V_{UVLOR}	Rising	2.3	2.5	2.65	V
	V_{UVLOF}	Falling	2.2	2.4	2.55	V
Oscillator Frequency	f_{SW}		2.0	2.2	2.4	MHz
SYNC Input Frequency Range	f_{SYNC}		1.8		2.6	MHz
Spread-Spectrum Range	SS	V_{SSEN} = V_{AV}		±3		%
Skip Mode Peak Current	I_{SKIP}		0.04 x I_{LIM}	0.12 x I_{LIM}	0.20 x I_{LIM}	mA
Voltage Accuracy	V_{OUT}	PWM mode, 0A ≤ I_{LOAD} ≤ I_{MAX} 2.7V ≤ V_{AV} = V_{PV} ≤ 5.5V	-1.5		+1.5	%
OUT Bias Current	I_{OUT_ADJ}	Adjustable mode	-500	15	+500	nA
OUT Bias Current	I_{OUT_FIX}	Fixed mode	4	5	6	µA
DC Load Regulation	L_{D_REG}	0A ≤ I_{LOAD} ≤ I_{MAX} (PWM Mode)		0.02		%/A
DC Line Regulation	L_{N_REG}	2.7V ≤ V_{AV} = V_{PV} ≤ 5.5V		0.05		%/V
pMOS On-Resistance	R_{HS}	V_{PV} = V_{AV} = 5V, I_{LX} = 0.1A	30	60	120	mΩ
nMOS On-Resistance	R_{LS}	V_{PV} = V_{AV} = 5V, I_{LX} = 0.1A	20	38	80	mΩ

Electrical Characteristics (continued)

(V_{AV} = V_{PV} = 5.0V, V_{EN} = 5.0V, V_{SSEN} = 0V, . T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 3)

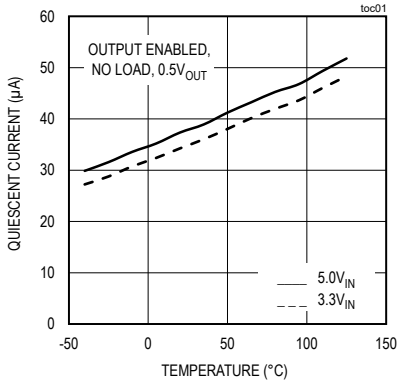
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Current-Limit Threshold	I_{LIM}	MAX20073 (2.0A DC)	3.0	3.8		A
		MAX20074 (3.0A DC)	4.5	5.8		A
nMOS Zero-Crossing Threshold	I_{ZX}			130		mA
Soft-Start Ramp Time	t_{SS}			0.8		ms
Maximum Duty Cycle	DC_{MAX}				100	%
Minimum On-Time	t_{MINTON}		25	40	70	ns
OUT_ Discharge Resistance	R_{DISCH}	V_{EN} = 0V	20	40	80	Ω
RESET OUTPUT ($\overline{RESET}$)						
Overvoltage Threshold (Rising)	OUT_{OV_R}	Rising, % of nominal output	104	107	110	%
Undervoltage Threshold (Falling)	OUT_{UV_F}	Falling, % of nominal output	90	93	96	%
Overvoltage-Protection Threshold (Rising)	OUT_{OVP_R}	Rising, % of nominal output		120	129	%
Overvoltage-Protection Threshold (Falling)	OUT_{OVP_F}	Falling, % of nominal output		118		%
Active Timeout Period	t_{HOLD}			7.4		ms
Output Low Level	V_{ROL}	I_{SINK} = 3mA		0.1	0.2	V
$\overline{RESET}$ Leakage Current	I_{OZ}		-500		+500	nA
Undervoltage-Propagation Time	t_{UVDEL}	OUT less than 20% below target		5		µs
Overvoltage-Propagation Time	t_{OVDEL}	OUT greater than 20% above target		55		µs
Thermal-Shutdown Temperature	T_{SHDN}	T_J rising		+170		ºC
Thermal-Shutdown Hysteresis	T_{HYST}			15		ºC
ENABLE INPUTS (EN, SSEN)						
Input High	V_{IHEN}	2.7V ≤ V_{AV} = V_{PV} ≤ 5.5V	1.5			V
Input Low	V_{ILEN}	2.7V ≤ V_{AV} = V_{PV} ≤ 5.5V			0.5	V
Hysteresis	V_{HYSTEN}			0.175		V
EN Pulldown Current	I_{ENPD}		0.20	0.5	1.6	µA
SSEN Pulldown Current	I_{SSENPD}		0.1	0.25	0.8	µA
SYNCHRONIZATION (SYNC)						
Input High	V_{IH_SYNC}	2.7V ≤ V_{AV} = V_{PV} ≤ 5.5V	1.5			V
Input Low	V_{IL_SYNC}	2.7V ≤ V_{AV} = V_{PV} ≤ 5.5V			0.5	V
Pulldown Resistance	R_{SYNCPD}		50	100	150	kΩ
Output Low	V_{SOL}	SYNC output option, I_{SYNC} = -3mA			0.4	V
Output High	V_{SOH}	SYNC output option, I_{SYNC} = 3mA	4.2			V

Note 3: All units are 100% production tested at +25˚C. All temperature limits are guaranteed by design.

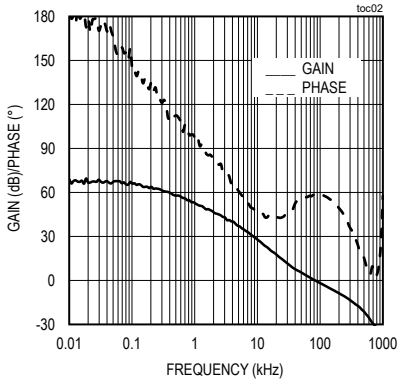
Typical Operating Characteristics

(V_{AV} = V_{PV} = 5.0V, T_A = +25°C, unless otherwise noted.)

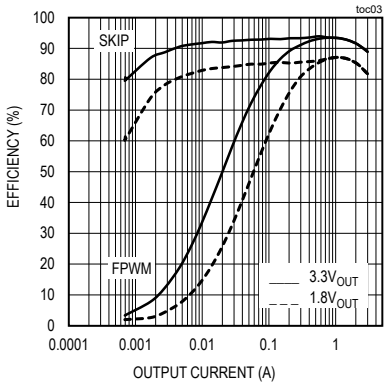
QUIESCENT CURRENT vs. TEMPERATURE
NORMAL OPERATION



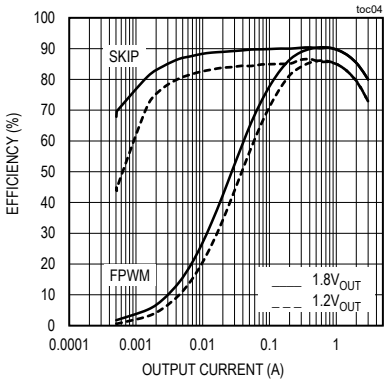
GAIN/PHASE vs. FREQUENCY
1.8V OUTPUT (ADJUSTABLE)



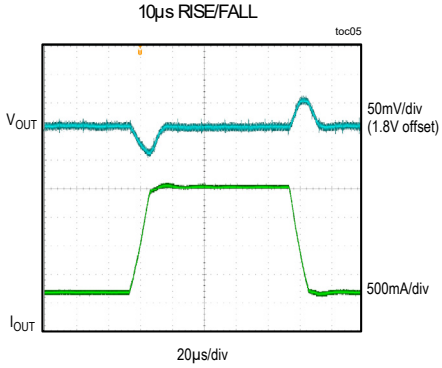
EFFICIENCY vs. OUTPUT CURRENT



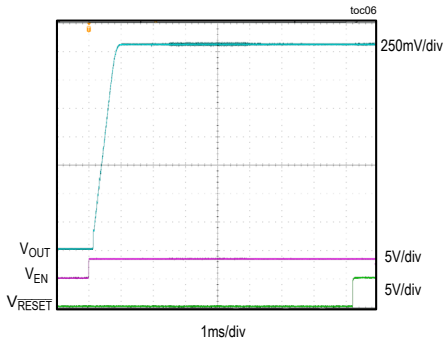
EFFICIENCY vs. OUTPUT CURRENT
3.3V INPUT (MAX20074)



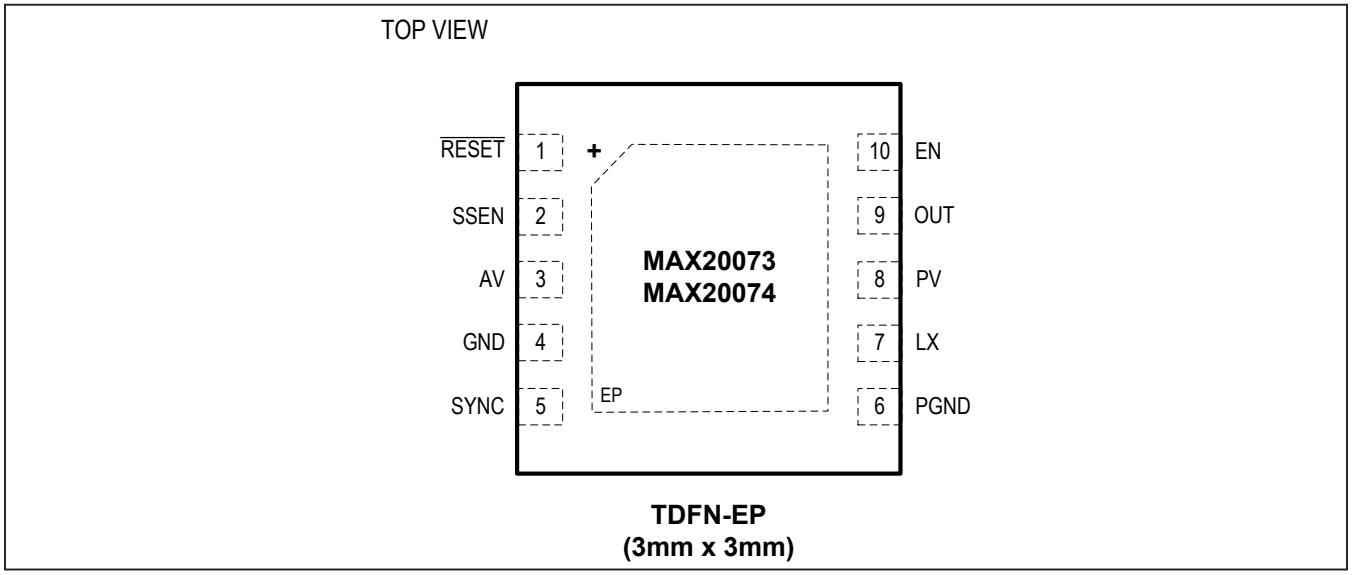
LOAD TRANSIENT RESPONSE
20% - 80% - 20%
10µs RISE/FALL



STARTUP BEHAVIOR
NO LOAD



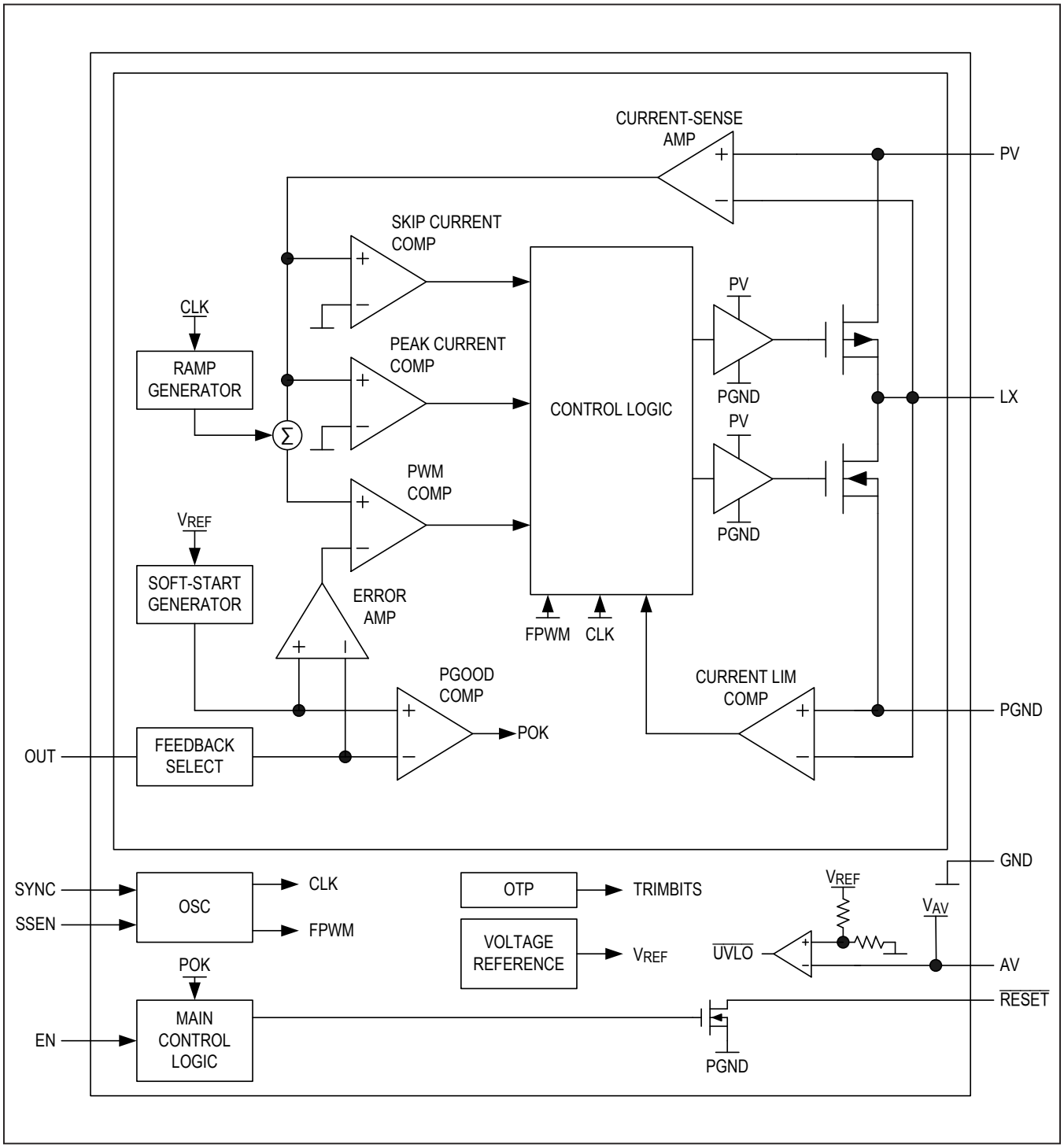
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	$\overline{\text{RESET}}$	Active-Low Open-Drain $\overline{\text{RESET}}$ Output. External pullup resistor required if used.
2	SSEN	Spread-Spectrum Enable. Drive SSEN high for spread-spectrum operation.
3	AV	Analog Voltage Supply. Connect a 0.1µF ceramic capacitor from AV to GND. Connect AV to PV with a 10Ω resistor.
4	GND	Analog Ground
5	SYNC	SYNC I/O. When configured as an input, connect SYNC to GND or leave unconnected to enable skip mode operation under light loads. Connect SYNC to AV or an external clock to enable fixed-frequency FPWM mode operation. When configured as an output, connect SYNC to other device's SYNC inputs.
6	PGND	Power Ground
7	LX	Inductor Connection. Connect LX to the switched side of the inductor.
8	PV	Power Input-Voltage Supply. Connect a 4.7µF or larger ceramic capacitor from PV to PGND.
9	OUT	Feedback Input. Connect an external resistive divider from the converter's output to OUT and GND to set the output voltage. Connect to the output capacitor when configured as a fixed-output device.
10	EN	Active-High Enable Input. Drive EN high for normal operation. On the rising edge, the device enters soft-start; on the falling edge, the device turns off.
—	EP	Exposed pad. Internally connected to GND. Connect to a large ground plane to maximize thermal performance. Not intended as an electrical connection point.

Internal Block Diagram



Detailed Description

The MAX20073/MAX20074 high-efficiency switching regulator family delivers up to a 3A load current from 0.5V to 3.8V. The devices operate from 2.7V to 5.5V, making them ideal for on-board point-of-load and post-regulation applications. Total output error is less than ±1.5% over load, line, and temperature.

The devices feature fixed-frequency PWM mode operation with a 2.2MHz switching frequency. High-frequency operation allows for an all-ceramic capacitor design. The high operating frequency also allows for small-size external components.

The low-resistance on-chip switches ensure high efficiency at heavy loads while minimizing critical inductances, making the layout a much simpler task with respect to discrete solutions. Following a simple layout and footprint ensures first-pass success in new designs.

The devices provide an enable input (EN) and a reset output ($\overline{RESET}$). The output voltage can be preset at the factory, allowing customers to achieve ±1.5% output-voltage accuracy without using expensive 0.1% resistors. In addition, the output voltage can be set to any customer value by either using two external resistors at the feedback with 0.5V internal reference. The devices offer a fixed 0.85ms soft-start time.

Enable Input (EN)

The enable (EN) control input activates the device from a low-power shutdown state. EN has an input threshold of 1.15V (typ) with hysteresis of 175mV (typ). When the enable input goes high, the associated output voltage ramps up with the soft-start time.

Reset Output ($\overline{RESET}$)

The devices feature an open-drain reset output pin ($\overline{RESET}$) that asserts low when the output voltage is outside of the undervoltage/overvoltage window. The $\overline{RESET}$ pin remains asserted low for a fixed timeout period after the output rises up to its regulated voltage. A fixed hold period of 7.4ms is applied after the output is in regulation. To obtain a logic signal, place a resistor pullup between the $\overline{RESET}$ pin to the system input/output (I/O) voltage. The pullup resistance should normally be ≥ 2kΩ to ensure that the device can pull down to the specified voltage level.

Spread-Spectrum Oscillator

The devices have a spread-spectrum oscillator option that varies the internal operating frequency up by ±3% relative to the internally generated 2.2MHz (typ) operating frequency. This function does not apply to externally applied oscillation frequency. The spread frequency generated is pseudorandom. Connect the SSEN pin to PV to enable the spread-spectrum oscillator or to ground to disable the spread-spectrum oscillator.

Synchronization (SYNC)

The devices have an on-chip oscillator that provides a 2.2MHz (typ) switching frequency. Depending on the condition of the SYNC pin, two operation modes exist. If SYNC is unconnected or at GND, and if the load current is below the skip mode current threshold, the device operates in a highly efficient pulse-skipping mode. If SYNC is at PV or has a frequency applied to it, the device is in forced-PWM (FPWM) mode. The device can be switched during operation between FPWM mode and skip mode by switching SYNC.

The SYNC pin can be used as an input or an output (see *Pin Description*). SYNC-pin mode is factory configurable. When configured as an output, the clock will be 180° out-of-phase from the internal clock. The devices always operate in PWM mode when SYNC is configured as an output.

Soft-Start

The devices include a fixed soft-start of 0.80ms. Soft-start time limits startup inrush current by forcing the output voltage to ramp up towards its regulation point.

Current Limit/Short-Circuit Protection

The devices feature current limit that protects against short-circuit and overload conditions at the output. In the event of a short-circuit or overload condition, the high-side MOSFET remains on until the inductor current reaches the high-side MOSFET's current-limit threshold. The converter then turns on the low-side MOSFET to allow the inductor current to ramp down. Once the inductor current crosses below the low-side MOSFET's current-limit threshold, the converter turns on the high-side MOSFET again. This cycle repeats until the short or overload condition is removed.

PWM and Skip Modes

The devices feature a SYNC input that puts the converter either in skip mode or FPWM mode of operation (see the *Pin Description* section for mode details). In FPWM mode, the converter switches at a constant frequency with variable on-time. In skip mode, the converter's switching frequency is load-dependent until the output load reaches a certain threshold. At higher load currents, the switching frequency does not change and the operating mode is similar to the PWM mode. Skip mode helps improve efficiency in light-load applications by allowing the converter to turn on the high-side switch only when the output voltage falls below a set threshold. As such, the converter does not switch MOSFETs on and off as often as in PWM mode. Consequently, the gate charge and switching losses are much lower in skip mode.

Overtemperature Protection

Thermal-overload protection limits the total power dissipation in the device. When the junction temperature exceeds 170°C (typ), an internal thermal sensor shuts down the internal bias regulator and the step-down controller, allowing the device to cool. The thermal sensor turns on the device again after the junction temperature cools by 15°C.

Applications Information

Input Capacitors

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. A 4.7µF ceramic capacitor is recommended for the PV pin. A 0.1µF ceramic capacitor is recommended for the AV pin, with a series 10Ω resistor to the supply.

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). Use Equation 1 to determine the minimum inductor value.

Equation 1:

$$L_{MIN} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times I_{MAX} \times 30\%}$$

where:

- R_{CS} = 0.263Ω for 2A channel and 0.176Ω for 3A channel
- I_{MAX} = 3A or 2A depending on part number. Use the maximum output capability of the output channel for the part number in use.
- f_{SW} = The operating frequency. This value is 2.2MHz unless externally synchronized to a different frequency.

Equation 2 ensures that the inductor current downslope is less than twice the internal slope compensation. This is a minimum requirement for stability and requires that Equation 2 is satisfied.

Equation 2:

$$-m \geq \frac{m_2}{2}$$

where:

- m_2 = Inductor current downslope:

$$\left[\frac{V_{OUT}}{L} \times R_{CS}\right]$$

- -m = Adjustable versions and fixed output voltages ≤ 3.2V, slope compensation:

$$[0.535V / \mu s]$$

- Fixed-output versions and output voltages > 3.2V, slope compensation:

$$[0.94V / \mu s]$$

Solving for L and adding a 1.3 multiplier to account for tolerances in the system is shown in Equation 3.

Equation 3:

$$L_{MIN2} = V_{OUT} \times \frac{R_{CS}}{2 \times m} \times 1.3$$

where:

- L_{MIN} = The larger of L_{MIN1} and L_{MIN2} must be used:

  $L_{MIN} = \max(L_{MIN1}, L_{MIN2})$
- The maximum inductor value recommended is 2 times the chosen value from the above formula.

  $L_{MAX} = 2 \times L_{MIN}$
- The nominal inductor value is selected using:

  $L_{MIN} < L_{NOM} < L_{MAX}$

Output Capacitor

The devices are designed to be stable with low-ESR ceramic capacitors. Other capacitor types are not recommended as the ESR zero can affect stability of the device. The output capacitor calculations in Equation 4 are guidelines based on nominal conditions. The phase margin must be measured on the final circuit to verify proper stability is achieved.

Equation 4:

$$C_{OUT\_MIN} = 10.5\mu s \times \frac{I_{MAX}}{V_{OUT}}$$

$$C_{OUT\_NOM} = 27.5\mu s \times \frac{I_{MAX}}{V_{OUT}}$$

$$C_{OUT\_MAX} = 3 \times C_{OUT\_NOM}$$

- C_{OUT_MIN} = The minimum fully derated output capacitance needed for a stable output.
- C_{OUT_NOM} = The nominal output capacitance. This capacitance value normally provides the highest stability.
- C_{OUT_MAX} = The maximum recommended output capacitance. Increased capacitance beyond this value is not recommended without measuring the phase margin to ensure acceptable stability. While the device does not become unstable with large output capacitance, the phase margin does degrade.
- I_{MAX} = The maximum DC current capability.

  I_{MAX} = 2A (MAX20073)

  I_{MAX} = 3A (MAX20074)
- V_{OUT} = Nominal output voltage.

Adjustable Output-Voltage Option

The devices' adjustable output-voltage version allows the customer to set the outputs to any voltage between 0.5V and approximately PV - 0.5V (see *Ordering Information*). The actual maximum output-voltage setting will be limited by the specific application conditions and components. Connect a resistive divider from the output capacitor (V_{OUT}) to OUT to GND to set the output voltage (Figure 1). Select R_2 (OUT to GND resistor) ≤ 100kΩ. Calculate R_1 (V_{OUT} to OUT resistor) with the Equation 5.

Equation 5:

$$R_1 = R_2 \left[\left(\frac{V_{OUT}}{V_{FB}} \right) - 1 \right]$$

where V_{FB} = 500mV (see the *Electrical Characteristics* table).

The external feedback resistive divider must be frequency compensated for proper operation. Place a capacitor across R_1 in the resistive divider network. Use Equation 6 to determine the value of the capacitor.

Equation 6:

$$C_1 = 50 \frac{R_2}{R_1} pF$$

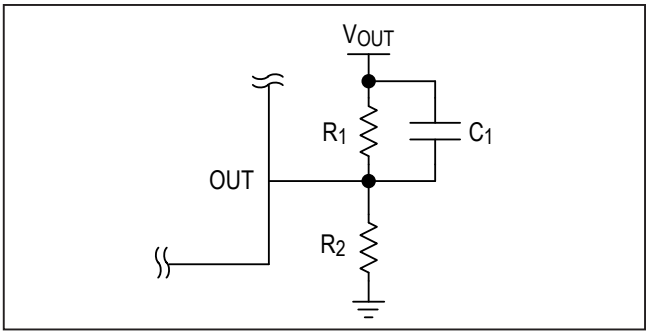


Figure 1. Adjustable Output-Voltage Configuration

PCB Layout Guidelines

The following guidelines should be followed to obtain the vbest performance from the device:

- Place several vias in the exposed pad (EP) and connect them all to ground layers below the part. EP is attached to the die with epoxy, making it a good method for transferring heat out of the IC. An array of 0.3mm-diameter vias is recommended.
- Place all DC-DC components on the same layer as the IC, and locatet hem as close to the IC as possible.Route the traces in a tight loop. Trace length should be prioritized over trace thickness, and a shorter trace is preferable. This decreases the loop area of the circuit, minimizing EMI and jitter.
- The layer directly below the IC and DC-DC components should be a solid ground plane. Connect the GND and PGND pins of the device and components together with a low-impedance connection and add several vias to ground near those pins. Do not split the ground plane at or near the circuit. See Figure 2 for an example layout of the IC and DC-DC components.

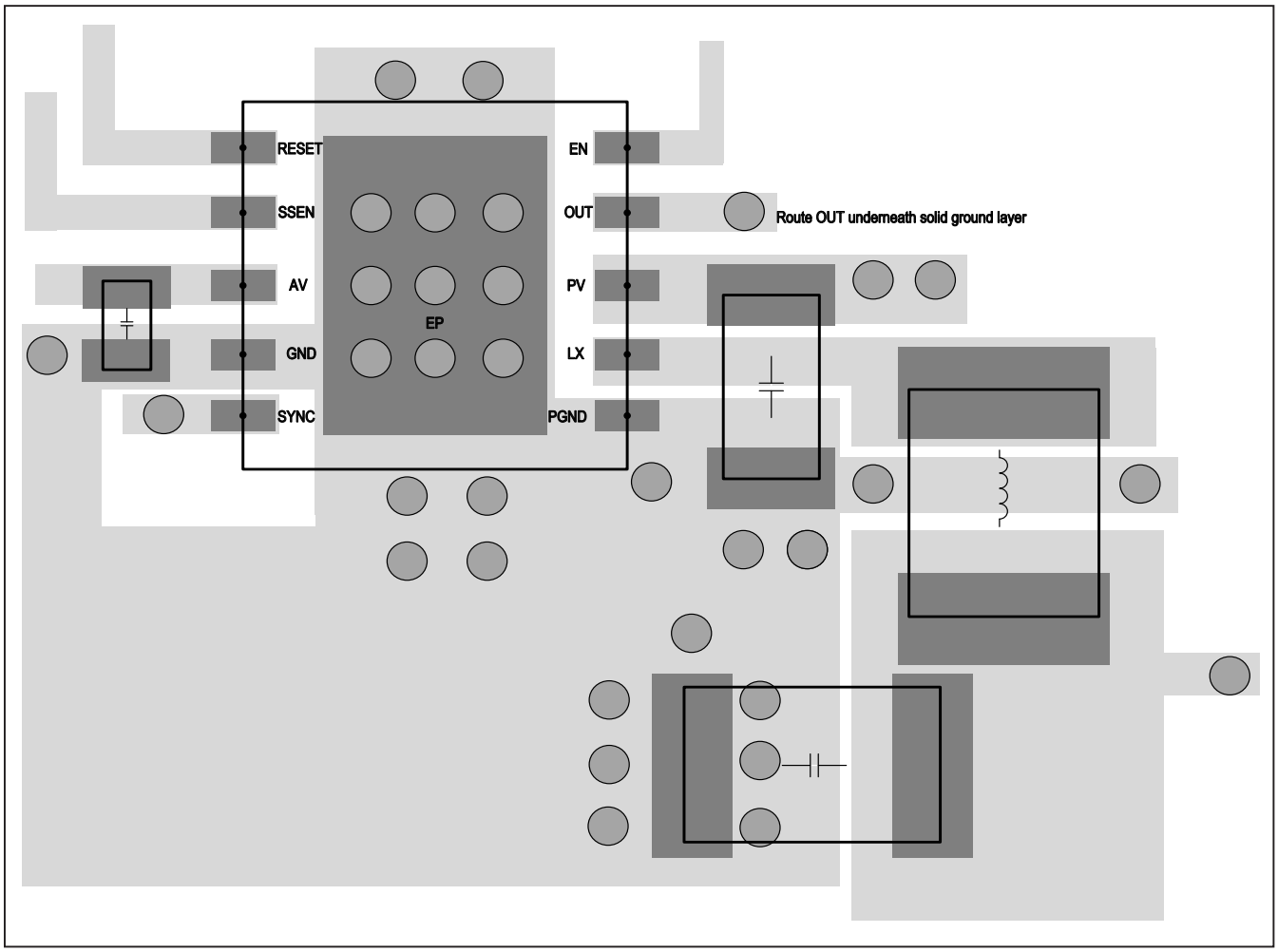


Figure 2. Example Layout of IC and DC-DC Components

Ordering Information

PART	V_{OUT} (V)	I_{OUT} (A)	PIN-PACKAGE
MAX20073ATBA/V+	Adjustable	2	10 TDFN-EP*
MAX20073ATBB/V+	3.3	2	10 TDFN-EP*
MAX20074ATBA/V+	Adjustable	3	10 TDFN-EP*

For variants with different options, contact factory.

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
10 TDFN-EP*	T1033+1C	**21-0137**	**90-0003**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/16	Initial release	—
1	7/18	Updated Typical Application Circuit, Absolute Maximum Ratings, Pin Description, Internal Block Diagram, Synchronization (SYNC), Input Capacitors, Induction Selection, Figure 1, and added PCB Layout Guidelines and Figure 2	1,2, 5–10