ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- V+ to DGND .....-0.3V < V+ < +6.0V
- V- to DGND .....+0.3V < V- < -9.0V
- V+ to V- .....+15V

Analog Input Voltage (any input).....V+ to V-
Digital Input Voltage .....(DGND - 0.3V) to (V+ + 0.3V)
Continuous Power Dissipation
- Narrow Plastic DIP (derate 8.70mW/°C above +70°C)....478mW
- Wide SO (derate 11.76mW/°C above +70°C).....647mW
- Narrow CERDIP (derate 12.50mW/°C above +70°C) ..688mW

Operating Temperature Ranges
- MAX132C_ _ .....0°C to +70°C
- MAX132E_ _ .....-40°C to +85°C
- MAX132MRG .....-55°C to +125°C

Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, DGND = AGND = IN LO = REF- = 0V, REF+ = 545mV, R_{INT} = 602kΩ, C_{INT} = 0.0047µF, C_{REF} = 0.1µF, f_{CLK} = 32,768Hz, 60Hz mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY						
Resolution	(Note 1)				±18	Bits
Zero Error	V_{IN} HI = 0V	T_A = +25°C		0	±0.0076	% of FSR
		T_A = T_{MIN} to T_{MAX}			±0.0168	
Integral Nonlinearity	(Notes 2, 3)	T_A = +25°C		±0.0015	±0.006	% of FSR
Rollover Error	(Note 4)	T_A = +25°C		0	±0.010	% of FSR
		T_A = T_{MIN} to T_{MAX}			±0.032	
Conversion Time	f_{CLK} = 32.768Hz		63			ms
Input Voltage Range	IN HI to IN LO, for specified accuracy				±512	mV
Leakage Current	IN HI, IN LO	T_A = +25°C		±2	±10	pA
		T_A = T_{MIN} to T_{MAX}		±12	±250	
Common-Mode Rejection Ratio	IN HI = IN LO	V_{CM} = ±500mV		±0.009	±0.032	% of FSR
		V_{CM} = ±3.0V		±0.25	±0.50	
Common-Mode Range	IN HI = IN LO				±3.0	V
Read-Zero 50Hz/60Hz Range					±3.1	% of FSR
RMS Noise		T_A = +25°C		15		µV
Zero-Reading Drift	(Note 3)			±0.15	±1.5	ppm/°C
Scale Factor Temp. Coefficient	(Note 3)				±5	ppm/°C
POWER REQUIREMENTS						
Positive Supply Voltage			4.5		5.5	V
Negative Supply Voltage			-5.5		-4.5	V
Positive Supply Rejection	V_{IN} HI = 400mV, V- = -5.0V, 4.5V ≤ V+ ≤ 5.5V	T_A = +25°C		±0.003	±0.0061	% of FSR
		T_A = T_{MIN} to T_{MAX}		±0.003	±0.0168	
Negative Supply Rejection	V_{IN} HI = 400mV, V- = 5.0V, -5.5V ≤ V- ≤ -4.5V	T_A = +25°C		±0.003	±0.0061	% of FSR
		T_A = T_{MIN} to T_{MAX}		±0.003	±0.0168	
Positive Supply Current	Digital input = 0V or V+			60	125	µA
Negative Supply Current	Digital input = 0V or V+			-35	-65	µA
Digital Ground Supply Current	Digital input = 0V or V+			-25	-60	µA
Positive Sleep-Mode Current	Digital input = 0V or V+			1	10	µA
Negative Sleep-Mode Current	Digital input = 0V or V+			-1	-10	µA
Digital Ground Sleep-Mode Current	Digital input = 0V or V+			0	±2	µA

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 5V, V- = -5V, DGND = AGND = IN LO = REF- = 0V, REF+ = 545mV, R_{INT} = 602kΩ, C_{INT} = 0.0047µF, C_{REF} = 0.1µF, f_{CLK} = 32,768Hz, 60Hz mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL SECTION						
Output High	V_{OH}	DOUT, I_{OUT} = -1mA	3.5	4.3		V
		DOUT, I_{OUT} = -100µA	4.0	4.5		
		EOC, P0–P3, I_{OUT} = -100µA	4.0	4.7		
Output Low	V_{OL}	DOUT, I_{OUT} = 1.6mA		0.1	0.4	V
		EOC, P0–P3, I_{OUT} = 100µA		0.1	0.4	
Input High	V_{IH}	Referred to DGND, 4.5V ≤ V+ ≤ 5.5V, $\overline{CS}$, DIN, SCLK	2.4			V
Input Low	V_{IL}	Referred to DGND, 4.5V ≤ V+ ≤ 5.5V, $\overline{CS}$, DIN, SCLK			0.8	V
Input Current	I_{IN}	$\overline{CS}$, DIN, SCLK, and DOUT when three-stated		±10	±500	nA
Input Capacitance	C_{IN}	$\overline{CS}$, DIN, SCLK, and DOUT when three-stated			5	pF

INTERFACE TIMING

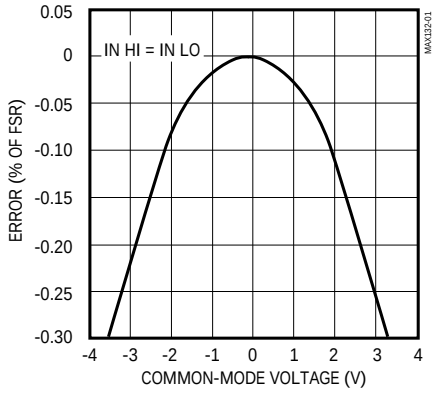
(Test Circuit of Figure 1, Figure 2, V+ = 5V, V- = -5V, DGND = AGND = 0V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ Lead Time	t_1		500			ns
$\overline{CS}$ Lag Time	t_2		400			ns
S_{CLK} High Time	t_3		400			ns
S_{CLK} Low Time	t_4		300			ns
$\overline{CS}$ High Pulse Width	t_5		1			µs
DIN to SCLK Setup Time	t_6		0			ns
DIN to SCLK Hold Time	t_7		200			ns
DOUT Access Time from Three-State	t_8	See Figure 3			320	ns
Data Valid	t_9				60	ns
DOUT Disable Time to Three-State	t_{10}	See Figure 4			320	ns
Delay to P0–P3 High	t_{11}			230	350	ns
Delay to P0–P3 Low	t_{12}			230	350	ns

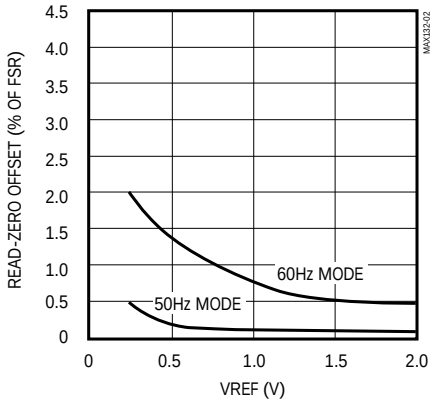
Note 1: ±18-bit accuracy achieved by averaging multiple conversions.
Note 2: Maximum deviation from best straight-line fit.
Note 3: Guaranteed by design, not tested.
Note 4: Difference in reading for equal positive and negative inputs near full scale.

Typical Operating Characteristics

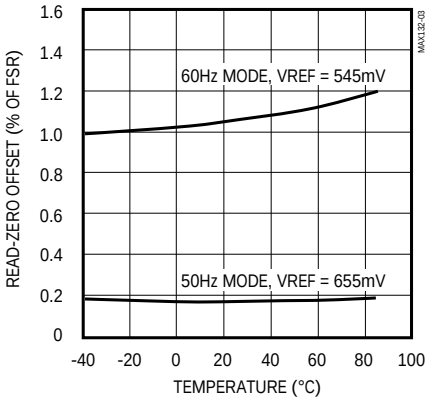
ERROR vs. COMMON-MODE INPUT VOLTAGE (V_{IN} LO–AGND)



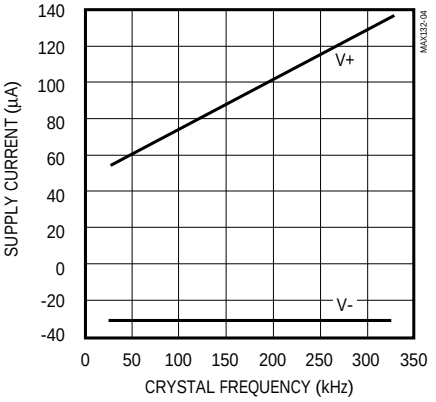
50Hz/60Hz READ-ZERO OFFSET vs. VREF



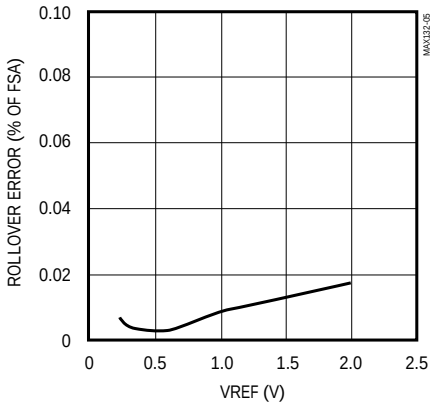
50Hz/60Hz READ-ZERO OFFSET vs. TEMPERATURE



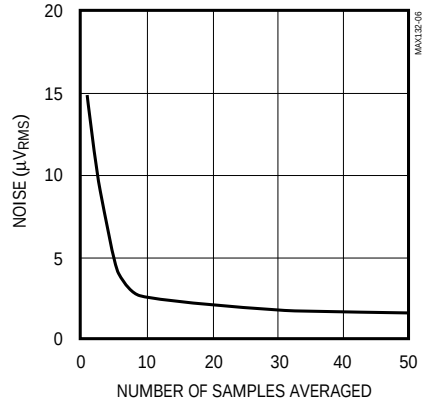
SUPPLY CURRENT vs. CRYSTAL FREQUENCY



FULL-SCALE ROLLOVER ERROR vs. VREF



NOISE vs. NUMBER OF SAMPLES AVERAGED



Pin Description

PIN	NAME	FUNCTION
1	$\overline{CS}$	$\overline{CHIP\ SELECT}$ Input has 3 functions: 1) When low, selects IC for communication; 2) on rising edge, loads input shift register data into one of the command registers; 3) on falling edge, loads data from one of the output registers into the output shift register. When $\overline{CS}$ is high, DOUT is high impedance.
2	DIN	Serial Data In, D7 first bit in. Data is clocked into the register on the rising edge of SCLK.
3	DOUT	Serial Data Out, D7 first bit out. Data is clocked out at the falling edge of SCLK. High impedance when $\overline{CS}$is high.
4	SCLK	Serial Clock Input. On SCLK's rising edge, data is shifted into the internal shift register through DIN. On SCLK's falling edge, data is clocked out of DOUT.
5	OSC2	Oscillator Output 2 is normally connected to a 32,768Hz crystal. Do not connect with external clock source.
6	OSC1	Oscillator Input 1 is normally connected to a 32,768Hz crystal, or may be connected to an external clock.
7	P0	User-programmable output bit 0—programmed through the serial port.
8	P1	User-programmable output bit 1—programmed through the serial port.

Pin Description (continued)

PIN	NAME	FUNCTION
9	P2	User-programmable output bit 2—programmed through the serial port.
10	P3	User-programmable output bit 3—programmed through the serial port.
11	EOC	End of Conversion Output goes high at end of conversion.
12	DGND	Digital Ground—power-supply return
13	V-	Negative Supply, nominally -5V
14	IN HI	Positive Analog Input
15	IN LO	Negative Analog Input
16	AGND	Analog Ground
17	REF-	Negative Reference Input
18	REF+	Positive Reference Input
19	CREF+	Positive Reference Capacitor connection
20	CREF-	Negative Reference Capacitor connection
21	INT IN	Integrator Input. Connect the integration capacitor between INT IN and INT OUT.
22	INT OUT	Integrator Output. To minimize noise, this pin should drive the capacitor's outside foil (negative end).
23	BUF OUT	Buffer-Amplifier Output drives the integrator resistor.
24	V+	Positive Supply, nominally +5V

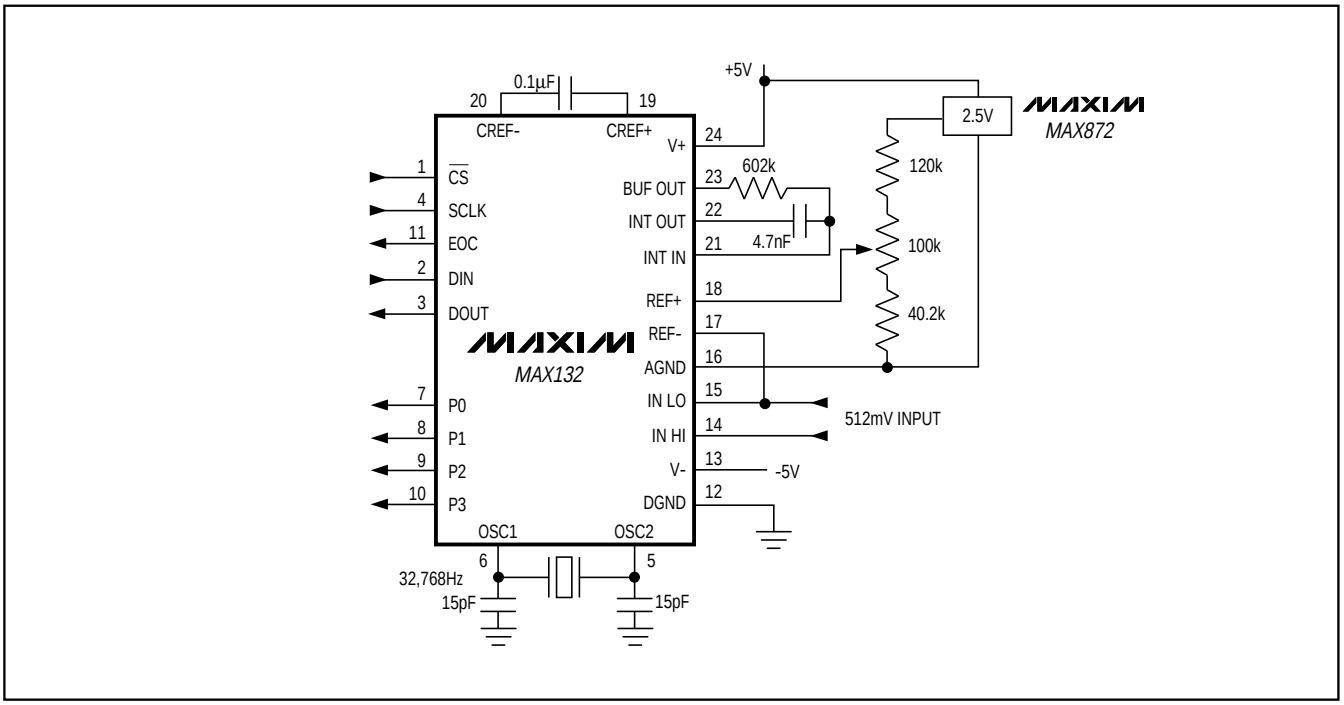


Figure 1. Test and Typical Application Circuit

Functional Description

The MAX132 integrates the input voltage for a fixed period of time, then deintegrates a known reference voltage and measures the time required to reach zero. Good line rejection is achieved by setting the (input) integration time equal to one 50Hz or 60Hz period. The MAX132 has a 50Hz/60Hz mode selection bit that sets the integration time to 655/545 clock periods, respectively, so that 50Hz/60Hz rejection is obtained with a 32,768Hz crystal. The MAX132 is tested and guaranteed at a 16 conv/sec throughput rate. Figure 1 shows the basic MAX132 application circuit, with component values selected for 16 conv/sec .

For applications that don't require 50Hz/60Hz rejection, the MAX132 will operate up to 100 conv/sec at reduced accuracy (typically 0.012% FSR nonlinearity, or ±13 bits). In these applications, the 50Hz mode is recommended because of its longer (655 count) integration time. See *Increased Speed* section.

Analog Design Procedure

Input Voltage Range and Input Protection

The recommended analog full-scale input range is ±512mV. Performance is tested and guaranteed at ±512mV full scale, corresponding to a 2µV/LSB resolution at 18 bits. Resolution is defined as follows:

$$\text{Resolution}\left[\text{Volts/LSB}\right] = V_{IN}(FS) / 262{,}144$$

which corresponds to 2µV/LSB resolution at 18 bits. Consult the *Typical Operating Characteristics* for Noise vs. Number of Samples Averaged and other important operating parameters. Note how accuracy depends on common-mode input voltage (common mode is defined here as $|V_{IN}$ LO - AGND$|$). For optimum performance, set the analog input full-scale between ±470mV and

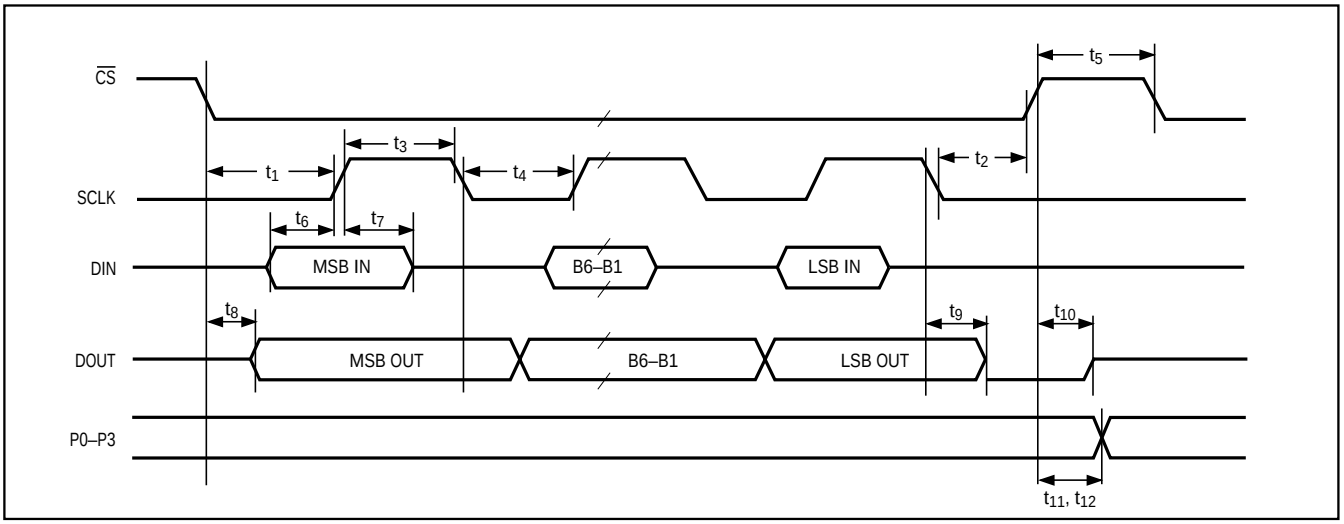


Figure 2. Serial-Mode Timing

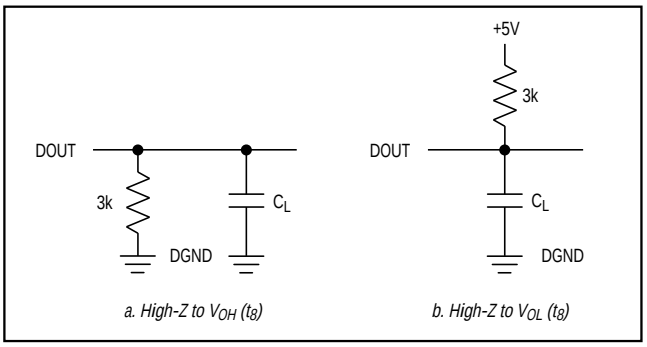


Figure 3. Load Circuits for Access Time

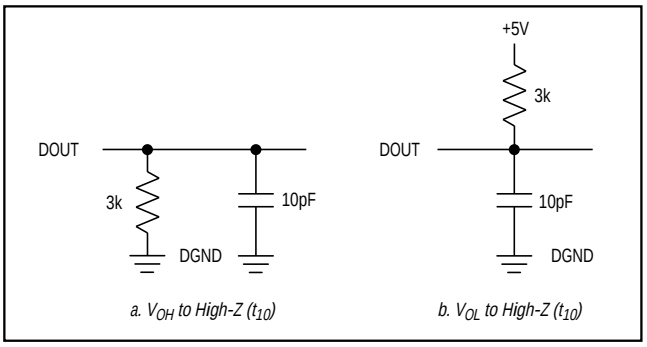


Figure 4. Load Circuits for Disable Time to Three-State

±660mV for 60Hz mode operation or between ±390mV and ±550mV for 50Hz mode operation. The pseudo-differential input voltage is applied across pins 14 and 15 (IN HI, IN LO), and can range to within 2V of either supply rail.

The inputs IN HI and IN LO lead directly to CMOS transistor gates, yielding extremely high input impedances that are useful when converting signals from a high input source impedance, such as a sensor. Input currents are only 2pA typical at +25°C. Figure 6 shows an RC filter at the input to optimize noise performance. Fault protection is accomplished by the 100kΩ series resistance. Internal protection diodes, which clamp the analog inputs from V+ to V-, allow the channel input pins to swing from (V- - 0.3V) to (V+ + 0.3V) without damage. However, if the analog input voltage at the pins IN HI or IN LO exceed the supplies, limit the current into the device to less than 1mA, as excessive current will damage the device.

Reference Voltage Selection

The reference voltage sets the analog input voltage range. For the nominal ±512mV full-scale input range, a 545mV reference voltage is used for the 60Hz mode and a 655mV reference voltage is used in the 50Hz mode. The reference voltage can be calculated as follows:

$$\text{60Hz Mode: } V_{REF} = \frac{(545 \text{ counts})\ (512)\ V_{IN(FS)})}{262{,}144}$$

or

$$\text{50Hz Mode: } V_{REF} = \frac{(655 \text{ counts})\ (512)\ V_{IN(FS)})}{262{,}144}$$

The recommended reference voltage range is 500mV to 700mV. The MAX132 is tested with the nominal 545mV reference voltage in 60Hz mode. Use amplifiers or attenuators (resistor dividers) to scale other full-scale input signal ranges to the recommended ±512mV full-scale range.

References outside the recommended range may be used with a degradation of linearity. A reference voltage from 200mV to 500mV will result in a lower signal-to-noise ratio; a reference voltage from 700mV to 2V will increase the rollover error.

The MAX872 2.50V reference, with its 10µA supply current, is ideally suited for the MAX132. Figure 7 shows how 2.50V can be divided to obtain the desired reference voltage. The reference input accepts voltages anywhere within the converter's power-supply range; however, for best performance, neither REF+ nor REF- should come within 2V of the supplies.

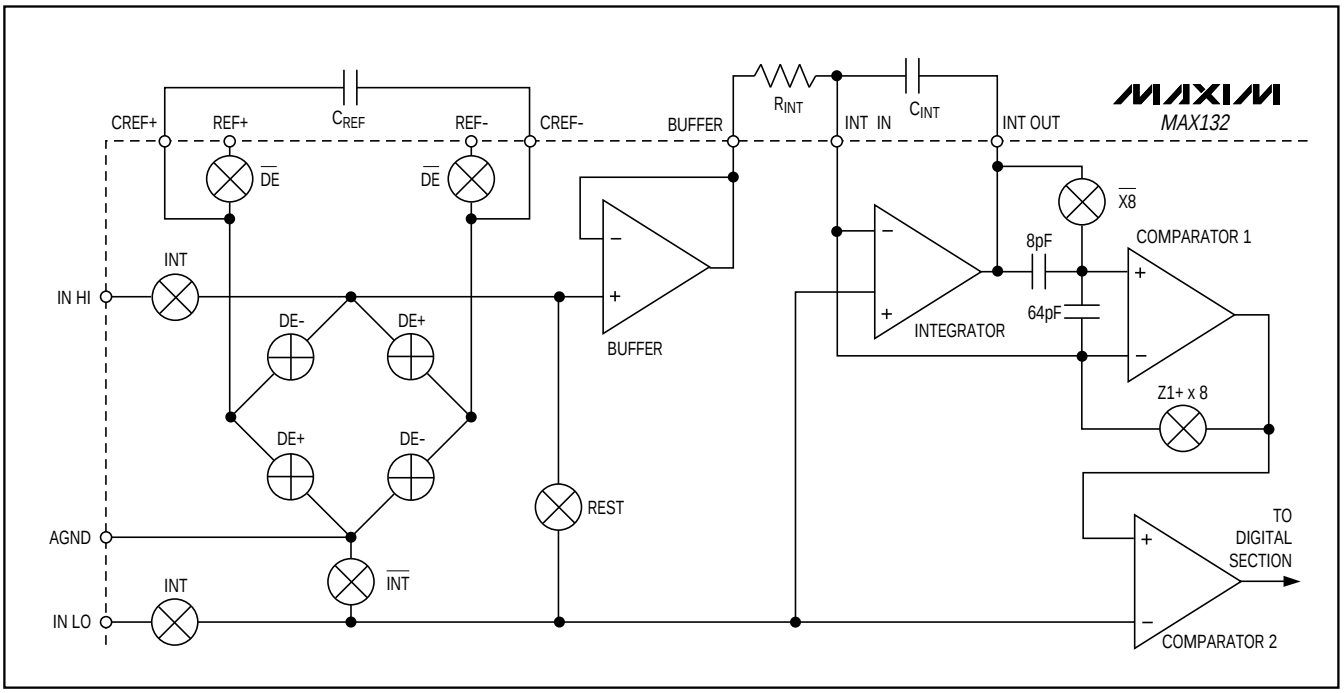


Figure 5. Analog Section Block Diagram

Differential Reference Inputs and Rollover Error

The main source of rollover voltage error is due to common-mode voltages. This error is caused by the reference capacitor losing or gaining charge to stray capacitance. A positive signal with a large common-mode voltage can cause the reference capacitor to gain charge (increase voltage). In contrast, the reference capacitor will lose charge (decrease voltage) when deintegrating a negative input signal. Rollover error is a direct result of the difference in reference to positive or negative input voltages. With the recommended reference capacitor types, the worst-case rollover error is 0.01% of full-scale. Connect REF- to AGND to minimize rollover error. As outlined in the reference section, reference voltages below 500mV also contribute to rollover errors.

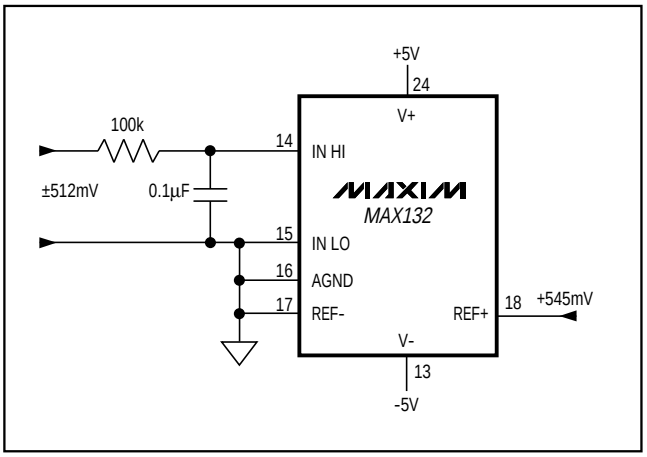


Figure 6. MAX132 Input Circuit

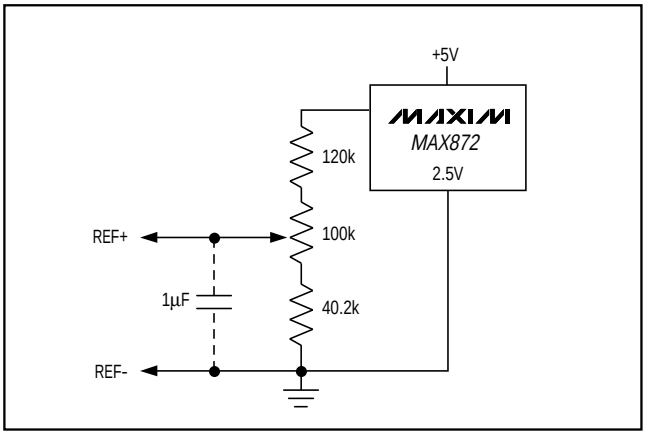


Figure 7. Dividing MAX872 to Generate the MAX132's Reference Voltage

Oscillator Circuit

The internal oscillator is typically driven by a crystal, as shown in Figure 8, or by an external clock. If an external clock is used, connect the clock to OSC1 and leave OSC2 floating. The duty-cycle can vary from 20% to 80%. The typical threshold voltage is approximately 2V. For proper start-up, a full +5V CMOS-logic swing is required.

The oscillator frequency sets the conversion rate. Use 32,768Hz for applications that require 50Hz or 60Hz line rejection. This frequency yields 16 conv/sec. The same clock frequency can be used to reject both line frequencies because the MAX132 integrates for a different number of clock cycles in its 50Hz and 60Hz modes. In each case, the MAX132 integrates for a single complete line cycle (20ms for the 50Hz mode, 16.67ms for the 60Hz mode). Refer to the *Increased Speed* section for operation at higher conversion rates.

External Components

The MAX132 requires an integrator resistor (R_{INT}) and capacitor (C_{INT}), a reference capacitor (C_{REF}), and a crystal. All MAX132 tests are performed with a 32,768Hz crystal frequency. The crystal frequency, reference voltage, and integrator current determine the values of R_{INT} and C_{INT}.

Crystal

Figure 8 shows the internal oscillator drive circuitry used with external crystals. The two external capacitors provide DC bias at start-up. The 15pF capacitors shown are typical values. The actual capacitance will vary, depending on the crystal manufacturer's recommendation and board layout.

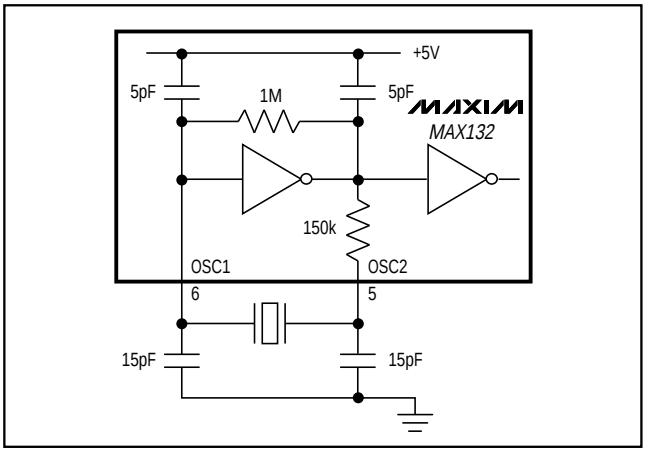


Figure 8. MAX132 Internal Oscillator Drive Circuitry

Table 1. Crystal Frequencies and Integrator Capacitors for 50Hz to 60Hz Operation

Conv/sec	Crystal Freq. (Hz)	C_{INT}/60Hz (pF)	C_{INT}/50Hz (pF)	Resistor (kΩ)
16	32,768	4700	6800	602
32	65,536	2700	3300	602
48	98, 304	1800	2000	602
64	131,072	1200	1500	602
80	163,840	1000	1200	602
96	196,608	820	1000	602

Note: Capacitor values are for a 3.0V integrator swing.
Manufactures of miniature quartz resonators include:
Epson of America
C-2 (through-hole), MC-306 (SMD)
Phone: (310) 787-6300; Fax: (310) 782-5320

Integrator Resistor

The integrator resistor sets the maximum integrator output current for the integrate phase. A 602kΩ low-noise, metal-film integrator resistor is recommended for use with reference voltages between 545mV and 655mV. Best linearity is achieved when the integration current (I_{INT}) does not exceed 2.5µA. For other reference voltages, select R_{INT} as follows:

$$R_{INT} = \frac{V_{REF}}{2.5\mu A < I_{INT} < 0.5\mu A}$$

and

$$I_{INT} = \frac{V_{REF}}{R_{INT}}$$

Integrator Capacitor

The oscillator frequency, integrator resistor, and integrator capacitor set the maximum integrator output voltage swing for full-scale reading. The integrator voltage swing is about 3V and should not come within 2V of either supply rail to avoid saturation. A 602kΩ integrator resistor and a 4.7nF integrator capacitor are recommended with a clock frequency of 32,768Hz. If different clock frequencies are used, select C_{INT} using the following equations:

$$C_{INT} = \frac{(V_{IN(FS)})\ (t_{INT})}{(R_{INT})\ (V_{SWING})}, \text{ where } 1V < V_{SWING} < 3.5V;$$

and

$$t_{INT} = \frac{545}{f_{OSC}}, \text{ for 60Hz mode}$$

or

$$t_{INT} = \frac{655}{f_{OSC}}, \text{ for 50Hz mode}$$

The integrator capacitor's dielectric absorption directly affects integral nonlinearity. High-quality metal-film capacitors are recommended in the following order of preference: polypropylene, polystyrene, polycarbonate, and polyester (Mylar). The polyester capacitor will generate some integral nonlinearity.

To minimize noise, INT OUT should drive the outside foil (negative end) of the capacitor. Manufacturers of polypropylene capacitors include Sprague (715P), Panasonic (ECQ-P), Roderstein (KP1835), Wima (FKP), and CSF Thompson (PL/PS).

Reference Capacitor

The reference capacitor must be small enough to fully charge from a discharged state on power-up in reasonable time, and large enough so the charge does not droop excessively during a conversion. The reference capacitor is normally 0.1µF for all oscillator frequencies. For applications that require a physically smaller capacitor, the equation below will maintain C_{REF} proportionality:

$$C_{REF} = \frac{0.0033}{f_{OSC}}$$

The reference capacitor must have low leakage, since it stores the reference voltage while floating during the deintegrate phase. Any leakage or charge loss during this phase changes the scale factor and will cause an error. Appropriate metal-film capacitors recommended for their low-leakage characteristics[1] are (in this order): polypropylene (up to +105°C, large size), teflon (suitable for use up to +125°C, large size), polystyrene, polycarbonate, and polyester.

At temperatures above +85°C, capacitor leakage may affect accuracy. In such cases, increasing the value of C_{REF} up to 50% and more will help at the expense of longer start-up time at power-on. The start-up time is proportional to C_{REF} and can be estimated by:

$$t_{START-UP} = C_{REF}(\mu F)\ x\ 10\ x\ 100k\Omega$$

[1] Pease, R.A., "Understanding Capacitor Soakage to Optimize Analog Systems," *EDN*, October 13, 1982, p.125.

Digital Interface

Serial data at DIN is sent in 8-bit packets and is shifted into the internal 8-bit shift register with each rising edge of SCLK. The data is then latched into either command input register 0 or command input register 1, as determined by the LSB of the data sent, and is latched on the rising edge of CHIP SELECT (CS) Data is clocked out of the selected output register on each falling edge of SCLK. D7(MSB) must be the first data bit to be shifted in and is the first bit to be shifted out.

Output data is shifted out at the same time command data is shifted in. Command data must be clocked in on the previous 8-bit read-write cycle to receive conversion data in the present cycle.

Since there is no internal power-on reset, initialize the MAX132 immediately after power-up to insure correct operation.

Table 2 defines each bit of five registers: the two command input registers, output register 0, output register 1, and the status output register.

Command Input Register 0

Register-Set Bits

Data bits D1 and D2 of command register 0 (RS1 and RS0) determine the data to be read on the data bus. These bits select which register outputs data to the bus. Table 3 defines the bit values that determine which register is read on the next cycle (Figure 9).

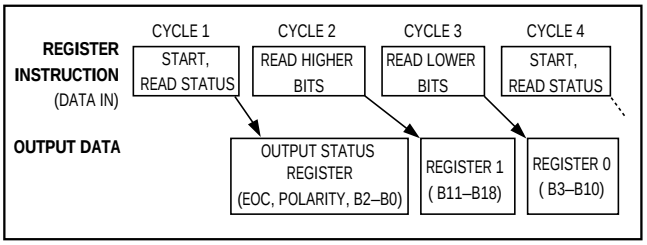


Figure 9. Instruction and Data Sequencing

Read-Zero Bit

The read-zero bit allows the ADC to calibrate on command for zero offset. The read-zero bit, when set to 1, internally shorts the inputs; when a start-conversion command is given, the zero error is converted. Subtract the results from the standard external measurement conversion when the read-zero conversion ends. If the read-zero bit is set to 0, the converter measures the voltage between IN HI and IN LO once a start bit is given. Take a new zero reading periodically and whenever the ambient temperature, the reference voltage, or the common-mode input voltage are changed.

Table 3. Register Set-Bit Definitions

RS1	RS0	DEFINITIONS
0	0	Selects Register 0; output for data bits B3–B10
0	1	Selects Register 1; output for data bits B11–B18
1	0	Selects Register 2; output status for data bits B0–B2, polarity, sleep, integrating, EOC, and collision bit
1	1	Invalid data

Table 2. Register Map of Input and Output Data

REGISTER		DATA BIT							
		D7	D6	D5	D4	D3	D2	D1	D0
Command Input Register 0	"1"	Start Convert	50Hz	Sleep	Read Zero	Don't Care	RS0*	RS1*	0
	"0"	Returns to 0 at EOC	60Hz	Awake	Read V_{IN}	Don't Care			
Command Input Register 1		Set P3 Output	Set P2 Output	Set P1 Output	Set P0 Output	Don't Care	Don't Care	Don't Care	1
Output Register 0 RS1 = 0, RS0 = 0		B10	B9	B8	B7	B6	B5	B4	B3
Output Register 1 RS1 = 0, RS0 = 1		B18 MSB	B17	B16	B15	B14	B13	B12	B11
Output Status Register RS1 = 1, RS0 = 0	"1"	Collision	EOC	Integrating Input	Sleep	-Polarity	B2	B1	B0 LSB
	"0"	No Collision	Converting	Not Integrating	Awake	+Polarity			

***Note**: Refer to Table 3.

Averaging 2 or 3 read-zero measurements provides the most accurate read-zero value. Perform a read-zero sequence whenever a large change in the input voltage is expected.

Sleep Bit

When the sleep bit is set to 1, (bit D5 in command input register 0), the low-power sleep mode starts when EOC returns high. In sleep mode, the supply current is typically 1µA and the oscillator shuts down. The interface remains active and data can be read. When exiting sleep mode, the analog circuitry needs time to stabilize before the next conversion starts. Accomplish this by writing a dummy instruction to emerge from sleep mode, and wait at least one conversion cycle before writing a start instruction.

50Hz/60Hz

With a 32,768Hz crystal, the 50Hz/60Hz bit sets the integrate period equal to one line cycle for 50Hz/60Hz environments. When D6 (in command input register 0) is set to 0, the integrate count is an integer multiple of 60Hz (32,768Hz/60Hz = 546 counts). When D6 is set to 1, the integrate input count is an integer multiple of 50Hz (32,768Hz/50Hz = 655 counts). Achieve the greatest AC rejection by adjusting the integration period for 50Hz or 60Hz.

Start Conversion Bit

The start conversion bit (D7) in command input register 0 initiates a conversion when set to 1. The MAX132 immediately starts a conversion, stops at conversion end, and then waits for the next start-bit command. A start instruction is needed to initiate each conversion. To initiate a continuous data stream, write a separate start command for each conversion in three ways:

1) Wait longer than a known conversion time and then write another start command.
2) Poll either the EOC status register bit or the EOC line to determine conversion end and start time for the next conversion. EOC becomes 1 at conversion end at count 0000 of the conversion counter (Figure 10).
3) Set the start bit to 1 before a conversion end. The internal conversion counter is then checked for its count. If the count is 0000 (EOC = 1), a new conversion starts and the conversion counter is set to 0001. The start bit resets to 0 after 5 clock cycles. The MAX132 will not check the start bit again until the conversion counter returns to a 0000 count. This means a start command can be given any time after 0005 internal conversion count; the next conversion starts when the counter returns to 0000.

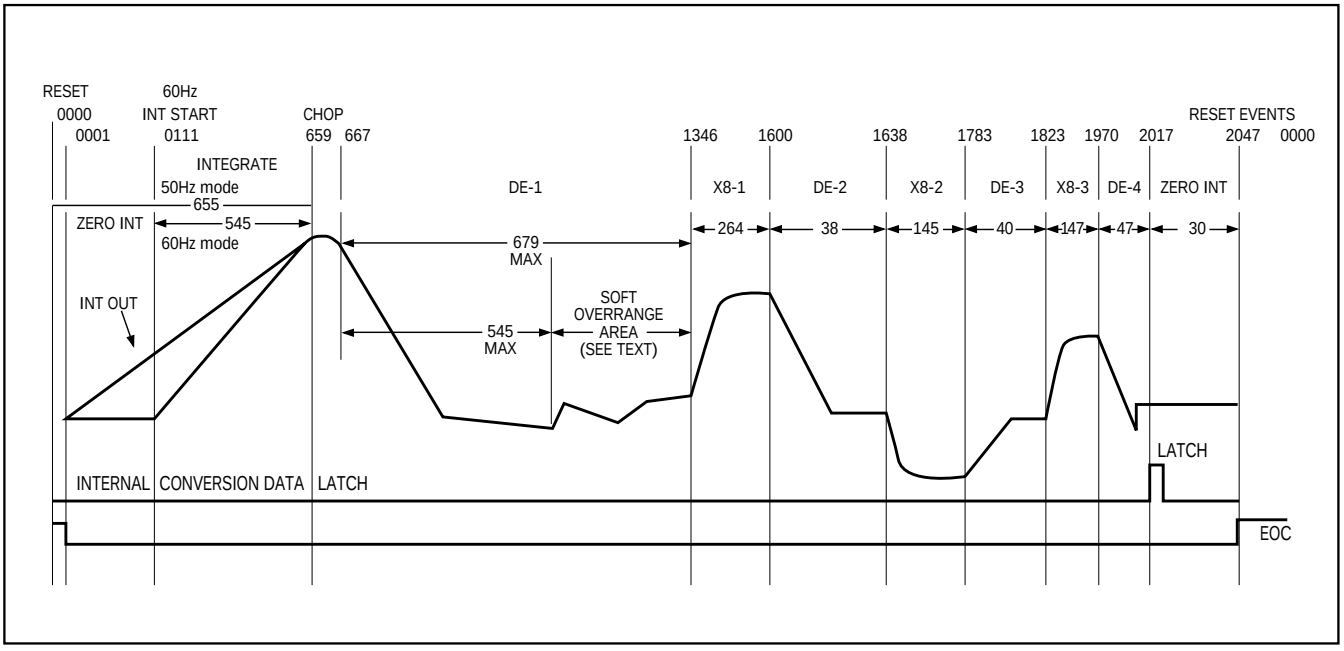


Figure 10. Conversion Timing (Negative Input Shown)

Table 4. Overrange Values for Resolution Used

Bits Used	Resolution Bits	Soft Overrange Start Value	Hard Overrange Maximum Value
B18–B3	±15	34,880	43,805
B18–B2	±16	69,760	87,610
B18–B1	±17	139,520	175,220
B18–B0	±18	279,040	350,440

Table 5. Output Values for 16-Bit Resolution (Offset Corrected)

Input	Hexadecimal Reading	Decimal Counts	Comment
+640mV	+A000	+40960*	
+576mV	+9000	+36864*	
+545mV	+8840	+34880*	Positive Reference Voltage
+512mV	+8000	+32768	Positive Full Scale
+448mV	+7000	+28672	
+384mV	+6000	+24576	
+320mV	+5000	+20480	
+256mV	+4000	+16384	
+192mV	+3000	+12288	
+128mV	+2000	+8192	
+64mV	+1000	+4096	
+15µV	+0001	+1	
0	+0000	0	
-15µV	-FFFF	-1	
-64mV	-F000	-4096	
-128mV	-E000	-8192	
-192mV	-D000	-12288	
-256mV	-C000	-16384	
-320mV	-B000	-20480	
-384mV	-A000	-24576	
-448mV	-9000	-28672	
-512mV	-8000	-32768	Negative Full Scale
-545mV	-77C0	-34880*	Negative Reference Voltage
-576mV	-7000	-36864*	
-640mV	-6000	-40960*	

* Soft Overrange Operation

Note: The MAX132 exhibits additional errors when operating in the soft overrange area. Operation in this region is not included in the specifications. The soft overrange values listed in Table 5 do not include error correction.

Command Input Register 1

User-Programmable Output Bits P0 to P3

Command input register 1 always has data bit D0 = 1. Data bits D4 to D7 of command register 1 control the states of the user-programmable output pins P0 to P3, respectively (Table 2). These four outputs can be used to control an external multiplexer, programmable gain amplifier, or other devices.

Output Registers

Output data is the sum of system offset (read zero) plus the results of the external input voltage measurement.

Register 0

Register 0 contains the low-byte (bits B3–B10) conversion data. New data is available after EOC goes high. Access register 0 by setting RS0 and RS1 to 0.

Register 1

Register 1 contains the high-byte (bits B11–B18) data. Data is in a twos-complement format, where the polarity bit is a 1 for negative polarity data. Access register 1 by setting control bits RS0 = 1 and RS1 = 0 when writing to the command input register.

Status Register

Bits B0–B2

The B0, B1, and B2 bits are located in the status register. At the end of each conversion these bits are updated and read back from the status register. For full 18-bit resolution, use bits B0–B2. Average multiple results to increase accuracy. The polarity bit information is necessary to determine if the reading is not in overrange (Tables 4 and 5).

Integrate Bit

The integrate (INT) bit is set to 1 at the beginning of the integration phase and becomes 0 at the end. Poll INT to determine the earliest time the input can be changed without affecting the conversion.

End-of-Conversion Bit

The end-of-conversion (EOC) bit signals conversion status. If EOC is 1, the conversion is complete and the ADC waits in zero-integrate mode at time = 0000 for the next start instruction. A conversion cycle has 2048 counts. EOC becomes 1 at count 0000 and 0 at count 0001.

Collision Bit

The collision bit warns the microprocessor (µP) that the register's data was changed during the read cycle. A collision occurs if the internal result latches on the falling edge of $\overline{CS}$, causing the collision bit to be set to 1 on the rising edge of the next $\overline{CS}$. This occurs because these two pulses are asynchronous. Once the status register is

read, the collision bit is automatically reset to 0. To determine collision status, read the status register collision bit before and after reading output registers 0 and 1.

Collisions will not occur if a conversion's read cycle is completed before the next conversion begins.

Sequence Counter and Results Counter

A binary sequencing counter controls the conversion phase's sequencing (or timing). In integrate phase, both start and stop occur at preset counts. The deintegration phases start at predetermined counts, but are terminated when the comparator detects zero crossing at the integrator output.

The results counter accumulates counts during all deintegrate phases. It is an up/down binary counter, with the count direction determined by the deintegration polarity. In the first deintegrate phase, the results counter counts by 512. Since the second deintegrate phase deintegrates a residual voltage multiplied by 8, the results counter increments or decrements by 64 during this phase. It increments or decrements by 8 during the third deintegrate phase, and by 1 during the fourth deintegrate phase. The results counter content transfers to the results register at each conversion end.

Overrange Indication

B18 is not strictly an overrange bit. This 19th bit is necessary to exploit the converter's full range, and to ensure that a full 18-bit result can be achieved after a zero reading has been deducted.

The actual overrange value is a function of the number of bits of resolution used. Table 4 lists the overrange values for different resolutions.

The MAX132 has two overrange levels (Figure 10 and Table 4). The first level is a soft overrange that is set by the user. Overrange is arbitrarily set at a value, preferably less than the 279,040 (including any zero offset) raw counts soft limit. A nonlinearity step of about 64 counts occurs at raw count 279,040 and again at 330,240 counts.

The second level is a hard overrange with a maximum value of 350,440 counts. Attempts to deintegrate values greater than this will result in a value of ±350,440 counts.

Multislope Conversion Phases

Multislope conversion allows 350,440 counts with a clock frequency of only 32.768kHz. After zero-crossing, the main comparator (with some delay) sends a signal to the digital control section, which then terminates the deintegrate period by issuing commands to the analog switches. This action entails further delay because the commands must be synchronous with the clock. As a result, the delay between zero-crossing and switch actuation can exceed one clock cycle. A "residue" voltage that represents unwanted extra counts in the conversion result is left on the capacitor, while the integrator's output continues past the zero crossing.

Dual-slope converters ignore this residue voltage error. However, the multislope MAX132 inverts, amplifies, and deintegrates the residue, canceling the extra counts by driving an up/down counter in the opposite direction.

This process of measuring and accounting for the residue can be repeated for the successively smaller errors remaining after each deintegration. (Deintegration is simply an integration of V_{REF}, with polarity chosen so the integrator output ramps toward zero.) The MAX132, for example, executes three cycles in which the residue is inverted, multiplied by eight, and deintegrated (Figure 10).

Integrate Phase

The MAX132 integrates the input signal by connecting the integrator's noninverting input to IN LO, and the buffer input to IN HI. The integration period is 545 counts for 60Hz mode and 655 counts for 50Hz

Deintegrate Phase

The integrator capacitor's voltage polarity at the end of integrate phase determines the polarity of the first deintegration phase. The first deintegration phase ends when the comparator detects that the integration capacitor has been discharged. The MAX132 then goes into a rest phase, where both the buffer input and the integrator's noninverting input are connected to AGND, integrating the system offset.

Near the end of the maximum allowable deintegration period, the integrator capacitor voltage polarity is again sampled, resulting in either a positive or negative deintegrate cycle.

Rest Phase

A rest phase follows each deintegrate phase. The rest phase starts when the integrator crosses zero and ends when the maximum count for that deintegration phase has been reached.

First Times-Eight Phase

When the zero crossing is detected at the end of the deintegrate phase, deintegration continues until the next clock cycle. This causes the integrator to overshoot zero crossing slightly, leaving a small residual voltage on the integration capacitor. The first times-eight (X8) phase inverts and multiplies this residual by a factor of 8.

Second Deintegrate Phase

The second deintegrate phase deintegrates residual voltage on the integration capacitor that has been through the X8 phase. Since the voltage across the integration capacitor has been multiplied by 8, each deintegration clock cycle corresponds to 1/8 of one clock cycle during the first deintegration.

Additional Times-Eight and Deintegrate Phases

At the end of the second and third deintegration phases, the device performs a X8 multiplication of the residual voltage left on the integration capacitor. After each of these X8 multiplications, a deintegration occurs, resulting in a second, third, and fourth deintegration phase. Each time the residual voltage on the integration capacitor is multiplied by 8, the following deintegration has 8 times finer resolution.

Zero-Integrate Phase

The zero-integrate phase zeros out the integrator to prepare for the next integration (Figure 10). This phase occurs at the beginning and end of each conversion. At power-up, or in the hold mode prior to a conversion, the MAX132 continues to zero integrate until a conversion starts. When a conversion starts in 60Hz mode, another 111 clocks of zero integrate are completed before the beginning of a conversion. In 50Hz mode, only one additional zero integrate is performed before the conversion starts. An additional 20 clocks of zero integrate occur at each conversion end.

Applications Information

Extended Delays Between Conversions

An extended delay between conversions can degrade the subsequent conversion result due to capacitor droop and internal offset/common-mode voltages. The initial reading may be off by 4 to 6 counts in a ±15-bit configuration. When the delay between conversions exceeds 2 seconds (either because of a slower conversion rate or the use of sleep mode), it is recommended that the first reading after this delay be discarded.

Increased Speed

The MAX132 is tested with a 32,768Hz clock frequency, which results in 16 conv/sec. Up to 96 conv/sec may be achieved with higher clock frequencies and some changes in component values, as shown in Table 1. Operation at higher conversion rates reduces accuracy, and care must be taken to get the best results.

Although either the 50Hz or 60Hz mode can be used, complete rejection of 50Hz or 60Hz normal-mode noise at conversion rates above 16 conv/sec is impossible. Use the 50Hz mode when operating at more than 16 conv/sec, irrespective of the local line frequency. The 50Hz mode uses a slightly longer integration time than the 60Hz mode, and generally gives lower-noise performance.

Table 1 lists the crystal frequencies and integrating capacitor values for the 50Hz and 60Hz modes for various conversion rates, although the 50Hz mode is recommended for clock rates above 32,768Hz.

The raw data can be used where highest accuracy is not required, and the least significant bits can be ignored. At 96 conv/sec, the accuracy is 13 bits. Improvements in accuracy can be gained by averaging both the data and the zero readings, although data averaging compromises the converter's speed performance.

To maximize throughput, take zero readings only when necessary, i.e., when the common-mode voltage changes. It is not normally necessary to take a zero reading after every data reading, as an excessive number of zero readings reduces the converter's effective speed.

Noise Reduction

To minimize noise, each supply must be bypassed to GND with a 0.1µF capacitor. A ground plane should also be placed under the analog circuitry. Use the RC network at the inputs as shown in Figure 6. Also refer to the section "Noise Reduction Techniques" in the notes for the MAX132 evaluation kit. To minimize the coupling effects of stray capacitance, keep digital lines as far from analog components and lines as possible. Also, connect the integrator capacitor's outside foil to the INT OUT pin to minimize stray capacitive coupling. If possible, keep the digital interface inactive while the MAX132 is converting.

Ratiometric Measurements

Figure 11 shows an application to measure temperature ratiometrically with an RTD sensor. The voltage drops across the RTD sensor and the 250Ω reference resistor are generated by the same current source. The voltage of the sensor (V_S) is fed directly into the differential inputs, and the voltage drop across the reference resistor (V_R) is brought into the differential reference inputs. The relationship of these voltages is ratiometric and unaffected by the actual current. The MAX132's output is proportional to V_S divided by V_R, independent

of the overall accuracy of the current source. The current source delivers 2mA, resulting in about 500mV across the 250Ω resistor—suitable to fit the MAX132's ±512mV full-scale range. Note that the accuracy of the reference resistor (0.1%) sets the circuit's accuracy. The power consumption of the RTD sensor is small (0.5mW), minimizing errors caused by self-heating.

Interfacing to a µP Parallel Port

Figure 12 shows a high-level software subroutine for reading output/status data and writing command data to the MAX132. It provides an algorithm for serial communication when the µP port does not have a predefined serial interface protocol (i.e., SPI™ or Microwire™). The routine sends command data (TxByte) to the MAX132 while concurrently collecting the MAX132's output register data (selected by the **previous** write cycle). Note that a write is required before each read to change the next output register to be read, and that the subroutine must be repeated three times to read the output status register, Output Register 0, and Output Register 1.

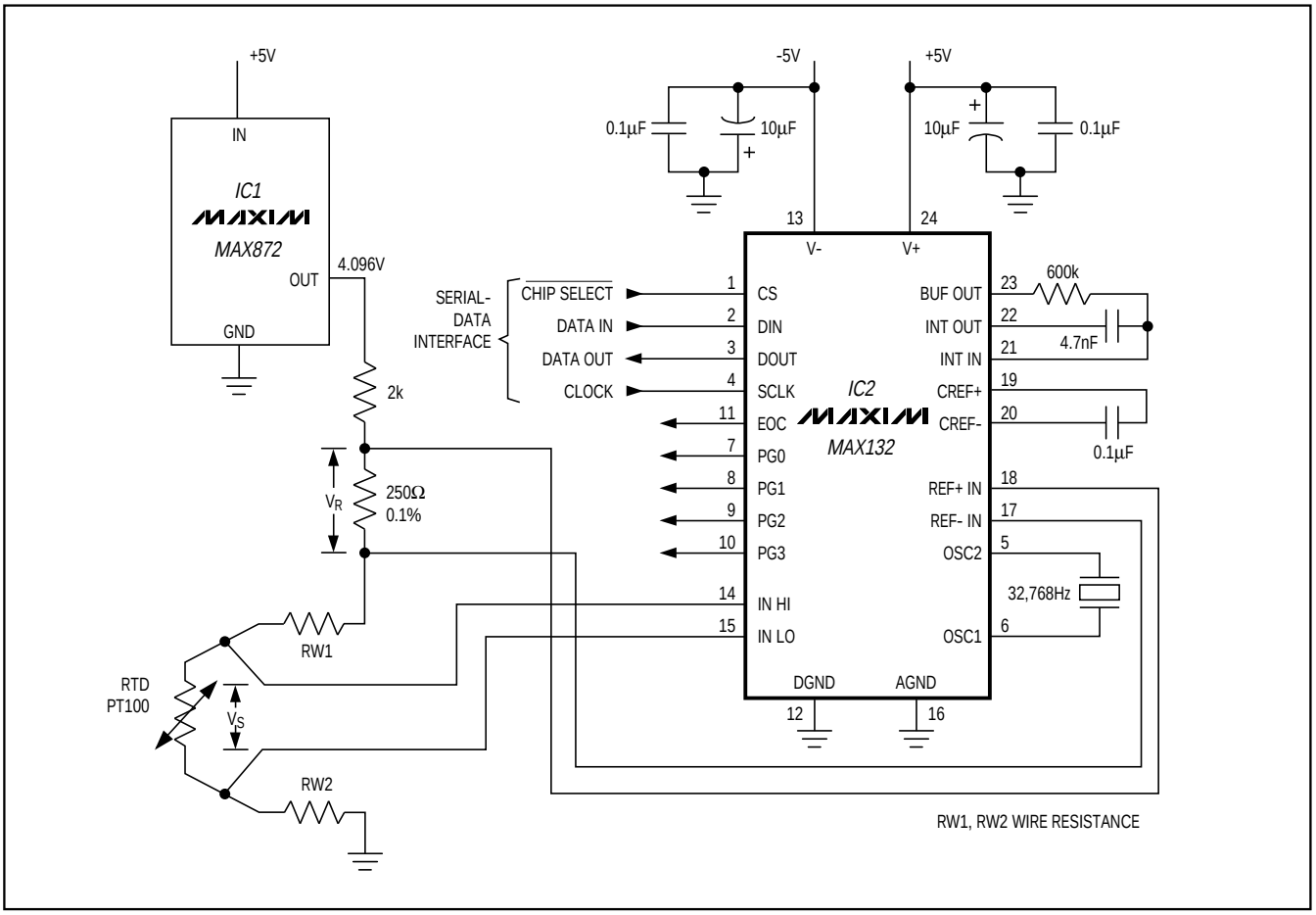


Figure 11. Ratiometric Configuration Using the Differential Reference Inputs

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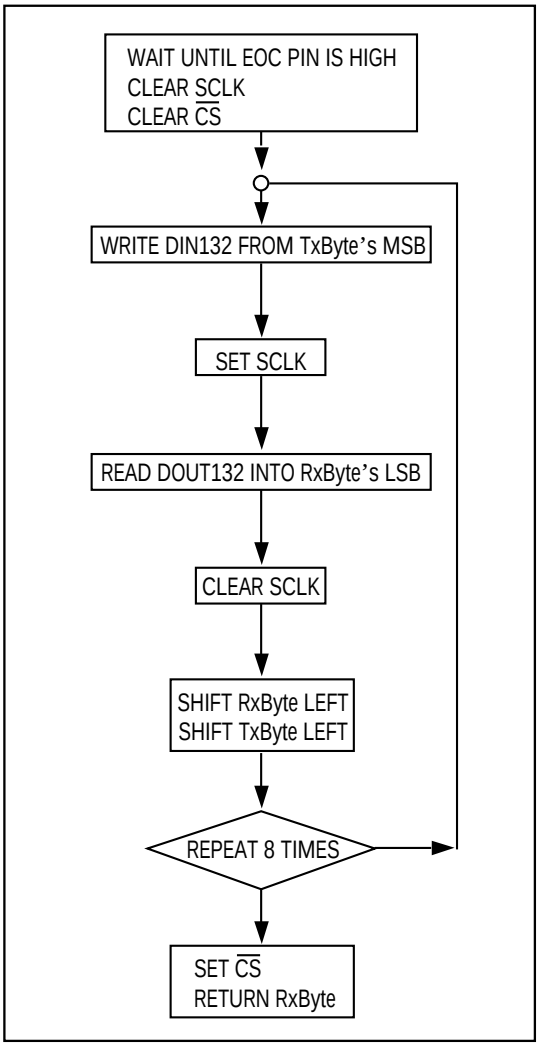
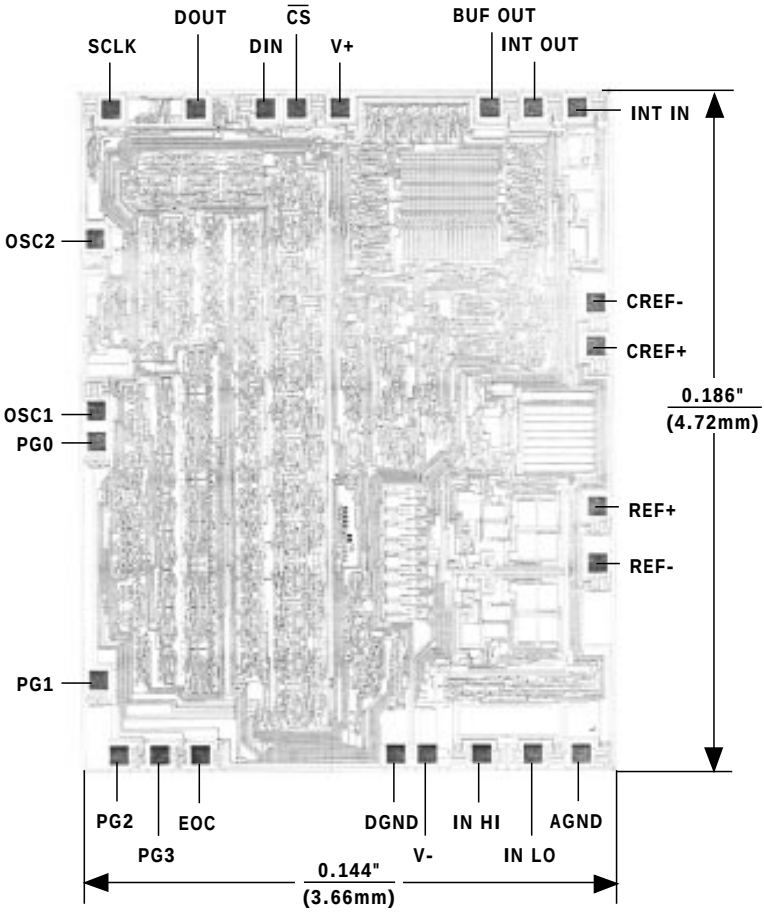


Figure 12. MAX132 Read/Write Algorithm

Chip Topography



TRANSISTOR COUNT: 2799

SUBSTRATE CONNECTED TO V+