Pin Configuration and Pinout

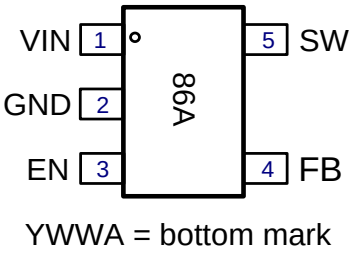


Figure 2 · **Pinout TSOT-5 Top View**

Marking: Front Mark 86A
Bottom Mark YWWA
Year/Work Week/Lot Code

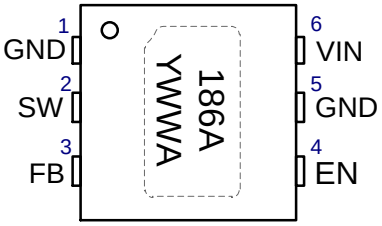


Figure 3 · **Pinout UDFN 2x2 6L Top View**

Marking: Line1 186A
Line2 YWWA
Year/Work Week/Lot Code

Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type
-40°C to 85°C	RoHS Compliant, Pb-free	TSOT-5L	LX7186AISG	Bulk / Tube
			LX7186AISG-TR	Tape and Reel
		UDFN 2x2 6L	LX7186AILU	Bulk / Tube
			LX7186AILU-TR	Tape and Reel

Pin Description

Pin Number		Pin Designator	Description
TSOT-5L	UDFN 2x2 6L		
1	6	VIN	Supply Input Pin. A 4.7µF ceramic capacitor should be connected between the VIN pin and GND pin to bypass the supply.
2	1, 5	GND	Ground Pin.
3	4	EN	Enable Input. Setting this pin above 1.5V enables the IC. Setting this pin below 0.4V shuts down the IC. When the IC is in shutdown mode, all functions are disabled to decrease the supply current below 1µA.
4	3	FB	Feedback Pin. This pin is connected to an external resistor divider to program the system output voltage.
5	2	SW	Power Switch Output Pin. Inductor connection to drain of the internal PFET and NFET switches.

Block Diagram

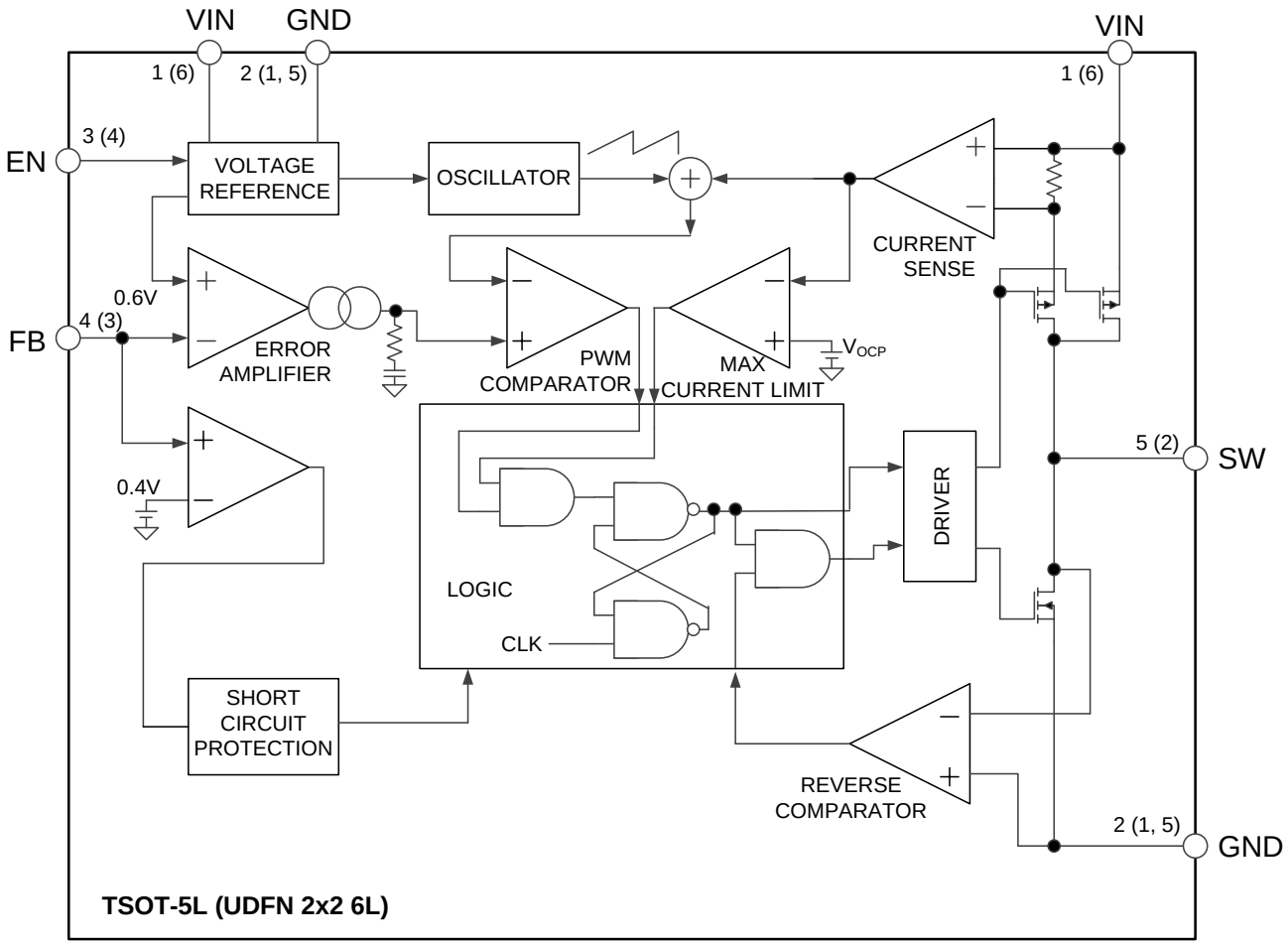


Figure 4 · **Simplified Block Diagram of LX7186A**

Absolute Maximum Ratings

Parameter	Min	Max	Units
VIN to GND	-0.3	6	V
EN, FB to GND	-0.3	VIN + 0.3	V
SW to GND	-0.3	VIN + 0.3	V
Junction Temperature		150	°C
Storage Temperature	-65	150	°C
Peak Package Solder Reflow Temperature (40s, reflow)		260 (+0,-5)	°C
Lead Soldering Temperature (10 seconds)		260	°C

Note: Performance is not necessarily guaranteed over this entire range. These are maximum stress ratings only. Exceeding these ratings, even momentarily, can cause immediate damage, or negatively impact long-term operating reliability

Operating Ratings

	Min	Max	Units
VIN	2.5	5.5	V
V_{OUT}	0.6	VIN – 0.5	V
Ambient Temperature	-40	85	°C
Output Current	0	1	A

Thermal Properties

Package	Thermal Resistance	Typ	Units
TSOT-5	θ_{JA}	160	°C/W
UDFN 2x2 6L	θ_{JA}	86	°C/W

Note: The θ_{JA} number assumes no forced airflow. Junction Temperature is calculated using $T_J = T_A + (PD \times \theta_{JA})$. In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

Electrical Characteristics

Note: Unless otherwise specified, the following specifications apply at VIN = V_{EN} = 3.3V. -40°C < T_A < 85°C.

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
Operating Current						
I_Q	Quiescent Current	V_{FB} = 0.65V		62	100	µA
I_{SHDN}	Shutdown Supply Current	V_{EN} = GND		0.1	1	µA
VIN UVLO						
V_{UVLO}	Under Voltage Lockout	VIN rising		2.3		V
V_{HYS}	UVLO Hysteresis			200		mV

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
FEEDBACK VOLTAGE						
V_{REF}	Feedback Voltage		0.588	0.6	0.612	V
I_{FB}	FB Pin Input Bias Current	V_{FB} = VIN	-100		100	nA
ΔV_{OUT}	Output Voltage Accuracy		-2		2	%
OUTPUT						
R_{DSON_P}	PMOS Switch R_{DSON}	I_{SW} = 200mA		0.28		Ω
R_{DSON_N}	NMOS Switch R_{DSON}	I_{SW} = -200mA		0.25		Ω
I_{LEAK}	NMOS Switch Leakage Current	VIN = 3.3V, V_{SW} = 3.3V		0.1		µA
I_{LIM}	Switch Current Limit	V_{FB} = 0.55V	1.5	2.0		A
T_{OTSD}	Thermal Shutdown			160		°C
T_{HYS}	Thermal Shutdown Hysteresis			20		°C
OSCILLATOR						
f_{OSC}	Oscillator Frequency		1.12	1.40	1.68	MHz
D_{MAX}	Maximum Duty Cycle	V_{FB} = 0V	100			%
D_{MIN}	Minimum Duty Cycle	V_{FB} = 0.65V			0	%
SOFT START						
T_{SS}	Soft Start Time			1		ms
EN INPUT						
V_{EN_H}	EN Pin Threshold		1.5			V
V_{EN_L}					0.4	V

Typical Performance Curves -- (Efficiency in PSM)

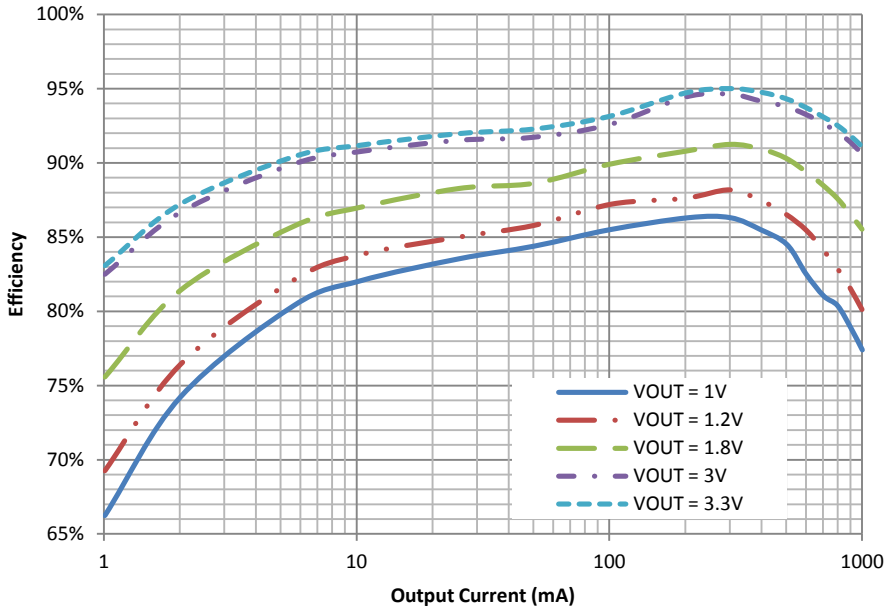


Figure 5 · **Efficiency vs. Output Current with 5V Input UDFN Package**

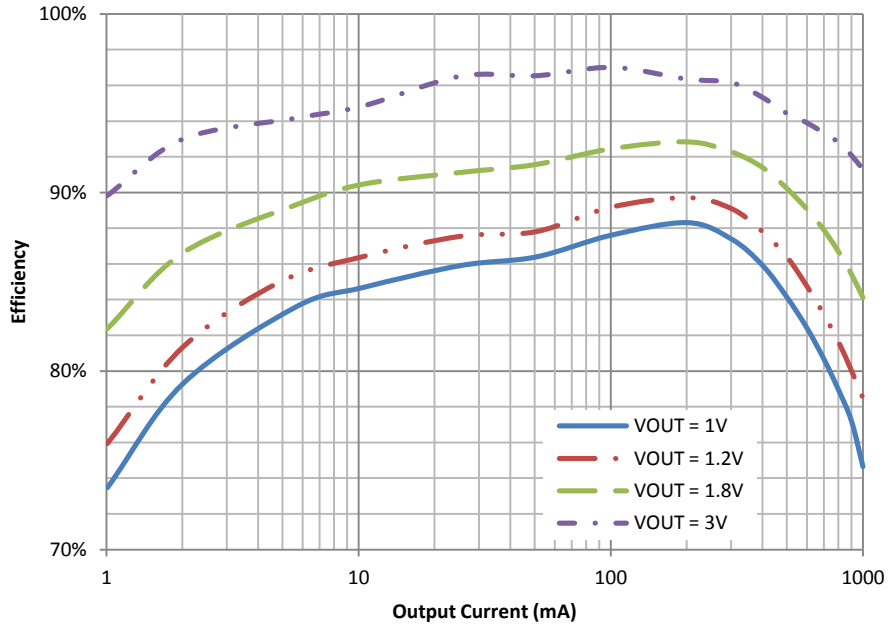


Figure 6 · **Output Voltage vs. Output Current with 3.3V Input UDFN Package**

Typical Performance Curves -- (VIN = 3.3V, V_{OUT} = 2.5V)

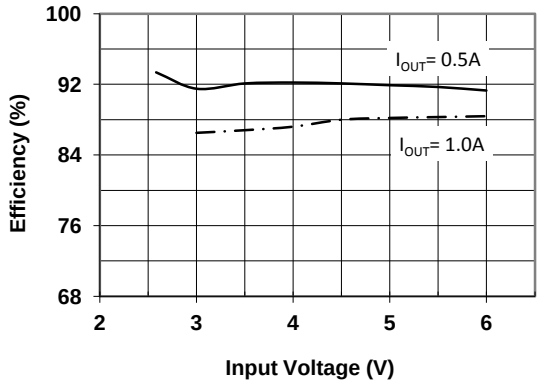


Figure 7 · **Efficiency vs. Input Voltage**

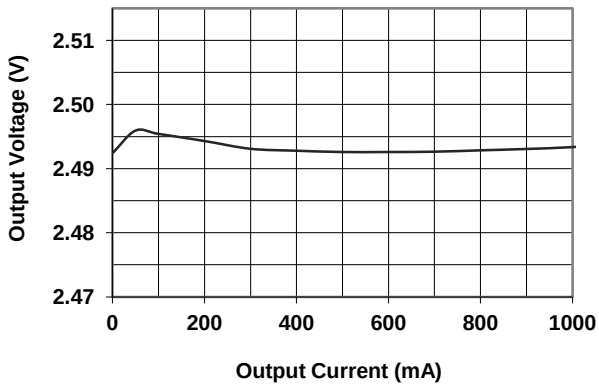


Figure 8 · **Output Voltage vs. Output Current**

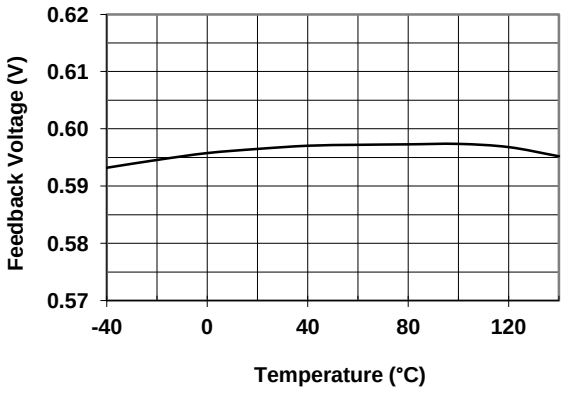


Figure 9 · **Feedback Voltage vs. Temperature**

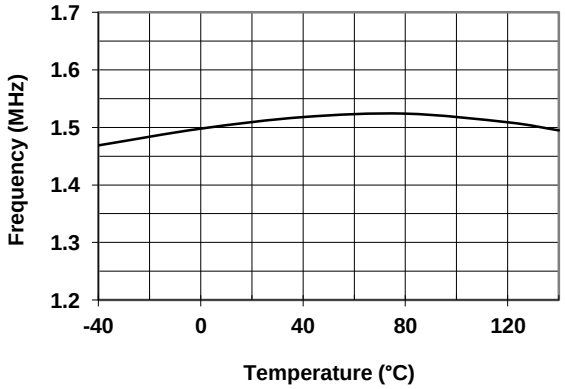


Figure 10 · **Frequency vs. Temperature**

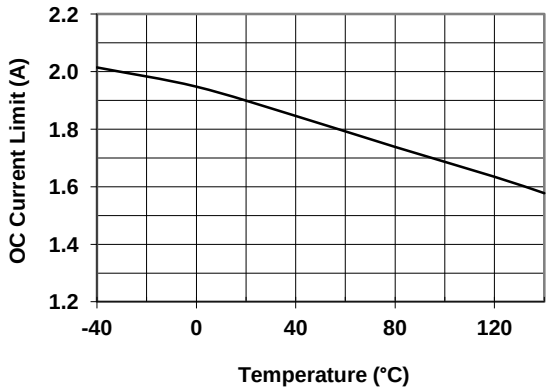


Figure 11 · **OCP Current Limit vs. Temperature**

Theory of Operation / Application Information

Basic Operation

The LX7186A is a synchronous step-down converter operating with a typically 1.4MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents and in power-saving mode (PSM) when operating at light load currents. It is capable of delivering a 1A output current over a wide input voltage range from 2.5 to 5.5V.

At the beginning of each cycle initiated by the clock signal (from the internal oscillator), the P-channel MOSFET switch is turned on, and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator also turns off the switch in case the current limit of the P-channel MOSFET is exceeded. Then the N-channel synchronous switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock signal again, turning off the N-channel synchronous switch and turning on the P-channel switch (See Figure 4).

Two operational modes are available: PSM and PWM. The internal synchronous rectifier with low R_{DSON} dramatically reduces conduction loss at PWM mode. No external Schottky diode is required in practical application. The LX7186A enters PSM at extremely light load condition. The equivalent switching frequency is reduced to increase the efficiency in PSM.

As the input supply voltage decreases to a value approaching the output voltage, the duty cycle increases to the maximum. Further reduction of the supply voltage forces the P-channel main switch to remain on for more than one cycle until it reaches 100% duty cycle. The output voltage will then be determined by the input voltage minus the voltage drop across the P-channel MOSFET and the inductor. This is particularly useful in battery powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range.

Typical Application

A general LX7186A application circuit is shown in Figure 12. External component selection is driven by the load requirement, and begins with the selection of the inductor L. Once L is chosen, C_{IN} and C_{OUT} can be selected.

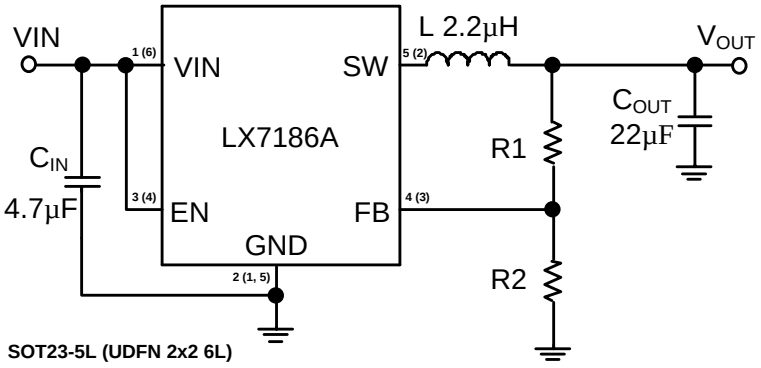


Figure 12 · **Typical Application**

Component Selection

Inductor Selection

Although the inductor does not influence the operating frequency, the inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L decreases with higher inductance and increases with higher VIN or V_{OUT}.

$$\Delta I_L = \frac{V_{OUT}}{f_{OSC} x\, L} \times \left(1 - \frac{V_{OUT}}{VIN}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple, greater core losses, and lower output current capability. A typical ΔI_L value is 20% to 40% of output current.

Another important parameter for the inductor is the current rating. Exceeding an inductor's maximum current rating may cause the inductor to saturate and overheat. Once the inductor value has been selected, the peak inductor current can be calculated as the following:

$$I_{PEAK} = I_{OUT} + V_{OUT} \times \frac{VIN - V_{OUT}}{2 \times f_{OSC} \times VIN \times L}$$

It should be ensured that the current rating of the selected inductor is 1.5 times of the I_{PEAK}.

Input Capacitor Selection

Because the buck converter has a pulsating input current, a low ESR input capacitor is required. This results in the best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. Also the input capacitor must be sufficiently large to stabilize the input voltage during heavy load transients. Ceramic capacitors show a good performance because of the low ESR value, and they are less sensitive to voltage transients and spikes. Place the input capacitor as close as possible to the input pin of the device for best performance. The typical value is about 4.7µF. The X5R or X7R ceramic capacitors have the best temperature and voltage characteristics, which is good for the input capacitor.

Output Capacitor Selection

The output capacitor is the most critical component of a switching regulator, it is used for output filtering and keeping the loop stable. The selection of C_{OUT} is driven by the required ESR to minimize voltage ripple and load step transients. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is determined by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{8 \times f_{OSC} \times C_{OUT}}\right)$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Once the ESR requirements for C_{OUT} have been met, the RMS current rating generally far exceeds the I_{RIPPLE} (P-P) requirement, except for an all ceramic solution. In most applications, a 22µF ceramic capacitor is usually enough for these conditions.

At light load currents, the device operates in PSM mode, and the output voltage ripple is independent of the output capacitor value. The output voltage ripple is set by the internal comparator thresholds. The typical output voltage ripple is 1% of the output voltage V_{OUT}.

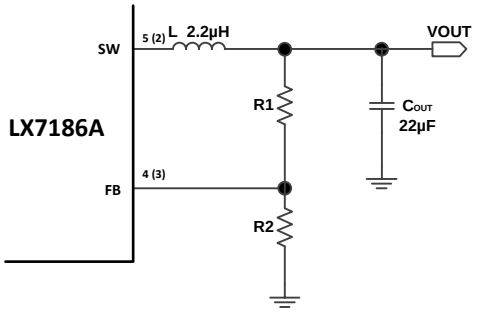
Feedback Divider Resistors

The LX7186A develops a 0.6V reference voltage between the feedback pin, FB, and the signal ground as shown in Figure 13. The output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} = 0.6 \times \left(1 + \frac{R1}{R2}\right)$$

Keeping the current small (<40µA) in these resistors maximizes efficiency, but making them too small (<20µA) may allow stray capacitance to cause noise problems and reduce the phase margin of the error amp loop.

The Output resistor divider values are recommended below.



V_{OUT}	R1	R2
0.9V	12.1k	24.3k
1.2V	24.3k	24.3k
1.8V	47.5k	24.3k
2.5V	76.8k	24.3k
3.0V	95.3k	24.3k
3.3V	107k	24.3k

Figure 13 · **Output Circuit**

Layout Consideration

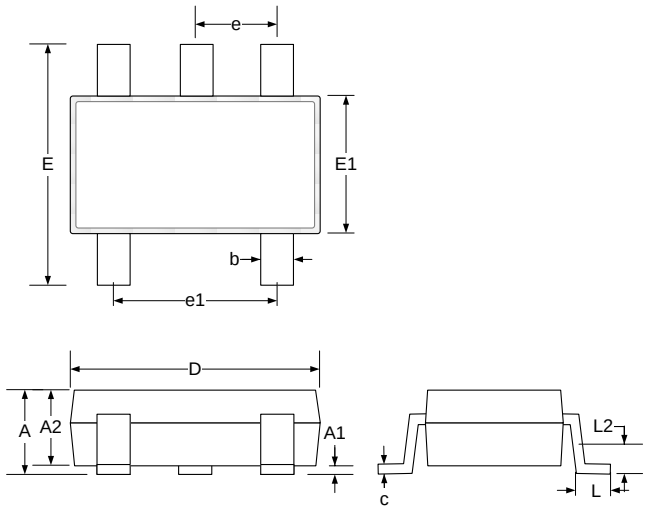
PCB layout is very important to the performance of the LX7186A. The traces where switching current flows should be kept as short as possible. The external components (especially C_{IN}) should be placed as close to the IC as physically possible, therefore use wide and short traces for the main current paths.

Try to route the feedback trace as far from the inductor and noisy power traces as possible. You should also make the feedback trace connection as direct as possible and of reasonable thickness. These two criteria sometimes involve a trade-off, but keeping the trace it away from the inductor and other noise sources is the more critical of the two. Locate the feedback divider resistor network near the feedback pin with short leads.

Flood all unused areas on all layers with copper. Flooding with copper will help to reduce the temperature rise of power components. These copper areas should be connected to one of the input supplies.

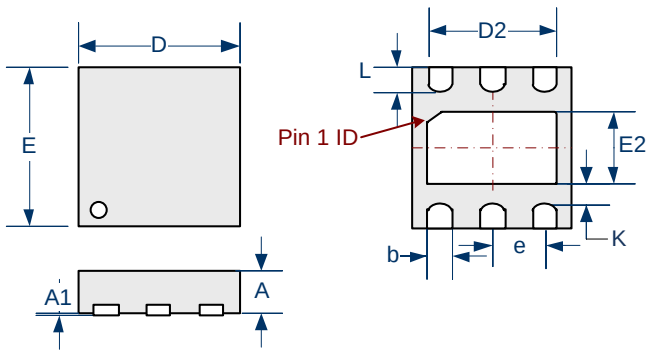
For detailed PCB layout consideration, please refer to LX7186A EVB User Guide.

Package Outline Dimensions



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.00	-	0.039
A1	0.01	0.10	0.0004	0.004
A2	0.84	0.90	0.033	0.035
b	0.30	0.45	0.012	0.018
C	0.12	0.20	0.005	0.008
D	2.90 BSC		0.114 BSC	
E	2.80 BSC		0.110 BSC	
E1	1.60 BSC		0.063 BSC	
e1	1.90 BSC		0.075 BSC	
e	0.95 BSC		0.037 BSC	
L	0.30	0.50	0.012	0.020
L2	0.25 BSC		0.010 BSC	

Figure 14 · **SG 5-Pin TSOT Package Dimensions**



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A		0.6		0.024
A1	0.00	0.05	0.000	0.002
K	0.15 MIN		0.006MIN	
e	0.65 BSC		0.026 BSC	
L	0.25	0.35	0.010	0.014
b	0.25	0.35	0.010	0.014
D2	1.35	1.55	0.059	0.067
E2	0.90	1.10	0.031	0.039
D	2.00 BSC		0.079 BSC	
E	2.00 BSC		0.079 BSC	

Figure 15 · **LU 6-Pin Plastic UDFN 2mm x 2mm x 0.6mm Package Dimensions**

Note: 1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006”) on any side. Lead dimension shall not include solder coverage.

Note: 2. Dimensions are in mm, inches are for reference only.

Land Pattern Recommendation

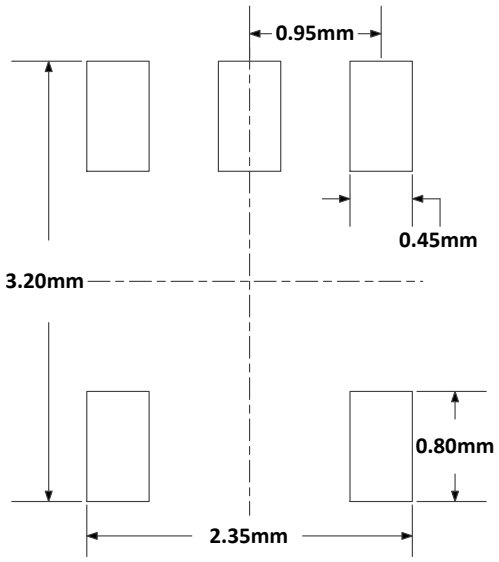


Figure 16 · **SG 5-Pin TSOT Package Footprint**

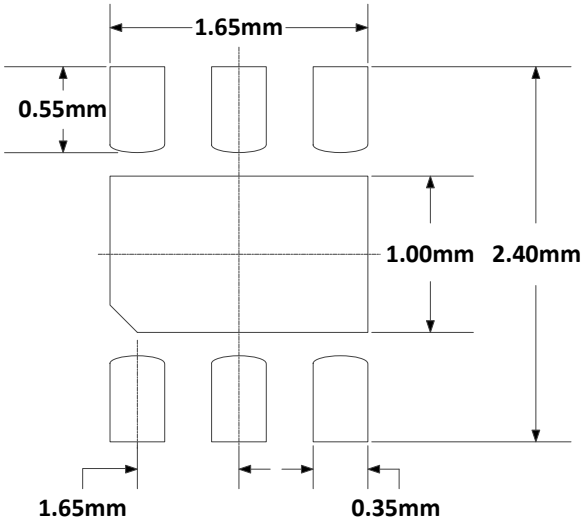


Figure 17 · **LU 6-Pin UDFN Package Footprint**

Disclaimer:
This PCB land pattern recommendation is based on information available to Microsemi by its suppliers. The actual land pattern to be used could be different depending on the materials and processes used in the PCB assembly, end user must account for this in their final layout. Microsemi makes no warranty or representation of performance based on this recommended land pattern.

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1(949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor solutions for: aerospace, defense and security; enterprise and communications; and industrial and alternative energy markets. Products include high-performance, high-reliability analog and RF devices, mixed signal and RF integrated circuits, customizable SoCs, FPGAs, and complete subsystems. Microsemi is headquartered in Aliso Viejo, Calif. Learn more at **www.microsemi.com**.