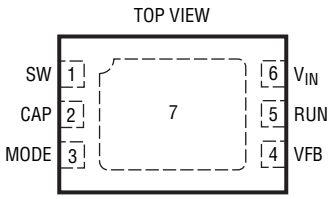
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} Voltage ..... –0.3V to 6V
RUN, V_{FB}, MODE, CAP Voltages ..... –0.3V to V_{IN}
SW Voltage ..... –0.3V to (V_{IN} + 0.3V)
Operating Temperature Range (Note 2) .... –40°C to 85°C
Junction Temperature (Note 3) ..... 125°C
Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



DCB PACKAGE
6-LEAD (2mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 64°C/W
EXPOSED PAD (PIN 7) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3543EDCB#PBF	LTC3543EDCB#TRPBF	LCCK	6-Lead (2mm × 3mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RUN	Run Threshold			0.3	1	1.5	V
V_{FB}	Regulated Feedback Voltage	(Note 4)	●	0.588	0.6	0.612	V
I_{VFB}	Feedback Pin Current					50	nA
I_{PK}	Peak Inductor Current	V_{IN} = 3.6V, V_{FB} = 0V		0.7	1	1.3	A
$V_{LOADREG}$	Output Voltage Load Regulation				0.5		%/mA
$V_{LINEREG}$	Output Voltage Line Regulation	(Note 4)				0.5	%/V
V_{IN}	Input Voltage Range		●	2.5		5.5	V
I_S	Input DC Bias Current Active Mode Sleep Mode Shutdown	(Note 5) V_{OUT} = 90%, I_{LOAD} = 0A V_{OUT} = 103%, I_{LOAD} = 0A V_{RUN} = 0V, V_{IN} = 5.5V			 375 45 0.1	 500 70 1	 µA µA µA
f_{OSC}	Nominal Oscillator Frequency		●	1.80	2.25		MHz
R_{PFET}	$R_{DS(ON)}$ of P-Channel FET	I_{SW} = 100mA			0.45		Ω
R_{NFET}	$R_{DS(ON)}$ of N-Channel FET	I_{SW} = 100mA			0.35		Ω
I_{SW}	SW Leakage	V_{RUN} = 0V, V_{SW} = 0V or 5.5V, V_{IN} = 5.5V				±1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3543E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature ranges are assured by design, characterization and correlation with statistical process controls.

ELECTRICAL CHARACTERISTICS

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula: $T_J = T_A + (P_D)(64°C/W)$

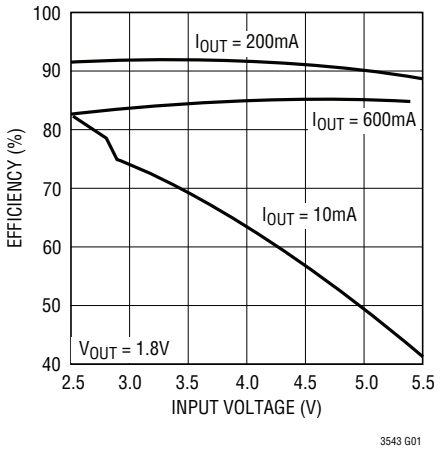
Note 4: The LTC3543 is tested in a proprietary test mode that connects V_{FB} to the output of the error amplifier. This test mode is equivalent to continuous mode operation.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

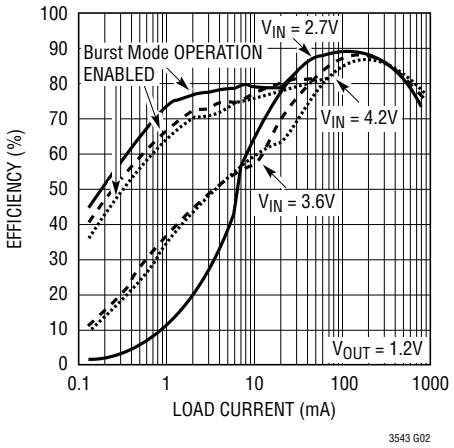
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C unless otherwise noted. (From Figure 1a)

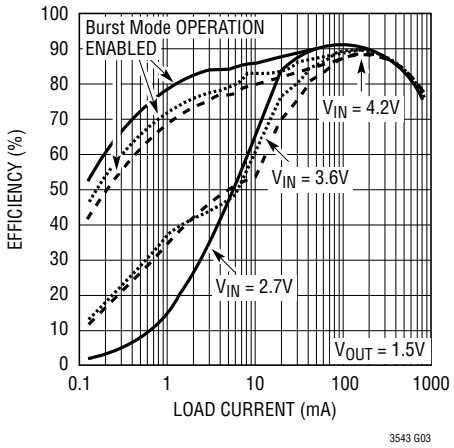
Efficiency vs Input Voltage (V_{IN})



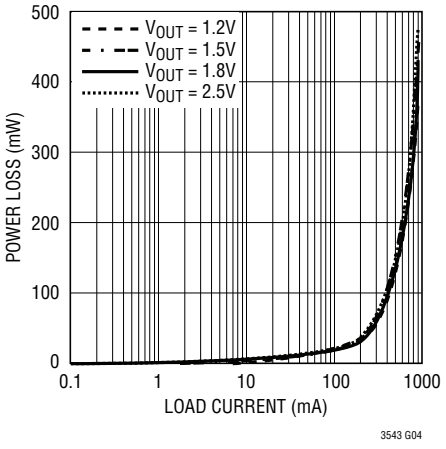
Efficiency vs Load Current



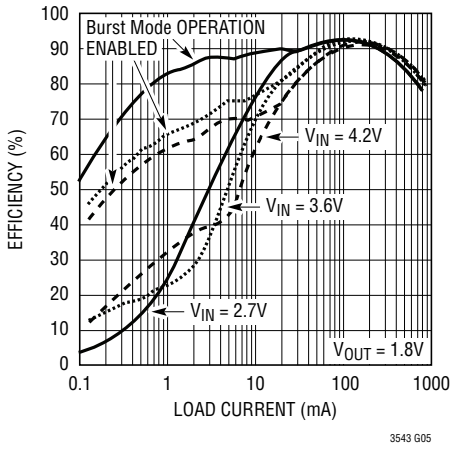
Efficiency vs Load Current



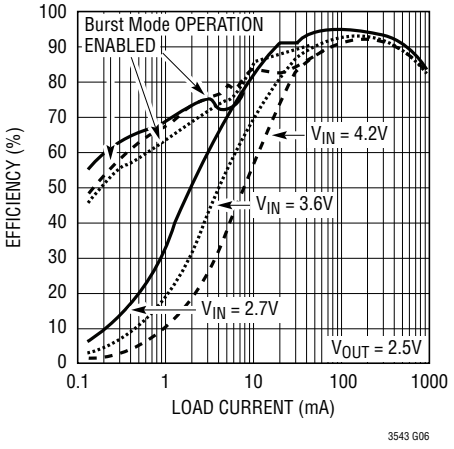
Power Loss vs Load Current



Efficiency vs Load Current

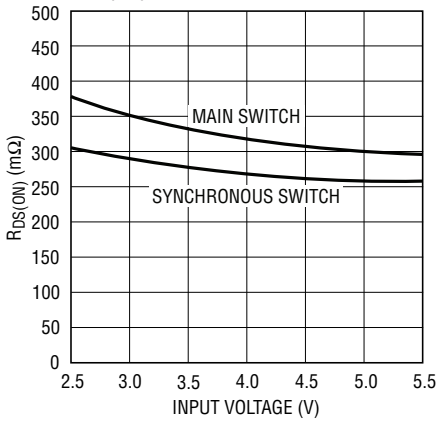


Efficiency vs Load Current



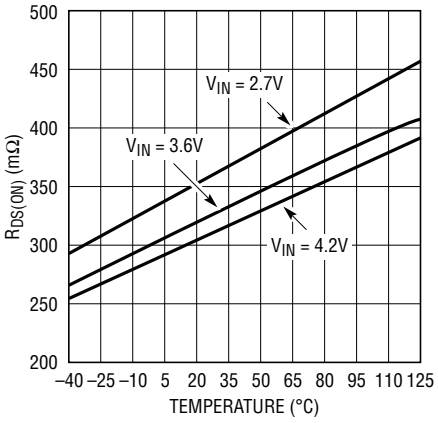
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

$R_{DS(ON)}$ vs Input Voltage (V_{IN})



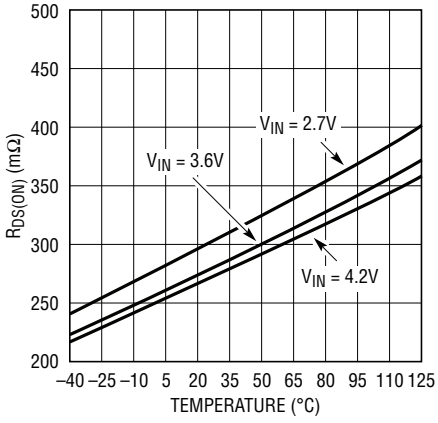
3543 G07

Main Switch Resistance vs Temperature



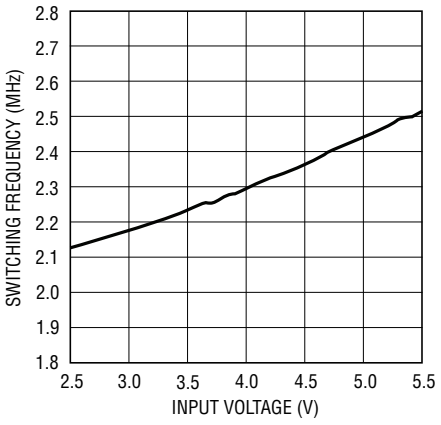
3543 G08

Synchronous Switch Resistance vs Temperature



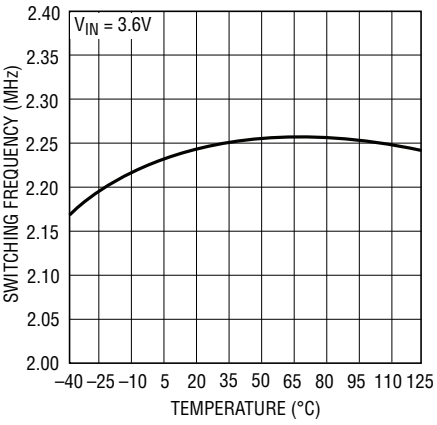
3543 G09

Switching Frequency vs Input Voltage (V_{IN})



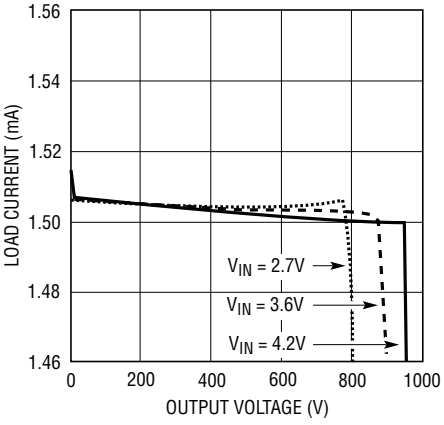
3543 G10

Switching Frequency vs Temperature



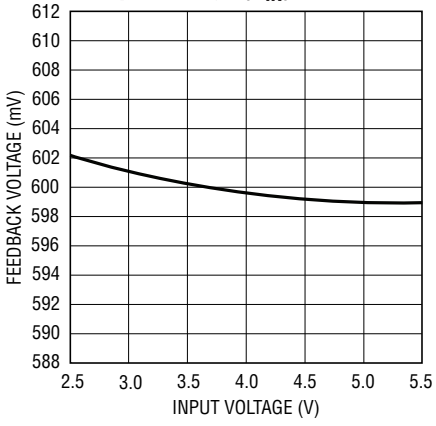
3543 G11

Output Voltage vs Load Current



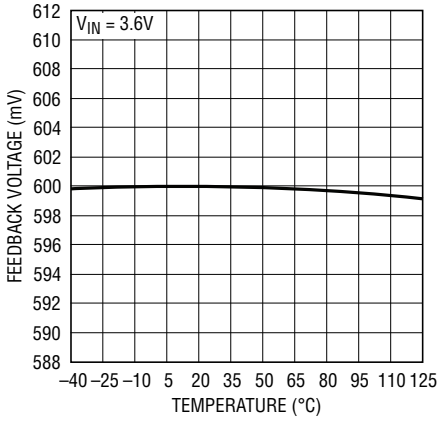
3543 G12

Feedback Voltage (V_{FB}) vs Input Voltage (V_{IN})



3543 G13

Feedback Voltage (V_{FB}) vs Temperature

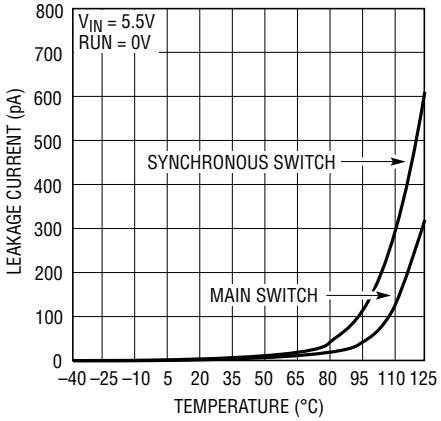


3543 G14

TYPICAL PERFORMANCE CHARACTERISTICS

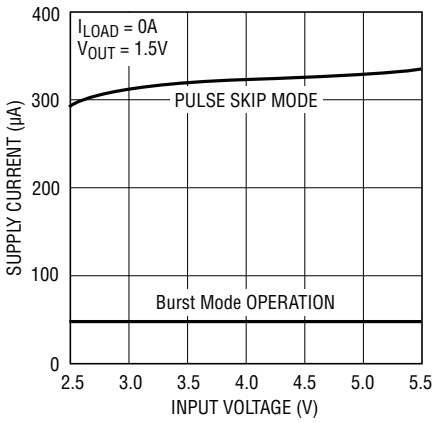
T_A = 25°C, unless otherwise noted.

Switch Leakage (I_{SW}) vs Temperature



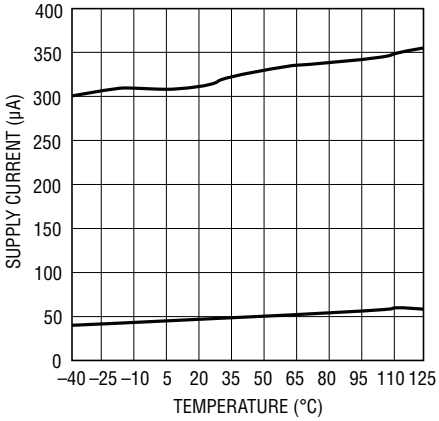
3543 G15

Dynamic Supply Current vs Input Voltage (V_{IN})



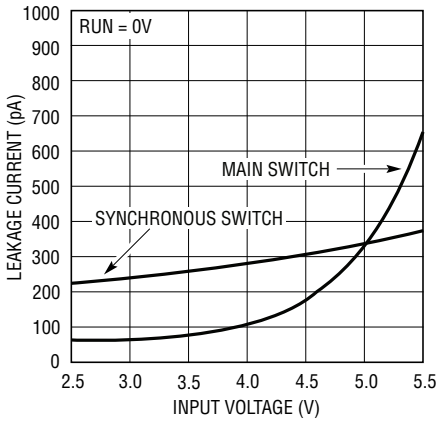
3543 G16

Dynamic Supply Current vs Temperature



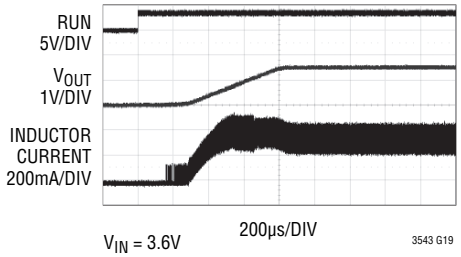
3543 G17

Switch Leakage (I_{SW}) vs Input Voltage (V_{IN})



3543 G18

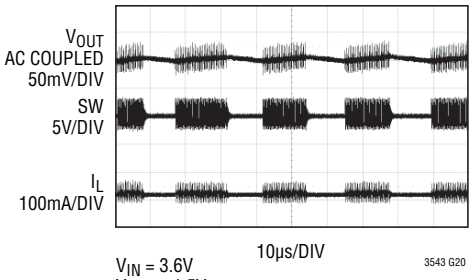
Start-Up from Shutdown



3543 G19

V_{IN} = 3.6V
V_{OUT} = 1.5V
I_{LOAD} = 300mA

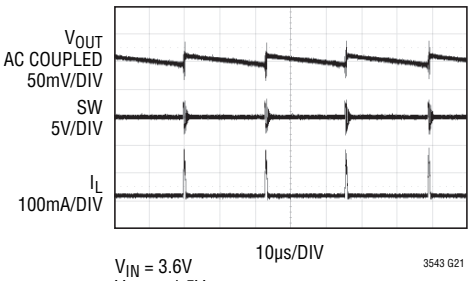
Pulse Skip Operation



3543 G20

V_{IN} = 3.6V
V_{OUT} = 1.5V
I_{LOAD} = 3mA
V_{MODE} = 3.6V

Burst Mode Operation

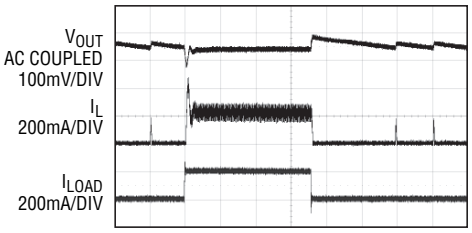


3543 G21

V_{IN} = 3.6V
V_{OUT} = 1.5V
I_{LOAD} = 3mA
V_{MODE} = 0V

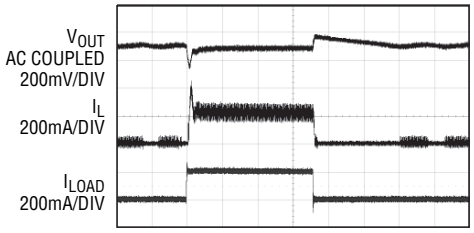
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Load Step



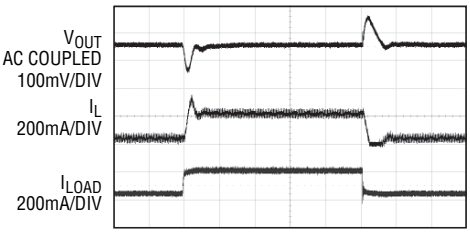
V_{IN} = 3.6V
V_{OUT} = 1.5V
I_{LOAD} = 3mA TO 200mA
V_{MODE} = 0V

Load Step



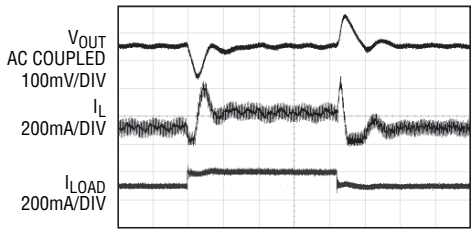
V_{IN} = 3.6V
V_{OUT} = 1.5V
I_{LOAD} = 3mA TO 200mA
V_{MODE} = 3.6V

Load Step



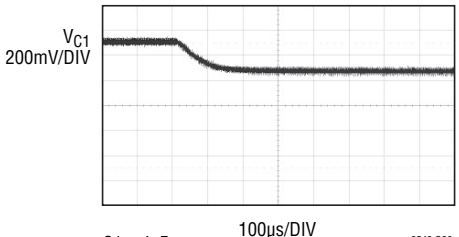
V_{IN} = 3.6V
V_{OUT} = 1.5V
I_{LOAD} = 100mA TO 600mA
V_{MODE} = 3.6V

Spread Spectrum Load Step



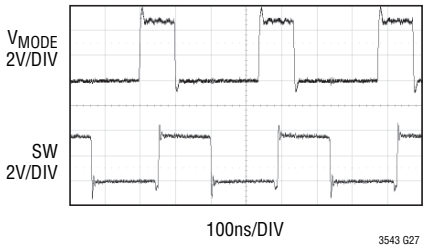
V_{IN} = 3.6V
V_{OUT} = 1.5V
I_{LOAD} = 100mA TO 200mA
V_{MODE} = 0.6V

PLL Operation



C1 = 4µF
3MHz TO 1MHz STEP

PLL Operation at 3MHz



PIN FUNCTIONS

SW (Pin 1): Switch Node Connector to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.

CAP (Pin 2): Capacitor used for smoothing out spread spectrum or for PLL response. Connect to a capacitor whose other plate is connected to GND, or allow the pin to float. Value = 1nF – 10nF.

MODE (Pin 3): Mode Selection Pin. Connect as follows to invoke desired operation: MODE = GND → Burst Mode operation, MODE = V_{FB} → Pulse skip with spread spectrum, MODE = V_{IN} → Pulse skip, MODE = External clock → PLL mode.

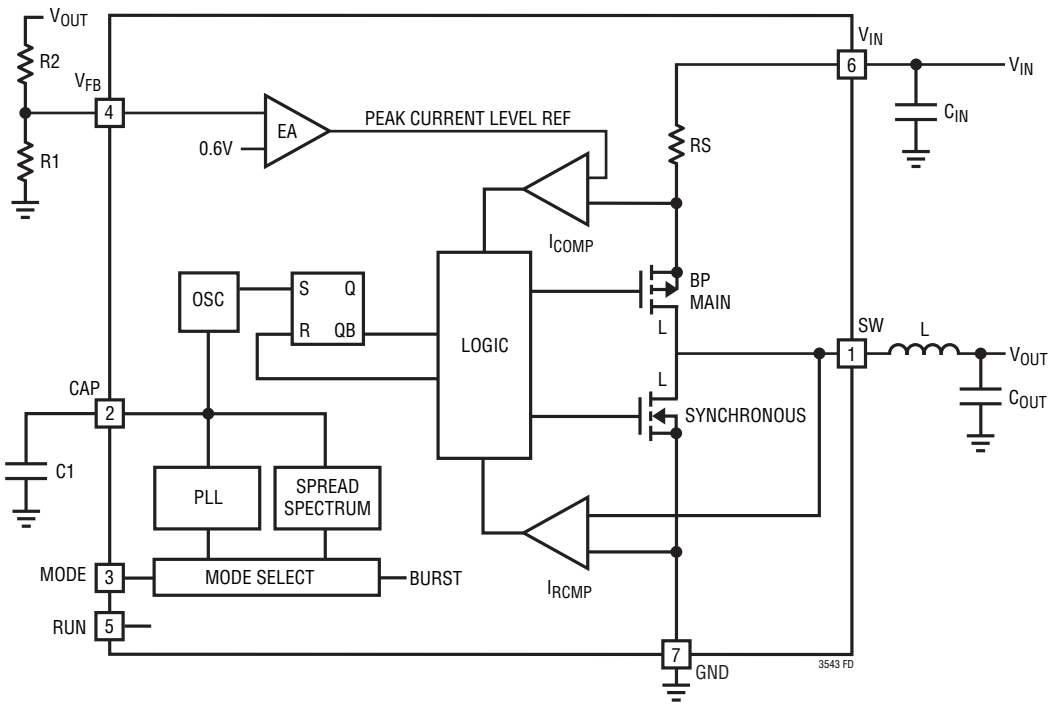
V_{FB} (Pin 4): Feedback sensing pin for the external feedback resistors.

RUN (Pin 5): Run Control Input. Forcing pin above 1.5V enables the part. Forcing the pin below 0.3V shuts down the device. In shutdown, all functions are disabled, drawing <1µA of supply current. Do not leave the RUN pin floating.

V_{IN} (Pin 6): Main Supply Pin.

Exposed Pad (Pin 7): Exposed Pad connected to ground.

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC3543 uses current mode step-down architecture with both the main (P-channel MOSFET) and synchronous (N-channel MOSFET) switches internal. During normal operation, the internal top power MOSFET is turned on each cycle as the oscillator sets the RS latch, and turned off when the current comparator, I_{COMP}, resets the RS latch. The peak inductor current at which I_{COMP} resets the RS latch, is controlled by the output of error amplifier, EA. When the load current increases, it causes a slight decrease in the feedback voltage, V_{FB}, relative to an internal reference voltage which, in turn, causes the EA amplifier's output voltage to increase until the average inductor current matches the new load current. While the top MOSFET is off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current reversal comparator I_{RCMP}, or the beginning of the next clock cycle.

Burst Mode Operation

The LTC3543 is capable of Burst Mode operation in which the internal power MOSFETs operate intermittently based on load demand. Burst Mode operation is enabled by connecting the MODE pin to ground.

During Burst Mode operation, the LTC3543's internal circuits sense when the inductor peak current falls below 100mA. When below this level, the power MOSFETs and any unneeded circuitry are turned off, reducing the quiescent current to 45µA, and holding the peak current reference level at 100mA. The LTC3543 remains in this sleep state until the feedback voltage falls below its internal reference. Once this occurs, the regulator wakes up and allows the inductor to develop 100mA current pulses. In light loads, this will cause the output voltage to increase and the internal peak current reference to decrease. When the peak current reference falls to below 100mA, the part re-enters sleep mode and the cycle is repeated. This process repeats at a rate dependent on the load demand.

Pulse Skip Mode Operation

Connecting the MODE pin to V_{IN} places the LTC3543 in pulse skip mode. During light loads, the inductor can reach zero amps or reverse current on each pulse. This is caused by the bottom MOSFET being turned off by the current reversal comparator, I_{RCMP}, at which time the switch voltage will ring. This is discontinuous mode operation, and is normal behavior for a switching regulator. At very light loads, the LTC3543 will automatically skip pulses in order to maintain output regulation.

Spread Spectrum Operation

Setting the MODE pin from 0.55V to 0.8V will place the part in pulse skip mode with spread spectrum; an easy way to do this is to connect the MODE pin to the V_{FB} pin. In this mode, an external capacitor is required between CAP and GND. The external capacitor assists in smoothing frequency transitions.

The spread spectrum architecture randomly varies the LTC3543's switching frequency from 2MHz to 3MHz, significantly reducing the peak radiated and conducting noise on both the input and output supplies, making it easier to comply with electromagnetic interference (EMI) standards.

Switching regulators can be particularly troublesome in applications where electromagnetic interference (EMI) is a concern. Switching regulators operate on a cycle-by-cycle basis to transfer power to an output. In most cases, the frequency of operation is either fixed or constant, based on the output load. This method of conversion creates large components of noise at the frequency of operation (fundamental) and multiples of the operating frequency (harmonics). Figure 1a depicts the output noise spectrum of a conventional buck switching converter (LTC3543 with spread spectrum operation disabled) with V_{IN} = 3.6V, V_{OUT} = 1.5V and I_{OUT} = 300mA.

OPERATION

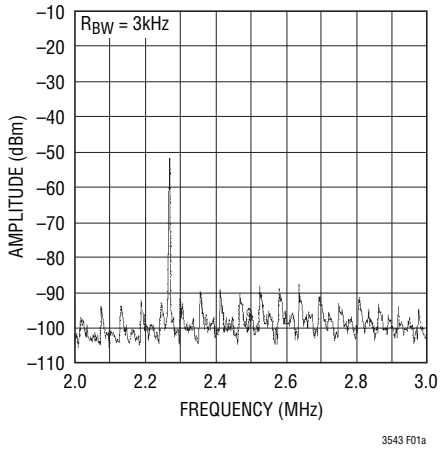


Figure 1a. Output Noise Spectrum of Conventional Buck Switching Converter (LTC3543 with Spread Spectrum Disabled) Showing Fundamental and Harmonic Frequencies

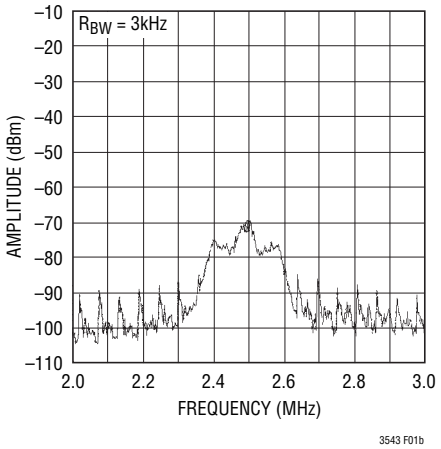


Figure 1b. Output Noise Spectrum of the LTC3543 Spread Spectrum Buck Switching Converter. Note the Reduction in Fundamental and Harmonic Peak Spectral Amplitude Compared to Figure 1a.

Unlike conventional buck converters, the LTC3543's internal oscillator is designed to produce a clock pulse whose frequency is randomly varied between 2MHz and 3MHz. This has the benefit of spreading the switching noise over a range of frequencies, significantly reducing the peak noise. Figure 1b shows the output noise spectrum of the LTC3543 (with spread spectrum operation enabled) with V_{IN} = 3.6V, V_{OUT} = 1.5V and I_{OUT} = 300mA. Note the significant reduction in peak output noise (≅ 20dBm).

Phase-Locked Loop Operation

A phase-locked loop (PLL) is available on the LTC3543 to synchronize the internal oscillator to an external clock source that is connected to the MODE pin. In this case, an external capacitor should be connected between the CAP pin and GND to serve as part of the PLL's loop filter. The LTC3543's phase detector adjusts the voltage on the CAP pin to align the turn-on of the internal P-channel MOSFET to the rising edge of the synchronizing signal. Note that when the MODE pin is not being driven by an external clock source, the MODE pin must be held to one of the following voltage potentials: V_{IN}, GND, or V_{FB}.

The typical capture range of the LTC3543 's PLL is guaranteed over temperature to be 1MHz to 3MHz. In other words, the LTC3543's PLL is guaranteed to lock to an external clock source whose frequency is between 1MHz and 3MHz.

Selecting the switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

Note that the PLL is inhibited during soft-start and uses the internal 2.25MHz frequency until regulation is established. Also the regulator is in pulse skip mode during PLL operation.

Short-Circuit Protection

When the output is shorted to ground, the LTC3543 senses the high inductor current and disallows the main power FET from turning on. The main FET is held off until the inductor current decays to a normal level.

Dropout Operation

Depending upon the external feedback resistor ratio, it is possible for V_{IN} to approach the output voltage level. As the input supply voltage decreases to a value approaching the output voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle until it reaches 100% duty cycle. The output voltage will then be determined by the input voltage minus the voltage drop across the P-channel MOSFET and the inductor.

OPERATION

An important detail to remember is that at low input supply voltages, the $R_{DS(ON)}$ of the P-channel switch increases (see the Typical Performance Characteristics section). Therefore, the user should calculate the power dissipation when the LTC3543 is used at 100% duty cycle with low input voltage (see Thermal Considerations in the Applications Information section).

Low Supply Operation

The LTC3543 will operate with input supply voltages as low as 2.5V, but the maximum allowable output current is reduced at this low voltage. Figure 2 shows the reduction in the maximum output current as a function of input voltage for various output voltages.

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant-frequency architectures by preventing subharmonic oscillations at high duty cycles. It is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 40%. Normally, this results in a reduction of maximum inductor peak current for duty cycles >40%; however, the LTC3543 uses a patent pending scheme that counteracts this compensating ramp, allowing the maximum inductor peak current to remain unaffected throughout all duty cycles.

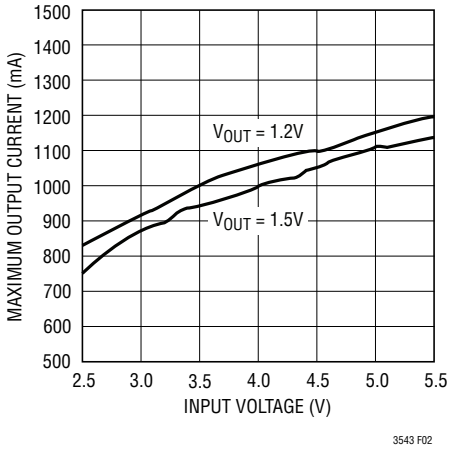


Figure 2. Maximum Output Current vs Input Voltage (V_{IN})

APPLICATIONS INFORMATION

The basic LTC3543 application circuit is shown on the front page of this data sheet. External component selection is driven by the load requirement and begins with the selection of L followed by C_{IN} and C_{OUT}.

Inductor Selection

For most applications, the value of the inductor will fall in the range of 1µH to 4.7µH. Its value is chosen based on the desired ripple current. Large value inductors lower ripple current, and small value inductors result in higher ripple currents. Higher V_{IN} or V_{OUT} also increases the ripple current, as shown in Equation 1. A reasonable starting point for setting ripple current is ΔI_L = 130mA 20% $I_{LOAD(MAX)}$.

$$\Delta I_L = \frac{V_{OUT}}{f \bullet L} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (1)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 665mA rated inductor should be enough for most applications (600mA + 65mA). For better efficiency, choose a low DC-resistance inductor.

The inductor value also has an effect on Burst Mode operation. The transition to low current operation begins when the inductor current peaks fall to approximately 100mA. Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to increase.

Inductor Core Selection

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and do not radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs size requirements, and any radiated field/EMI requirements, than on what the LTC3543 requires to operate. Table 1 shows some typical surface mount inductors that work well in LTC3543 applications.

Table 1. Representative Surface Mount Inductors

MANUFACTURER	PART NUMBER	VALUE (µH)	MAX DC CURRENT (A)	DCR (mΩ)	HEIGHT (mm)
TDK	VLF3010AT-2R2M1R0	2.2	1.0	100	1.0
	VLF3012AT-2R2M1R0	2.2	1.0	88	1.2
	VLCF4020T-2R2N1R7	2.2	1.7	54	2.0
	VLCF5020-2R7N1R7	2.7	1.7	58	2.0
	VLCF5020-3R3N1R6	3.3	1.6	69	2.0
	VLCF5020-4R7N1R4	4.7	1.4	79	2.0
Sumida	CDRH2D18/HP-2R2NC	2.2	1.6	48	2.0
Taiyo Yuden	NR4018T4R7M	4.7	1.7	90	1.8
	NP03SB4R7M	4.7	1.2	47	1.8
CoEv	DN4835-2R2	2.2	2.6	47	3.5
	DN4835-3R3	3.3	2.43	58	3.5
	DN4835-6R8	6.8	1.41	117	3.5
Murata	LQH32CN2R2M33	2.2	0.79	97	3.2
	LQH55DN2R2M03	2.2	3.2	29	4.7
	LQH55DN3R3M03	3.3	2.9	36	4.7
	LQH55DN4R7M03	4.7	2.7	41	4.7

APPLICATIONS INFORMATION

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{required}\ I_{RMS} \cong I_{O(MAX)} \bullet \frac{[V_{OUT}(V_{IN}-V_{OUT})]^{1/2}}{V_{IN}} \quad (2)$$

This formula has a maximum of $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there are any questions.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically, once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right) \quad (3)$$

where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalum. These are specially constructed and tested for low ESR so they give the lowest ESR for a given volume. Other capacitor types include the Sanyo POSCAP, the Kemet T510 and T495 series, and the Sprague 593D and 595D series. Consult the manufacturer for other specific recommendations.

C1 Selection

When spread spectrum operation is enabled, the frequency of the LTC3543 is randomly varied over the range of frequencies between 2MHz and 3MHz. In this case, a capacitor should be connected between the CAP pin and GND to smooth out the changes in frequency. This not only provides a smoother frequency spectrum but also ensures that the switching regulator remains stable by preventing abrupt changes in frequency.

When the PLL mode is enabled, if the external clock frequency is greater than the internal oscillator's frequency (OSC), then current is sourced continuously, pulling up the voltage on the CAP pin. If the external clock frequency is less than OSC, current is sunk continuously, pulling down the voltage on the CAP pin. When the external and internal frequencies are the same but exhibit a phase difference, current pulses (sourcing or sinking) are used for an amount of time corresponding to the phase difference. The current pulses adjust the voltage on the CAP pin until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the CAP pin is high impedance and the external capacitor holds the voltage. The external cap is used by the PLL's loop filter to help smooth out the voltage change and provide a stable input to the voltage-controlled oscillator. The value of C1 will determine how fast the loop acquires lock. Typically C1 is 1nF to 10nF in PLL mode. A value of 2.2nF is suitable in most applications.

APPLICATIONS INFORMATION

Using Ceramic Capacitors for C_{IN}, C_{OUT} and C1

High value, low cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. Because the LTC3543's control loop does not depend on the output capacitor's ESR for stable operation, ceramic capacitors can be used freely to achieve very low output ripple and small circuit size.

However, care must be taken when ceramic capacitors are used at the input and the output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. This ringing can couple to the output and be mistaken as loop instability. Even worse, the sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN}, large enough to damage the part.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Output Voltage Programming

The output voltage is set by a resistor divider according to the following formula:

$$V_{OUT} = 0.6V \bullet \left(1 + \frac{R2}{R1}\right) \quad (4)$$

The external resistor divider is connected to the output allowing remote voltage sensing as shown in Figure 3.

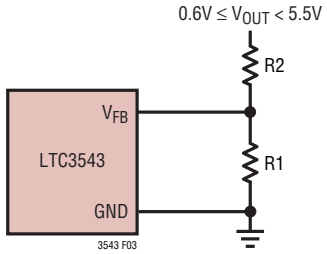


Figure 3. Setting Output Voltage

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses in LTC3543 circuits: V_{IN} quiescent current and I^2R losses. The V_{IN} quiescent current loss dominates the efficiency loss at very low load currents whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence as illustrated in Figure 4.

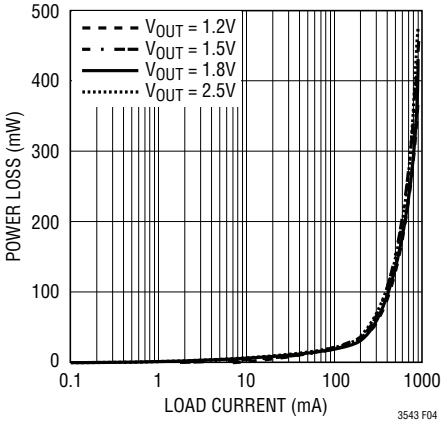


Figure 4. Power Loss vs Load Current

APPLICATIONS INFORMATION

1. The V_{IN} quiescent current is due to two components: the DC bias current as given in the Electrical Characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge, dQ, moves from V_{IN} to ground. The resulting dQ/dt is the current out of V_{IN} that is typically larger than the DC bias current. In continuous mode, $I_{GATECHG} = f(QT + QB)$ where QT and QB are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.

2. I^2R losses are calculated from the resistances of the internal switches, R_{SW}, and external inductor RL. In continuous mode, the average output current flowing through inductor L is "chopped" between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = (R_{DS(ON)TOP} \bullet DC) + (R_{DS(ON)BOT} \bullet (1 - DC))$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses, simply add R_{SW} to RL and multiply the result by the square of the average output current.

Other losses, including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses, generally account for less than 2% total additional loss.

Thermal Considerations

In most applications, the LTC3543 does not dissipate much heat due to its high efficiency. But, in applications where the LTC3543 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 150°C, both power switches will be turned off and the SW node will become high impedance.

To avoid the LTC3543 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_R = \theta_{JA} \bullet P_D$$

where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the temperature.

The junction temperature, T_J, is given by:

$$T_J = T_A + T_R$$

where T_A is the ambient temperature.

As an example, consider the LTC3543 in dropout at an input voltage of 2.7V, an ambient temperature of 80°C, and a load current of 600mA. From the typical performance graph of switch resistance, the $R_{DS(ON)}$ of the P-channel switch at 80°C is approximately 0.41Ω. There, power dissipated by the part is:

$$P_D = I_{LOAD}^2 \bullet R_{DS(ON)} = 147.6mW$$

For the DFN package, the θ_{JA} is 64°C/W. Thus, the junction temperature of the regulator is:

$$T_J = 80°C + 0.1476 \bullet 64 = 89.4°C$$

which is well below the maximum junction temperature of 125°C. Note that at higher supply voltages, the junction temperature is lower due to reduced switch resistance ($R_{DS(ON)}$).

APPLICATIONS INFORMATION

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to (ΔI_{LOAD} • ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, which generates a feedback error signal.

The regulator loop then acts to return V_{OUT} to its steady state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem. For a detailed explanation of the switching control loop theory, see Application Note 76.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately 25 • C_{LOAD}. Thus, a 10µF capacitor charging to 3.3V would require a 250µs rise time, limiting the charging current to about 130mA.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3543. These items are also illustrated graphically in Figures 5 and 6. Check the following in your layout:

1. The power traces, consisting of the GND trace, the SW trace, and the V_{IN} trace should be kept short, direct and wide.
2. Does the V_{FB} pin connect directly to the feedback voltage reference? Ensure that there is no load current running from the feedback reference voltage and the V_{FB} pin.
3. Does the (+) plate of C_{IN} connect to V_{IN} as closely as possible? This capacitor provides the AC current to the internal power MOSFETs.
4. Keep the switching node, SW, away from the sensitive V_{FB} node.
5. Keep the (–) plates of C_{IN} and C_{OUT} as close as possible.

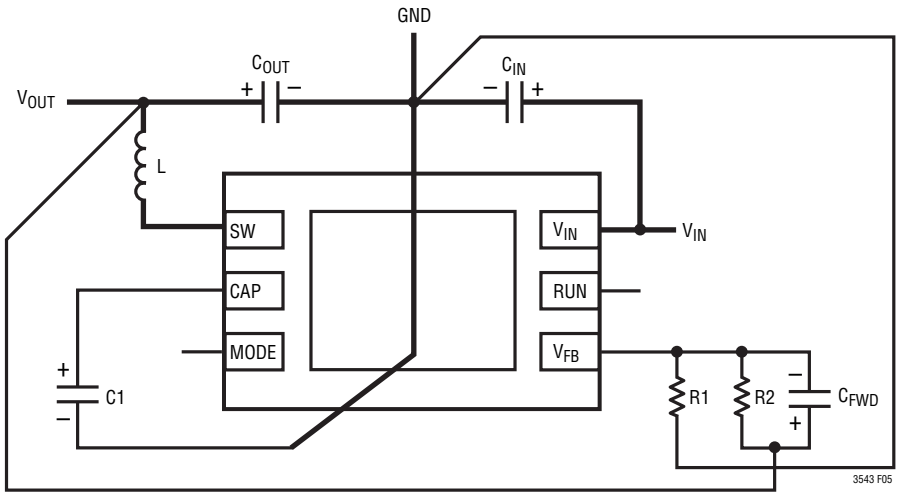


Figure 5. LTC3543 Layout Diagram

APPLICATIONS INFORMATION

Design Example

As a design example, assume the LTC3543 is used in a single lithium-ion battery-powered cellular phone application. The V_{IN} will be operating from a maximum of 4.2V down to about 2.7V. The load current requirement is a maximum of 600mA, but most of the time it will be in standby mode, requiring only 2mA. Efficiency at both low and high load currents is important. Output voltage is 1.5V. With this information we can calculate L using Equation 1,

$$L = \frac{V_{OUT}}{f \bullet \Delta I_L} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

A 3.3µH inductor works well for this application, yielding a ripple current of only 130mA. For best efficiency choose a 665mA or greater inductor with less than 0.05Ω series resistance.

In Equation 2, C_{IN} will require an RMS current rating of at least 0.3A at $I_{LOAD(MAX)}/2$ at temperature.

Using Equation 3, Selecting a 4.7µF capacitor with an ESR of 0.05Ω for C_{OUT} yields an 8mV voltage ripple on the regulated output voltage.

For feedback resistors, choose R1 = 402k. R2 can then be calculated using Equation 4.

$$R2 = \left(\frac{V_{OUT}}{0.6V} - 1\right) \bullet R1 = 604k$$

Figure 6 shows the complete circuit along with its efficiency curve.

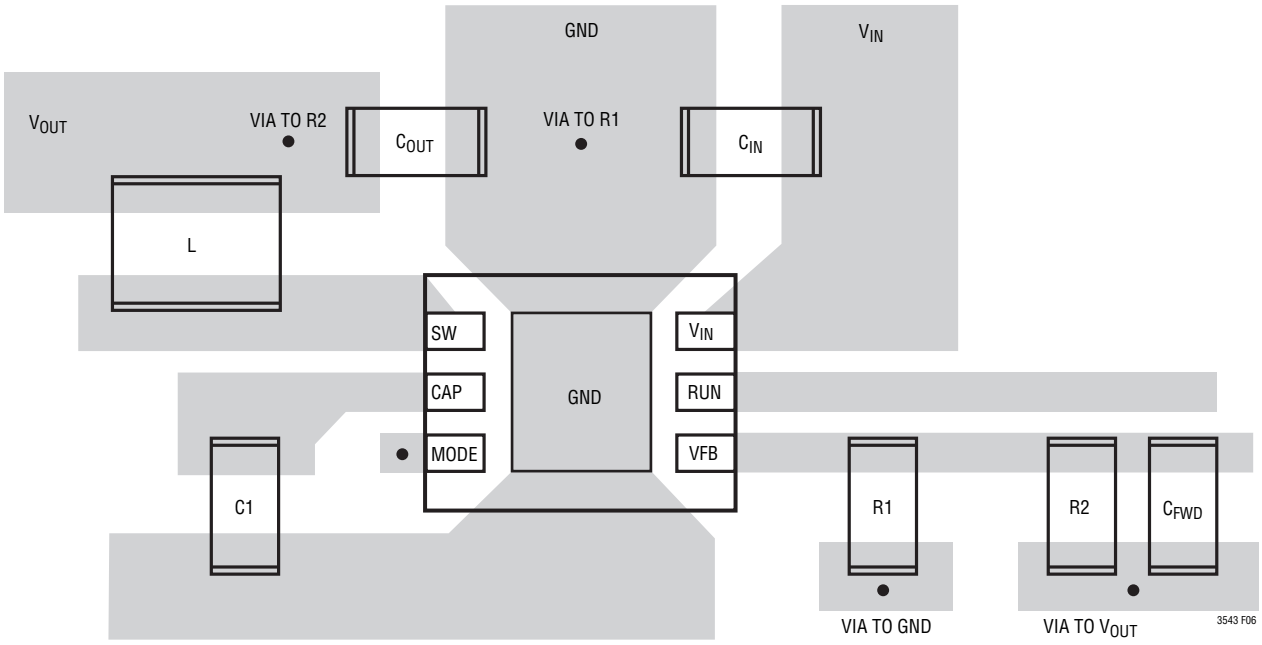
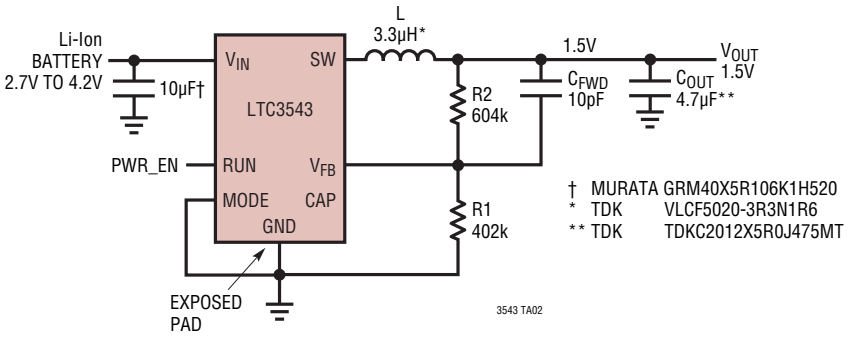
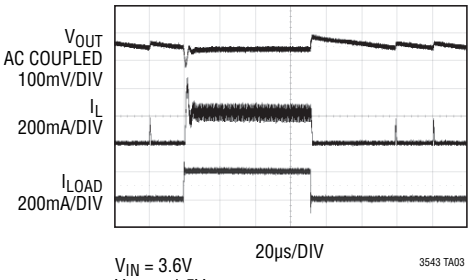


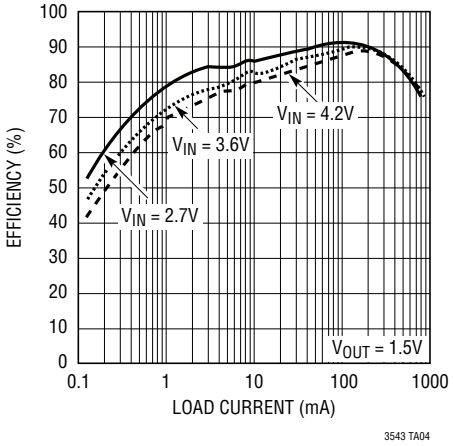
Figure 6. LTC3543 Suggested Layout

TYPICAL APPLICATIONS



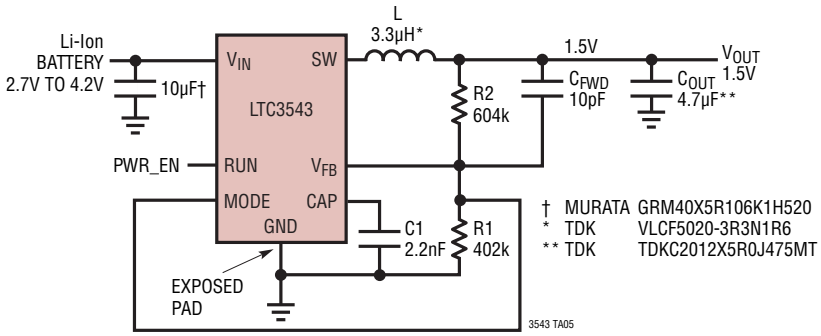


V_{IN} = 3.6V
V_{OUT} = 1.5V
I_{LOAD} = 3mA TO 200mA
V_{MODE} = 0V

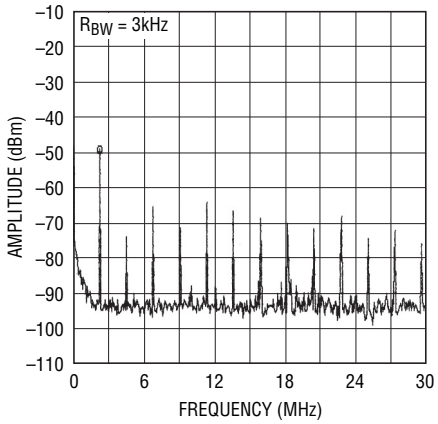


TYPICAL APPLICATIONS

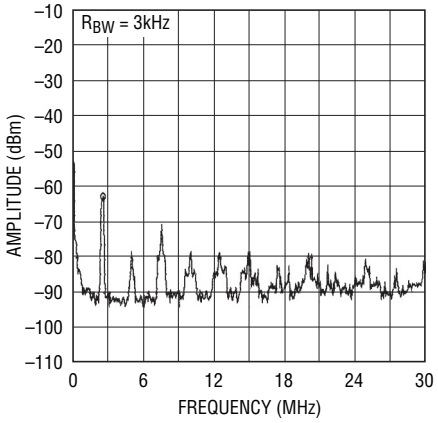
Spread Spectrum Application

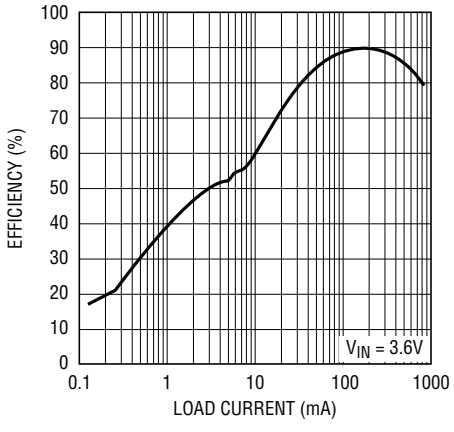


Output Noise Spectrum of a Conventional Buck Switching Converter (LTC3543 with Spread Spectrum Disabled) Showing Fundamental and Harmonic Frequencies



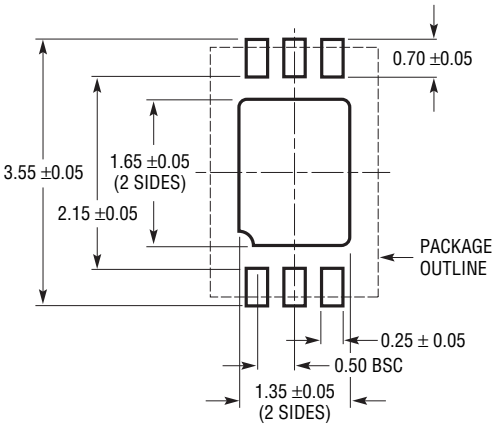
Output Noise Spectrum of the LTC3543 Spread Spectrum Buck Switching Converter. Note the Reduction in Fundamental and Harmonic Peak Spectral Amplitude Compared to Conventional Buck Switching Converter Output Noise



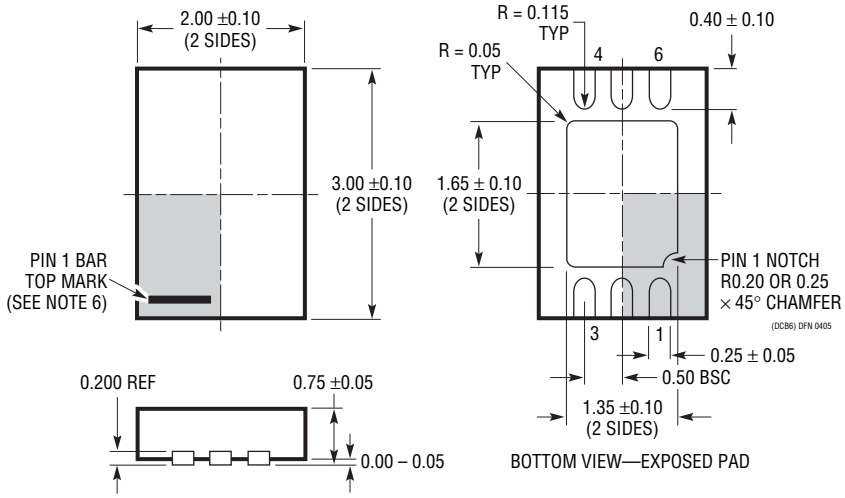


PACKAGE DESCRIPTION

DCB Package
6-Lead Plastic DFN (2mm × 3mm)
(Reference LTC DWG # 05-08-1715 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

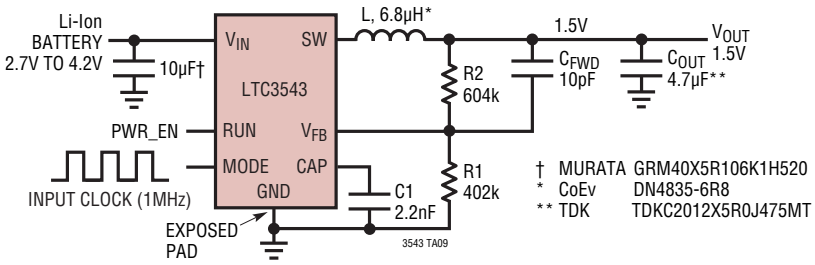


BOTTOM VIEW—EXPOSED PAD

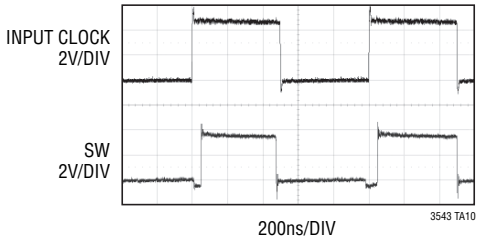
NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (TBD)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

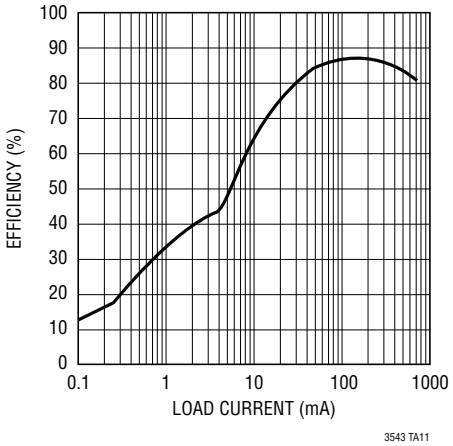
TYPICAL APPLICATION

PLL Application



† MURATA GRM40X5R106K1H520
* CoEv DN4835-6R8
** TDK TDKC2012X5R0J475MT





RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3405/LTC3405A	300mA (I_{OUT}), 1.5MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 20µA, I_{SD} = <1µA, ThinSOT™ Package
LTC3406/LTC3406B	600mA (I_{OUT}), 1.5MHz, Synchronous Step-Down DC/DC Converter	96% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 20µA, I_{SD} = <1µA, ThinSOT Package
LTC3407/LTC3407-2	Dual 600mA/800mA (I_{OUT}), 1.5MHz/2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} = <1µA, MS10E and DFN Packages
LTC3409	600mA (I_{OUT}), 1.7MHz/2.6MHz, Synchronous Step-Down DC/DC Converter	96% Efficiency, V_{IN}: 1.6V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 65µA, I_{SD} = <1µA, DFN Package
LTC3410/LTC3410B	300mA (I_{OUT}), 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 26µA, I_{SD} = <1µA, SC70 Package
LTC3411	1.25A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 60µA, I_{SD} = <1µA, MS10 and DFN Packages
LTC3441/LTC3442/ LTC3443	1.2A (I_{OUT}), 2MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN}: 2.4V to 5.5V, $V_{OUT(MIN)}$: 2.4V to 5.25V, I_Q = 50µA, I_{SD} = <1µA, DFN Package
LTC3531/LTC3531-3/ LTC3531-3.3	200mA (I_{OUT}), 1.5MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN}: 1.8V to 5.5V, $V_{OUT(MIN)}$: 2V to 5V, I_Q = 16µA, I_{SD} = <1µA, ThinSOT and DFN Packages
LTC3532	500mA (I_{OUT}), 2MHz, Synchronous Buck-Boost DC/DC Converter	96% Efficiency, V_{IN}: 2.4V to 5.5V, $V_{OUT(MIN)}$: 2.4V to 5.25V, I_Q = 35µA, I_{SD} = <1µA, MS10 and DFN Packages
LTC3542	500mA (I_{OUT}), 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 26µA, I_{SD} = <1µA, 2mm × 2mm DFN and ThinSOT Packages
LTC3547/LTC3547B	Dual 300mA (I_{OUT}), 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} = <1µA, DFN Package
LTC3548/LTC3548-1/ LTC3548-2	Dual 400mA/800mA (I_{OUT}), 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} = <1µA, MS10E and DFN Packages
LTC3561	1.25A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 240µA, I_{SD} = <1µA, DFN Package

ThinSOT is a trademark of Linear Technology Corporation.

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

LT 0509 REV A • PRINTED IN USA