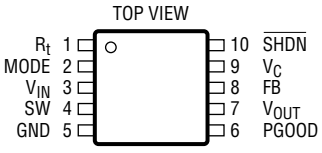
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, V_{OUT} Voltages ..... –0.5V to 6V
SW Voltage ..... –0.5V to 6V
V_C, R_t Voltages ..... –0.5V to (V_{OUT} + 0.3V)
PGOOD, $\overline{SHDN}$, FB, MODE Voltages ..... –0.5V to 6V
Operating Temperature Range (Note 2) .. –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec)..... 300°C

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

PACKAGE/ORDER INFORMATION



MS PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C
θ_{JA} = 130°C/W 1 LAYER BOARD
θ_{JA} = 100°C/W 4 LAYER BOARD

ORDER PART NUMBER
LTC3402EMS
MS PART MARKING
LTSK

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 1.2V, V_{OUT} = 3.3V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Start-Up Voltage	I_{LOAD} = <1mA			0.85	1.0	V
Minimum Operating Voltage	(Note 4)	●			0.5	V
Output Voltage Adjust Range		●	2.6		5.5	V
Feedback Voltage		●	1.22	1.25	1.28	V
Feedback Input Current	V_{FB} = 1.25V			1	50	nA
Quiescent Current—Burst Mode Operation	V_C = 0V, MODE/SYNC = 3.3V (Note 3)			38	65	µA
Quiescent Current—$\overline{SHDN}$	$\overline{SHDN}$ = 0V, Not Including Switch Leakage			0.1	1	µA
Quiescent Current—Active	V_C = 0V, MODE/SYNC = 0V, R_t = 300k (Note 3)			440	800	µA
NMOS Switch Leakage				0.1	5	µA
PMOS Switch Leakage				0.1	10	µA
NMOS Switch On Resistance				0.16		Ω
PMOS Switch On Resistance				0.18		Ω
NMOS Current Limit		●	2	2.5		A
NMOS Burst Current Limit				0.66		A
Maximum Duty Cycle	R_t = 15k	●	80	85		%
Minimum Duty Cycle		●			0	%
Switching Frequency	R_t = 15k	●	1.6	2	2.4	MHz
MODE/SYNC Input High			1.4			V
MODE/SYNC Input Low					0.4	V
MODE/SYNC Input Current	$V_{MODE/SYNC}$ = 5.5V			0.01	1	µA
Error Amp Transconductance	ΔI = –5µA to 5µA, V_C = V_{FB}			85		µmhos
PGOOD Threshold	Referenced to Feedback Voltage		–6	–9	–12	%

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 1.2V, V_{OUT} = 3.3V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PGOOD Low Voltage	I_{PGOOD} = 1mA V_{OUT} = 1V, I_{PGOOD} = 20µA			0.1 0.1	0.2 0.4	V V
PGOOD Leakage	V_{PGOOD} = 5.5V			0.01	1	µA
$\overline{SHDN}$ Input High	V_{IN} = $V_{\overline{SHDN}}$		1			V
$\overline{SHDN}$ Input Low					0.4	V
$\overline{SHDN}$ Input Current	$V_{\overline{SHDN}}$ = 5.5V			0.01	1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime..

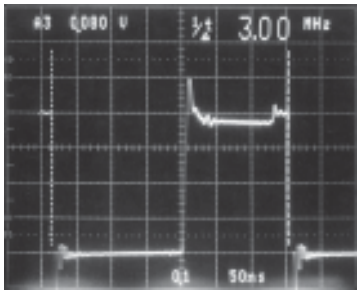
Note 2: The LTC3402E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Current is measured into the V_{OUT} pin since the supply current is bootstrapped to the output pin and in the application will reflect to the input supply by (V_{OUT}/V_{IN}) • I/Efficiency. The outputs are not switching.

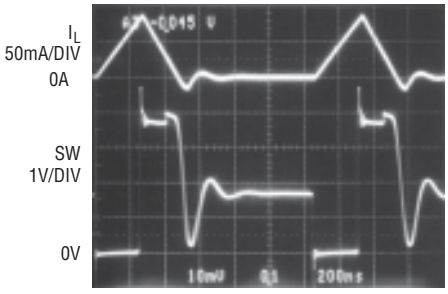
Note 4: Once the output is started, the IC is not dependent upon the V_{IN} supply.

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise noted)

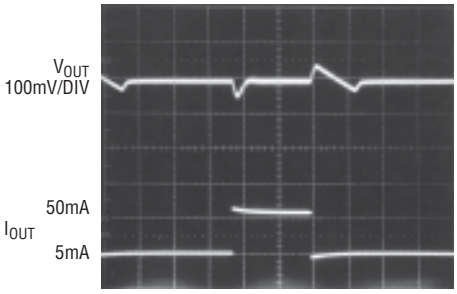
Switching Waveform on SW Pin



SW Pin and Inductor Current (I_C) in Discontinuous Mode. Ringing Control Circuitry Eliminates High Frequency Ringing

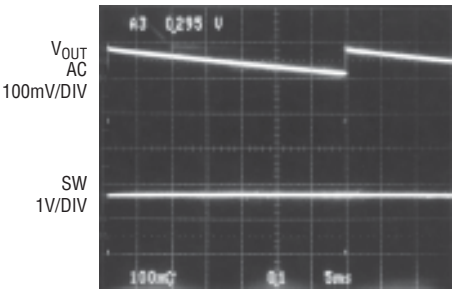


Transient Response 5mA to 50mA

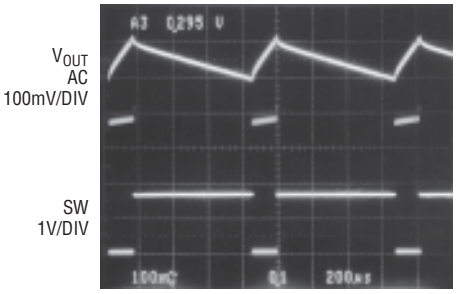


Transient Response 50mA to 500mA

Burst Mode Operation

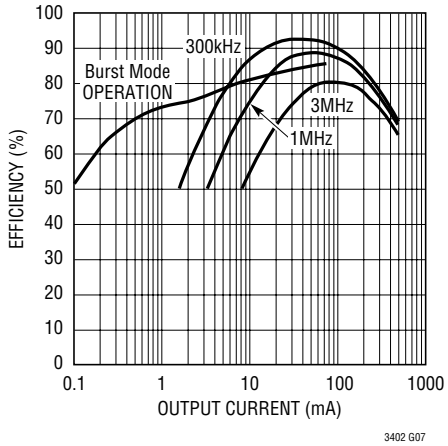


Burst Mode Operation

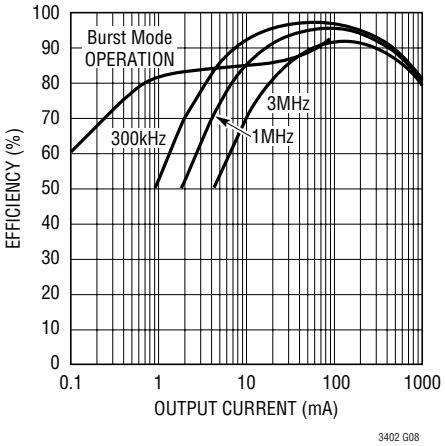


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise noted)

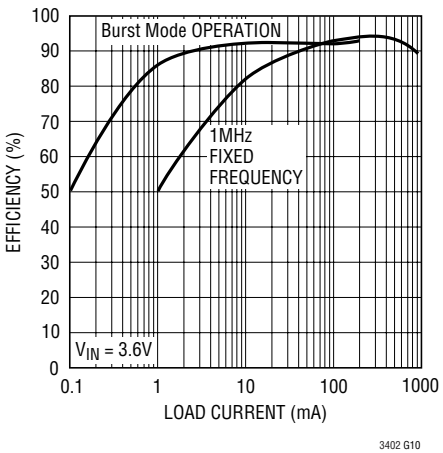
Converter Efficiency 1.2V to 3.3V



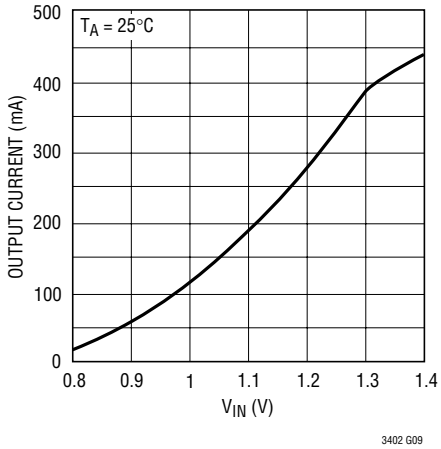
Converter Efficiency 2.4V to 3.3V



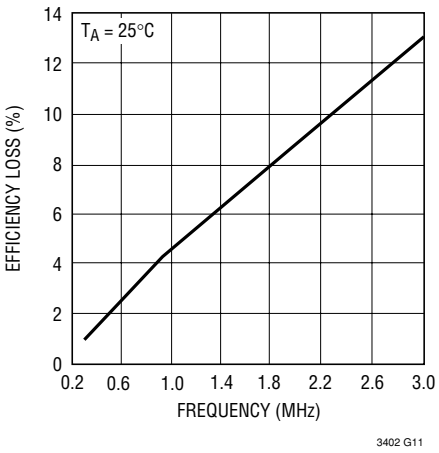
Converter Efficiency 3.6V to 5V



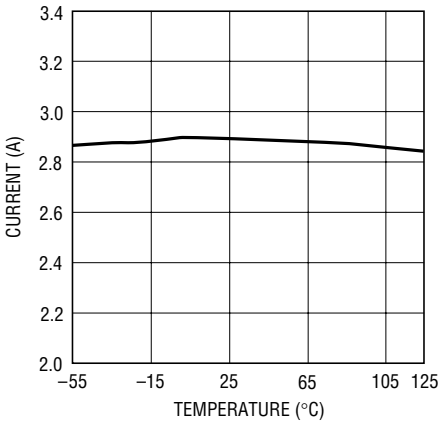
Start-Up Voltage vs I_{OUT}



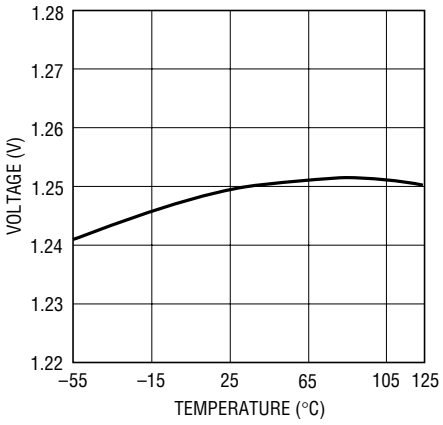
Efficiency Loss Without Schottky vs Frequency



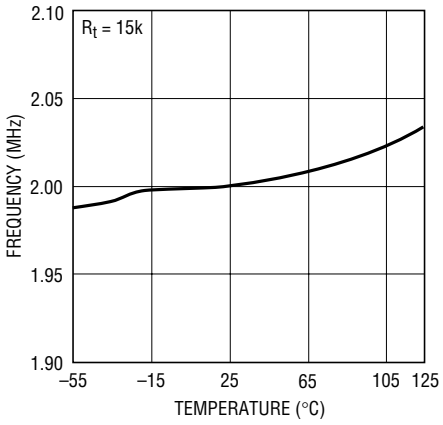
Current Limit



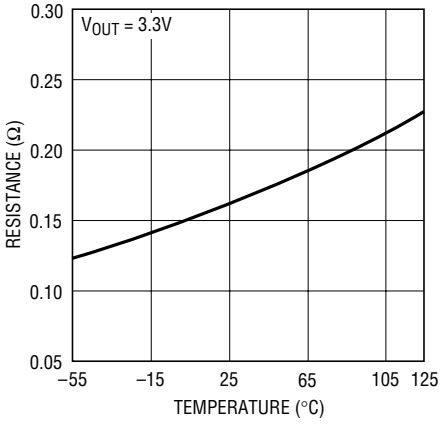
EA FB Voltage



Oscillator Frequency Accuracy

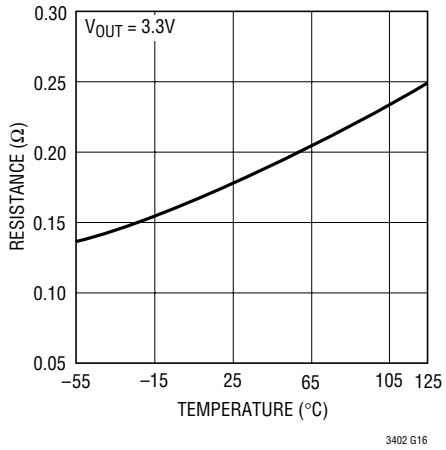


NMOS $R_{DS(ON)}$

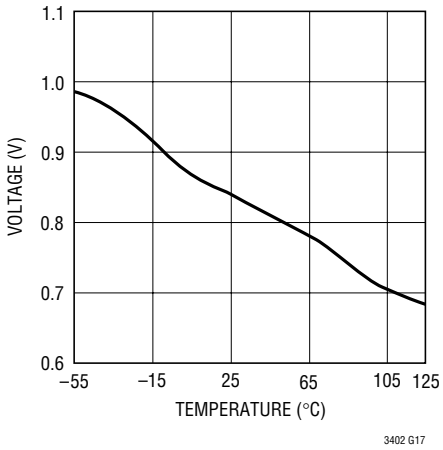


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise noted)

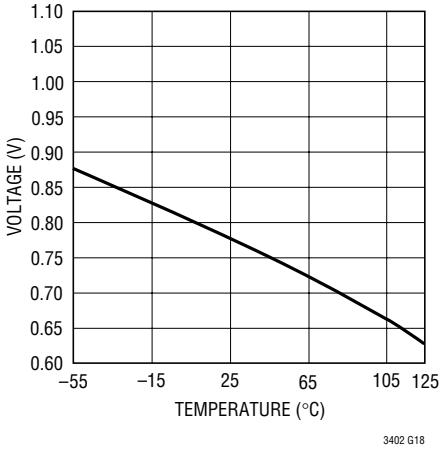
PMOS $R_{DS(ON)}$



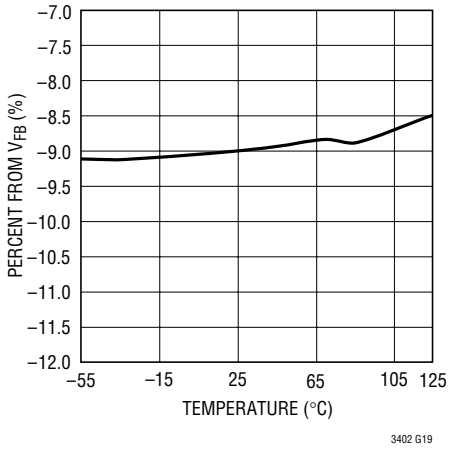
Start-Up Voltage



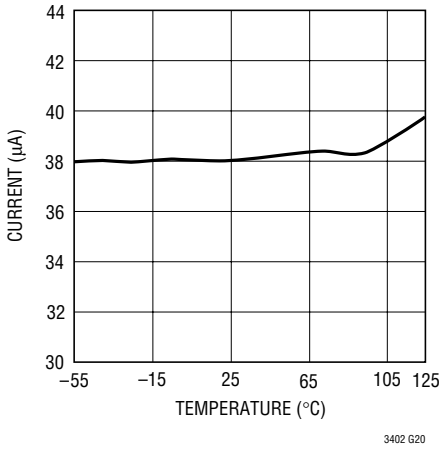
Shutdown Threshold



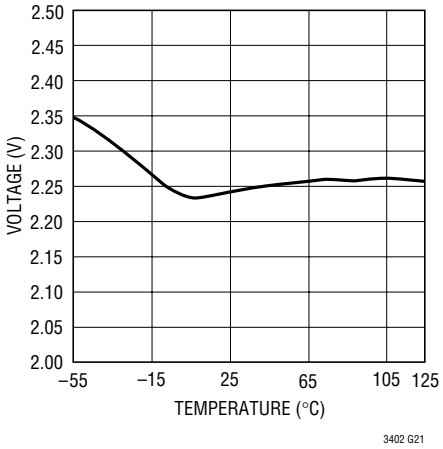
PGOOD Threshold



Burst Mode Operation Current



V_{OUT} Turn-Off Voltage



PIN FUNCTIONS

R_t (Pin 1): Timing Resistor to Program the Oscillator Frequency.

$$f_{OSC} = \frac{3 \bullet 10^{10}}{R_t} \text{ Hz}$$

MODE/SYNC (Pin 2): Burst Mode Select and Oscillator Synchronization.

MODE/SYNC = High. Enable Burst Mode operation. The inductor peak inductor current will be 1/3 the current limit value and return to zero current on each cycle. During Burst Mode operation the operation is variable frequency, providing a significant efficiency improvement at light loads. It is recommended the Burst Mode operation only be entered once the part has started up.

MODE/SYNC = Low. Disable Burst Mode operation and maintain low noise, constant frequency operation.

MODE/SYNC = External CLK. Synchronization of the internal oscillator and Burst Mode operation disable. A clock pulse width of 100ns to 2µs is required to synchronize.

V_{IN} (Pin 3): Input Supply Pin.

SW (Pin 4): Switch Pin. Connect inductor and Schottky diode here. For applications with output voltages over 4.3V, a Schottky diode is required to ensure that the SW pin voltage does not exceed its absolute maximum rating. Minimize trace length to keep EMI and high ringing down. For discontinuous inductor current, a controlled impedance is placed from SW to V_{IN} from the IC to eliminate high frequency ringing due to the resonant tank of the inductor and SW node capacitance, therefore reducing EMI radiation.

GND (Pin 5): Signal and Power Ground for the IC.

PGOOD (Pin 6): Power Good Comparator Output. This open-drain output is low when V_{FB} < –9% from its regulation voltage.

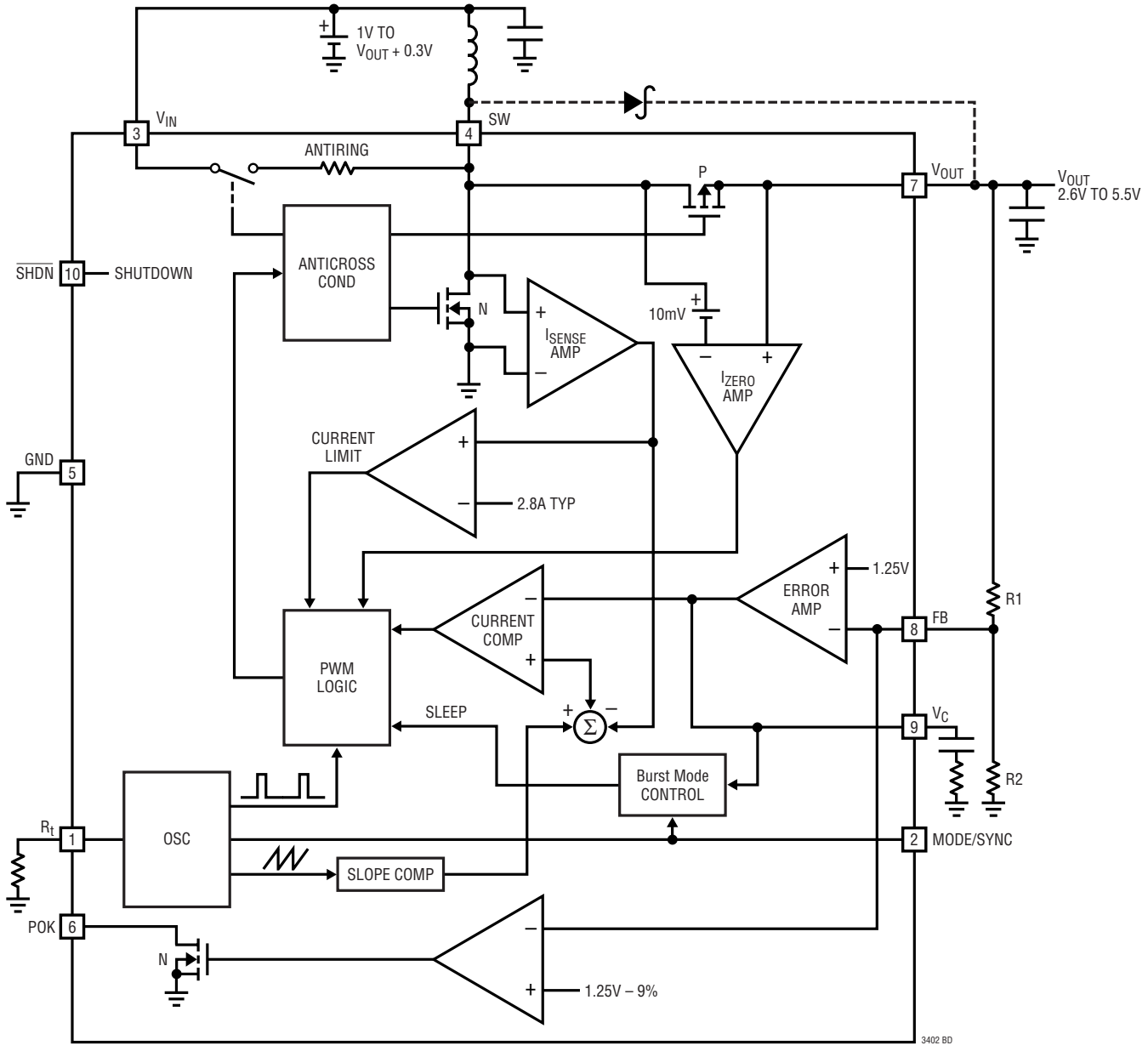
V_{OUT} (Pin 7): Output of the Synchronous Rectifier and Bootstrapped Power Source for the IC. A ceramic capacitor of at least 1µF is required and should be located as close to the V_{OUT} and GND pins as possible (Pins 7 and 5).

FB (Pin 8): Feedback Pin. Connect resistor divider tap here. The output voltage can be adjusted from 2.6V to 5V. The feedback reference voltage is typically 1.25V.

V_C (Pin 9): Error Amp Output. A frequency compensation network is connected to this pin to compensate the loop. See the section "Compensating the Feedback Loop" for guidelines.

$\overline{SHDN}$ (Pin 10): Shutdown. Grounding this pin shuts down the IC. Tie to >1V to enable (V_{IN} or digital gate output). To operate with input voltages below 1V once the converter has started, a 1M resistor from $\overline{SHDN}$ to V_{IN} and a 5M resistor from $\overline{SHDN}$ to V_{OUT} will provide sufficient hysteresis. During shutdown, the output voltage will hold up to V_{IN} minus a diode drop due to the body diode of the PMOS synchronous switch. If the application requires a complete disconnect during shutdown, refer to the section "Output Disconnect Circuits."

BLOCK DIAGRAM



APPLICATIONS INFORMATION

DETAILED DESCRIPTION

The LTC3402 provides high efficiency, low noise power for applications such as portable instrumentation. The current mode architecture with adaptive slope compensation provides ease of loop compensation with excellent transient load response. The low $R_{DS(ON)}$, low gate charge synchronous switches provide the pulse width modulation control at high efficiency.

The Schottky diode across the synchronous PMOS switch provides a lower drop during the break-before-make time (typically 20ns) of the NMOS to PMOS transition. The addition of the Schottky diode will improve efficiency (see graph "Efficiency Loss Without Schottky vs Frequency"). While the IC's quiescent current is a low 38µA, high efficiency is achieved at light loads when Burst Mode operation is entered.

Low Voltage Start-Up

The LTC3402 is designed to start up at input voltages of typically 0.85V. The device can start up under some load, (see graph Start-Up vs Input Voltage). Once the output voltage exceeds a threshold of 2.3V, then the IC powers itself from V_{OUT} instead of V_{IN}. At this point, the internal circuitry has no dependency on the input voltage, eliminating the requirement for a large input capacitor. The input voltage can drop below 0.5V without affecting the operation, but the limiting factor for the application becomes the availability of the power source to supply sufficient energy to the output at the low voltages.

Low Noise Fixed Frequency Operation

Oscillator. The frequency of operation is set through a resistor from the R_t pin to ground where $f = 3 \bullet 10^{10}/R_t$. An internally trimmed timing capacitor resides inside the IC. The oscillator can be synchronized with an external clock inserted on the MODE/SYNC pin. When synchronizing the oscillator, the free running frequency must be set to approximately 30% lower than the desired synchronized frequency. Keeping the sync pulse width below 2µs will ensure that Burst Mode operation is disabled.

Current Sensing. Lossless current sensing converts the peak current signal to a voltage to sum in with the internal slope compensation. This summed signal is compared to the error amplifier output to provide a peak current control command for the PWM. The slope compensation in the IC is adaptive to the input and output voltage. Therefore, the converter provides the proper amount of slope compensation to ensure stability and not an excess causing a loss of phase margin in the converter.

Error Amp. The error amplifier is a transconductance amplifier with g_m = 0.1ms. A simple compensation network is placed from the V_C pin to ground.

Current Limit. The current limit amplifier will shut the NMOS switch off once the current exceeds its threshold. The current amplifier delay to output is typically 50ns.

Zero Current Amp. The zero current amplifier monitors the inductor current to the output and shuts off the synchronous rectifier once the current is below 50mA, preventing negative inductor current.

Antiringing Control. The anitringing control will place an impedance across the inductor to damp the ringing on the SW pin during discontinuous mode operation. The LC_{SW} ringing (L = inductor, C_{SW} = capacitance on the switch pin) is low energy, but can cause EMI radiation.

Burst Mode Operation

Burst Mode operation is when the IC delivers energy to the output until it is regulated and then goes into a sleep mode where the outputs are off and the IC is consuming only 38µA. In this mode, the output ripple has a variable frequency component with load current and the steady state ripple will be typically below 3%.

During the period where the device is delivering energy to the output, the peak current will be equal to 1/6 the current limit value and the inductor current will terminate at zero current for each cycle. In this mode the maximum output current is given by:

$$I_{OUT(MAXBURST)} \approx \frac{V_{IN}}{6 \bullet V_{OUT}} \text{ Amps}$$

Burst Mode operation is user controlled by driving the MODE/SYNC pin high to enable and low to disable. It is recommended that Burst Mode operation be entered after the part has started up.

APPLICATIONS INFORMATION

COMPONENT SELECTION

Inductor Selection

The high frequency operation of the LTC3402 allows the use of small surface mount inductors. The minimum inductance value is proportional to the operating frequency and is limited by the following constraints:

$$L > \frac{3}{f}\mu H \text{ and } L > \frac{V_{IN(MIN)} \bullet V_{OUT(MAX)} - V_{IN(MIN)}}{f \bullet Ripple \bullet V_{OUT(MAX)}} H$$

where

f = Operating Frequency (Hz)

Ripple = Allowable Inductor Current Ripple (A)

$V_{IN(MIN)}$ = Minimum Input Voltage (V)

$V_{OUT(MAX)}$ = Maximum Output Voltage (V)

The inductor current ripple is typically set to 20% to 40% of the maximum inductor current.

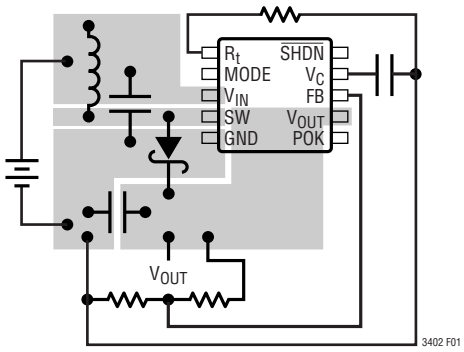


Figure 1. Recommended Component Placement. Traces Carrying High Current Are Direct. Trace Area FB and V_C Pins Are Kept Low. Lead Length to Battery Should be Kept Short

For high efficiency, choose an inductor with a high frequency core material, such as ferrite, to reduce core losses. The inductor should have low ESR (equivalent series resistance) to reduce the I^2R losses and must be able to handle the peak inductor current without saturating. Molded chokes or chip inductors usually do not have enough core to support the peak inductor currents in the 1A to 2A region. To minimize radiated noise, use a toroid, pot core or shielded bobbin inductor. See Table 1 for suggested components and Table 1 for a list of component suppliers.

Table 1. Inductor Vendor Information

SUPPLIER	PHONE	FAX	WEBSITE
Coilcraft	(847) 639-6400	(847) 639-1469	www.coilcraft.com
Coiltronics	(516) 241-7876	(516) 241-9339	www.coiltronics.com
Murata	(814) 237-1431 (800) 831-9172	(814) 238-0490	www.murata.com
Sumida USA: Japan:	 (847) 956-0666 81-3-3607-5111	 (847) 956-0702 81-3-3607-5144	 www.japanlink.com sumida

Output Capacitor Selection

The output voltage ripple has several components. The bulk value of the capacitor is set to reduce the ripple due to charge into the capacitor each cycle. The max ripple due to charge is given by:

$$VR_{BULK} = \frac{I_P \bullet V_{IN}}{C_{OUT} \bullet V_{OUT} \bullet f} V$$

where

I_P = Peak Inductor Current

The ESR can be a significant factor for ripple in most power converters. The ripple due to capacitor ESR is simply given by:

$$VR_{CESR} = I_P \bullet R_{ESR} V$$

where

R_{ESR} = Capacitor Series Resistance

Low ESR capacitors should be used to minimize output voltage ripple. For surface mount applications, AVX TPS series tantalum capacitors and Sanyo POSCAP or Taiyo-Yuden ceramic X5R or X7R type capacitors are recommended. For through-hole applications Sanyo OS-CON capacitors offer low ESR in a small package size. See Table 2 for a list of component suppliers. In some layouts it may be required to place a 1µF low ESR capacitor as close to the V_{OUT} and GND pins as possible.

Table 2. Capacitor Vendor Information

SUPPLIER	PHONE	FAX	WEBSITE
AVX	(803) 448-9411	(803) 448-1943	www.avxcorp.com
Sanyo	(619) 661-6322	(619) 661-1055	www.sanyovideo.com
Taiyo Yuden	(408) 573-4150	(408) 573-4159	www.t-yuden.com

APPLICATIONS INFORMATION

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the input source and reduces input switching noise. Since the IC can operate at voltages below 0.5V once the output is regulated, then demand on the input capacitor is much less and in most applications a 4.7µF is recommended.

Output Diode

For applications with output voltages over 4.3V, a Schottky diode is required to ensure that the SW pin voltage does not exceed its absolute maximum rating. The Schottky diode across the synchronous PMOS switch provides a lower drop during the break-before-make time (typically 20ns) of the NMOS to PMOS transition. The Schottky diode improves peak efficiency (see graph "Efficiency Loss Without Schottky vs Frequency). Use of a Schottky diode such as a MBR0520L, 1N5817 or equivalent. Since slow recovery times will compromise efficiency, do not use ordinary rectifier diodes.

Operating Frequency Selection

There are several considerations in selecting the operating frequency of the converter. The first is determining the sensitive frequency bands that cannot tolerate any spectral noise. For example, in products incorporating RF communications, the 455kHz IF frequency is sensitive to any noise, therefore switching above 600kHz is desired. Some communications have sensitivity to 1.1MHz. In this case, a 2MHz converter frequency may be employed.

The second consideration is the physical size of the converter. As the operating frequency goes up, the inductor and filter caps go down in value and size. The trade off is in efficiency since the switching losses due to gate charge are going up proportional with frequency. For example in Figure 2, for a 2.4V to 3.3V converter, the efficiency at 100mA is 5% less at 2MHz compared to 300kHz.

Another operating frequency consideration is whether the application can allow "pulse skipping." In this mode, the minimum on time of the converter cannot support the duty cycle, so the converter ripple will go up and there will be a low frequency component of the output ripple. In many applications where physical size is the main criterion then running the converter in this mode is acceptable. In applications where it is preferred not to enter this mode, then the maximum operating frequency is given by:

$$f_{MAX\_NOSKIP} = \frac{V_{OUT} - V_{IN}}{V_{OUT} \bullet t_{ON(MIN)}} Hz$$

where $t_{ON(MIN)}$ = minimum on time = 120ns.

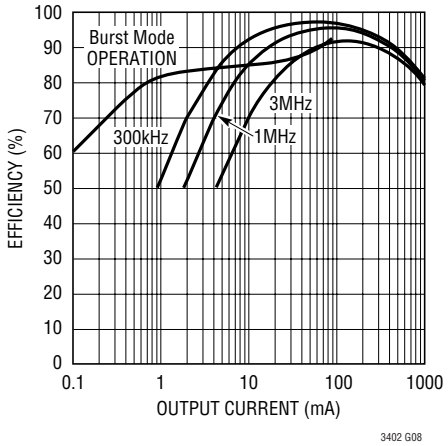


Figure 2. Converter Efficiency 2.4V to 3.3V

Reducing Output Capacitance with a Load Feed Forward Signal

In many applications the output filter capacitance can be reduced for the desired transient response by having the device commanding the change in load current, (i.e. system microcontroller), inform the power converter of the changes as they occur. Specifically, a "load feed forward" signal coupled into the V_C pin gives the inner current loop a head start in providing the change in output current. The transconductance of the LTC3402 converter at the V_C pin with respect to the inductor current is typically 170mA/100mV, so the amount of signal injected is proportional to the anticipated change of inductor current with load. The outer voltage loop performs the remainder of the correction, but because of the load feed forward signal, the range over which it must slew is greatly reduced. This results in an improved transient response. A logic level feed forward signal, V_{FF}, is coupled through components C5 and R6. The amount of feed forward

APPLICATIONS INFORMATION

signal is attenuated with resistor R6 and is given by the following relationship:

$$R6 \approx \left(\frac{V_{FF} \bullet R5 \bullet V_{IN} \bullet 1.5}{V_{OUT} \bullet \Delta I_{OUT}} \right) - R5$$

where ΔI_{OUT} = load current change.

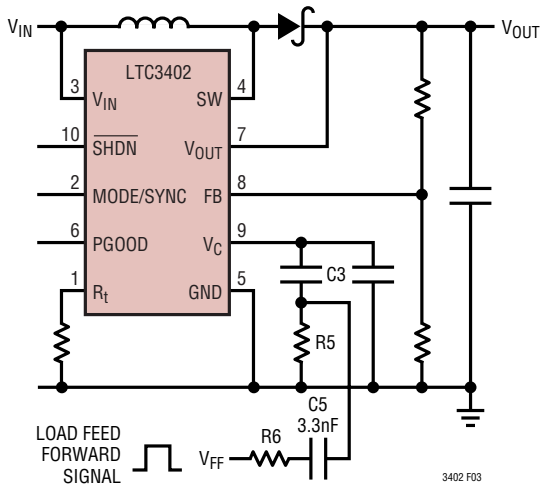


Figure 3

Closing the Feedback Loop

The LTC3402 used current mode control with internal adaptive slope compensation. Current mode control eliminates the 2nd order filter due to the inductor and output capacitor exhibited in voltage mode controllers, and simplifies it to a single-pole filter response. The product of the modulator control to output DC gain plus the error amp open-loop gain equals the DC gain of the system.

$$G_{DC} = G_{CONTROLOUTPUT} \bullet G_{EA}$$

$$G_{CONTROL} = \frac{2 \bullet V_{IN}}{I_{OUT}}, \; G_{EA} \approx 2000$$

The output filter pole is given by:

$$f_{FILTERPOLE} = \frac{I_{OUT}}{\pi \bullet V_{OUT} \bullet C_{OUT}} Hz$$

where C_{OUT} is the output filter capacitor.

The output filter zero is given by:

$$f_{FILTERZERO} = \frac{1}{2 \bullet \pi \bullet R_{ESR} \bullet C_{OUT}} Hz$$

where R_{ESR} is the capacitor equivalent series resistance.

A troublesome feature of the boost regulator topology is the right half plane zero (RHP) and is given by:

$$f_{RHPZ} = \frac{V_{IN}^2 R_O}{2\pi L V_O^2} Hz$$

At heavy loads this gain increase with phase lag can occur at a relatively low frequency. The loop gain is typically rolled off before the RHP zero frequency.

The typical error amp compensation is shown in Figure 4. The equations for the loop dynamics are as follows:

$$f_{POLE1} \approx \frac{1}{2 \bullet \pi \bullet 20 \bullet 10^6 \bullet C_{C1}} Hz$$

which is extremely close to DC

$$f_{ZERO1} = \frac{1}{2 \bullet \pi \bullet R_Z \bullet C_{C1}} Hz$$

$$f_{POLE2} \approx \frac{1}{2 \bullet \pi \bullet R_Z \bullet C_{C2}} Hz$$

Refer to AN76 for more closed-loop examples.

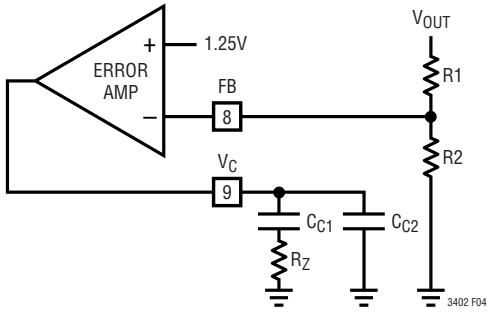
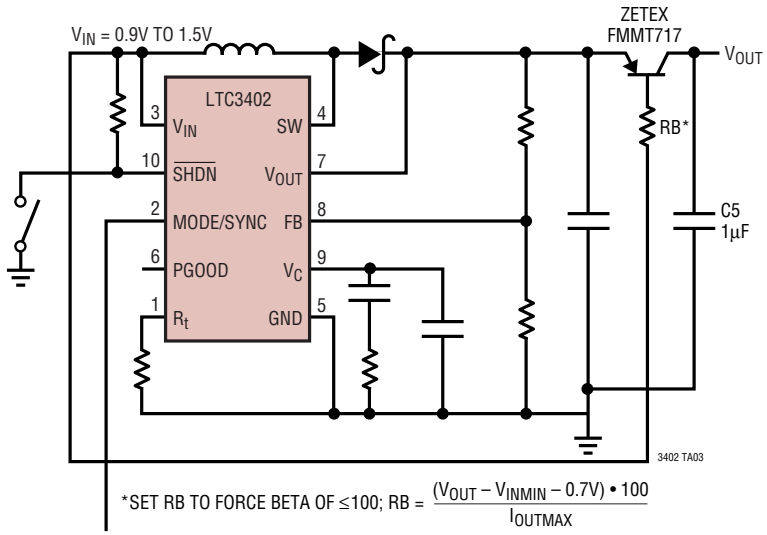


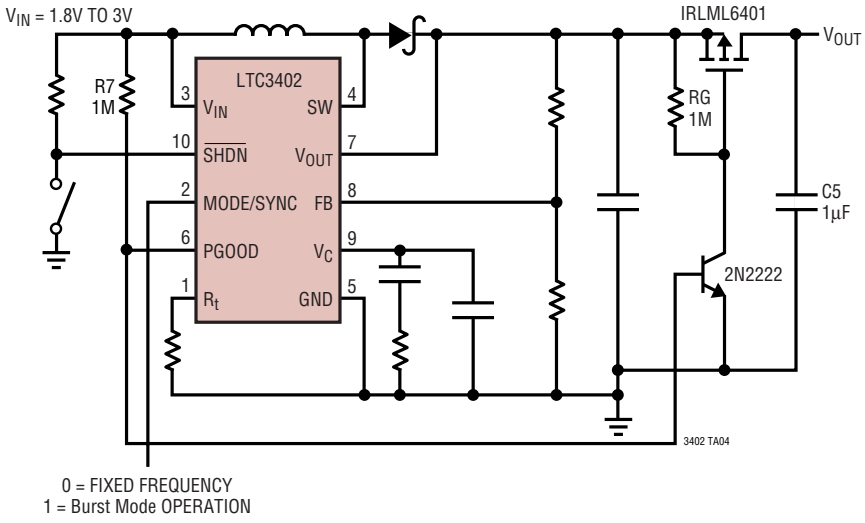
Figure 4

OUTPUT DISCONNECT CIRCUITS

Single Cell Output Disconnect

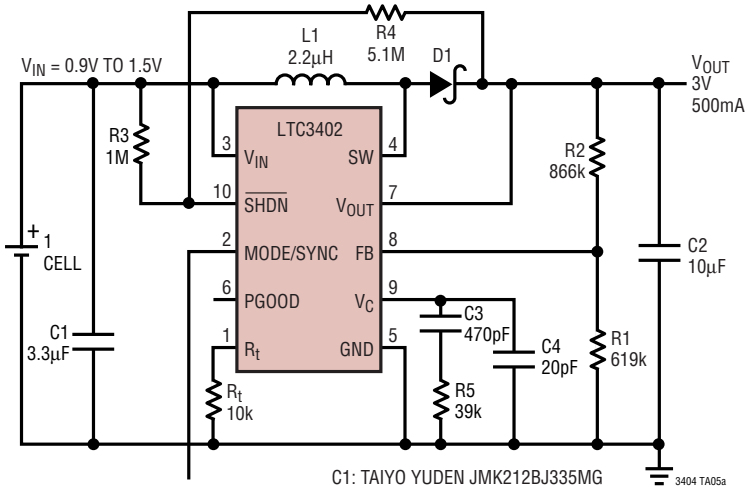


Dual Cell Output Disconnect Allowing Full Load Start-Up



TYPICAL APPLICATIONS

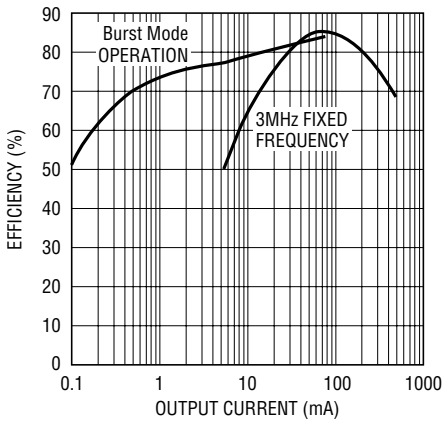
Single Cell to 3V at 500mA, All Ceramic Capacitor, 3MHz Step-Up Converter



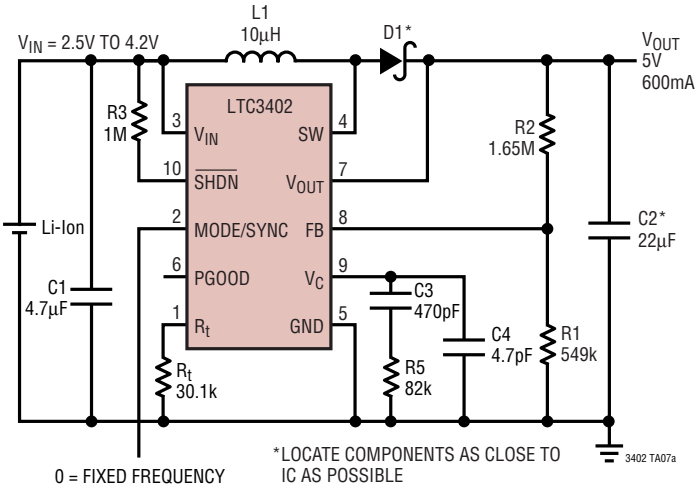
0 = FIXED FREQUENCY
1 = Burst Mode OPERATION

C1: TAIYO YUDEN JMK212BJ335MG
C2: TAIYO YUDEN JMK325BJ106MM
D1: ON SEMICONDUCTOR MBRM120T3
L1: COILCRAFT DO1608-222

Efficiency



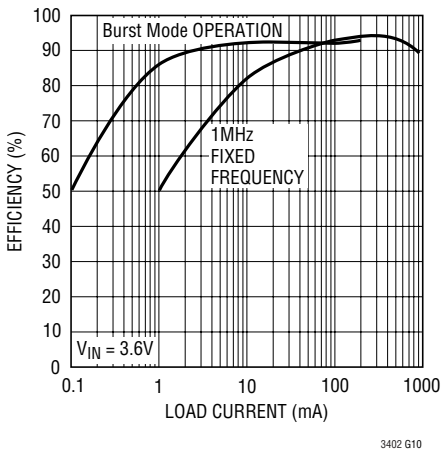
Li-Ion to 5V at 300mA, 1MHz Step-Up Converter



0 = FIXED FREQUENCY
1 = Burst Mode OPERATION

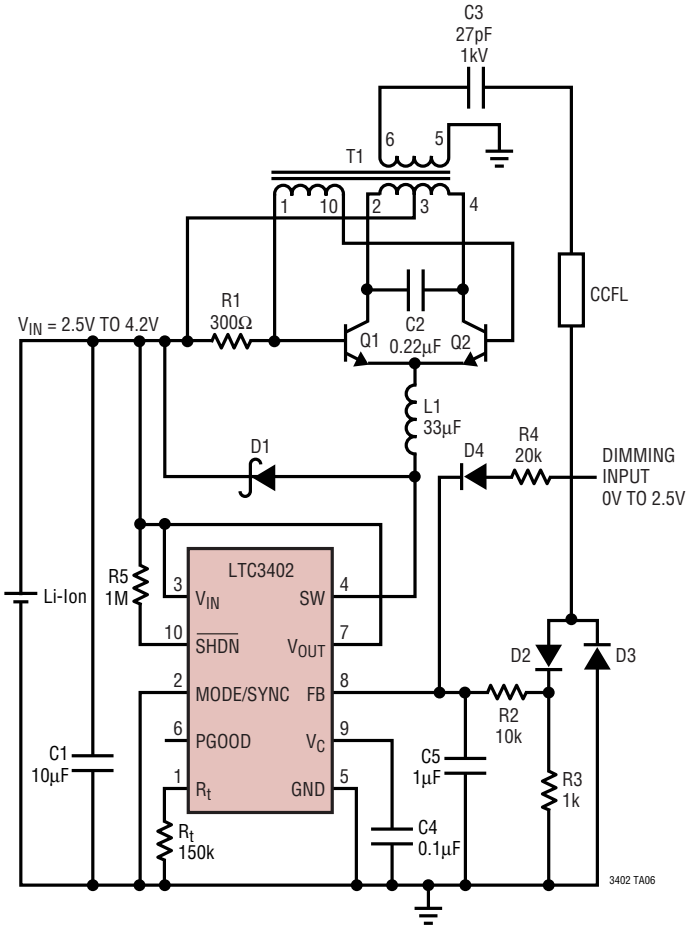
*LOCATE COMPONENTS AS CLOSE TO IC AS POSSIBLE
C1: TAIYO YUDEN JMK212BJ475MG
C2: TAIYO YUDEN JMK325BJ226MM
D1: ON SEMICONDUCTOR MBRM120T3
L1: SUMIDA CDH53-100

Efficiency



TYPICAL APPLICATIONS

High Efficiency, Compact CCFL Supply with Remote Dimming



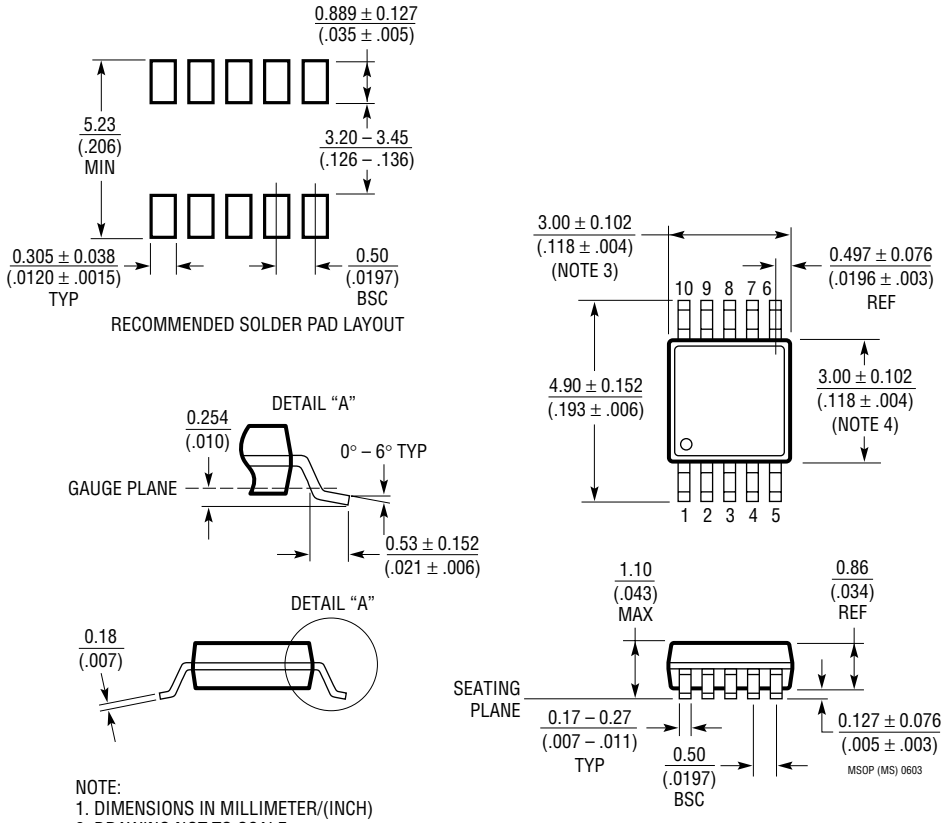
C1: TAIYO YUDEN JMK212BJ106MG
C2: PANASONIC ECH-U
D1: ZETEX ZHCS-1000
D2 TO D4: 1N4148

L1: SUMIDA CD-54-330MC
Q1, Q2: ZETEX FMMT-617
T1: SUMIDA C1Q122

CCFL BACKLIGHT APPLICATION CIRCUITS CONTAINED IN THIS DATA SHEET ARE COVERED BY U.S. PATENT NUMBER 5408162 AND OTHER PATENTS PENDING

PACKAGE DESCRIPTION

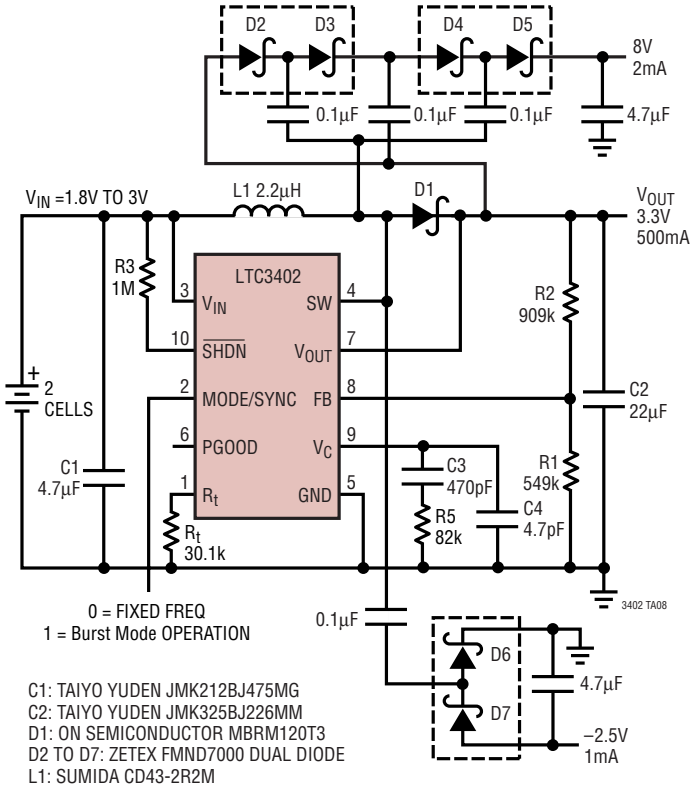
MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

TYPICAL APPLICATION

Triple Output Converter



C1: TAIYO YUDEN JMK212BJ475MG
C2: TAIYO YUDEN JMK325BJ226MM
D1: ON SEMICONDUCTOR MBRM120T3
D2 TO D7: ZETEX FMND7000 DUAL DIODE
L1: SUMIDA CD43-2R2M

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT®1306	Sync, Fixed Frequency, Step-Up DC/DC Converter	Internal 2A Switches; V_{IN} As Low As 1.8V
LT1308A/LT1308B	High Current, Micropower, Single Cell 600kHz DC/DC Converter	5V at 1A with Single Li-Ion Cell, V_{OUT} to 34V
LT1613	1.4MHz, Single Cell DC/DC Converter in SOT-23	V_{IN} As Low As 1.1V, 3V at 30mA from Single Cell
LT1615	Micropower Step-Up DC/DC Converter in SOT-23	I_Q = 20µA, 1µA Shutdown Current, V_{IN} As Low As 1V
LT1619	High Efficiency Boost DC/DC Controller	1A Gate Drive, 1.1V to 20V Input, Separate V_{CC} for Gate Drive
LTC1872	SOT-23 Boost DC/DC Controller	550kHz, 2.5V to 9.8V Input
LT1930/LT1930A	1.2MHz/2.2MHz DC/DC Converters in SOT-23	V_{IN} = 2.6V to 16V, 5V at 450mA from 3.3V Input
LT1949	600kHz, 1A Switch PWM DC/DC Converter	1A, 0.5Ω, 30V Internal Switch, V_{IN} As Low As 1.5V, Low-Battery Detect Active in Shutdown
LTC3400	Single Cell, High Current (600mA), Micropower, Synchronous 1.2MHz Step-Up DC/DC Converter	V_{IN} = 0.85V to 5.5V, Up to 92% Efficiency Synchronizable Oscillator from 100kHz to 1.2MHz, ThinSOT Package
LTC3401	Single Cell, High Current (1A), Micropower, Synchronous 3MHz Step-Up DC/DC Converter	V_{IN} = 0.5V to 5V, Up to 97% Efficiency Synchronizable Oscillator from 100kHz to 3MHz, 10-Lead MSOP Package
LTC3424	Single Cell, High Current (2A), Micropower, Synchronous 3MHz Step-Up DC/DC Converter	V_{OUT} = 1.5V, Up to 97% Efficiency Synchronizable Oscillator from 100kHz to 3MHz, 10-Lead MSOP Package

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