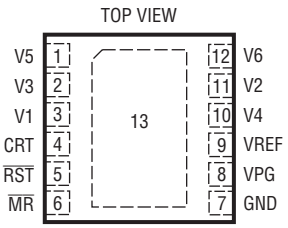
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2, 3)

V1, V2, V3, V4, V5, V6, VPG, $\overline{RST}$ ..... –0.3V to 7V
CRT, VREF, $\overline{MR}$ ..... –0.3V to (V_{CC} + 0.3V)
Reference Load Current (I_{VREF}) ..... ±1mA
V4 Input Current (–ADJ Mode) ..... –1mA
$\overline{RST}$ Current ..... ±10mA
Operating Temperature Range
LTC2930C ..... 0°C to 70°C
LTC2930I ..... –40°C to 85°C
LTC2930H ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



DD PACKAGE
12-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 130°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 13) IS GND
(PCB CONNECTION OPTIONAL)

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2930CDD#PBF	LTC2930CDD#TRPBF	LDMJ	12-Lead 3mm × 3mm DFN	0°C to 70°C
LTC2930IDD#PBF	LTC2930IDD#TRPBF	LDMJ	12-Lead 3mm × 3mm DFN	–40°C to 85°C
LTC2930HDD#PBF	LTC2930HDD#TRPBF	LDMJ	12-Lead 3mm × 3mm DFN	–40°C to 125°C

*The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, unless otherwise specified. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Minimum Internal Operating Voltage	$\overline{RST}$ in Correct Logic State	●			1	V
V_{CCMINP}	Minimum Required for Mode Selection	V_{CC} Rising	●			2.4	V
V_{RT50}	5V, 5% Reset Threshold	V1 Input Threshold	●	4.600	4.675	4.750	V
V_{RT33}	3.3V, 5% Reset Threshold	V1, V2 Input Threshold	●	3.036	3.086	3.135	V
V_{RT30}	3V, 5% Reset Threshold	V2 Input Threshold	●	2.760	2.805	2.850	V
V_{RT25}	2.5V, 5% Reset Threshold	V2, V3 Input Threshold	●	2.300	2.338	2.375	V
V_{RT18}	1.8V, 5% Reset Threshold	V3, V4 Input Threshold	●	1.656	1.683	1.710	V
V_{RT15}	1.5V, 5% Reset Threshold	V3, V4 Input Threshold	●	1.380	1.403	1.425	V
V_{RTA}	ADJ Reset Threshold	V3, V4, V5, V6 Input Threshold	●	492.5	500	507.5	mV
V_{RTAN}	–ADJ Reset Threshold	V4 Input Threshold	●	–18	0	18	mV
V_{REF}	Reference Voltage	$V_{CC} \geq$ 2.3V, I_{VREF} = ±1mA, $C_{REF} \leq$ 1000pF	●	1.192	1.210	1.228	V
V_{PG}	Mode Selection Voltage Range	$V_{CC} \geq V_{CCMINP}$	●	0		V_{REF}	V
I_{VPG}	VPG Input Current	$V_{PG} = V_{REF}$	●			±20	nA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, unless otherwise specified. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{V1}	V1 Input Current	V1 = 5V, I_{VREF} = 12µA (Note 4)	●		52	75	µA
I_{V2}	V2 Input Current	V2 = 3.3V	●		0.8	2	µA
I_{V3}	V3 Input Current	V3 = 2.5V V3 = 0.55V (ADJ Mode)	● ●		0.52	1.2 ±15	µA nA
I_{V4}	V4 Input Current	V4 = 1.8V V4 = 0.55V (ADJ Mode) V4 = –0.02V (–ADJ Mode)	● ● ●		0.34	0.8 ±15 ±15	µA nA nA
I_{V5}, I_{V6}	V5, V6 Input Current	V5, V6 = 0.55V	●			±15	nA
$I_{CRT(UP)}$	CRT Pull-Up Current	V_{CRT} = GND	●	–1.4	–2	–2.6	µA
$I_{CRT(DN)}$	CRT Pull-Down Current	V_{CRT} = 1.3V	●	10	20	30	µA
t_{RST}	Reset Timeout Period	C_{RT} = 1500pF	●	2	3	4	ms
t_{UV}	V_n Undervoltage Detect to $\overline{RST}$	V_n Less Than Reset Threshold by More than 1%			150		µs
V_{OL}	Voltage Output Low $\overline{RST}$	I_{SINK} = 3mA, V_{CC} = 3V I_{SINK} = 100µA, V_{CC} = 1V	● ●		0.15 0.05	0.4 0.3	V V
V_{OH}	Voltage Output High $\overline{RST}$ (Note 5)	I_{SOURCE} = –1µA	●	V2-1			V
V_{IL}	$\overline{MR}$ Input Threshold Low	V_{CC} = 3.3V to 5.5V	●			0.4	V
V_{IH}	$\overline{MR}$ Input Threshold High	V_{CC} = 3.3V to 5.5V	●	1.6			V
t_{MRW}	$\overline{MR}$ Input Pulse Width	V_{CC} = 3.3V	●	150			ns
t_{MRD}	Manual Reset Propagation Delay	V_{CC} = 3.3V, V_{MR} Falling	●		0.1	1	µs
I_{MR}	$\overline{MR}$ Pull-Up Current	V_{MR} = 1V	●	–4	–10	–16	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive, all voltages are referenced to GND unless otherwise noted.

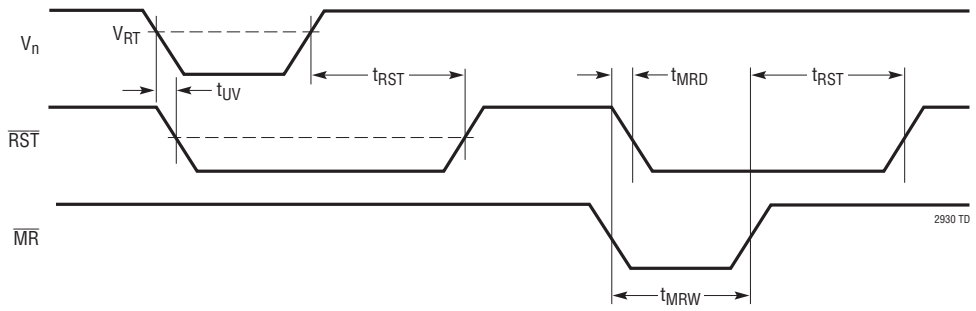
Note 3: The greater of V1, V2 is the internal supply voltage (V_{CC}).

Note 4: Under static no-fault conditions, V1 will necessarily supply quiescent current. If at any time V2 is larger than V1, V2 must be capable of supplying the quiescent current, programming (transient) current and reference load current.

Note 5: The output pin $\overline{RST}$ has a diode protected internal pull-up to V2 of typically 6µA. However, an external pull-up resistor may be used when faster rise times are required or for V_{OH} voltages greater than V2.

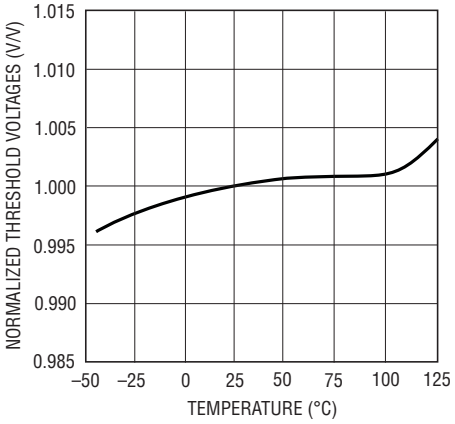
TIMING DIAGRAM

V_n Monitor Timing

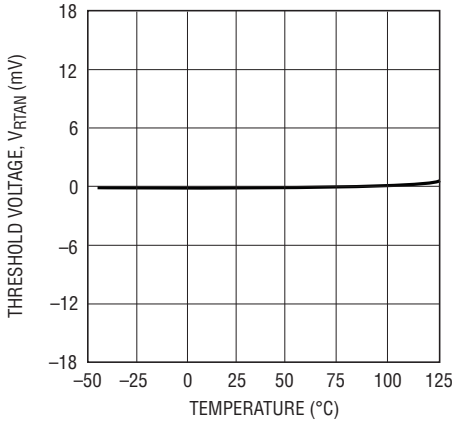


TYPICAL PERFORMANCE CHARACTERISTICS

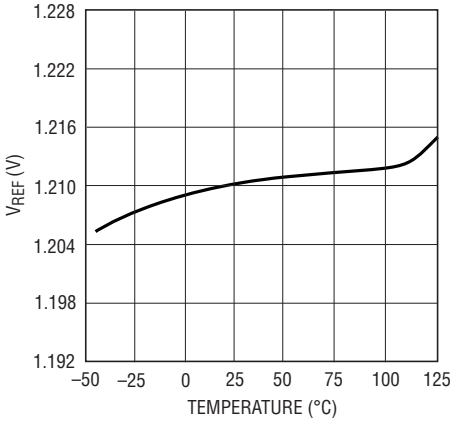
Normalized Threshold Voltages vs Temperature



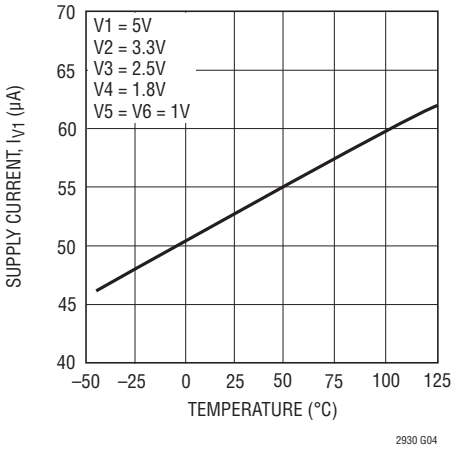
–ADJ Threshold Voltage vs Temperature



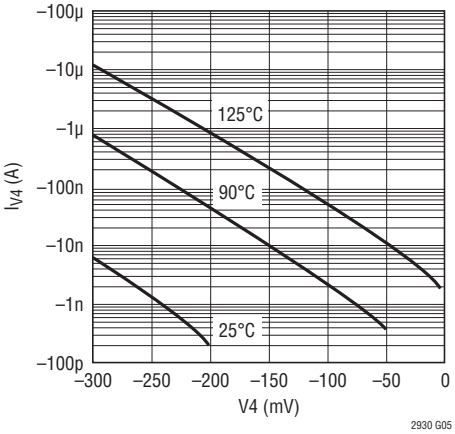
V_{REF} vs Temperature



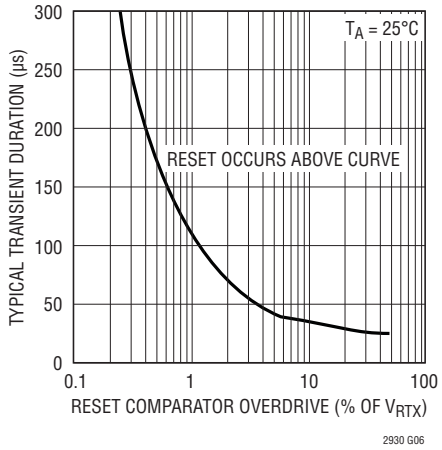
Supply Current vs Temperature



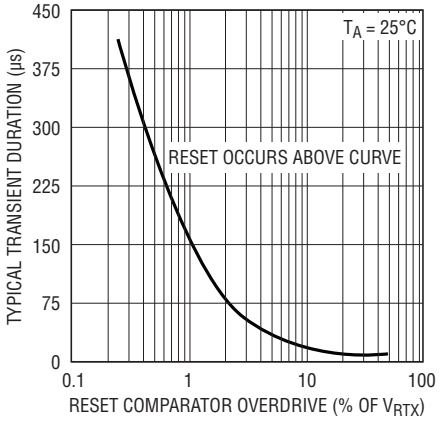
I(V4) vs V4 in Negative Adjust Mode



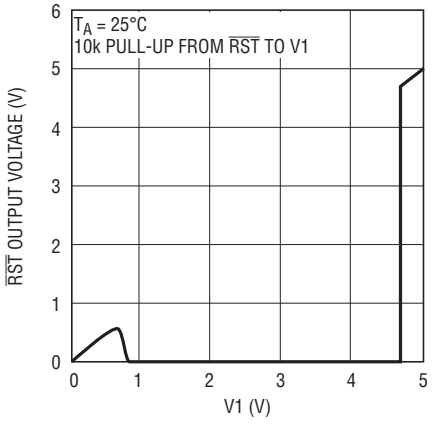
Transient Duration vs Comparator Overdrive (V1,V2)



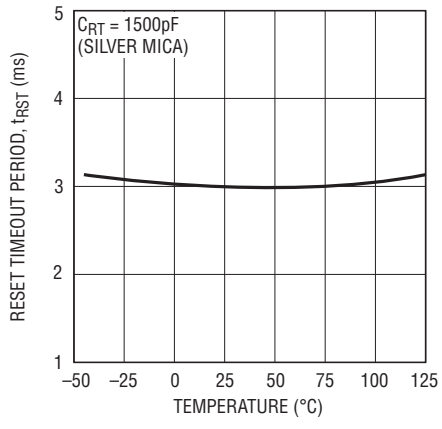
Transient Duration vs Comparator Overdrive (V3, V4, V5, V6)



$\overline{RST}$ Output Voltage vs V1, V_{PG} = GND

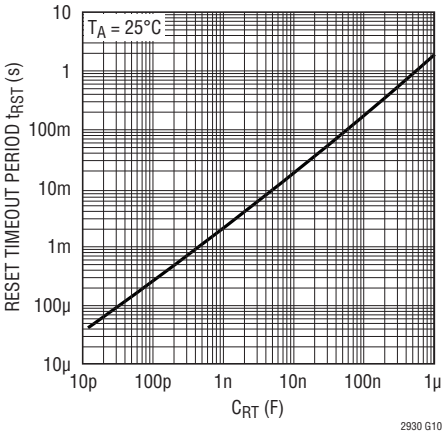


Reset Timeout Period vs Temperature

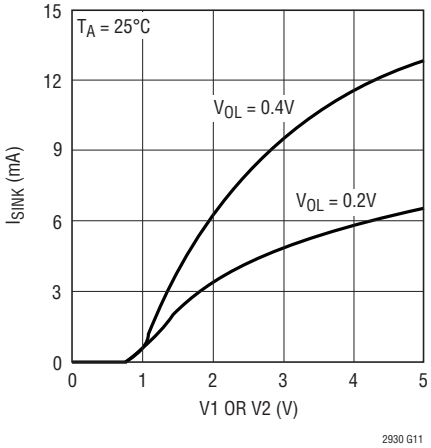


TYPICAL PERFORMANCE CHARACTERISTICS

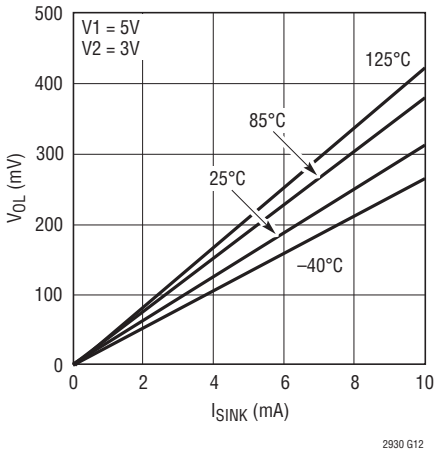
Reset Timeout Period vs C_{RT}



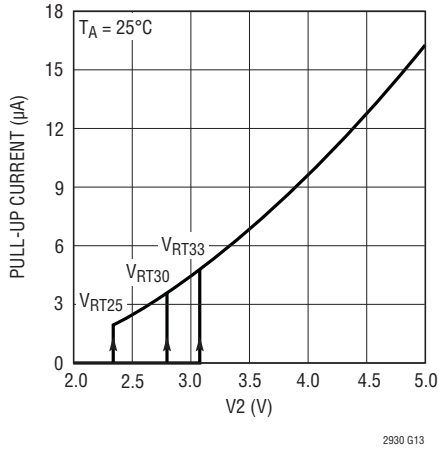
I_{SINK} vs Supply Voltage ($\overline{RST}$)



Voltage Output Low vs Output Sink Current ($\overline{RST}$)



$\overline{RST}$ Pull-Up Current vs V2



PIN FUNCTIONS

V5 (Pin 1): Adjustable Voltage Input 5. High impedance comparator input with 0.5V typical threshold. See Applications Information for details. Tie to V1 if unused.

V3 (Pin 2): Voltage Input 3. Select from 2.5V, 1.8V, 1.5V, or ADJ. See Applications Information for details. Tie to V1 if unused.

V1 (Pin 3): Voltage Input 1. Select from 5V or 3.3V. See Applications Information for details. The greater of V1 or V2 is also V_{CC} for the device. Bypass this pin to ground with a 0.1µF (or greater) capacitor.

CRT (Pin 4): Reset Timeout Capacitor. Attach an external capacitor (C_{RT}) to GND to set a reset timeout of 2ms/nF. Leaving the pin open generates a minimum delay of approximately 25µs. A 47nF capacitor generates a 94ms reset delay time.

$\overline{RST}$ (Pin 5): Reset Output. Logic output with weak 6µA pull-up to V2. Pulls low when any voltage input is below the reset threshold and held low for the configured delay time after all voltage inputs are above threshold. Use an external pull-up to pull greater than V2. Leave open if unused.

PIN FUNCTIONS

$\overline{MR}$ (Pin 6): Manual Reset Input. A logic low on this pin pulls $\overline{RST}$ low. When the $\overline{MR}$ pin returns high, $\overline{RST}$ returns high after the configured reset timeout if all six voltage inputs are above threshold. A weak internal pull-up allows the pin to be left open for normal monitor operation. When using a switch, the switch is debounced through the reset circuitry using the delay provided by the C_{RT} timing capacitor.

GND (Pin 7): Ground.

VPG (Pin 8): Threshold Select Input. Connect to an external 1% resistive divider between VREF and GND to select 1 of 16 combinations and/or ±adjustable voltage thresholds (See Table 1). Do not add capacitance on the VPG pin.

VREF (Pin 9): Buffered Reference Voltage Output. A 1.210V nominal reference used for the mode selection voltage (V_{PG}) and for the offset of negative adjustable applications. The buffered reference can source and sink up to 1mA. The reference can drive a bypass capacitor of up to 1000pF without oscillation.

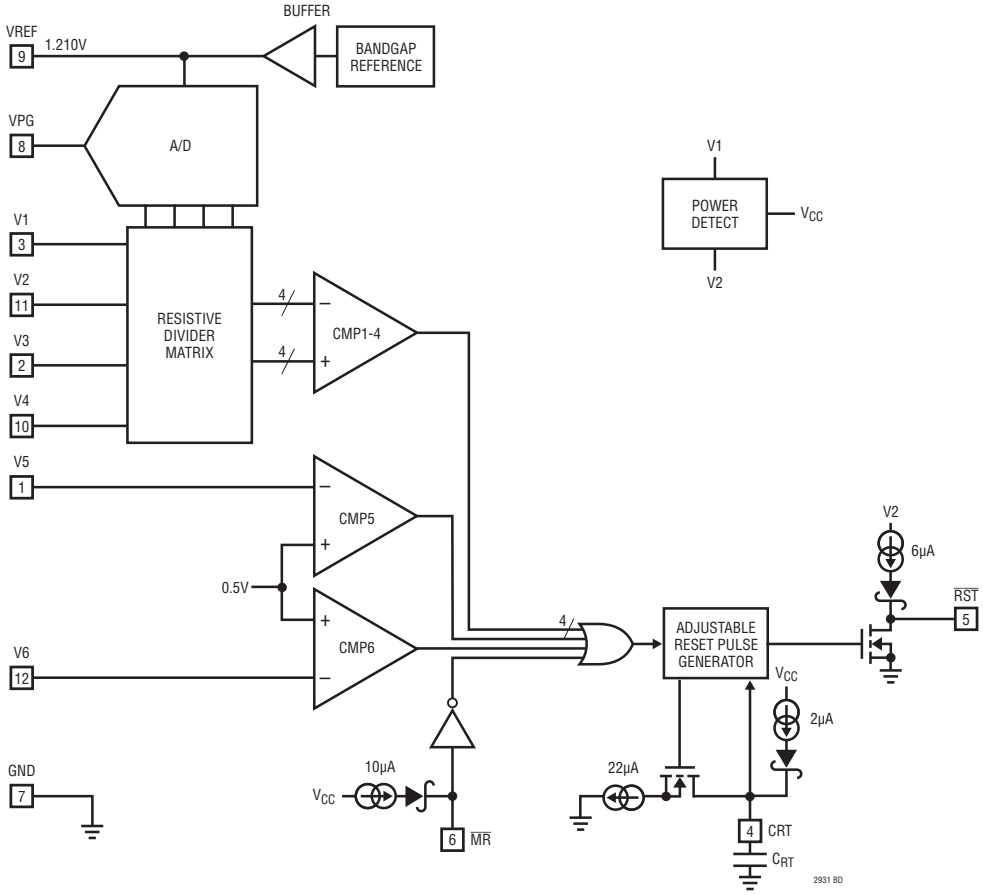
V4 (Pin 10): Voltage Input 4. Select from 1.8V, 1.5V, ADJ or –ADJ. See Applications Information for details. Tie to V1 if unused.

V2 (Pin 11): Voltage Input 2. Select from 3.3V, 3V or 2.5V. See Applications Information for details. The greater of V1, V2 is also V_{CC} for the device. Bypass this pin to ground with a 0.1µF (or greater) capacitor. $\overline{RST}$ is weakly pulled up to V2.

V6 (Pin 12): Adjustable Voltage Input 6. High impedance comparator input with 0.5V typical threshold. See Applications Information for details. Tie to V1 if unused.

Exposed Pad (Pin 13): Exposed pad may be left open or connected to device ground.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Supply Monitoring

The LTC2930 is a low power, high accuracy configurable six supply monitoring circuit with a common reset output. An external capacitor sets the reset timeout period. An external resistive divider between VREF, VPG and GND selects 1 of 16 possible input voltage monitor combinations. All six voltage inputs must be above their predetermined thresholds for the reset not to be activated. The LTC2930 asserts the reset output during power-up, power-down and brownout conditions on any one of the voltage inputs.

Power-Up

The greater of V1 and V2 serves as the internal supply voltage (V_{CC}). On power-up, V_{CC} powers the drive circuits for the $\overline{RST}$ pin. This ensures that the $\overline{RST}$ output will be low as soon as either V1 or V2 reaches 1V. The $\overline{RST}$ output remains low until the part is configured. Once voltage thresholds are set, if any of the supply monitor inputs is below its configured threshold, $\overline{RST}$ will be a logic low. Once all the monitor inputs rise above their thresholds, an internal timer is started and $\overline{RST}$ is released after the delay time. If V_{CC} < (V3 – 1.0V) and V_{CC} < 2.4V, the V3 input impedance will be low (10kΩ typical).

Threshold Accuracy

Consider a 5V system with ±5% tolerance. The 5V supply may vary between 4.75V to 5.25V. System ICs powered by this supply must operate reliably within this band (and a little more as explained below). A perfectly accurate supervisor for this supply generates a reset at exactly 4.75V, however no supervisor is this perfect. The actual reset threshold of a supervisor varies over a specified band; the LTC2930 varies ±1.5% around its nominal threshold voltage (see Figure 1) over temperature.

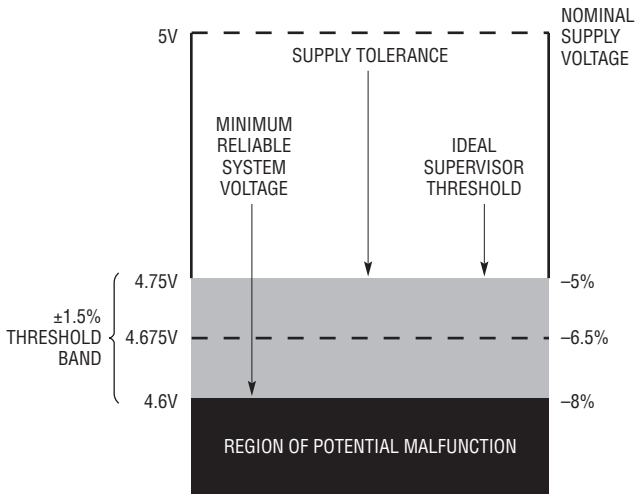


Figure 1. 1.5% Threshold Accuracy Improves System Reliability

Table 1. Voltage Threshold Modes*

MODE	V1 (V)	V2 (V)	V3 (V)	V4 (V)	R1 (kΩ)	R2 (kΩ)	$\frac{V_{PG}}{V_{REF}}$
0	5.0	3.3	ADJ	ADJ	Open	Short	0.000
1	5.0	3.3	ADJ	–ADJ	93.1	9.53	0.094
2	3.3	2.5	ADJ	ADJ	86.6	16.2	0.156
3	3.3	2.5	ADJ	–ADJ	78.7	22.1	0.219
4	3.3	2.5	1.5	ADJ	71.5	28.0	0.281
5	5.0	3.3	2.5	ADJ	66.5	34.8	0.344
6	5.0	3.3	2.5	1.8	59.0	40.2	0.406
7	5.0	3.3	2.5	1.5	53.6	47.5	0.469
8	5.0	3.0	2.5	ADJ	47.5	53.6	0.531
9	5.0	3.0	ADJ	ADJ	40.2	59.0	0.594
10	3.3	2.5	1.8	1.5	34.8	66.5	0.656
11	3.3	2.5	1.8	ADJ	28.0	71.5	0.719
12	3.3	2.5	1.8	–ADJ	22.1	78.7	0.781
13	5.0	3.3	1.8	–ADJ	16.2	86.6	0.844
14	5.0	3.3	1.8	ADJ	9.53	93.1	0.906
15	5.0	3.0	1.8	ADJ	Short	Open	1.000

*V5 and V6 are always adjustable (ADJ).

The reset threshold band and the power supply tolerance bands should not overlap. This prevents false or nuisance resets when the power supply is actually within its specified tolerance band.

The LTC2930 has a ±1.5% reset threshold accuracy, so a "5%" threshold is typically set to 6.5% below the nominal input voltage. Therefore, a typical 5V, "5%" threshold is 4.675V. The threshold is guaranteed to lie in the band between 4.750V and 4.600V over temperature. The powered system must work reliably down to the low end of the threshold band, or risk malfunction before a reset signal is properly issued.

A less accurate supervisor increases the required system voltage margin and increases the probability of system malfunction. The LTC2930 ±1.5% specification improves the reliability of the system over supervisors with wider threshold tolerances.

APPLICATIONS INFORMATION

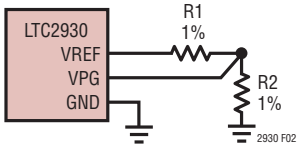


Figure 2. Mode Selection

Monitor Configuration

Select the LTC2930 input voltage combination by placing the recommended resistive divider from VREF to GND and connecting the tap point to VPG, as shown in Figure 2. Table 1 offers recommended 1% resistor values for each of the 16 modes. The last column in Table 1 specifies optimum V_{PG}/V_{REF} ratios (± 0.01), when configuring with a ratiometric DAC.

At power-up, once V1 or V2 reaches 2.4V, the monitor enters a setup period of approximately 150µs. During the setup time, the voltage on the VPG pin is sampled and the monitor is configured to the desired input combination. The comparators are enabled and supply monitoring begins. Do not add capacitance to the VPG pin.

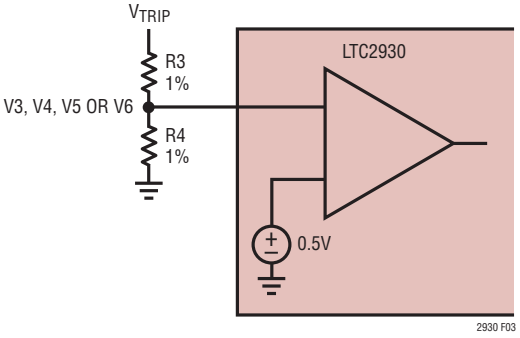


Figure 3. Setting the Positive Adjustable Trip Point

Using The Adjustable Thresholds

The reference inputs on the V3 and/or V4 comparators are set to 0.5V when the positive adjustable modes are selected (Figure 3). The reference inputs on the V5 and V6 comparators are always set to 0.5V. The tap point on an external resistive divider, connected between the positive voltage being sensed and ground, is connected to the high impedance, adjustable inputs (V3, V4, V5, V6). Calculate the trip voltage from:

Table 2. Suggested 1% Resistor Values for the ADJ Inputs

V_{SUPPLY} (V)	V_{TRIP} (V)	R3 (kΩ)	R4 (kΩ)
12	11.25	2150	100
10	9.4	1780	100
8	7.5	1400	100
7.5	7	1300	100
6	5.6	1020	100
5	4.725	845	100
3.3	3.055	511	100
3	2.82	464	100
2.5	2.325	365	100
1.8	1.685	237	100
1.5	1.410	182	100
1.2	1.120	124	100
1	0.933	86.6	100
0.9	0.840	68.1	100

*See Figure 3.

Table 3. Suggested 1% Resistor Values for the –ADJ Inputs

V_{SUPPLY} (V)	V_{TRIP} (V)	R3 (kΩ)	R4 (kΩ)
–2	–1.87	187	121
–5	–4.64	464	121
–5.2	–4.87	487	121
–10	–9.31	931	121
–12	–11.30	1130	121

*See Figure 4.

$$V_{TRIP} = 0.5V \bullet \left(1 + \frac{R3}{R4}\right)$$

In the negative adjustable mode, the reference level on the V4 comparator is connected to ground (Figure 4). The tap point on an external resistive divider, connected between the negative voltage being sensed and the VREF pin, is

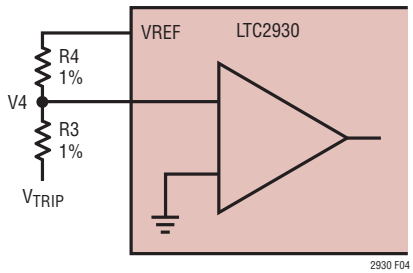


Figure 4. Setting the Negative Adjustable Trip Point

APPLICATIONS INFORMATION

connected to the high impedance adjustable input (V4). V_{REF} provides the necessary level shift required to operate at ground. The negative trip voltage is calculated from:

$$V_{TRIP} = -V_{REF} \bullet \frac{R3}{R4}; V_{REF} = 1.210V \text{ Nominal}$$

In a negative adjustable application, the minimum value for R4 is limited by the sourcing capability of VREF (±1mA). With no other load on VREF, R4 (minimum) is:

$$\frac{1.210V}{1mA} = 1.210k$$

Tables 2 and 3 offer suggested 1% resistor values for various positive and negative supply adjustable applications assuming 5% monitor thresholds.

Although all six supply monitor comparators have built-in glitch immunity, bypass capacitors on V1 and V2 are recommended because the greater of V1 or V2 is also the V_{CC} for the device. Filter capacitors on the V3, V4, V5 and V6 inputs are allowed.

Power-Down

On power-down, once any of the monitor inputs drops below its threshold, $\overline{RST}$ is held at a logic low. A logic low of 0.4V is guaranteed until both V1 and V2 drop below 1V. If the bandgap reference becomes invalid (V_{CC} < 2V typical), the LTC2930 will enter the 150µs setup period when V_{CC} rises above 2.4V max.

Selecting the Reset Timing Capacitor

The reset timeout period is adjustable in order to accommodate a variety of microprocessor applications. The reset timeout period, t_{RST}, is adjusted by connecting a capacitor, C_{RT}, between the CRT pin and ground. The value of this capacitor is determined by:

$$C_{RT} = \frac{t_{RST}}{2M\Omega} = 500\left[pF/ms\right] \bullet t_{RST}$$

Leaving the CRT pin unconnected generates a minimum reset timeout of approximately 25µs. Maximum reset timeout is limited by the largest available low leakage capacitor. The accuracy of the timeout period is affected by capacitor leakage (the nominal charging current is 2µA) and capacitor tolerance. A low leakage ceramic capacitor is recommended.

OR-ed System Reset

In Figure 5, two LTC2930s are configured to monitor 11 supply voltages simultaneously. The unused adjustable input pin is tied to the V1 input. The open-drain $\overline{RST}$ outputs are OR-tied and pulled up to 5V through a 10kΩ resistor. $\overline{RST}$ pulls high 94ms after all the inputs are above the threshold voltages. Should a reset event occur on either LTC2930, both $\overline{RST}$ outputs pull low. Similarly, if the manual reset pushbutton is pressed, both $\overline{RST}$ outputs also pull low.

Using a Pushbutton On/Off Controller with the LTC2930

In Figure 6, the LTC2950-1 pushbutton controller powers a system on and off. The system starts after the pushbutton is pressed, which brings the LTM4600's RUN pin high. Subsequently, the LTM4600 generates a 5V output which applies power to each of the four DC/DC converters.

The LTC2930 is configured to mode 13 (see Table 1). The voltages monitored are 5V, 3.3V, 1.8V, –5.2V, 2.5V and 12V.

If the $\overline{KILL}$ input is not driven high within 512ms of a valid turn-on event, EN pulls low shutting down the system. If the external 12V supply drops below 9.6V, EN pulls low, powering down the LTM4600 and subsequent circuitry. An external 4.7nF capacitor sets the 9.4ms reset timeout period. Therefore, 9.4ms after the last supply is above threshold, $\overline{RST}$ pulls high. The reset timing capacitor must be chosen to keep the reset timeout period below 512ms. Otherwise, the $\overline{KILL}$ timer will expire and shut down the system.

Pressing the pushbutton after the system is powered initiates the power off sequence. An interrupt is set, bringing EN low immediately and disabling the LTM4600.

APPLICATIONS INFORMATION

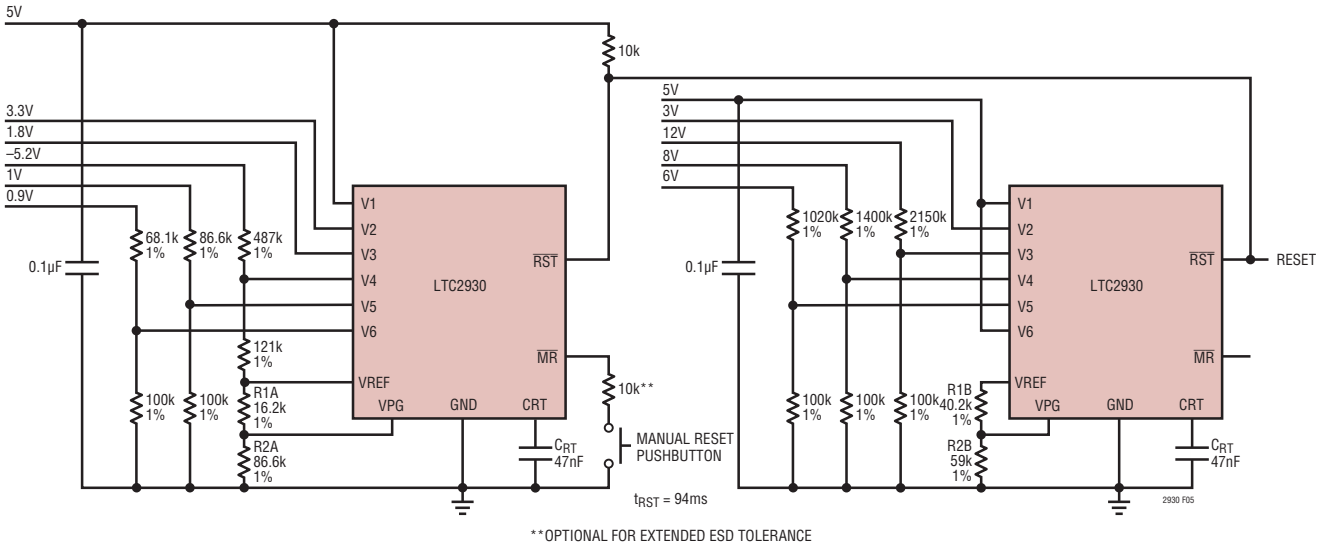


Figure 5. OR-ed System Reset

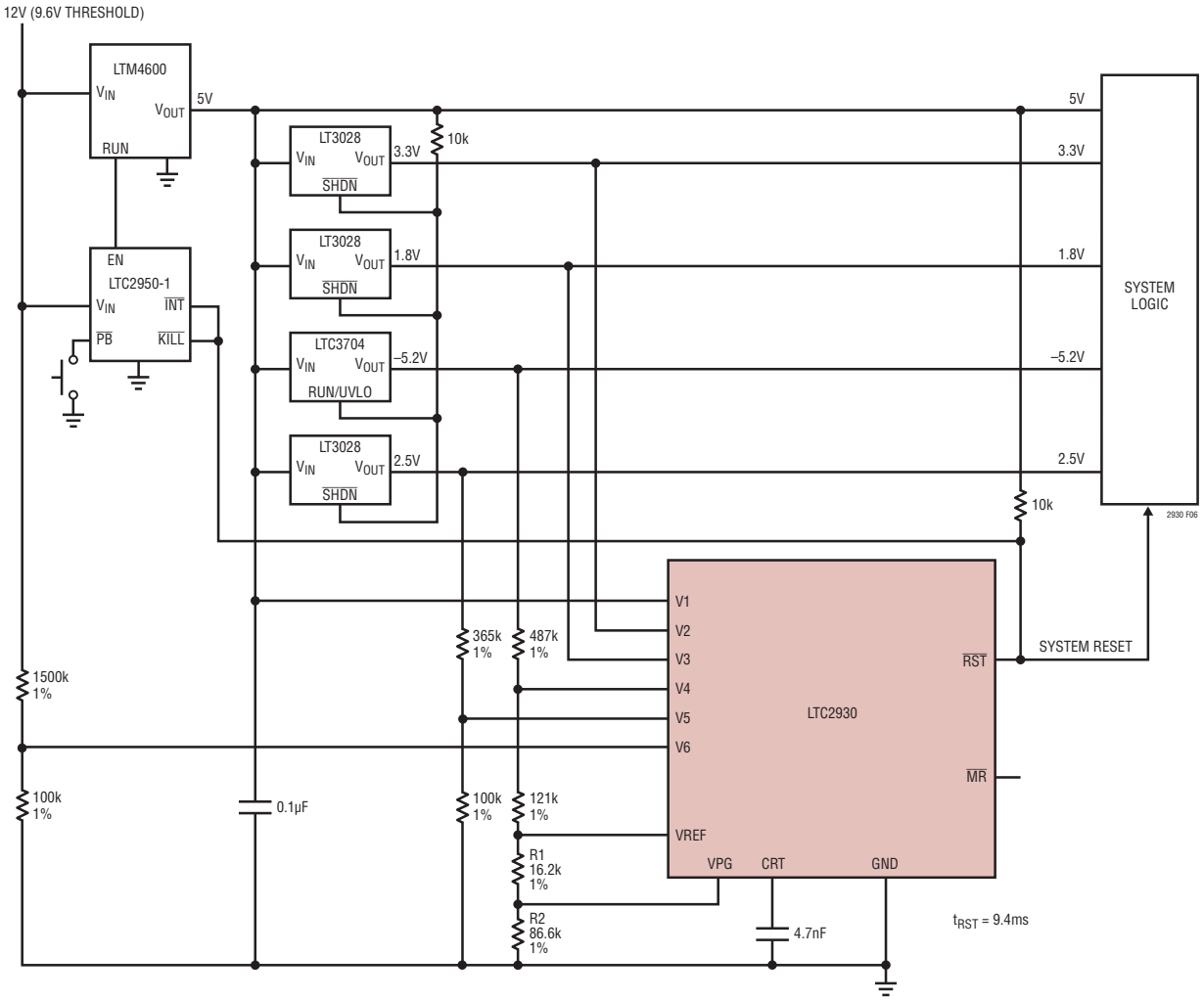
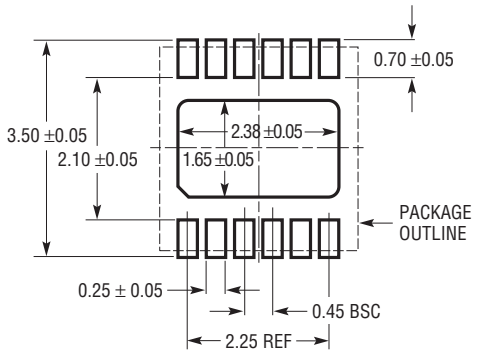


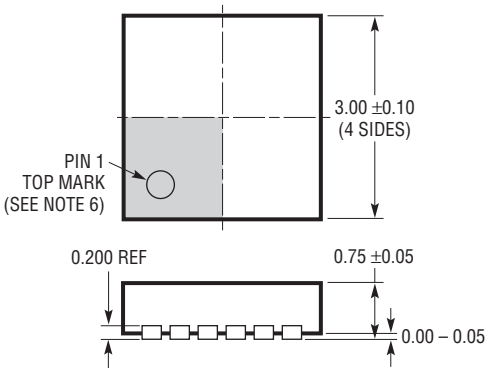
Figure 6. Using a Pushbutton On/Off Controller with the LTC2930

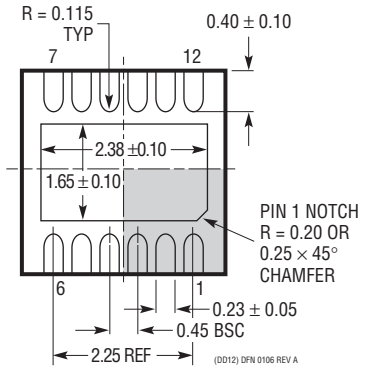
PACKAGE DESCRIPTION

DD Package
12-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1725 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



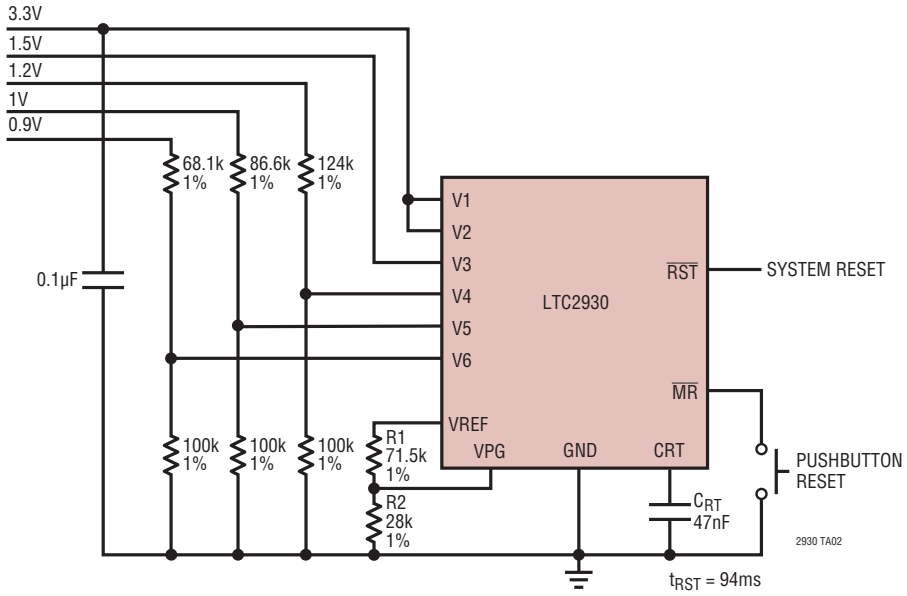


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD AND TIE BARS SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Five Supply Monitor, 5% Threshold (3.3V, 1.5V, 1.2V, 1V, 0.9V)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1326	Micropower Triple Supply Monitor for 5V/2.5V, 3.3V and ADJ	4.725V, 3.118V, 1V Threshold (±0.75%) and ADJ
LTC1728	Micropower Triple Supply Monitor with Open-Drain Reset	5-Lead SOT-23 Package
LTC2900	Programmable Quad Supply Monitor	Adjustable Reset, 10-Lead MSOP and DFN Packages
LTC2901	Programmable Quad Supply Monitor	Adjustable Reset and Watchdog Timer
LTC2902	Programmable Quad Supply Monitor	Adjustable Reset and Tolerance (5%, 7.5%, 10%, or 12.5%)
LTC2903	Precision Quad Supply Monitor	6-Lead SOT-23 Package
LTC2904-LTC2907	Three-State Programmable Precision Dual Supply Monitor	8-Lead SOT-23 and DFN Packages
LTC2908	Precision Six Supply Monitor (Four Fixed & Two Adjustable)	8-Lead TSOT-23 and DFN Packages
LTC2909	Precision Triple/Dual Input UV, OV and Negative Voltage Monitor	Shunt Regulated V_{CC} Pin, Adjustable Threshold and Reset, 8-Lead SOT-23 and DFN Packages
LTC2910	Precision Octal Positive/Negative Voltage Supply Monitor	16-Lead SSOP and 5mm × 3mm DFN Packages, H-Grade Temperature Range
LTC2912-LTC2914	Single/Dual/Quad UV and OV Voltage Monitors	Separate V_{CC} Pin, Adjustable Reset Timer, H-Grade Temperature Range
LTC2915-LTC2918	Single Supply Monitor with 27 Pin-Selectable Thresholds	Manual Reset, Watchdog, TSOT-8/MSOP-10 and 3mm × 2mm DFN Packages, H-Grade Temperature Range
LTC2928	Quad Power Supply Sequencer and Supervisor	Easily Configure Power Management without Software, 36-Lead 5mm × 7mm QFN and SSOP Packages
LTC2931	Configurable Six Supply Monitor with Individual Comparator Outputs	Adjustable Reset and Watchdog Timers, TSSOP-20 Package
LTC2932	Configurable Six Supply Monitor with Individual Comparator Outputs	Adjustable Reset Timer and Tolerance, TSSOP-20 Package, Pin-Selectable Tolerance (5%, 7.5%, 10%, or 12.5%), Reset Disable for Margining

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