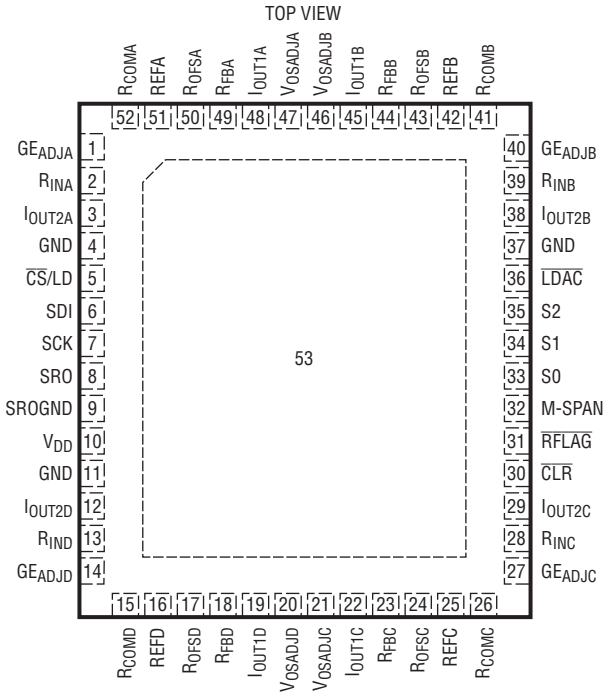
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

I_{OUT1X}, I_{OUT2X} to GND ..... ±0.3V
R_{INX}, R_{COMX}, REFX, R_{FBX}, R_{OFSX}, V_{OSADJX}, GE_{ADJX} to GND ..... ±18V
V_{DD} to GND ..... –0.3V to 7V
Digital Inputs and Outputs to GND ..... –0.3V to V_{DD}+0.3V (max 7V)
Operating Temperature Range
LTC2754C ..... 0°C to 70°C
LTC2754I ..... –40°C to 85°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2754CUKG-12#PBF	LTC2754CUKG-12#TRPBF	LTC2754UKG-12	52-Lead (7mm × 8mm) Plastic QFN	0°C to 70°C
LTC2754IUKG-12#PBF	LTC2754IUKG-12#TRPBF	LTC2754UKG-12	52-Lead (7mm × 8mm) Plastic QFN	–40°C to 85°C
LTC2754BCUKG-16#PBF	LTC2754BCUKG-16#TRPBF	LTC2754UKG-16	52-Lead (7mm × 8mm) Plastic QFN	0°C to 70°C
LTC2754BIUKG-16#PBF	LTC2754BIUKG-16#TRPBF	LTC2754UKG-16	52-Lead (7mm × 8mm) Plastic QFN	–40°C to 85°C
LTC2754ACUKG-16#PBF	LTC2754ACUKG-16#TRPBF	LTC2754UKG-16	52-Lead (7mm × 8mm) Plastic QFN	0°C to 70°C
LTC2754AIUKG-16#PBF	LTC2754AIUKG-16#TRPBF	LTC2754UKG-16	52-Lead (7mm × 8mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, V_{REF} = 5V unless otherwise specified. The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		LTC2754-12 MIN	LTC2754-12 TYP	LTC2754-12 MAX	LTC2754B-16 MIN	LTC2754B-16 TYP	LTC2754B-16 MAX	LTC2754A-16 MIN	LTC2754A-16 TYP	LTC2754A-16 MAX	UNITS
Static Performance													
	Resolution		●	12			16			16			Bits
	Monotonicity		●	12			16			16			Bits
DNL	Differential Nonlinearity		●			±1			±1		±0.2	±1	LSB
INL	Integral Nonlinearity		●			±1			±2		±0.4	±1	LSB
GE	Gain Error	All Output Ranges	●		±0.5	±2			±20		±2	±12	LSB
	Gain Error Temperature Coefficient	ΔGain/ΔTemp			±1			±1			±1		ppm/°C
BZE	Bipolar Zero Error	All Bipolar Ranges	●		±0.2	±1			±12		±1	±8	LSB
	Bipolar Zero Temperature Coefficient				±0.5			±0.5			±0.5		ppm/°C
PSR	Power Supply Rejection	V_{DD} = 5V, ±10% V_{DD} = 3V, ±10%	● ●			±0.025 ±0.06			±0.4 ±1		±0.03 ±0.1	±0.2 ±0.5	LSB/V LSB/V
I_{LKG}	I_{OUT1} Leakage Current	T_A = 25°C T_{MIN} to T_{MAX}	 ●		±0.05	±2 ±5		±0.05	±2 ±5		±0.05	±2 ±5	nA nA

V_{DD} = 5V, V_{REF} = 5V unless otherwise specified. The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Analog Pins							
	Reference Inverting Resistors	(Note 4)	●	16	20		kΩ
R_{REF}	DAC Input Resistance		●	8	10		kΩ
R_{FB}	Feedback Resistors	(Note 3)	●	8	10		kΩ
R_{OFS}	Bipolar Offset Resistors	(Note 3)	●	16	20		kΩ
R_{VOSADJ}	Offset Adjust Resistors		●	1024	1280		kΩ
R_{GEADJ}	Gain Adjust Resistors		●	2048	2560		kΩ
C_{IOUT1}	Output Capacitance	Full-Scale Zero-Scale			75 45		pF
Dynamic Performance							
	Output Settling Time	0V to 10V Range, 10V Step. To ±0.0015% FS (Note 5)			2		µs
	Glitch Impulse	V_{DD} = 5V (Note 6) V_{DD} = 3V (Note 6)			1.25 0.26		nV•s nV•s
	Digital-to-Analog Glitch Impulse	(Note 7)			2		nV•s
	Reference Multiplying BW	0V to 5V Range, V_{REF} = $3V_{RMS}$, Code = Full Scale, –3dB BW			2		MHz
	Multiplying Feedthrough Error	0V to 5V Range, V_{REF} = ±10V, 10kHz Sine Wave			0.5		mV
	Analog Crosstalk	(Note 8)			–109		dB
THD	Total Harmonic Distortion	(Note 9) Multiplying			–110		dB
	Output Noise Voltage Density	(Note 10) at I_{OUT1}			13		nV/√Hz

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, V_{REF} = 5V unless otherwise specified. The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
V_{DD}	Supply Voltage		●	2.7		5.5	V
I_{DD}	Supply Current, V_{DD}	Digital Inputs = 0V or V_{DD}	●		0.5	1	µA
Digital Inputs							
V_{IH}	Digital Input High Voltage	3.3V ≤ V_{DD} ≤ 5.5V 2.7V ≤ V_{DD} < 3.3V	● ●	2.4 2			V V
V_{IL}	Digital Input Low Voltage	4.5V < V_{DD} ≤ 5.5V 2.7V ≤ V_{DD} ≤ 4.5V	● ●			0.8 0.6	V V
	Hysteresis Voltage				0.1		V
I_{IN}	Digital Input Current	V_{IN} = GND to V_{DD}	●			±1	µA
C_{IN}	Digital Input Capacitance	V_{IN} = 0V (Note 11)	●			6	pF
Digital Outputs							
V_{OH}	I_{OH} = 200µA	2.7V ≤ V_{DD} ≤ 5.5V	●	V_{DD} – 0.4			V
V_{OL}	I_{OL} = 200µA	2.7V ≤ V_{DD} ≤ 5.5V	●			0.4	V

TIMING CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} = 4.5V to 5.5V							
t_1	SDI Valid to SCK Set-Up		●	7			ns
t_2	SDI Valid to SCK Hold		●	7			ns
t_3	SCK High Time		●	11			ns
t_4	SCK Low Time		●	11			ns
t_5	$\overline{CS}$/LD Pulse Width		●	9			ns
t_6	LSB SCK High to $\overline{CS}$/LD High		●	4			ns
t_7	$\overline{CS}$/LD Low to SCK Positive Edge		●	4			ns
t_8	$\overline{CS}$/LD High to SCK Positive Edge		●	4			ns
t_9	SRO Propagation Delay	C_{LOAD} = 10pF	●			18	ns
t_{10}	$\overline{CLR}$ Pulse Width Low		●	36			ns
t_{11}	$\overline{LDAC}$ Pulse Width Low		●	15			ns
t_{12}	$\overline{CLR}$ Low to $\overline{RFLAG}$ Low	C_{LOAD} = 10pF (Note 11)	●			50	ns
t_{13}	$\overline{CS}$/LD High to $\overline{RFLAG}$ High	C_{LOAD} = 10pF (Note 11)	●			40	ns
	SCK Frequency	50% Duty Cycle (Note 12)	●			40	MHz
V_{DD} = 2.7V to 3.3V							
t_1	SDI Valid to SCK Set-Up		●	9			ns
t_2	SDI Valid to SCK Hold	(Note 11)	●	9			ns
t_3	SCK High Time	C_L = 10pF	●	15			ns
t_4	SCK Low Time		●	15			ns
t_5	$\overline{CS}$/LD Pulse Width		●	12			ns
t_6	LSB SCK High to $\overline{CS}$/LD High		●	5			ns

TIMING CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_7	$\overline{CS}$/LD Low to SCK Positive Edge		●	5			ns
t_8	$\overline{CS}$/LD High to SCK Positive Edge		●	5			ns
t_9	SRO Propagation Delay	C_{LOAD} = 10pF	●			26	ns
t_{10}	$\overline{CLR}$ Pulse Width Low		●	60			ns
t_{11}	$\overline{LDAC}$ Pulse Width Low		●	20			ns
t_{12}	$\overline{CLR}$ Low to $\overline{RFLAG}$ Low	C_{LOAD} = 10pF (Note 11)	●			70	ns
t_{13}	$\overline{CS}$/LD High to $\overline{RFLAG}$ high	C_{LOAD} = 10pF (Note 11)	●			60	ns
	SCK Frequency	50% Duty Cycle (Note 12)	●			25	MHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 3: Because of the proprietary SoftSpan switching architecture, the measured resistance looking into each of the specified pins is constant for all output ranges if the I_{OUT1X} and I_{OUT2X} pins are held at ground.

Note 4: Input resistors measured from R_{INX} to R_{COMX}; feedback resistors measured from R_{COMX} to REFX.

Note 5: Using LT1469 with $C_{FEEDBACK}$ = 15pF. A ±0.0015% settling time of 1.7µs can be achieved by optimizing the time constant on an individual basis. See Application Note 74, Component and Measurement Advances Ensure 16-Bit DAC Settling Time.

Note 6: Measured at the major carry transition, 0V to 5V range. Output amplifier: LT1469; C_{FB} = 27pF.

Note 7. Full-scale transition; REF = 0V.

Note 8. Analog Crosstalk is defined as the AC voltage ratio V_{OUTB}/V_{REFA}, expressed in dB. REFB is grounded, and DAC B is set to 0V-5V span and zero-, mid- or full- scale code. V_{REFA} is a $3V_{RMS}$, 1kHz sine wave. Crosstalk between other DAC channels is similar or better.

Note 9. REF = $6V_{RMS}$ at 1kHz. 0V to 5V range. DAC code = FS. Output amplifier = LT1469.

Note 10. Calculation from $V_n = \sqrt{4kTRB}$, where k = 1.38E-23 J/°K (Boltzmann constant), R = resistance (Ω), T = temperature (°K), and B = bandwidth (Hz). 0V to 5V Range; zero-, mid-, or full- scale.

Note 11. Guaranteed by design, not subject to test.

Note 12. When using SRO, maximum SCK frequency f_{MAX} is limited by SRO propagation delay t_9 as follows:

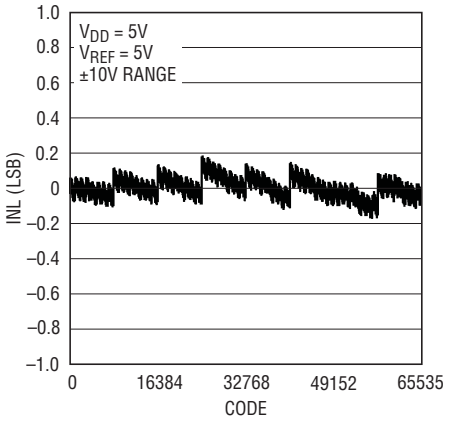
$$f_{MAX} = \left(\frac{1}{2(t_9 + t_S)}\right)$$, where t_S is the setup time of the receiving device.

TYPICAL PERFORMANCE CHARACTERISTICS

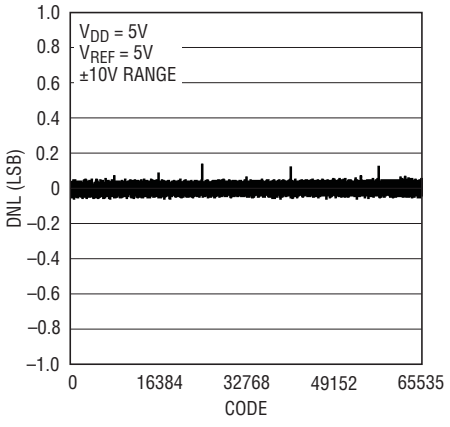
T_A = 25°C, unless otherwise noted.

LTC2754-16

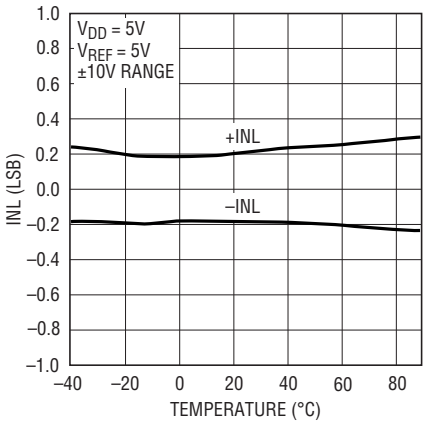
Integral Nonlinearity (INL)



Differential Nonlinearity (DNL)



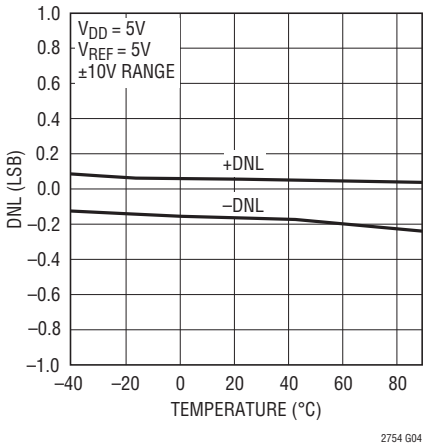
INL vs Temperature



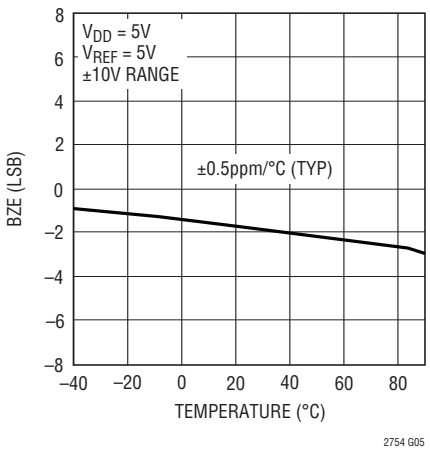
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

LTC2754-16

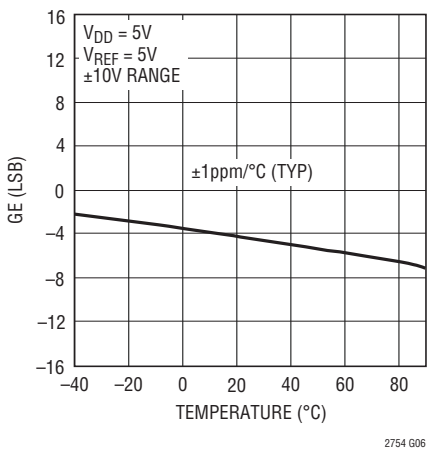
DNL vs Temperature



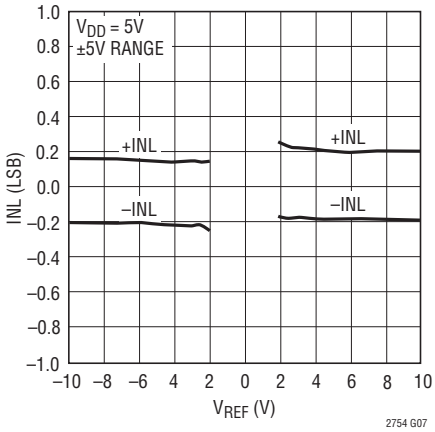
Bipolar Zero vs Temperature



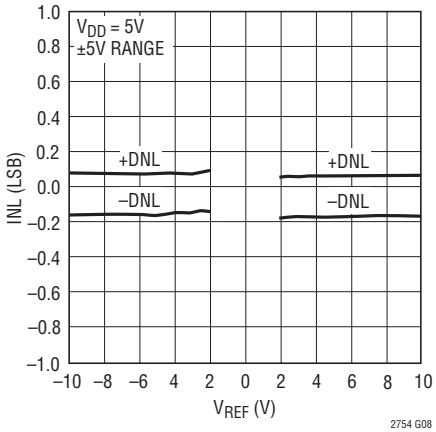
Gain Error vs Temperature



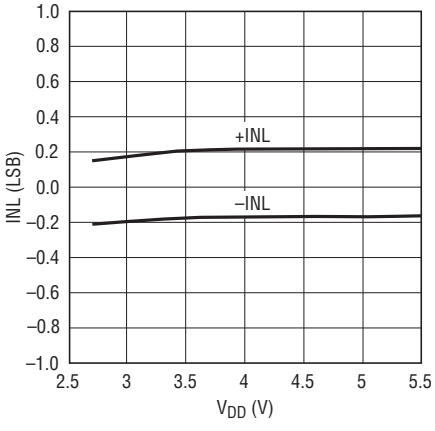
INL vs V_{REF}



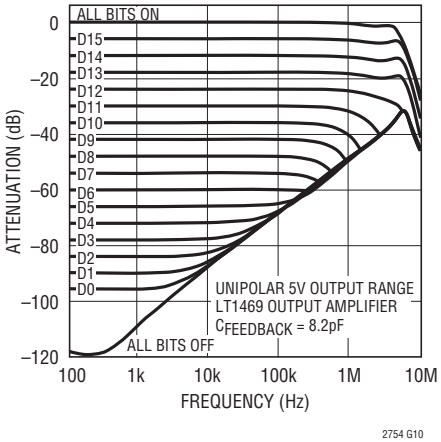
DNL vs V_{REF}



INL vs V_{DD}



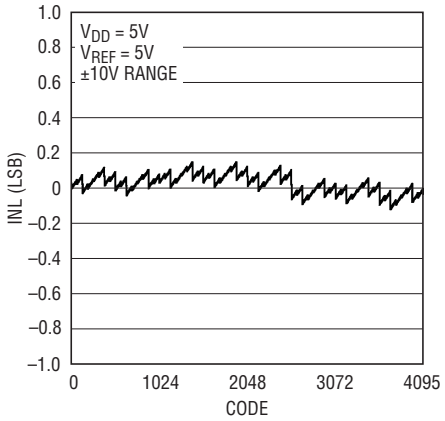
Multiplying Frequency Response vs Digital Code



TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

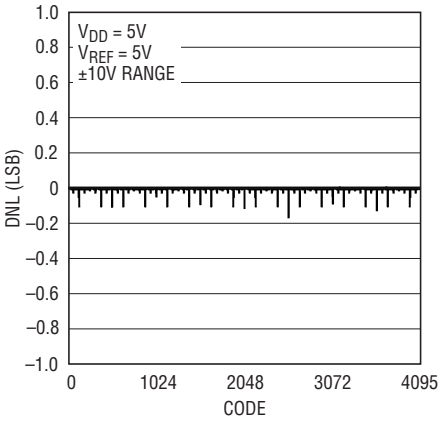
LTC2754-12

Integral Nonlinearity (INL)



2754 G11

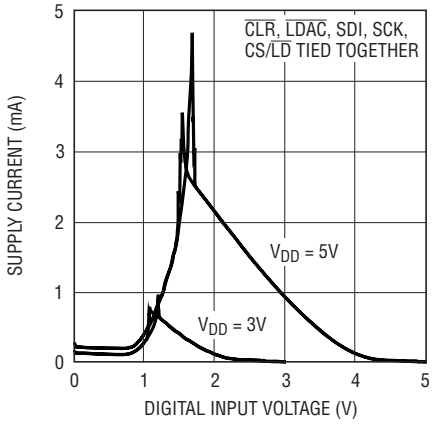
Differential Nonlinearity (DNL)



2754 G12

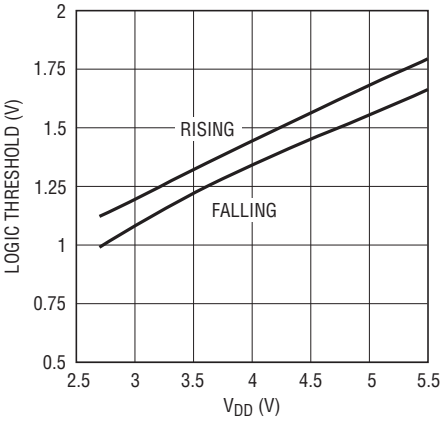
LTC2754

Supply Current vs Logic Input Voltage



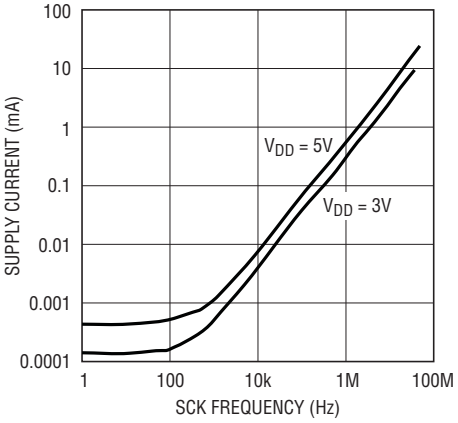
2754 G13

Logic Threshold vs Supply Voltage



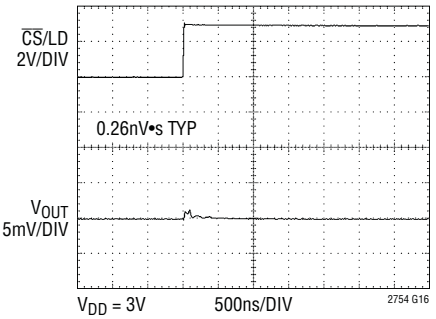
2754 G14

Supply Current vs Clock Frequency



2754 G15

Midscale Glitch

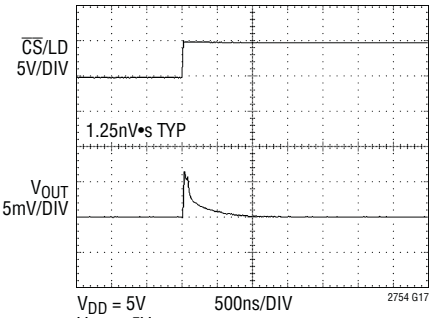


2754 G16

V_{DD} = 3V 500ns/DIV
V_{REF} = 5V
5V RANGE
LT1468 OUTPUT AMPLIFIER
$C_{FEEDBACK}$ = 27pF

RISING MAJOR CARRY TRANSITION.
FALLING TRANSITION IS SIMILAR OR BETTER

Midscale Glitch

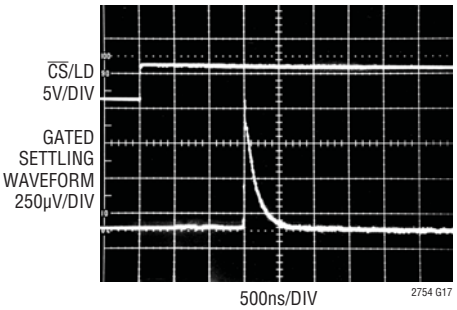


2754 G17

V_{DD} = 5V 500ns/DIV
V_{REF} = 5V
5V RANGE
LT1468 OUTPUT AMPLIFIER
$C_{FEEDBACK}$ = 27pF

RISING MAJOR CARRY TRANSITION.
FALLING TRANSITION IS SIMILAR OR BETTER

Settling 0V to 10V



2754 G17

USING LT1469 AMP
$C_{FEEDBACK}$ = 12pF
0V TO 10V STEP

PIN FUNCTIONS

GE_{ADJA} (Pin1): Gain Adjust Pin for DAC A. This control pin can be used to null gain error or to compensate for reference errors. Nominal adjustment range is ±512 LSB (LTC2754-16) for a voltage input range of $\pm V_{RINA}$ (i.e., ±5V for a 5V reference input). Tie to ground if not used.

R_{INA} (Pin 2): Input Resistor for Reference Inverting Amplifier. The 20k input resistor is connected internally from R_{INA} to R_{COMA}. For normal operation tie R_{INA} to the external reference voltage V_{REFA} (see Typical Applications). Any or all of these precision-matched resistor sets (Each set comprising R_{INX}, R_{COMX} and REFX) may be used to invert one or more positive reference voltages to the negative voltages needed by the DACs. Typically 5V; accepts up to ±15V.

I_{OUT2A} (Pin 3): DAC A Current Output Complement. Tie I_{OUT2A} to ground.

GND (Pin 4): Ground; provides shielding for I_{OUT2A}. Tie to ground.

$\overline{CS}$/LD (Pin 5): Synchronous Chip Select and Load Pin.

SDI (Pin 6): Serial Data Input. Data is clocked in on the rising edge of the serial clock (SCK) when $\overline{CS}$/LD is low.

SCK (Pin 7): Serial Clock.

SRO (Pin 8): Serial Readback Output. Data is clocked out on the falling edge of SCK. Readback data begins clocking out after the last address bit A0 is clocked in. SRO is an active output only when the chip is selected (i.e., when $\overline{CS}$/LD is low). Otherwise SRO presents a high-impedance output in order to allow other parts to control the bus.

SROGND (Pin 9): Ground pin for SRO. Tie to ground.

V_{DD} (Pin 10): Positive Supply Input; $2.7V \le V_{DD} \le 5.5V$. Bypass with a 0.1µF low-ESR ceramic capacitor to ground.

GND (Pin 11): Ground. Tie to ground.

I_{OUT2D} (Pin 12): DAC D Current Output Complement. Tie I_{OUT2D} to ground.

R_{IND} (Pin 13): Input Resistor for Reference Inverting Amplifier. The 20k input resistor is connected internally from R_{IND} to R_{COMD}. For normal operation tie R_{IND} to the external reference voltage V_{REFD} (see Typical Applications). Any or all of these precision-matched resistor sets (Each set comprising R_{INX}, R_{COMX} and REFX) may be used to invert one or more positive reference voltages to the negative voltages needed by the DACs. Typically 5V; accepts up to ±15V.

GE_{ADJD} (Pin 14): Gain Adjust Pin for DAC D. This control pin can be used to null gain error or to compensate for reference errors. Nominal adjustment range is ±512 LSB (LTC2754-16) for a voltage input range of $\pm V_{RIND}$ (i.e., ±5V for a 5V reference input). Tie to ground if not used.

R_{COMD} (Pin 15): Center Tap Point for Reference Amplifier Inverting Resistors. The 20k reference inverting resistors are connected internally from R_{IND} to R_{COMD} and from R_{COMD} to REFD, respectively (see Block Diagram). For normal operation tie R_{COMD} to the negative input of external reference inverting amplifier (see Typical Applications).

REFD (Pin 16): Inverted Reference Voltage for DAC D, with internal connection to the reference inverting resistor. The 20k resistor is connected internally from REFD to R_{COMD}. For normal operation tie this pin to the output of reference inverting amplifier (see Typical Applications). Typically –5V; accepts up to ±15V. The impedance looking into this pin is 10k to ground (R_{IND} and R_{COMD} floating).

R_{OFSD} (Pin 17): Bipolar Offset Network for DAC D. This pin provides the translation of the output voltage range for bipolar spans. Accepts up to ±15V; for normal operation tie to the positive reference voltage at R_{IND} (Pin 13). The impedance looking into this pin is 20k to ground.

R_{FBD} (Pin 18): DAC D Feedback Resistor. For normal operation tie to the output of the I/V converter amplifier for DAC D (see Typical Applications). The DAC output current from I_{OUT1D} flows through the feedback resistor to the R_{FBD} pin. The impedance looking into this pin is 10k to ground.

I_{OUT1D} (Pin 19): DAC D Current Output. This pin is a virtual ground when the DAC is operating and should reside at 0V. For normal operation tie to the negative input of the I/V converter amplifier for DAC D (see Typical Applications).

PIN FUNCTIONS

V_{OSADJD} (Pin 20): DAC D Offset Adjust Pin. This control pin can be used to null unipolar offset or bipolar zero error. The offset voltage delta is inverted and attenuated such that a 5V control voltage applied to V_{OSADJD} produces ΔV_{OS} = -512 LSB (LTC2754-16) in any output range (assumes a 5V reference voltage at R_{IND}). Tie to ground if not used.

V_{OSADJC} (Pin 21): DAC C Offset Adjust Pin. This control pin can be used to null unipolar offset or bipolar zero error. The offset voltage delta is inverted and attenuated such that a 5V control voltage applied to V_{OSADJC} produces ΔV_{OS} = -512 LSB (LTC2754-16) in any output range (assumes a 5V reference voltage at R_{INC}). Tie to ground if not used.

I_{OUT1C} (Pin 22): DAC C Current Output. This pin is a virtual ground when the DAC is operating and should reside at 0V. For normal operation tie to the negative input of the I/V converter amplifier for DAC C (see Typical Applications).

R_{FBC} (Pin 23): DAC C Feedback Resistor. For normal operation tie to the output of the I/V converter amplifier for DAC C (see Typical Applications). The DAC output current from I_{OUT1D} flows through the feedback resistor to the R_{FBC} pin. The impedance looking into this pin is 10k to ground.

R_{OFSC} (Pin 24): Bipolar Offset Network for DAC C. This pin provides the translation of the output voltage range for bipolar spans. Accepts up to ±15V; for normal operation tie to the positive reference voltage at R_{INC} (Pin 28). The impedance looking into this pin is 20k to ground.

REFC (Pin 25): Inverted Reference Voltage for DAC C, with internal connection to the reference inverting resistor. The 20k resistor is connected internally from REFC to R_{COMC}. For normal operation tie this pin to the output of reference inverting amplifier (see Typical Applications). Typically –5V; accepts up to ±15V. The impedance looking into this pin is 10k to ground (R_{INC} and R_{COMC} floating).

R_{COMC} (Pin 26): Center Tap Point for Reference Amplifier Inverting Resistors. The 20k reference inverting resistors are connected internally from R_{INC} to R_{COMC} and from R_{COMC} to REFC, respectively (see Block Diagram). For normal operation tie R_{COMC} to the negative input of external reference inverting amplifier (see Typical Applications).

GE_{ADJC} (Pin 27): Gain Adjust Pin for DAC C. This control pin can be used to null gain error or to compensate for reference errors. Nominal adjustment range is ±512 LSB (LTC2754-16) for a voltage input range of $\pm V_{RINC}$ (i.e., ±5V for a 5V reference input). Tie to ground if not used.

R_{INC} (Pin 28): Input Resistor for Reference Inverting Amplifier. The 20k input resistor is connected internally from R_{INC} to R_{COMC}. For normal operation tie R_{INC} to the external reference voltage V_{REFC} (see Typical Applications). Any or all of these precision-matched resistor sets (Each set comprising R_{INX}, R_{COMX} and R_{EFX}) may be used to invert one or more positive reference voltages to the negative voltages needed by the DACs. Typically 5V; accepts up to ±15V.

I_{OUT2C} (Pin 29): DAC C Current Output Complement. Tie I_{OUT2C} to ground.

$\overline{CLR}$ (Pin 30): Asynchronous Clear Pin. When this pin is low, all DAC registers (both code and span) are cleared to zero. All DAC outputs are cleared to zero volts.

$\overline{RFLAG}$ (Pin 31): Reset Flag Pin. An active low output is asserted when there is a power-on reset or a clear event. Returns high when an Update command is executed.

M-SPAN (Pin 32): Manual Span Control Pin. M-SPAN is used in conjunction with pins S2, S1 and S0 (Pins 33, 34 and 35) to configure all DACs for operation in a single, fixed output range.

To configure the part for manual-span use, tie M-SPAN directly to V_{DD}. The active output range is then set via hardware pin strapping of pins S2, S1 and S0 (rather than through the SPI port); and Write and Update commands have no effect on the active output span.

To configure the part for SoftSpan use, tie M-SPAN directly to GND. The output ranges are then individually and dynamically controllable through the SPI port; and pins S2, S1 and S0 have no effect.

See 'Manual Span Configuration' in the Operation section. M-SPAN must be connected either directly to GND (SoftSpan configuration) or to V_{DD} (manual-span configuration).

PIN FUNCTIONS

S0 (Pin 33): Span Bit 0. In Manual Span mode (M-SPAN tied to V_{DD}), Pins S0, S1 and S2 are pin-strapped to select a single fixed output range for all DACs. These pins should be tied to either GND or V_{DD} even if they are unused.

S1 (Pin 34): Span Bit 1. In Manual Span mode (M-SPAN tied to V_{DD}), Pins S0, S1 and S2 are pin-strapped to select a single fixed output range for all DACs. These pins should be tied to either GND or V_{DD} even if they are unused.

S2 (Pin 35): Span Bit 2. In Manual Span mode (M-SPAN tied to V_{DD}), Pins S0, S1 and S2 are pin-strapped to select a single fixed output range for all DACs. These pins should be tied to either GND or V_{DD} even if they are unused.

$\overline{\text{LDAC}}$ (Pin 36): Asynchronous DAC Load Input. When $\overline{\text{LDAC}}$ is a logic low, all DACs are updated ($\overline{\text{CS}}$/LD must be high).

GND (Pin 37): Ground; provides shielding for I_{OUT2B}. Tie to ground.

I_{OUT2B} (Pin 38): DAC B Current Output Complement. Tie I_{OUT2B} to ground.

R_{INB} (Pin 39): Input Resistor for Reference Inverting Amplifier. The 20k input resistor is connected internally from R_{INB} to R_{COMB}. For normal operation tie R_{INB} to the external reference voltage V_{REFB} (see Typical Applications). Any or all of these precision-matched resistor sets (Each set comprising R_{INX}, R_{COMX} and REFX) may be used to invert one or more positive reference voltages to the negative voltages needed by the DACs. Typically 5V; accepts up to ±15V.

GE_{ADJB} (Pin 40): Gain Adjust Pin for DAC B. This control pin can be used to null gain error or to compensate for reference errors. Nominal adjustment range is ±512 LSB (LTC2754-16) for a voltage input range of $\pm V_{RINB}$ (i.e., ±5V for a 5V reference input). Tie to ground if not used.

R_{COMB} (Pin 41): Center Tap Point for Reference Amplifier Inverting Resistors. The 20k reference inverting resistors are connected internally from R_{INB} to R_{COMB} and from R_{COMB} to REFB, respectively (see Block Diagram). For normal operation tie R_{COMB} to the negative input of external reference inverting amplifier (see Typical Applications).

REFB (Pin 42): Inverted Reference Voltage for DAC B, with internal connection to the reference inverting resistor. The 20k resistor is connected internally from REFB to R_{COMB}. For normal operation tie this pin to the output of reference inverting amplifier (see Typical Applications). Typically –5V; accepts up to ±15V. The impedance looking into this pin is 10k to ground (R_{INB} and R_{COMB} floating).

R_{OFSB} (Pin 43): Bipolar Offset Network for DAC B. This pin provides the translation of the output voltage range for bipolar spans. Accepts up to ±15V; for normal operation tie to the positive reference voltage at R_{INB} (Pin 39). The impedance looking into this pin is 20k to ground.

R_{FBB} (Pin 44): DAC B Feedback Resistor. For normal operation tie to the output of the I/V converter amplifier for DAC B (see Typical Applications). The DAC output current from I_{OUT1B} flows through the feedback resistor to the R_{FBB} pin. The impedance looking into this pin is 10k to ground.

I_{OUT1B} (Pin 45): DAC B Current Output. This pin is a virtual ground when the DAC is operating and should reside at 0V. For normal operation tie to the negative input of the I/V converter amplifier for DAC B (see Typical Applications).

V_{OSADJB} (Pin 46): DAC B Offset Adjust Pin. This control pin can be used to null unipolar offset or bipolar zero error. The offset-voltage delta is inverted and attenuated such that a 5V control voltage applied to V_{OSADJB} produces ΔV_{OS} = –512 LSB (LTC2754-16) in any output range (assumes a 5V reference voltage at R_{INB}). Tie to ground if not used.

V_{OSADJA} (Pin 47): DAC A Offset Adjust Pin. This control pin can be used to null unipolar offset or bipolar zero error. The offset-voltage delta is inverted and attenuated such that a 5V control voltage applied to V_{OSADJA} produces ΔV_{OS} = –512 LSB (LTC2754-16) in any output range (assumes a 5V reference voltage at R_{INA}). Tie to ground if not used.

I_{OUT1A} (Pin 48): DAC A Current Output. This pin is a virtual ground when the DAC is operating and should reside at 0V. For normal operation tie to the negative input of the I/V converter amplifier for DAC A (see Typical Applications).

R_{FBA} (Pin 49): DAC A Feedback Resistor. For normal operation tie to the output of the I/V converter amplifier for DAC A (see Typical Applications). The DAC output current from I_{OUT1A} flows through the feedback resistor to the R_{FBA} pin. The impedance looking into this pin is 10k to ground.

PIN FUNCTIONS

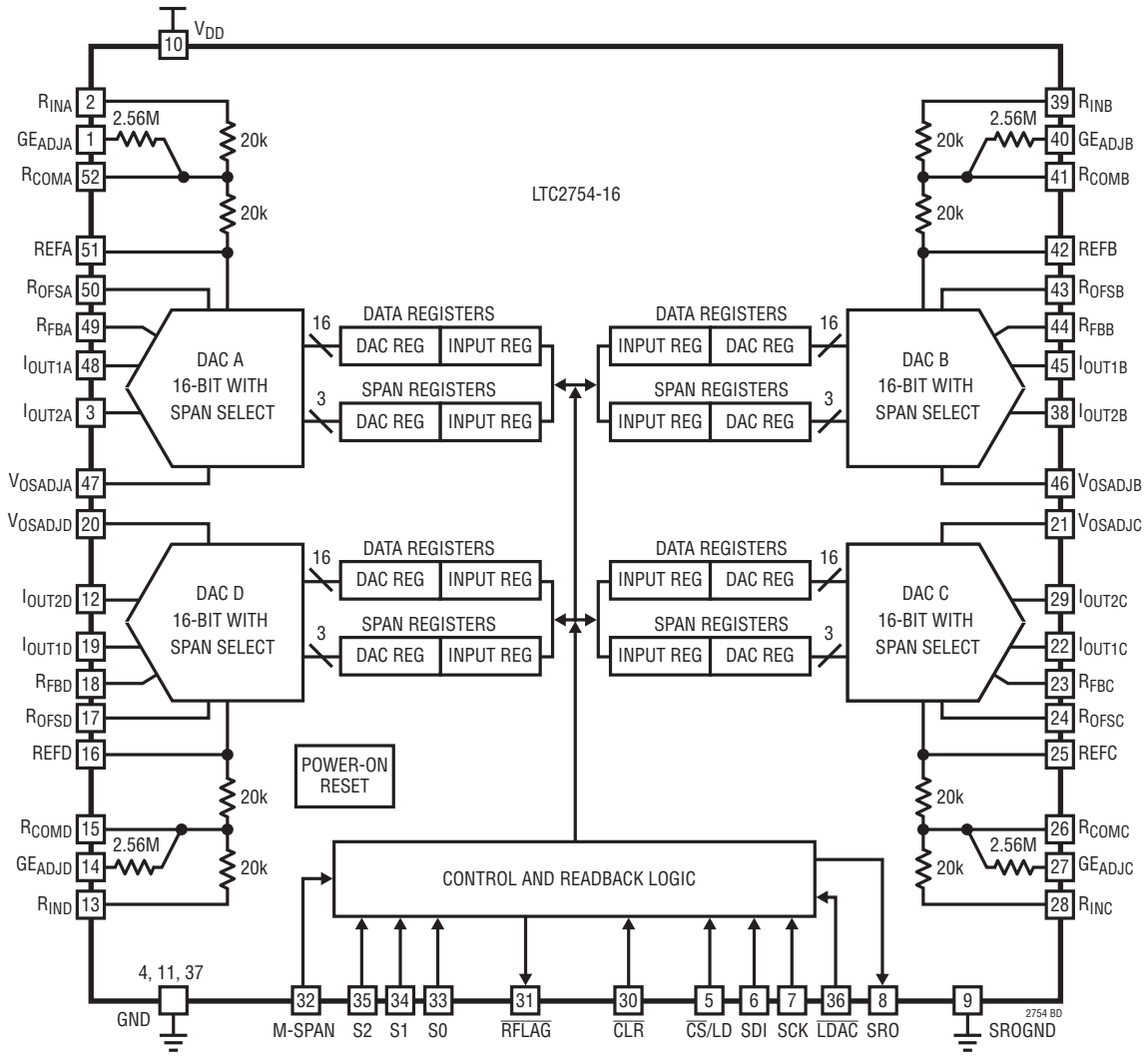
R_{OFSA} (Pin 50): Bipolar Offset Network for DAC A. This pin provides the translation of the output voltage range for bipolar spans. Accepts up to ±15V; for normal operation tie to the positive reference voltage at R_{INA} (Pin 2). The impedance looking into this pin is 20k to ground.

REFA (Pin 51): Inverted Reference Voltage for DAC A, with internal connection to the reference inverting resistor. The 20k resistor is connected internally from REFA to R_{COMA}. For normal operation tie this pin to the output of reference inverting amplifier (see Typical Applications). Typically –5V; accepts up to ±15V. The impedance looking into this pin is 10k to ground (R_{INA} and R_{COMA} floating).

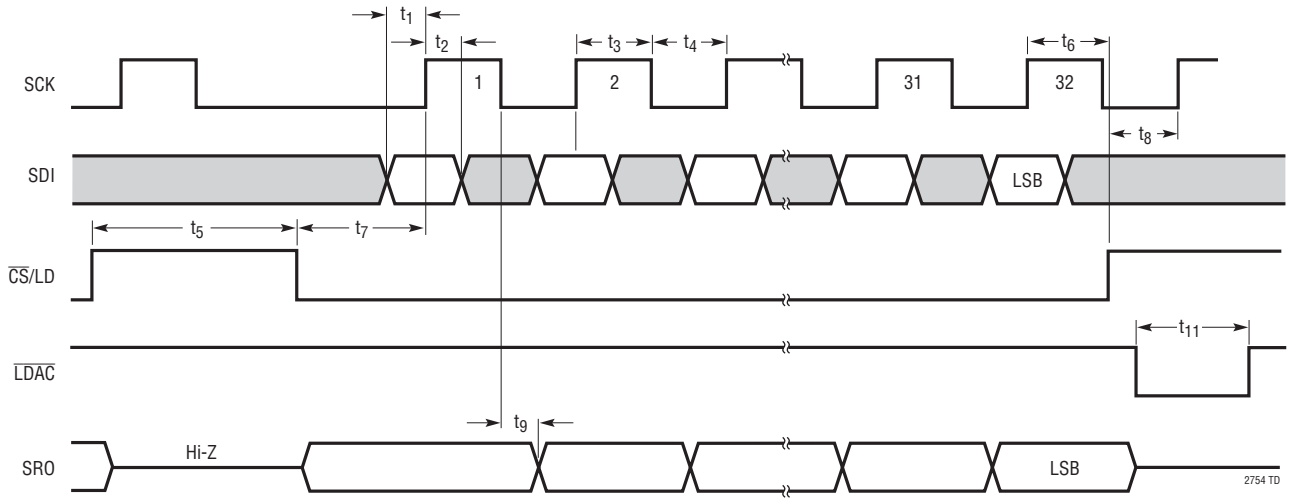
R_{COMA} (Pin 52): Center Tap Point for Reference Amplifier Inverting Resistors. The 20k reference inverting resistors are connected internally from R_{INA} to R_{COMA} and from R_{COMA} to REFA, respectively (see Block Diagram). For normal operation tie R_{COMA} to the negative input of external reference inverting amplifier (see Typical Applications).

Exposed Pad (Pin 53): Ground. The Exposed Pad must be soldered to the PCB.

BLOCK DIAGRAM



TIMING DIAGRAMS



OPERATION

Output Ranges

The LTC2754 is a quad, current-output, serial-input precision multiplying DAC with selectable output ranges. Ranges can either be programmed in software for maximum flexibility—each of the four DACs can be programmed to any one of six output ranges—or hardwired through pin-strapping. Two unipolar ranges are available (0V to 5V and 0V to 10V), and four bipolar ranges (±2.5V, ±5V, ±10V and –2.5V to 7.5V). These ranges are obtained when an external precision 5V reference is used. When a reference voltage of 2V is used, the ranges become: 0V to 2V, 0V to 4V, ±1V, ±2V, ±4V and –1V to 3V. The output ranges are linearly scaled for other reference voltages.

Manual Span Configuration

Multiple output ranges are not needed in some applications. To configure the LTC2754 to operate in a single span without additional operational overhead, tie the M-SPAN pin directly to V_{DD}. The active output range for all four DACs is then set via hardware pin strapping of pins S2, S1 and S0 (rather than through the SPI port); and Write and Update commands have no effect on the active output span. See Figure 1 and Table 3.

Tie the M-SPAN pin to ground for normal SoftSpan operation.

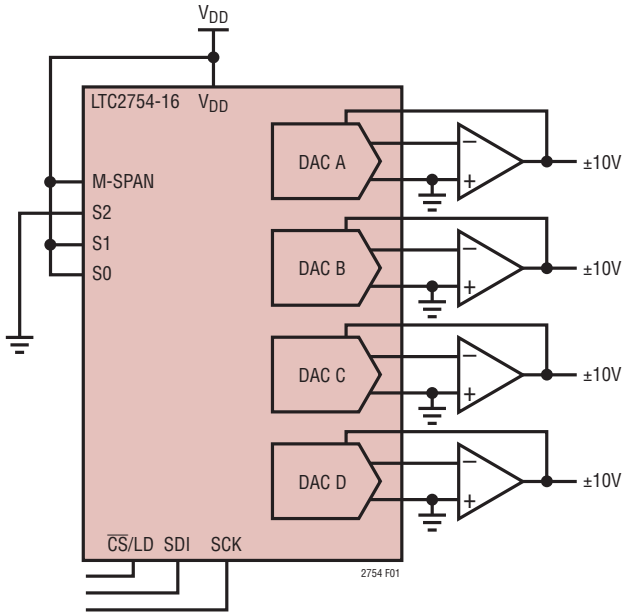


Figure 1. Using M-SPAN to Configure the LTC2754 for Single-Span Operation (±10V Range Shown).

OPERATION

Input and DAC Registers

The LTC2754 has 5 internal registers for each DAC, a total of 20 registers (see Block Diagram). Each DAC channel has two sets of double-buffered registers—one set for the code data, and one for the output range of the DAC—plus one readback register. Double buffering provides the capability to simultaneously update the span (output range) and code, which allows smooth voltage transitions when changing output ranges. It also permits the simultaneous updating of multiple DACs.

Each set of double-buffered registers comprises an Input register and a DAC register.

Input register: The Write operation shifts data from the SDI pin into a chosen Input register. The Input registers are holding buffers; Write operations do not affect the DAC outputs.

DAC register: The Update operation copies the contents of an Input register to its associated DAC register. The contents of a DAC register directly updates the associated DAC output voltage or output range.

Note that updates always include both Data and Span registers; but the values held in the DAC registers will only change if the associated Input register values have previously been changed via a Write operation.

Serial Interface

When the $\overline{CS}$/LD pin is taken low, the data on the SDI pin is loaded into the shift register on the rising edge of the clock (SCK pin). The minimum (24-bit wide) loading sequence required for the LTC2754 is a 4-bit command word (C3 C2 C1 C0), followed by a 4-bit address word (A3 A2 A1 A0) and 16 data (span or code) bits, MSB first. Figure 2 shows the SDI input word syntax to use when writing code or span. If a 32-bit input sequence is used, the first eight bits must be zeros, followed by the same sequence as for a 24-bit wide input. Figure 3 shows the input and readback sequences for both 24-bit and 32-bit operations.

When $\overline{CS}$/LD is low, the SRO pin (Serial Readback Output) is an active output.The readback data begins after the command (C3-C0) and address (A3-A0) words have been shifted into SDI. SRO outputs a logic low until the readback data begins. For a 24-bit input sequence, the 16 readback bits are shifted out on the falling edges of clocks 8-23, suitable for shifting into a microprocessor on the rising edges of clocks 9-24. For a 32-bit sequence, the bits are shifted out on clocks 16-31; see Figure 3b.

When $\overline{CS}$/LD is high, the SRO pin presents a high impedance (three-state) output.

$\overline{LDAC}$ is an asynchronous update pin. When $\overline{LDAC}$ is taken low, all DACs are updated with code and span data (data in the Input buffers is copied into the DAC buffers). $\overline{CS}$/LD must be high during this operation; otherwise $\overline{LDAC}$ is locked out and will have no effect. The use of $\overline{LDAC}$ is functionally identical to the “Update All DACs” serial input command.

The codes for the command word (C3-C0) are defined in Table 1; Table 2 defines the codes for the address word (A3-A0).

Readback

In addition to the Input and DAC registers, each DAC has one Readback register associated with it. When a Read command is issued to a DAC, the contents of one of its four buffers (Input and DAC registers for each of Span and Code) is copied into its Readback register and serially shifted out through the SRO pin. Figure 3 shows the loading and readback sequences.

In the data field (D15-D0) of any non-read instruction cycle, SRO shifts out the contents of the buffer that was specified in the preceding command. This “rolling readback” default mode of operation can dramatically reduce the number of instruction cycles needed, since any command can be verified during succeeding commands with no additional overhead. See Figure 4. Table 1 shows the storage location (‘readback pointer’) of the data which will be output from SRO during the next instruction.

For Read commands, the data is shifted out during the Read instruction itself (on the 16 falling SCK edges immediately after the last address bit is shifted in on SDI). When checking the span of a DAC using SRO, the span bits are the last four bits shifted out, corresponding to their sequence and positions when writing a span. See Figure 3.

OPERATION

Table 1. Command Codes

CODE C3	C2	C1	C0	COMMAND	READBACK POINTER– CURRENT INPUT WORD W_0	READBACK POINTER– NEXT INPUT WORD W_{+1}
0	0	1	0	Write Span DAC n	Set by Previous Command	Input Span Register DAC n
0	0	1	1	Write Code DAC n	Set by Previous Command	Input Code Register DAC n
0	1	0	0	Update DAC n	Set by Previous Command	DAC Span Register DAC n
0	1	0	1	Update All DACs	Set by Previous Command	DAC Code Register DAC A
0	1	1	0	Write Span DAC n Update DAC n	Set by Previous Command	DAC Span Register DAC n
0	1	1	1	Write Code DAC n Update DAC n	Set by Previous Command	DAC Code Register DAC n
1	0	0	0	Write Span DAC n Update All DACs	Set by Previous Command	DAC Span Register DAC n
1	0	0	1	Write Code DAC n Update All DACs	Set by Previous Command	DAC Code Register DAC n
1	0	1	0	Read Input Span Register DAC n	Input Span Register DAC n	
1	0	1	1	Read Input Code Register DAC n	Input Code Register DAC n	
1	1	0	0	Read DAC Span Register DAC n	DAC Span Register DAC n	
1	1	0	1	Read DAC Code Register DAC n	DAC Code Register DAC n	
1	1	1	1	No Operation	Set by Previous Command	DAC Code Register DAC n
–				System Clear	–	DAC Span Register DAC A
–				Initial Power-Up or Power Interupt	–	DAC Span Register DAC A

Codes not shown are reserved–do not use

Table 2. Address Codes

A3	A2	A1	A0	n
0	0	0	×	DAC A
0	0	1	×	DAC B
0	1	0	×	DAC C
0	1	1	×	DAC D
1	1	1	×	All DACs (Note 1)

Codes not shown are reserved–do not use. × = Don't Care.

Note 1. If readback is taken using the All DACs address, the LTC2754 defaults to DAC A.

Table 3. Span Codes

S3	S2	S1	S0	SPAN
×	0	0	0	Unipolar 0V to 5V
×	0	0	1	Unipolar 0V to 10V
×	0	1	0	Bipolar –5V to 5V
×	0	1	1	Bipolar –10V to 10V
×	1	0	0	Bipolar –2.5V to 2.5V
×	1	0	1	Bipolar –2.5V to 7.5V

Codes not shown are reserved–do not use. × = Don't Care.

OPERATION

Readback in M-Span Configuration

If the part is in M-Span configuration and a DAC Span register is specified for readback, then the data shifted out of SRO will reflect the actual active span. The hardware-configured output range is therefore software detectable and available for use in programming.

Examples

1. Using a 24-bit instruction, load DAC A with the unipolar range of 0V to 10V, output at zero volts and all other DACs with the bipolar range of ±10V, outputs at zero volts. Note all DAC outputs should change at the same time.

a) $\overline{CS}$/LD↓
Clock SDI = 0010 1111 0000 0000 0000 0011

b) $\overline{CS}$/LD↑
Input register- Range of all DACs set to bipolar ±10V.

c) $\overline{CS}$/LD↓
Clock SDI = 0010 0000 0000 0000 0000 0001

d) $\overline{CS}$/LD↑
Input register- Range of DAC A set to unipolar 0V to 10V.

e) $\overline{CS}$/LD↓
Clock SDI = 0011 1111 1000 0000 0000 0000

f) $\overline{CS}$/LD↑
Input register- Code of all DACs set to midscale.

g) $\overline{CS}$/LD↓
Clock SDI = 0011 0000 0000 0000 0000 0000

h) $\overline{CS}$/LD↑
Input register- Code of DAC A set to zero code.

i) $\overline{CS}$/LD↓
Clock SDI = 0100 1111 XXXX XXXX XXXX XXXX

j) $\overline{CS}$/LD↑
Update all DACs for both Code and Range.

k) Alternatively steps i and j could be replaced with $\overline{LDAC}$ ⎍.

2. Using a 32-bit load sequence, load DAC C with bipolar ±2.5V and its output at zero volts. Use readback to check Input register contents before updating the DAC output (i.e., before copying Input register contents into DAC register).

a) $\overline{CS}$/LD↓ (Note that after power-on, the code in Input register is zero)
Clock SDI = 0000 0000 0011 0100 1000 0000 0000 0000

b) $\overline{CS}$/LD↑
Input register- Code of DAC C set to midscale setting.

c) $\overline{CS}$/LD↓
Clock SDI = 0000 0000 0010 0100 0000 0000 0000 0100
Data out on SRO = 1000 0000 0000 0000 Verifies that Input register- Code DAC C is at midscale setting.

d) $\overline{CS}$/LD↑
Input register- Range of DAC C set to Bipolar ±2.5V range.

e) $\overline{CS}$/LD↓
Clock SDI = 0000 0000 1010 0100 xxxx xxxx xxxx xxxx
Data Out on SRO = 0000 0000 0000 0100
Verifies that Input register- range of DAC C set to Bipolar ±2.5V Range.
$\overline{CS}$/LD↑

f) $\overline{CS}$/LD↓
Clock SDI = 0000 0000 0100 0100 xxxx xxxx xxxx xxxx

g) $\overline{CS}$/LD↑
Update DAC C for both Code and Range

h) Alternatively steps f and g could be replaced with $\overline{LDAC}$ ⎍.

OPERATION

System Offset and Reference Adjustments

The LTC2754 has individual offset- and gain- adjust pins (V_{OSADJX} and GE_{ADJX}, respectively) for each of its four DACs.

Many systems require compensation for overall system offset. This may be an order of magnitude or more greater than the offset of the LTC2754, which is so low as to be dominated by external output amplifier errors even when using the most precise op amps.

The offset adjust pins V_{OSADJX} can be used to null unipolar offset or bipolar zero error. The offset-voltage delta is inverted and attenuated such that a 5V control voltage applied to V_{OSADJX} produces ΔV_{OS} = –512 LSB (LTC2754-16) in any output range (assumes a 5V reference voltage at R_{INX}).

In voltage terms, the offset delta is attenuated by a factor of 32, 64 or 128, depending on the output range. (These functions hold regardless of reference voltage.)

$\Delta V_{OS} = -(1/128)V_{OSADJX}$ [0V to 5V, ±2.5V spans]

$\Delta V_{OS} = -(1/64)V_{OSADJX}$ [0V to 10V, ±5V, –2.5V to 7.5V spans]

$\Delta V_{OS} = -(1/32)V_{OSADJX}$ [±10V span]

The gain error adjust pins GE_{ADJX} can be used to null gain error or to compensate for reference errors. Nominal adjustment range is ±512 LSB (LTC2754-16) for a voltage input range of $\pm V_{RINX}$ (i.e., ±5V for a 5V reference input). The gain-error delta is non-inverting for positive reference voltages.

Note that these pins compensate the gain by altering the inverted reference voltage V_{REFX}. In voltage terms, the V_{REFX} delta is inverted and attenuated by a factor of 128.

$\Delta V_{REFX} = -(1/128)GE_{ADJX}$

The nominal input range of these pins is ±5V; other voltages of up to ±15V may be used if needed. However, do not use voltages divided down from power supplies; reference-quality, low-noise inputs are required to maintain the performance of which the part is capable.

The V_{OSADJX} pins have an input impedance of 1.28MΩ. These pins should be driven with a Thevenin-equivalent impedance of 10k or less to preserve the settling performance of the LTC2754. They should be shorted to GND if not used.

The GE_{ADJX} pins have an input impedance of 2.56MΩ, and are intended for use with fixed reference voltages only. They should be shorted to GND if not used. If the reference inverting resistors are not used for that channel, then GE_{ADJX}, R_{COMX} and R_{INX} should all be shorted to REFX.

Power-On Reset and Clear

When power is first applied to the LTC2754, all DACs power-up in unipolar 5V mode (S3 S2 S1 S0 = 0000). All internal DAC registers are reset to 0 and the DAC outputs initialize to zero volts.

If the part is configured for manual span operation, all four DACs will be set into the pin-strapped range at the first Update command. This allows the user to simultaneously update span and code for a smooth voltage transition into the chosen output range.

When the $\overline{CLR}$ pin is taken low, a system clear results. The DAC buffers are reset to 0 and the DAC outputs are all reset to zero volts. The Input buffers are left intact, so that any subsequent Update command (including the use of $\overline{LDAC}$) restores the addressed DACs to their respective previous states.

If $\overline{CLR}$ is asserted during an instruction, i.e., when $\overline{CS}$/LD is low, the instruction is aborted. Integrity of the relevant Input buffers is not guaranteed under these conditions, therefore the contents should be checked using readback or replaced.

The $\overline{RFLAG}$ pin is used as a flag to notify the system of a loss of data integrity. The $\overline{RFLAG}$ output is asserted low at power-up, system clear, or if the supply V_{DD} dips below approximately 2V; and stays asserted until any valid Update command is executed.

OPERATION

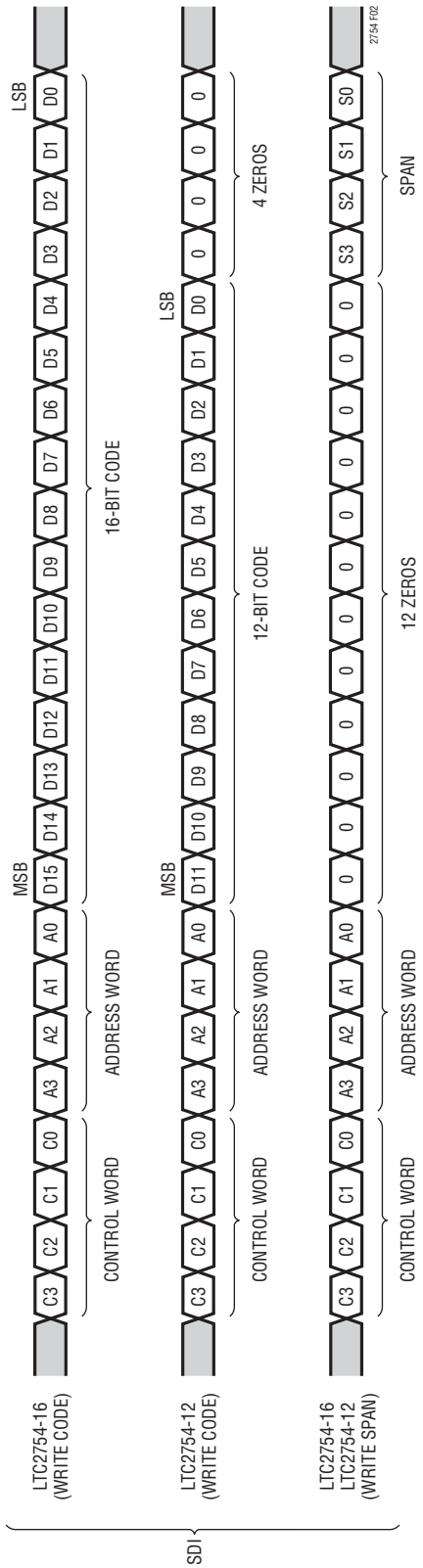


Figure 2. Serial Input Write Sequence

OPERATION

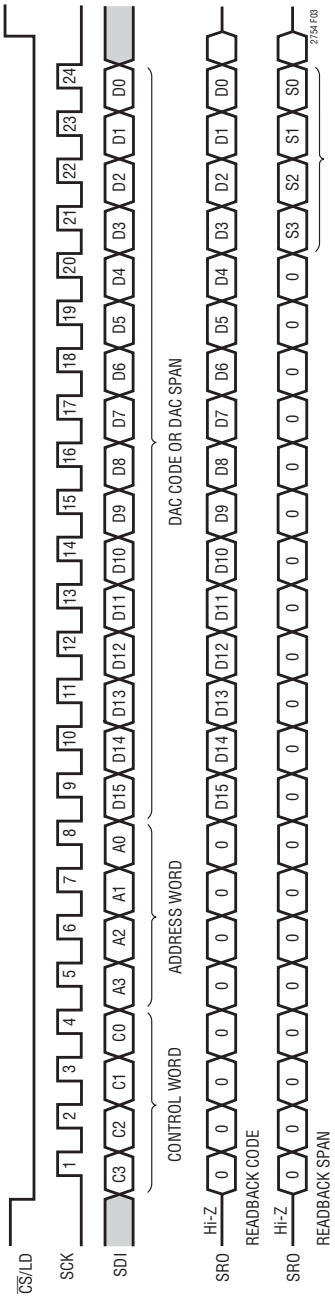


Figure 3a. 24-Bit Instruction Sequence

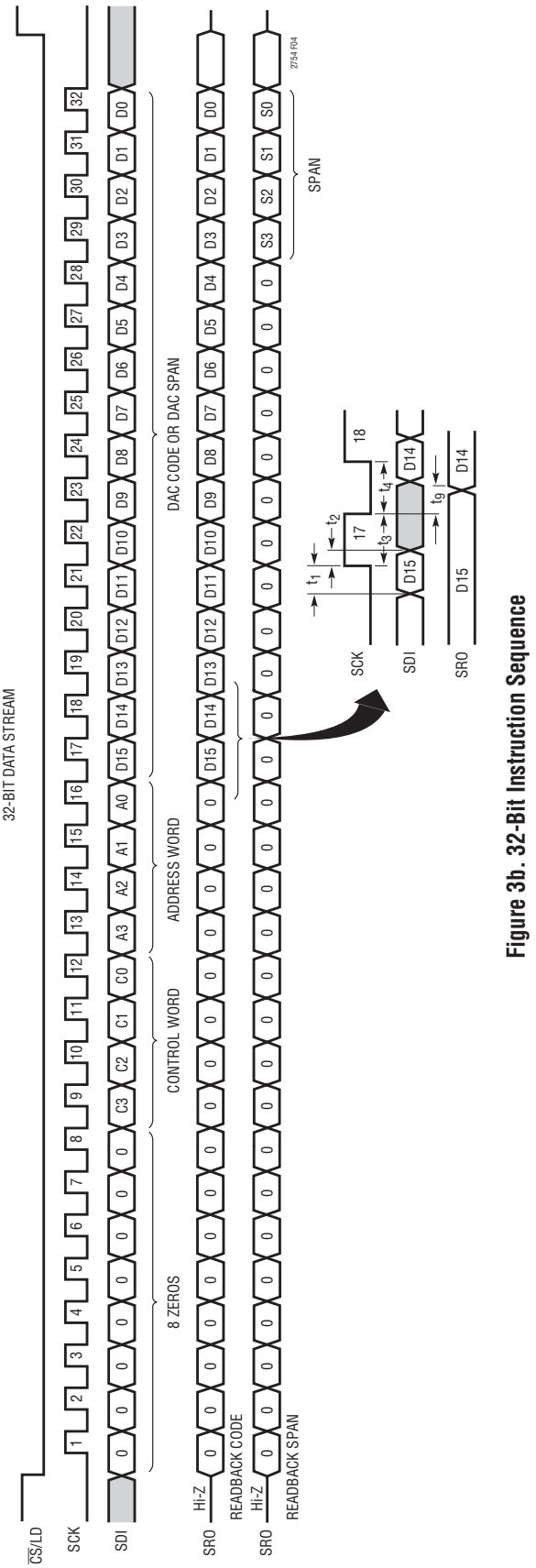


Figure 3b. 32-Bit Instruction Sequence

OPERATION

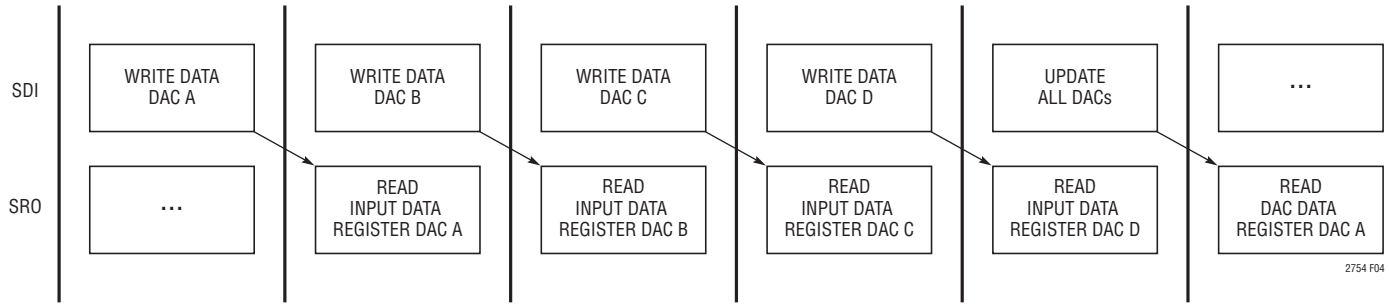


Figure 4. Rolling Readback

APPLICATIONS INFORMATION

Op Amp Selection

Because of the extremely high accuracy of the 16-bit LTC2754-16, careful thought should be given to op amp selection in order to achieve the exceptional performance of which the part is capable. Fortunately, the sensitivity of INL and DNL to op amp offset has been greatly reduced compared to previous generations of multiplying DACs.

Tables 4 and 5 contain equations for evaluating the effects of op amp parameters on the LTC2754's accuracy when programmed in a unipolar or bipolar output range. These are the changes the op amp can cause to the INL, DNL, unipolar offset, unipolar gain error, bipolar zero and bipolar gain error. Tables 4 and 5 can also be used to determine the effects of op amp parameters on the LTC2754-12. However, the results obtained from Tables 4 and 5 are in 16-bit LSBs. Divide these results by 16 to obtain the correct LSB sizing.

Table 6 contains a partial list of LTC precision op amps recommended for use with the LTC2754. The easy-to-use design equations simplify the selection of op amps to meet

Table 4. Coefficients for the Equations in Table 5

OUTPUT RANGE	A1	A2	A3	A4	A5
5V	1.1	2	1		1
10V	2.2	3	0.5		1.5
±5V	2	2	1	1	1.5
±10V	4	4	0.83	1	2.5
±2.5V	1	1	1.4	1	1
–2.5V to 7.5V	1.9	3	0.7	0.5	1.5

Table 5. Easy-to-Use Equations Determine Op Amp Effects on DAC Accuracy in All Output Ranges (Circuit of Page 1). Subscript 1 Refers to Output Amp, Subscript 2 Refers to Reference Inverting Amp.

OP AMP	INL (LSB)	DNL (LSB)	UNIPOLAR OFFSET (LSB)	BIPOLAR ZERO ERROR (LSB)	UNIPOLAR GAIN ERROR (LSB)	BIPOLAR GAIN ERROR (LSB)
V_{OS1} (mV)	$V_{OS1} \bullet 3.2 \bullet \left(\frac{5V}{V_{REF}}\right)$	$V_{OS1} \bullet 0.82 \bullet \left(\frac{5V}{V_{REF}}\right)$	$A3 \bullet V_{OS1} \bullet 13.2 \bullet \left(\frac{5V}{V_{REF}}\right)$	$A3 \bullet V_{OS1} \bullet 19.8 \bullet \left(\frac{5V}{V_{REF}}\right)$	$V_{OS1} \bullet 13.2 \bullet \left(\frac{5V}{V_{REF}}\right)$	$V_{OS1} \bullet 13.2 \bullet \left(\frac{5V}{V_{REF}}\right)$
I_{B1} (nA)	$I_{B1} \bullet 0.0003 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B1} \bullet 0.00008 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B1} \bullet 0.13 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B1} \bullet 0.13 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B1} \bullet 0.0018 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B1} \bullet 0.0018 \bullet \left(\frac{5V}{V_{REF}}\right)$
A_{VOL1} (V/V)	$A1 \bullet \left(\frac{16.5k}{A_{VOL1}}\right)$	$A2 \bullet \left(\frac{1.5k}{A_{VOL1}}\right)$	0	0	$A5 \bullet \left(\frac{131k}{A_{VOL1}}\right)$	$A5 \bullet \left(\frac{131k}{A_{VOL1}}\right)$
V_{OS2} (mV)	0	0	0	$A4 \bullet \left(V_{OS2} \bullet 13.1 \bullet \left(\frac{5V}{V_{REF}}\right)\right)$	$V_{OS2} \bullet 26.2 \bullet \left(\frac{5V}{V_{REF}}\right)$	$V_{OS2} \bullet 26.2 \bullet \left(\frac{5V}{V_{REF}}\right)$
I_{B2} (mV)	0	0	0	$A4 \bullet \left(I_{B2} \bullet 0.13 \bullet \left(\frac{5V}{V_{REF}}\right)\right)$	$I_{B2} \bullet 0.26 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B2} \bullet 0.26 \bullet \left(\frac{5V}{V_{REF}}\right)$
A_{VOL2} (V/V)	0	0	0	$A4 \bullet \left(\frac{66k}{A_{VOL2}}\right)$	$\left(\frac{131k}{A_{VOL2}}\right)$	$\left(\frac{131k}{A_{VOL2}}\right)$

Table 6. Partial List of LTC Precision Amplifiers Recommended for Use with the LTC2754 with Relevant Specifications

	AMPLIFIER SPECIFICATIONS								
AMPLIFIER	V_{OS} µV	I_B nA	A_{VOL} V/mV	VOLTAGE NOISE nV/√Hz	CURRENT NOISE pA/√Hz	SLEW RATE V/µs	GAIN BANDWIDTH PRODUCT MHz	$t_{SETTLING}$ with LTC2755 µs	POWER DISSIPATION mW
LT1001	25	2	800	10	0.12	0.25	0.8	120	46
LT1097	50	0.35	1000	14	0.008	0.2	0.7	120	11
LT1112 (Dual)	60	0.25	1500	14	0.008	0.16	0.75	115	10.5/Op Amp
LT1124 (Dual)	70	20	4000	2.7	0.3	4.5	12.5	19	69/Op Amp
LT1468	75	10	5000	5	0.6	22	90	2	117
LT1469 (Dual)	125	10	2000	5	0.6	22	90	2	123/Op Amp

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the system's specified error budget. Select the amplifier from Table 6 and insert the specified op amp parameters in Table 5. Add up all the errors for each category to determine the effect the op amp has on the accuracy of the part. Arithmetic summation gives an (unlikely) worst-case effect. A root-sum-square (RMS) summation produces a more realistic estimate.

Op amp offset will contribute mostly to output offset and gain error, and has minimal effect on INL and DNL. For example, for the LTC2754-16 with a 5V reference in 5V unipolar mode, a 250µV op amp offset will cause a 3.3LSB zero-scale error and a 3.3LSB gain error; but only 0.8LSB of INL degradation and 0.2LSB of DNL degradation.

While not directly addressed by the simple equations in Tables 4 and 5, temperature effects can be handled just as easily for unipolar and bipolar applications. First, consult an op amp's data sheet to find the worst-case V_{OS} and I_B over temperature. Then, plug these numbers into the V_{OS} and I_B equations from Table 5 and calculate the temperature-induced effects.

For applications where fast settling time is important, Application Note 74, "Component and Measurement Advances Ensure 16-Bit DAC Settling Time," offers a thorough discussion of 16-bit DAC settling time and op amp selection.

Precision Voltage Reference Considerations

Much in the same way selecting an operational amplifier for use with the LTC2754 is critical to the performance of the system, selecting a precision voltage reference also requires due diligence. The output voltage of the LTC2754 is directly affected by the voltage reference; thus, any voltage reference error will appear as a DAC output voltage error.

There are three primary error sources to consider when selecting a precision voltage reference for 16-bit applications: output voltage initial tolerance, output voltage temperature coefficient and output voltage noise.

Initial reference output voltage tolerance, if uncorrected, generates a full-scale error term. Choosing a reference with low output voltage initial tolerance, like the LT1236 (±0.05%), minimizes the gain error caused by the reference; however, a calibration sequence that corrects for system zero- and full-scale error is always recommended.

A reference's output voltage temperature coefficient affects not only the full-scale error, but can also affect the circuit's apparent INL and DNL performance. If a reference is chosen with a loose output voltage temperature coefficient, then the DAC output voltage along its transfer characteristic will be very dependent on ambient conditions. Minimizing the error due to reference temperature coefficient can be achieved by choosing a precision reference with a low output voltage temperature coefficient and/or tightly controlling the ambient temperature of the circuit to minimize temperature gradients.

Table 7. Partial List of LTC Precision References Recommended for Use with the LTC2754 with Relevant Specifications

REFERENCE	INITIAL TOLERANCE	TEMPERATURE DRIFT	0.1Hz to 10Hz NOISE
LT1019A-5, LT1019A-10	±0.05%	5ppm/°C	$12\mu V_{P-P}$
LT1236A-5, LT1236A-10	±0.05%	5ppm/°C	$3\mu V_{P-P}$
LT1460A-5, LT1460A-10	±0.075%	10ppm/°C	$20\mu V_{P-P}$
LT1790A-2.5	±0.05%	10ppm/°C	$12\mu V_{P-P}$
LTC6652A-2.048	±0.05%	5ppm/°C	$2.1ppm_{P-P}$
LTC6652A-2.5			$2.1ppm_{P-P}$
LTC6652A-3			$2.1ppm_{P-P}$
LTC6652A-3.3			$2.2ppm_{P-P}$
LTC6652A-4.096			$2.3ppm_{P-P}$
LTC6652A-5			$2.8ppm_{P-P}$

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As precision DAC applications move to 16-bit and higher performance, reference output voltage noise may contribute a dominant share of the system's noise floor. This in turn can degrade system dynamic range and signal-to-noise ratio. Care should be exercised in selecting a voltage reference with as low an output noise voltage as practical for the system resolution desired. Precision voltage references, like the LT1236, produce low output noise in the 0.1Hz to 10Hz region, well below the 16-bit LSB level in 5V or 10V full-scale systems. However, as the circuit bandwidths increase, filtering the output of the reference may be required to minimize output noise.

Grounding

As with any high resolution converter, clean grounding is important. A low impedance analog ground plane and star grounding techniques should be used. I_{OUT2X} must be tied to the star ground with as low a resistance as possible.

When it is not possible to locate star ground close to I_{OUT2}, a low resistance trace should be used to route this pin to star ground. This minimizes the voltage drop from this pin to ground caused by the code-dependent current flowing to ground. When the resistance of this circuit board trace becomes greater than 1Ω, a force/sense amplifier configuration should be used to drive this pin (see Figure 5). This preserves the excellent accuracy (1LSB INL and DNL) of the LTC2754-16.

Layout

Figures 6, 7, 8, and 9 show the layout for the LTC2754 evaluation board, DC1546. This shows how to route the digital signals around the device without interfering with the reference and output op amps. Complete demo board documentation is available in the DC1546 "Quick Start Guide."

APPLICATIONS INFORMATION

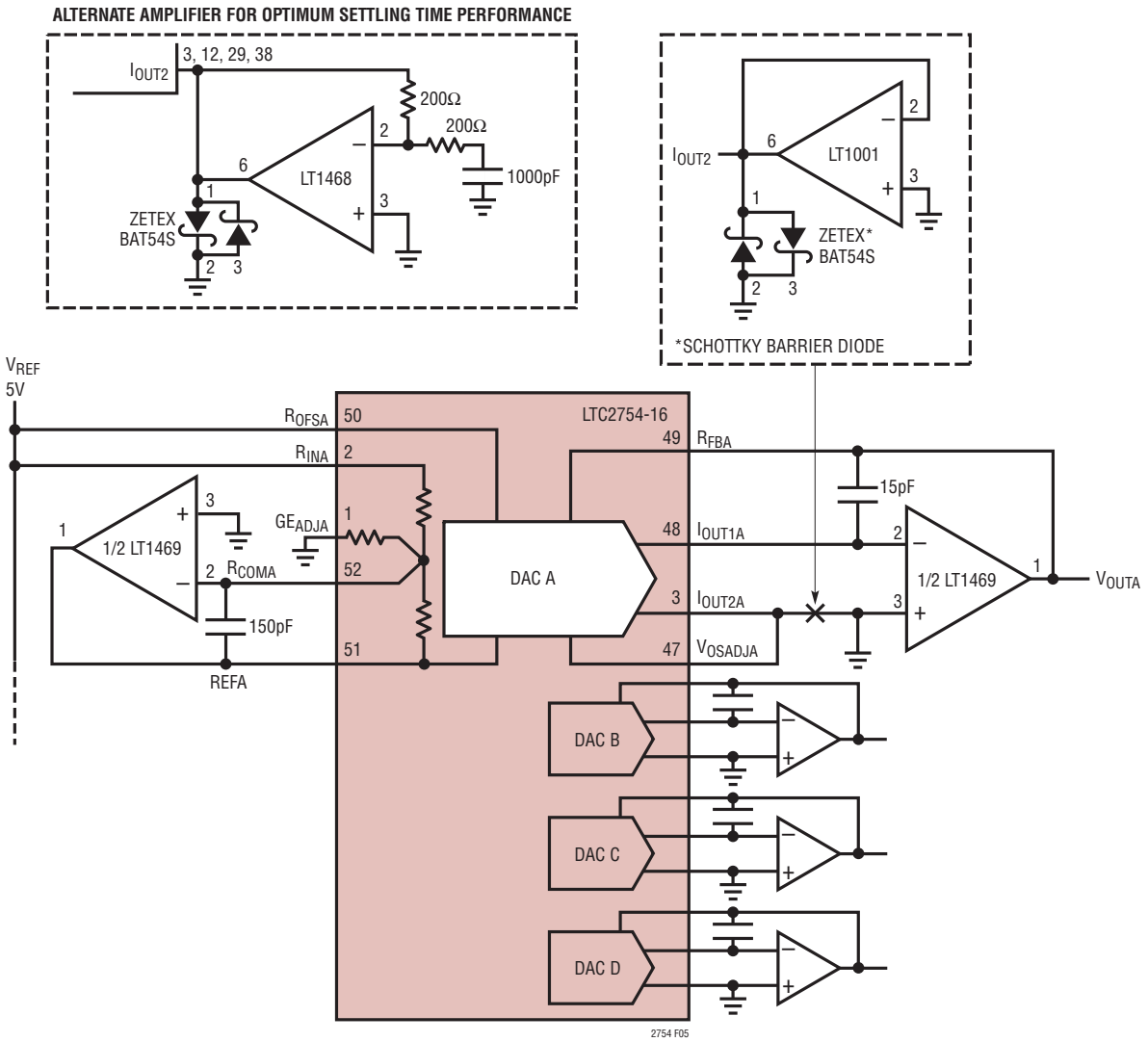


Figure 5. Optional Circuits for Driving I_{OUT2} from GND with a Force/Sense Amplifier.

APPLICATIONS INFORMATION

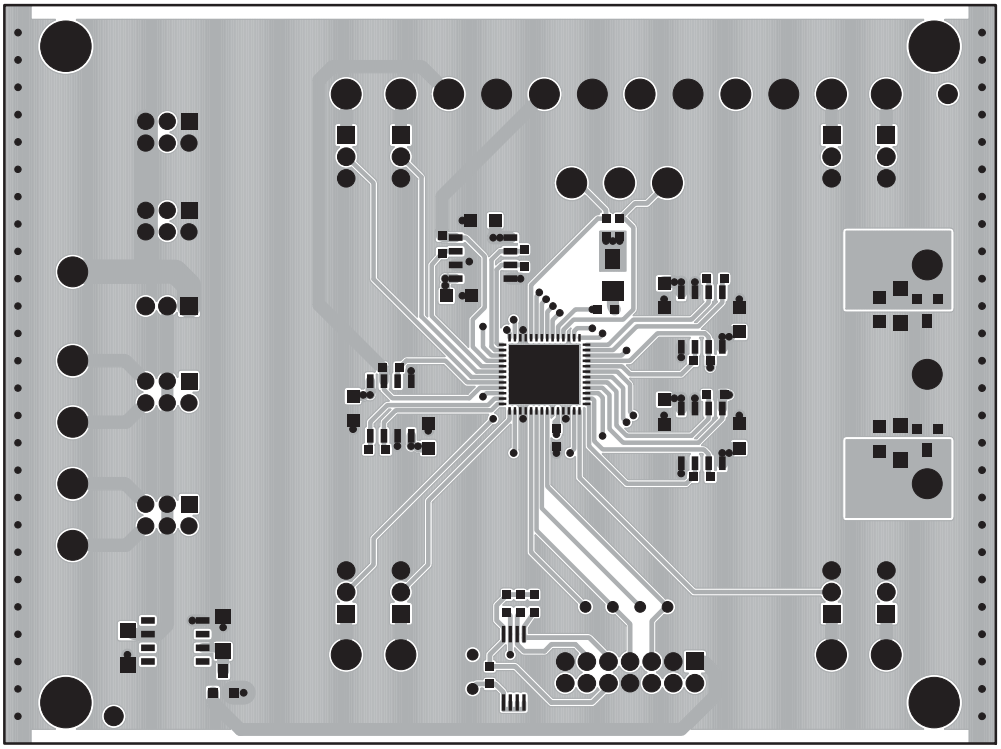


Figure 6. LTC2754 Evaluation Board DC1546. Layer 1, Top Layer (Component Side)

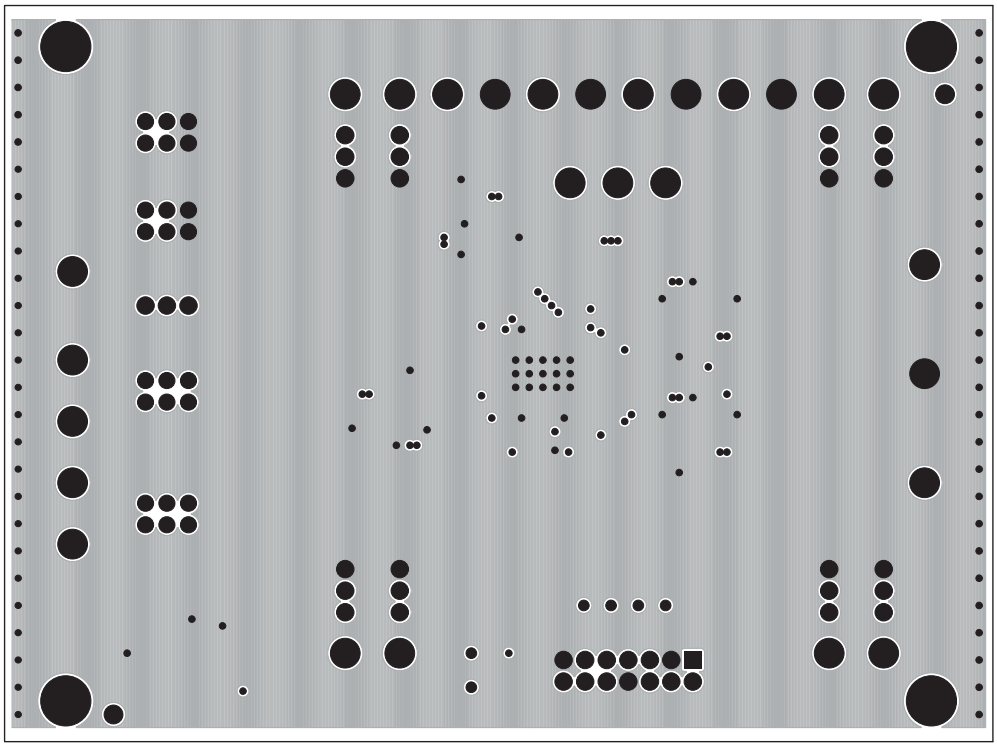


Figure 7. LTC2754 Evaluation Board DC1546. Layer 2, GND Plane

APPLICATIONS INFORMATION

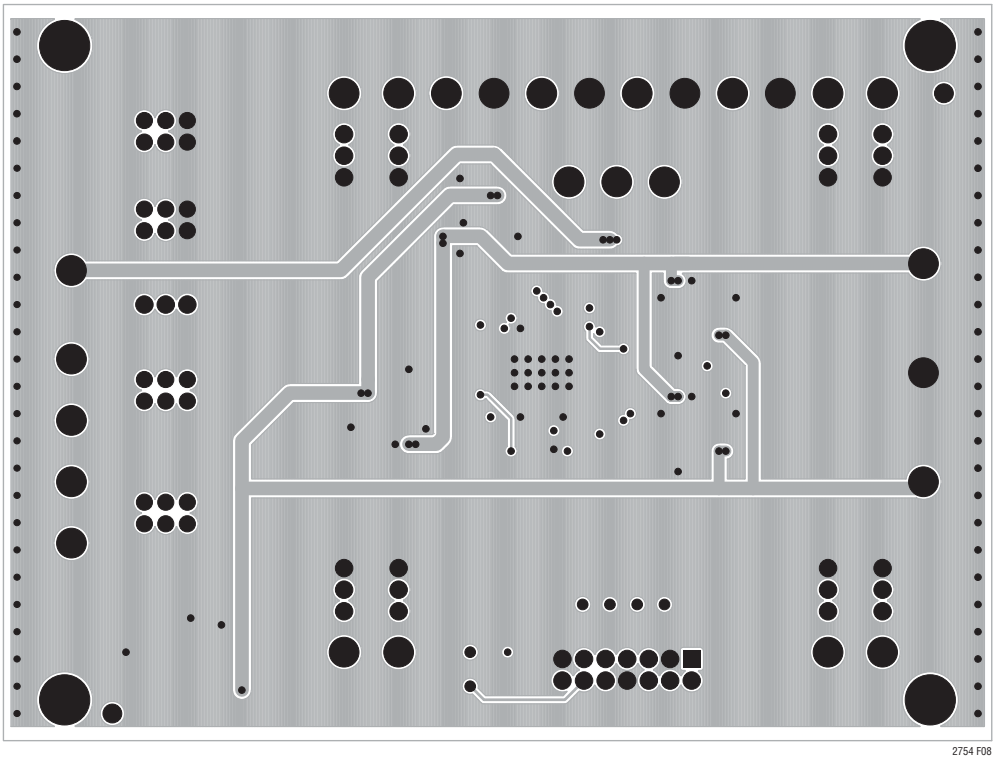


Figure 8. LTC2754 Evaluation Board DC1546. Layer 3, Power Traces

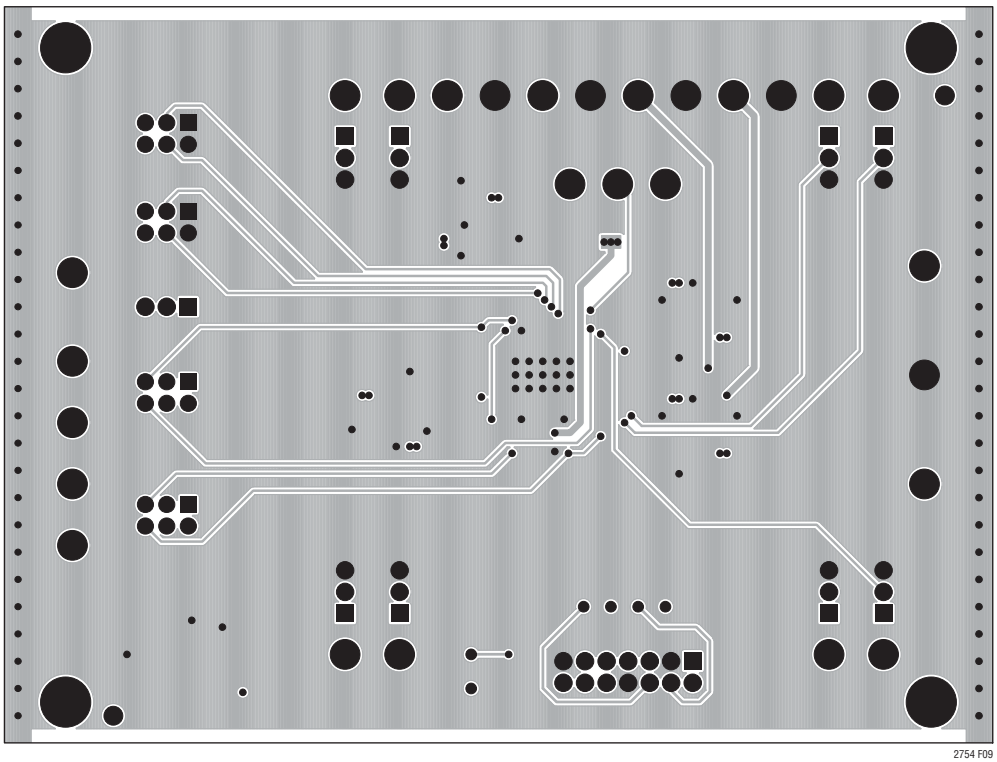
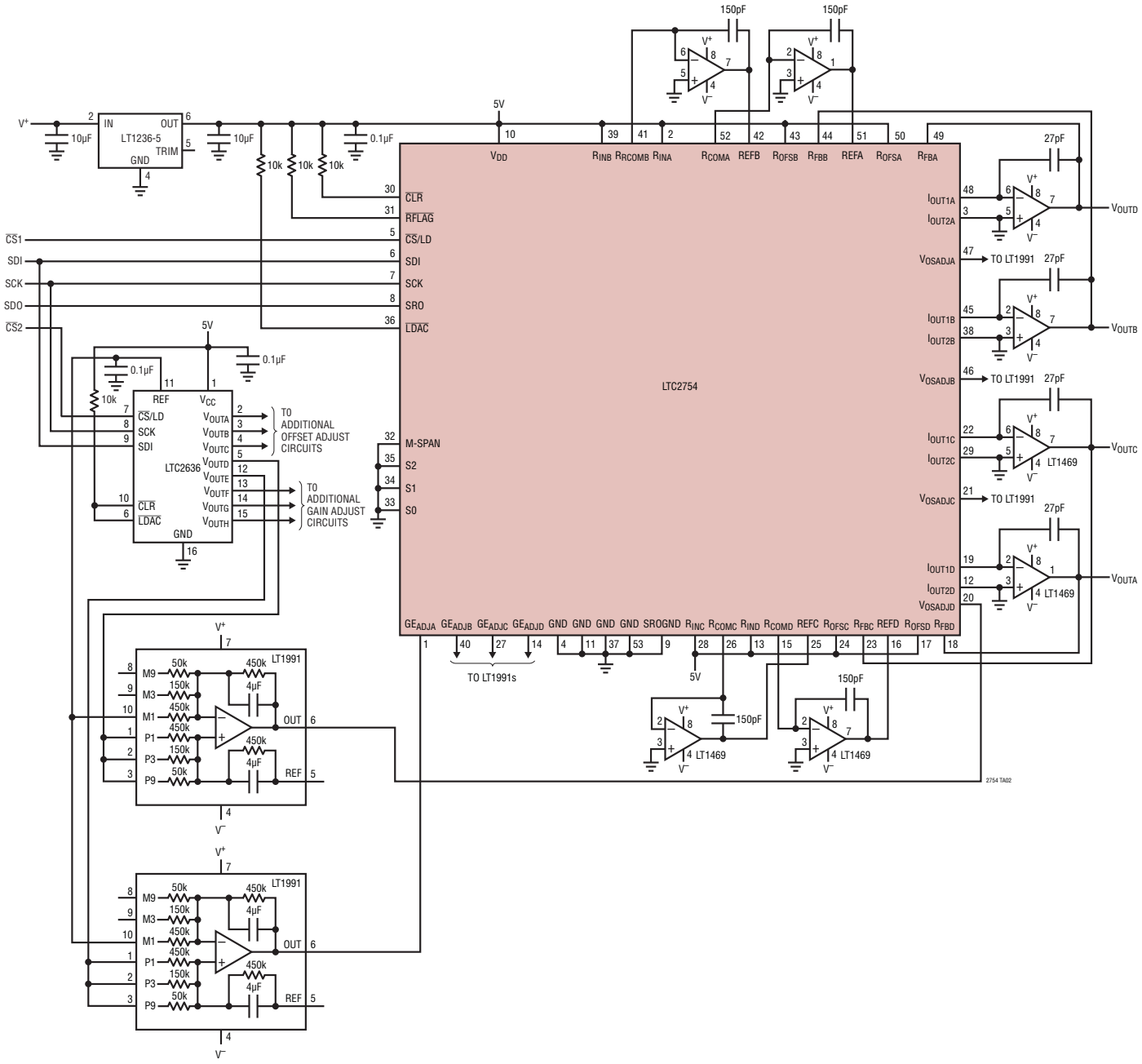


Figure 9. LTC2754 Evaluation Board DC1546. Layer 4, Bottom Layer (Solder Side)

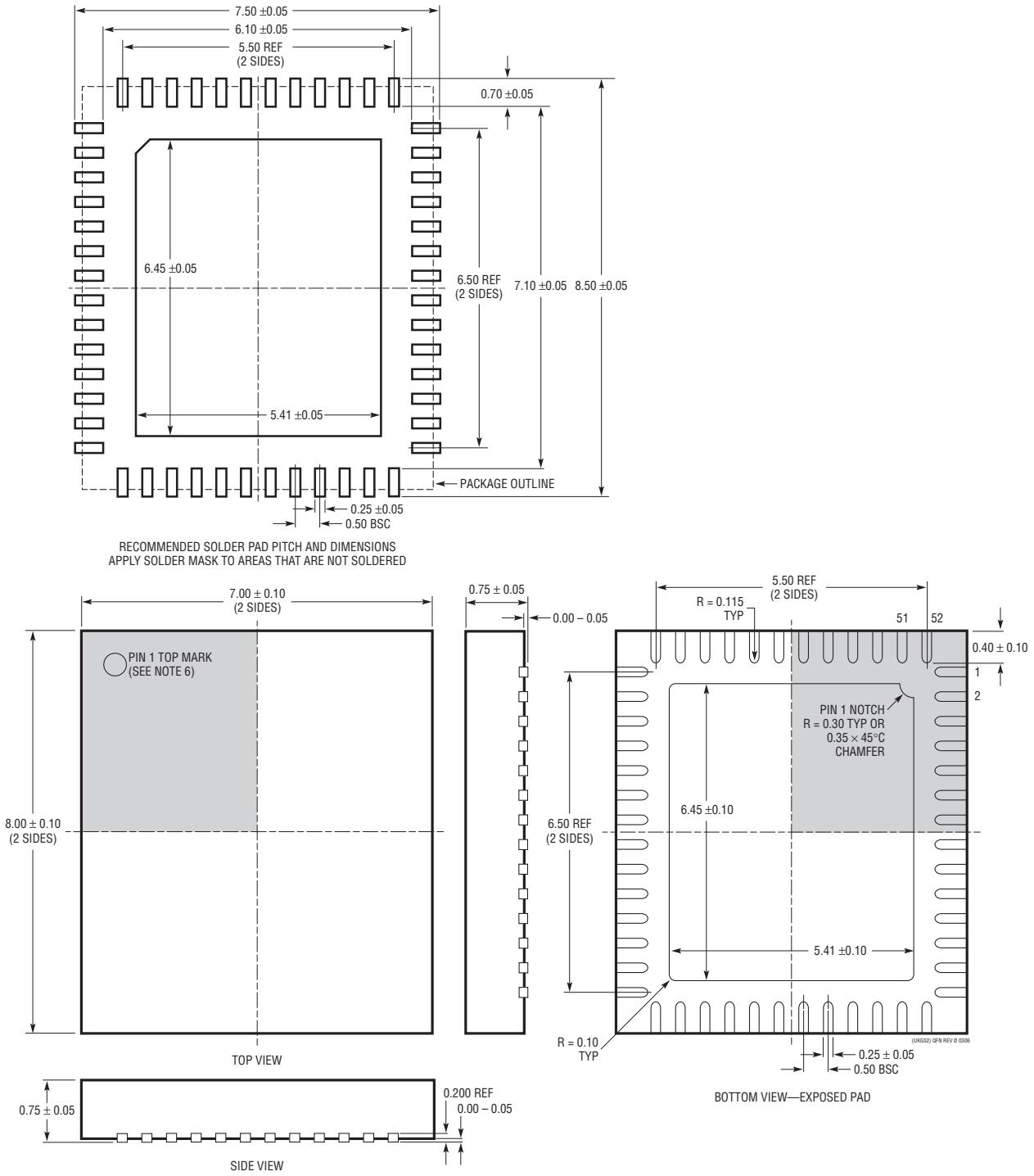
TYPICAL APPLICATION

Digitally Controlled Offset and Gain Trim Circuit. Powering V_{DD} from LT1236 Ensures Quiet Supply



PACKAGE DESCRIPTION

UKG Package
52-Lead Plastic QFN (7mm × 8mm)
(Reference LTC DWG # 05-08-1729 Rev Ø)



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1027	Precision Reference	1ppm/°C Maximum Drift
LT1236A-5	Precision Reference	0.05% Maximum Tolerance, 1ppm 0.1Hz to 10Hz Noise
LT1468	16-Bit Accurate Op-Amp	90MHz GBW, 22V/µs Slew Rate
LT1469	Dual 16-Bit Accurate Op-Amp	90MHz GBW, 22V/µs Slew Rate
LTC1588/LTC1589/ LTC1592	Serial 12-/14-/16-Bit I_{OUT} Single DAC	Software-Selectable (SoftSpan) Ranges, ±1LSB INL, DNL, 16-Lead SSOP Package
LTC1591/LTC1597	Parallel 14-/16-Bit I_{OUT} Single DAC	Integrated 4-Quadrant Resistors
LTC2704	Serial 12-/14-/16-Bit V_{OUT} Quad DACs	Software-Selectable (SoftSpan) Ranges, Integrated Amplifiers, ±1LSB INL
LTC2751	Parallel 12-/14-/16-Bit I_{OUT} SoftSpan Single DAC	±1LSB INL, DNL, Software-Selectable (SoftSpan) Ranges, 5mm × 7mm QFN-38 Package
LTC2753	Parallel 12-/14-16-Bit I_{OUT} SoftSpan Dual DACs	±1LSB INL, DNL, Software-Selectable (SoftSpan) Ranges, 7mm × 7mm QFN-48 Package
LTC2755	Parallel 12-/14-/16-Bit I_{OUT} SoftSpan Quad DACs	±1LSB INL, DNL, Software-Selectable (SoftSpan) Ranges, 9mm × 9mm QFN-64 Package

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