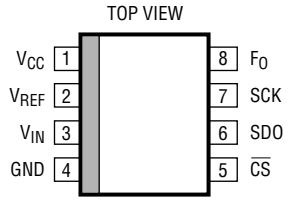
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) to GND ..... –0.3V to 7V
Analog Input Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Reference Input Voltage to GND .. –0.3V to (V_{CC} + 0.3V)
Digital Input Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Digital Output Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Operating Temperature Range
LTC2400C ..... 0°C to 70°C
LTC2400I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC2400CS8 LTC2400IS8
S8 PART MARKING
2400 2400I

Consult factory for Military grade parts.

CONVERTER CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)	0.1V ≤ V_{REF} ≤ V_{CC}, (Note 5)	●	24			Bits
Integral Nonlinearity	V_{REF} = 2.5V (Note 6) V_{REF} = 5V (Note 6)	● ●		2 4	10 15	ppm of V_{REF} ppm of V_{REF}
Offset Error	2.5V ≤ V_{REF} ≤ V_{CC}	●		0.5	2	ppm of V_{REF}
Offset Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}			0.01		ppm of V_{REF}/°C
Full-Scale Error	2.5V ≤ V_{REF} ≤ V_{CC}	●		4	10	ppm of V_{REF}
Full-Scale Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}			0.02		ppm of V_{REF}/°C
Total Unadjusted Error	V_{REF} = 2.5V V_{REF} = 5V			5 10		ppm of V_{REF} ppm of V_{REF}
Output Noise	V_{IN} = 0V (Note 13)			1.5		μV_{RMS}
Normal Mode Rejection 60Hz ±2%	(Note 7)	●	110	130		dB
Normal Mode Rejection 50Hz ±2%	(Note 8)	●	110	130		dB
Power Supply Rejection, DC	V_{REF} = 2.5V, V_{IN} = 0V			100		dB
Power Supply Rejection, 60Hz ±2%	V_{REF} = 2.5V, V_{IN} = 0V, (Notes 7, 15)			110		dB
Power Supply Rejection, 50Hz ±2%	V_{REF} = 2.5V, V_{IN} = 0V, (Notes 8, 15)			110		dB

ANALOG INPUT AND REFERENCE

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range	(Note 14)	●	–0.125 • V_{REF}		1.125 • V_{REF}	V
V_{REF}	Reference Voltage Range		●	0.1		V_{CC}	V
$C_{S(IN)}$	Input Sampling Capacitance				10		pF
$C_{S(REF)}$	Reference Sampling Capacitance				15		pF
$I_{IN(LEAK)}$	Input Leakage Current	$\overline{CS}$ = V_{CC}	●	–10	1	10	nA
$I_{REF(LEAK)}$	Reference Leakage Current	V_{REF} = 2.5V, $\overline{CS}$ = V_{CC}	●	–10	1	10	nA

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage $\overline{CS}$, F_O	2.7V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 3.3V	● ●	2.5 2.0			V V
V_{IL}	Low Level Input Voltage $\overline{CS}$, F_O	4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V	● ●			0.8 0.6	V V
V_{IH}	High Level Input Voltage SCK	2.7V ≤ V_{CC} ≤ 5.5V (Note 9) 2.7V ≤ V_{CC} ≤ 3.3V (Note 9)	● ●	2.5 2.0			V V
V_{IL}	Low Level Input Voltage SCK	4.5V ≤ V_{CC} ≤ 5.5V (Note 9) 2.7V ≤ V_{CC} ≤ 5.5V (Note 9)	● ●			0.8 0.6	V V
I_{IN}	Digital Input Current $\overline{CS}$, F_O	0V ≤ V_{IN} ≤ V_{CC}	●	–10		10	µA
I_{IN}	Digital Input Current SCK	0V ≤ V_{IN} ≤ V_{CC} (Note 9)	●	–10		10	µA
C_{IN}	Digital Input Capacitance $\overline{CS}$, F_O				10		pF
C_{IN}	Digital Input Capacitance SCK	(Note 9)			10		pF
V_{OH}	High Level Output Voltage SDO	I_O = –800µA	●	V_{CC} – 0.5V			V
V_{OL}	Low Level Output Voltage SDO	I_O = 1.6mA	●			0.4V	V
V_{OH}	High Level Output Voltage SCK	I_O = –800µA (Note 10)	●	V_{CC} – 0.5V			V
V_{OL}	Low Level Output Voltage SCK	I_O = 1.6mA (Note 10)	●			0.4V	V
I_{OZ}	High-Z Output Leakage SDO		●	–10		10	µA

POWER REQUIREMENTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	2.7		5.5	V
I_{CC}	Supply Current Conversion Mode Sleep Mode	 $\overline{CS}$ = 0V (Note 12) $\overline{CS}$ = V_{CC} (Note 12)	 ● ●		 200 20	 300 30	 µA µA

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range		●	2.56		307.2	kHz
t_{HEO}	External Oscillator High Period		●	0.5		390	µs
t_{LEO}	External Oscillator Low Period		●	0.5		390	µs
t_{CONV}	Conversion Time	F_O = 0V	●	130.66	133.33	136	ms
		F_O = V_{CC}	●	156.80	160	163.20	ms
		External Oscillator (Note 11)	●		20480/f_{EOSC} (in kHz)		ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Note 10)			19.2		kHz
		External Oscillator (Notes 10, 11)			f_{EOSC}/8		kHz
D_{ISCK}	Internal SCK Duty Cycle	(Note 10)	●	45		55	%
f_{ESCK}	External SCK Frequency Range	(Note 9)	●			2000	kHz
t_{LESCK}	External SCK Low Period	(Note 9)	●	250			ns
t_{HESCK}	External SCK High Period	(Note 9)	●	250			ns
t_{DOUT_ISCK}	Internal SCK 32-Bit Data Output Time	Internal Oscillator (Notes 10, 12)	●	1.64	1.67	1.70	ms
		External Oscillator (Notes 10, 11)	●		256/f_{EOSC} (in kHz)		ms
t_{DOUT_ESCK}	External SCK 32-Bit Data Output Time	(Note 9)	●		32/f_{ESCK} (in kHz)		ms
t_1	$\overline{CS}$ ↓ to SDO Low Z		●	0		150	ns
t2	$\overline{CS}$ ↑ to SDO High Z		●	0		150	ns
t3	$\overline{CS}$ ↓ to SCK ↓	(Note 10)	●	0		150	ns
t4	$\overline{CS}$ ↓ to SCK ↑	(Note 9)	●	50			ns
t_{KQMAX}	SCK ↓ to SDO Valid		●			200	ns
t_{KQMIN}	SDO Hold After SCK ↓	(Note 5)	●	15			ns
t_5	SCK Set-Up Before $\overline{CS}$ ↓		●	50			ns
t_6	SCK Hold After $\overline{CS}$ ↓		●			50	ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: V_{CC} = 2.7 to 5.5V unless otherwise specified.

Note 4: Internal Conversion Clock source with the F_O pin tied to GND or to V_{CC} or to external conversion clock source with f_{EOSC} = 153600Hz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: F_O = 0V (internal oscillator) or f_{EOSC} = 153600Hz ±2% (external oscillator).

Note 8: F_O = V_{CC} (internal oscillator) or f_{EOSC} = 128000Hz ±2% (external oscillator).

Note 9: The converter is in external SCK mode of operation such that the SCK pin is used as digital input. The frequency of the clock signal driving SCK during the data output is f_{ESCK} and is expressed in kHz.

Note 10: The converter is in internal SCK mode of operation such that the SCK pin is used as digital output. In this mode of operation the SCK pin has a total equivalent load capacitance C_{LOAD} = 20pF.

Note 11: The external oscillator is connected to the F_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 12: The converter uses the internal oscillator. F_O = 0V or F_O = V_{CC}.

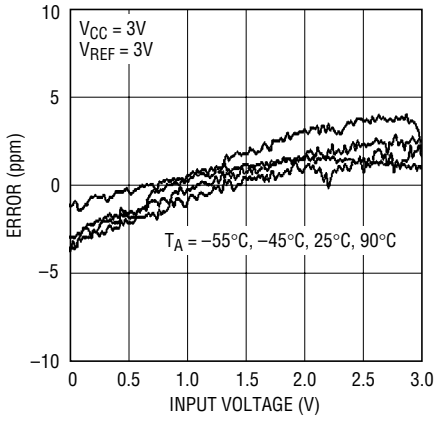
Note 13: The output noise includes the contribution of the internal calibration operations.

Note 14: For reference voltage values V_{REF} > 2.5V the extended input of –0.125 • V_{REF} to 1.125 • V_{REF} is limited by the absolute maximum rating of the Analog Input Voltage pin (Pin 3). For 2.5V < V_{REF} ≤ 0.267V + 0.89 • V_{CC} the input voltage range is –0.3V to 1.125 • V_{REF}. For 0.267V + 0.89 • V_{CC} < V_{REF} ≤ V_{CC} the input voltage range is –0.3V to V_{CC} + 0.3V.

Note 15: The DC voltage at V_{CC} = 4.1V, and the AC voltage applied to V_{CC} is $2.8V_{P-P}$

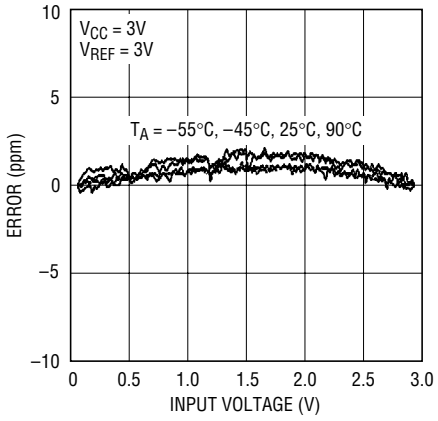
TYPICAL PERFORMANCE CHARACTERISTICS

Total Unadjusted Error (3V Supply)



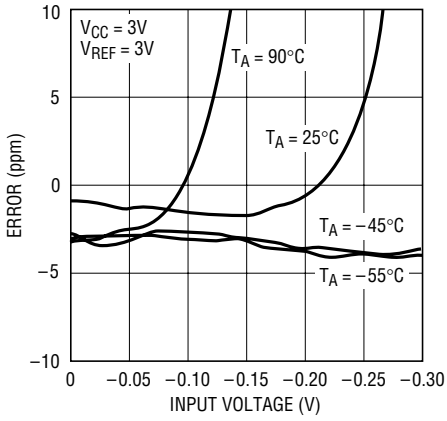
2400 G01

INL (3V Supply)



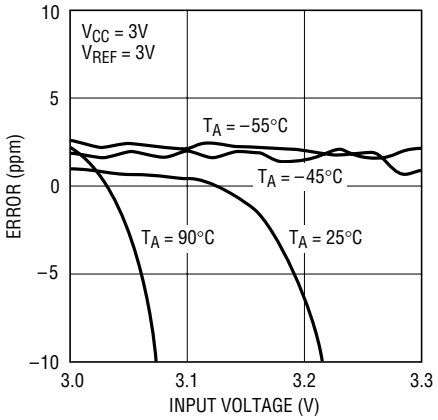
2400 G02

Negative Input Extended Total Unadjusted Error (3V Supply)



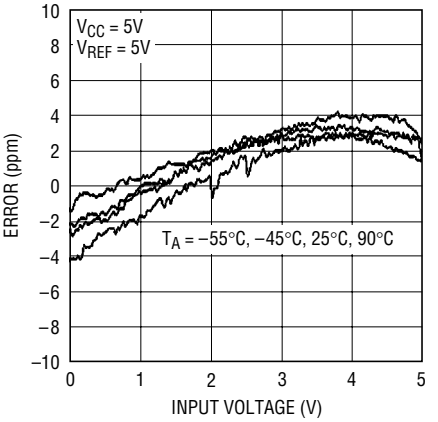
2400 G03

Positive Input Extended Total Unadjusted Error (3V Supply)



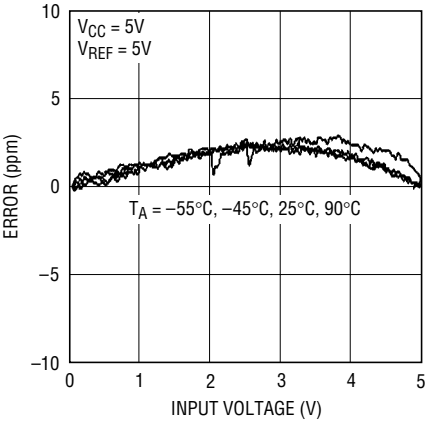
2400 G04

Total Unadjusted Error (5V Supply)



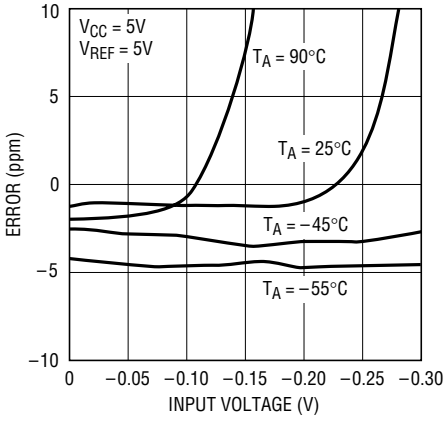
2400 G05

INL (5V Supply)



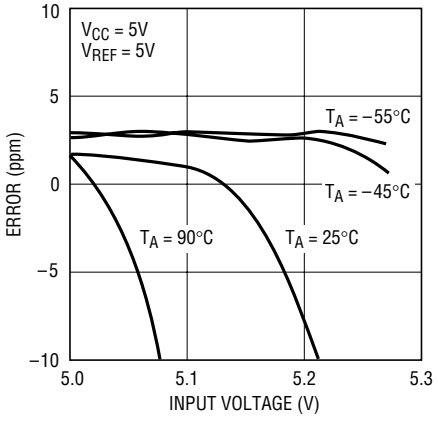
2400 G06

Negative Input Extended Total Unadjusted Error (5V Supply)



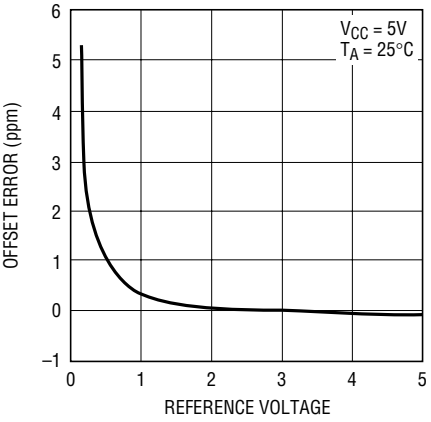
2400 G07

Positive Input Extended Total Unadjusted Error (5V Supply)



2400 G08

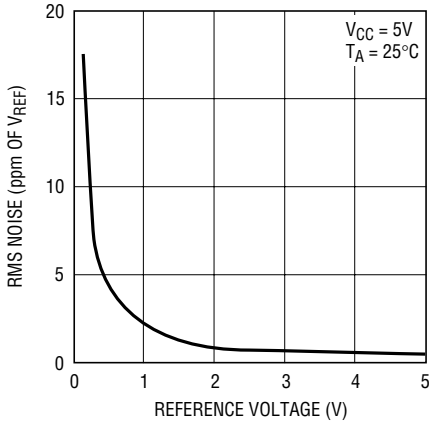
Offset Error vs Reference Voltage



2400 G09

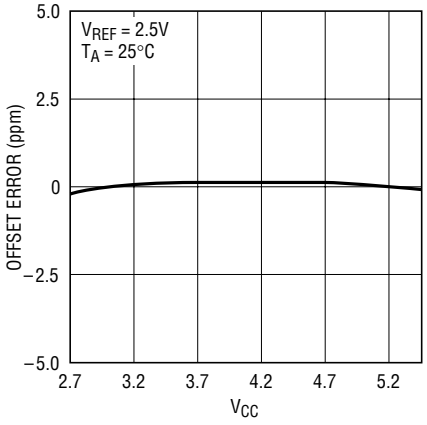
TYPICAL PERFORMANCE CHARACTERISTICS

RMS Noise vs Reference Voltage



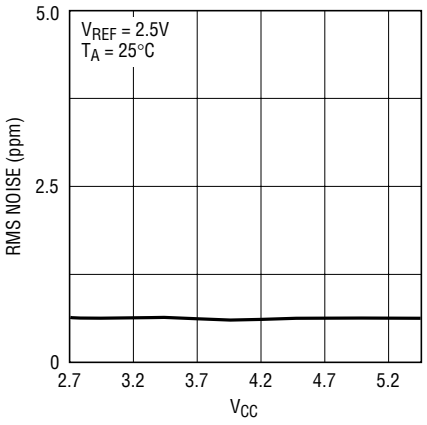
2400 G10

Offset Error vs V_{CC}



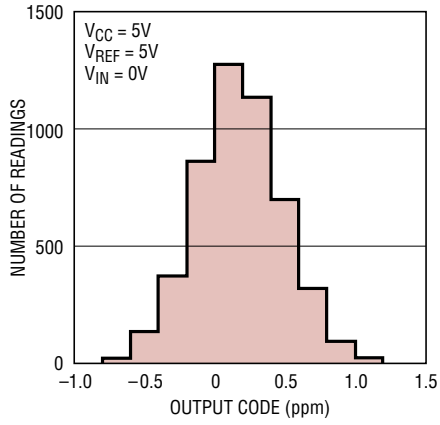
2400 G11

RMS Noise vs V_{CC}



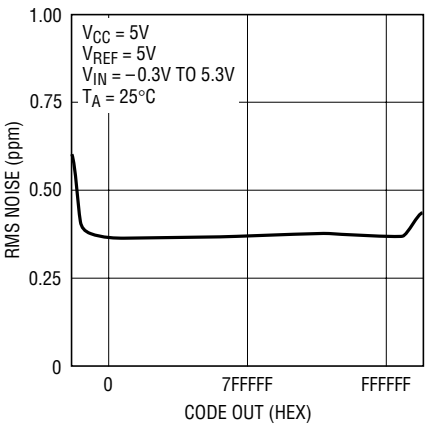
2400 G12

Noise Histogram



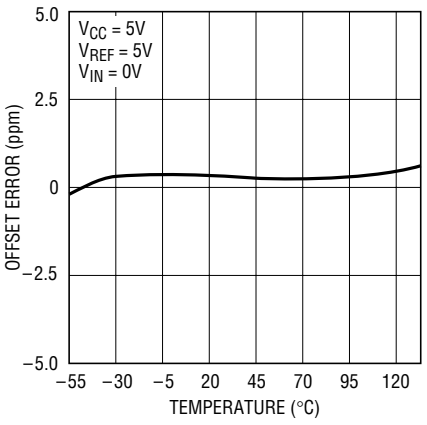
2400 G14

RMS Noise vs Code Out



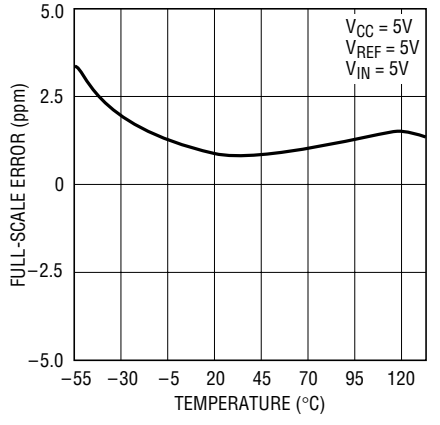
2400 G18

Offset Error vs Temperature



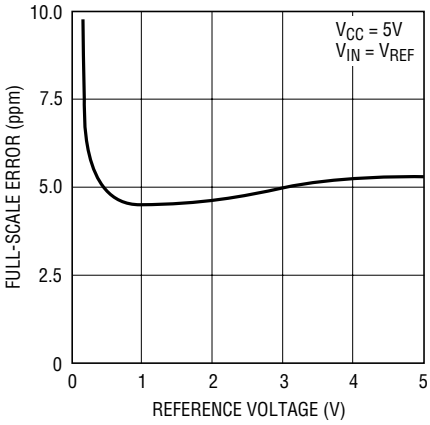
2400 G13

Full-Scale Error vs Temperature



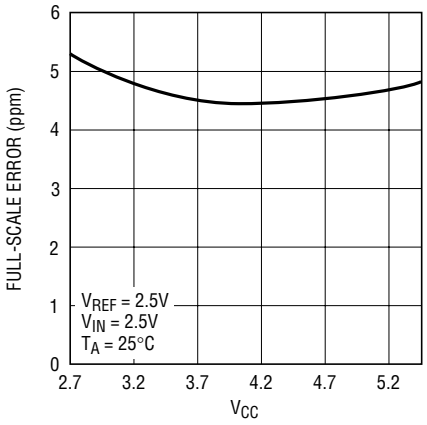
2400 G15

Full-Scale Error vs Reference Voltage



2400 G16

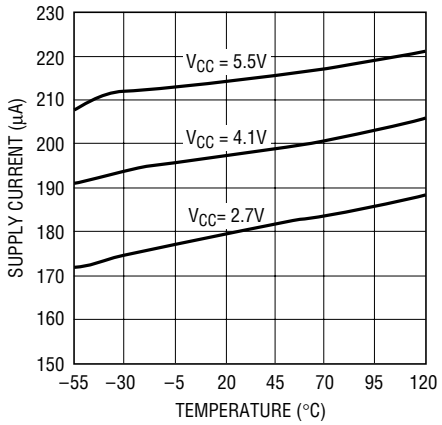
Full-Scale Error vs V_{CC}



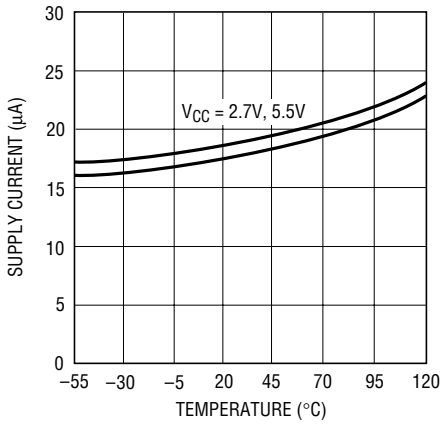
2400 G17

TYPICAL PERFORMANCE CHARACTERISTICS

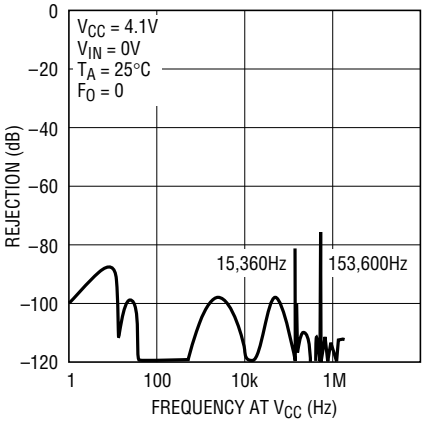
Conversion Current vs Temperature



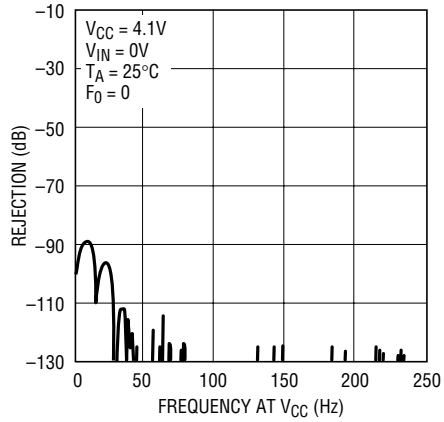
Sleep Current vs Temperature



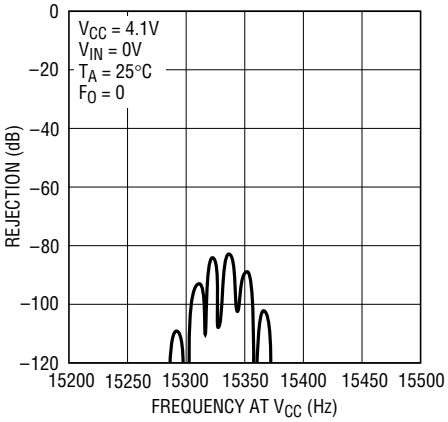
PSRR vs Frequency at V_{CC}



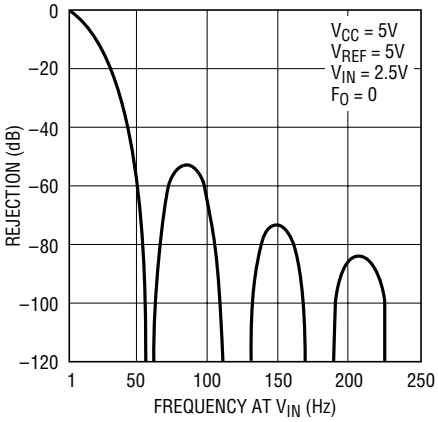
PSRR vs Frequency at V_{CC}



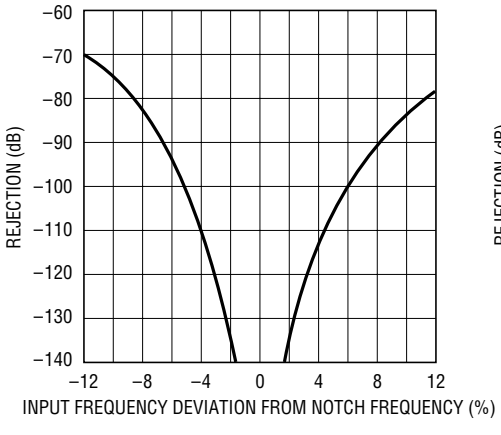
PSRR vs Frequency at V_{CC}



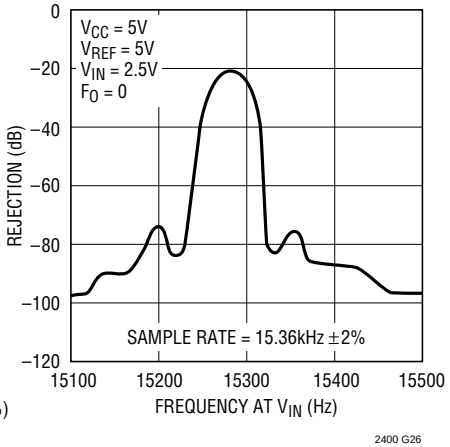
Rejection vs Frequency at V_{IN}



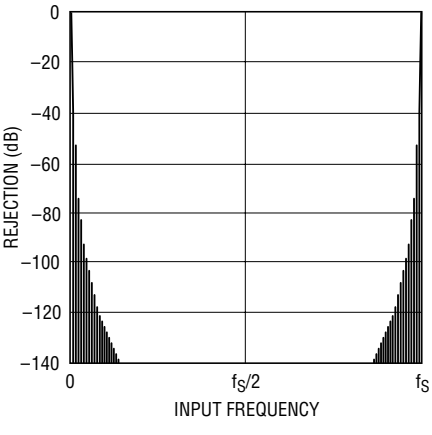
Rejection vs Frequency at V_{IN}



Rejection vs Frequency at V_{IN}

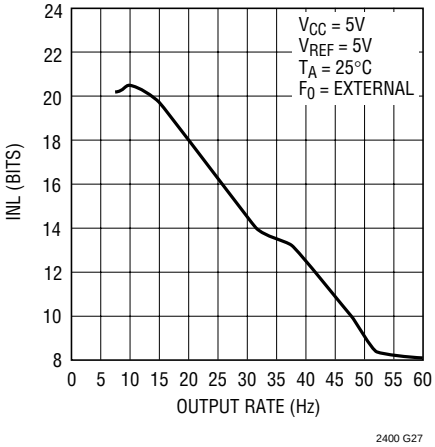


Rejection vs Frequency at V_{IN}

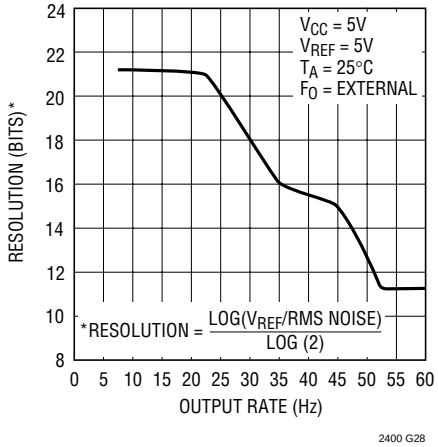


TYPICAL PERFORMANCE CHARACTERISTICS

INL vs Output Rate



Resolution vs Output Rate



PIN FUNCTIONS

V_{CC} (Pin 1): Positive Supply Voltage. Bypass to GND (Pin 4) with a 10µF tantalum capacitor in parallel with 0.1µF ceramic capacitor as close to the part as possible.

V_{REF} (Pin 2): Reference Input. The reference voltage range is 0.1V to V_{CC}.

V_{IN} (Pin 3): Analog Input. The input voltage range is $-0.125 \cdot V_{REF}$ to $1.125 \cdot V_{REF}$. For $V_{REF} > 2.5V$, the input voltage range may be limited by the pin absolute maximum rating of –0.3V to V_{CC} + 0.3V.

GND (Pin 4): Ground. Shared pin for analog ground, digital ground, reference ground and signal ground. Should be connected directly to a ground plane through a minimum length trace or it should be the single-point-ground in a single point grounding system.

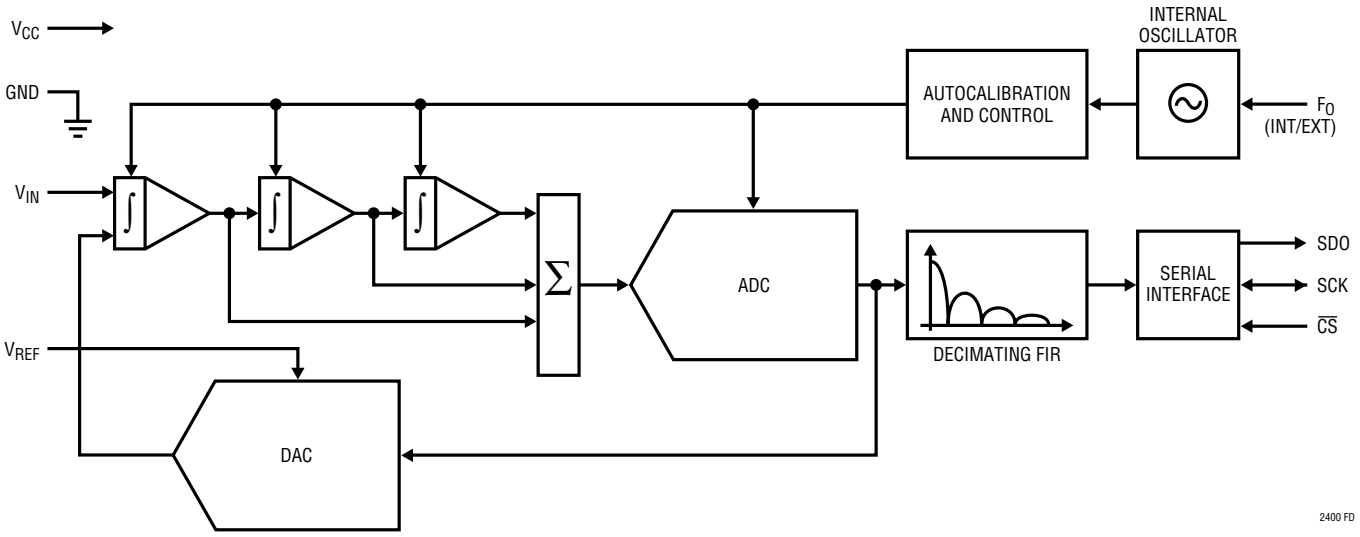
$\overline{CS}$ (Pin 5): Active LOW Digital Input. A LOW on this pin enables the SDO digital output and wakes up the ADC. Following each conversion the ADC automatically enters the Sleep mode and remains in this low power state as long as $\overline{CS}$ is HIGH. A LOW on $\overline{CS}$ wakes up the ADC. A LOW-to-HIGH transition on this pin disables the SDO digital output. A LOW-to-HIGH transition on $\overline{CS}$ during the Data Output transfer aborts the data transfer and starts a new conversion.

SDO (Pin 6): Three-State Digital Output. During the data output period, this pin is used for serial data output. When the chip select $\overline{CS}$ is HIGH ($\overline{CS} = V_{CC}$), the SDO pin is in a high impedance state. During the Conversion and Sleep periods this pin can be used as a conversion status output. The conversion status can be observed by pulling $\overline{CS}$ LOW.

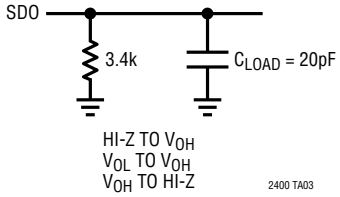
SCK (Pin 7): Bidirectional Digital Clock Pin. In Internal Serial Clock Operation mode, SCK is used as digital output for the internal serial interface clock during the data output period. In External Serial Clock Operation mode, SCK is used as digital input for the external serial interface. A weak internal pull-up is automatically activated in Internal Serial Clock Operation mode. The Serial Clock mode is determined by the level applied to SCK at power up and the falling edge of $\overline{CS}$.

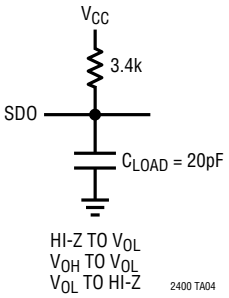
F_O (Pin 8): Frequency Control Pin. Digital input that controls the ADC's notch frequencies and conversion time. When the F_O pin is connected to V_{CC} ($F_O = V_{CC}$), the converter uses its internal oscillator and the digital filter first null is located at 50Hz. When the F_O pin is connected to GND (F_O = OV), the converter uses its internal oscillator and the digital filter first null is located at 60Hz. When F_O is driven by an external clock signal with a frequency f_{EOSC}, the converter uses this signal as its clock and the digital filter first null is located at a frequency $f_{EOSC}/2560$.

FUNCTIONAL BLOCK DIAGRAM



TEST CIRCUITS





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Converter Operation Cycle

The LTC2400 is a low power, delta-sigma analog-to-digital converter with an easy to use 3-wire serial interface. Its operation is simple and made up of three states. The converter operating cycle begins with the conversion, followed by a low power sleep state and concluded with the data output (see Figure 1). The 3-wire interface consists of serial data output (SDO), a serial clock (SCK) and a chip select ($\overline{CS}$).

Initially, the LTC2400 performs a conversion. Once the conversion is complete, the device enters the sleep state. While in this sleep state, power consumption is reduced by

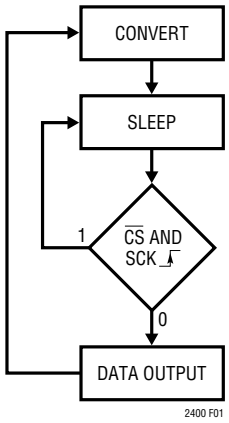

Figure 1. LTC2400 State Transition Diagram

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an order of magnitude. The part remains in the sleep state as long as $\overline{CS}$ is logic HIGH. The conversion result is held indefinitely in a static shift register while the converter is in the sleep state.

Once $\overline{CS}$ is pulled low, the device begins outputting the conversion result. There is no latency in the conversion result. The data output corresponds to the conversion just performed. This result is shifted out on the serial data out pin (SDO) under the control of the serial clock (SCK). Data is updated on the falling edge of SCK allowing the user to reliably latch data on the rising edge of SCK, see Figure 3. The data output state is concluded once 32 bits are read out of the ADC or when $\overline{CS}$ is brought HIGH. The device automatically initiates a new conversion cycle and the cycle repeats.

Through timing control of the $\overline{CS}$ and SCK pins, the LTC2400 offers several flexible modes of operation (internal or external SCK and free-running conversion modes). These various modes do not require programming configuration registers; moreover, they do not disturb the cyclic operation described above. These modes of operation are described in detail in the Serial Interface Timing Modes section.

Conversion Clock

A major advantage delta-sigma converters offer over conventional type converters is an on-chip digital filter (commonly known as Sinc or Comb filter). For high resolution, low frequency applications, this filter is typically designed to reject line frequencies of 50 or 60Hz plus their harmonics. In order to reject these frequencies in excess of 110dB, a highly accurate conversion clock is required. The LTC2400 incorporates an on-chip highly accurate oscillator. This eliminates the need for external frequency setting components such as crystals or oscillators. Clocked by the on-chip oscillator, the LTC2400 rejects line frequencies (50 or 60Hz ±2%) a minimum of 110dB.

Ease of Use

The LTC2400 data output has no latency, filter settling or redundant data associated with the conversion cycle. There is a one-to-one correspondence between the conversion and the output data. Therefore, multiplexing an analog input voltage is easy.

The LTC2400 performs offset and full-scale calibrations every conversion cycle. This calibration is transparent to the user and has no effect on the cyclic operation described above. The advantage of continuous calibration is extreme stability of offset and full-scale readings with respect to time, supply voltage change and temperature drift.

Power-Up Sequence

The LTC2400 automatically enters an internal reset state when the power supply voltage V_{CC} drops below approximately 2.2V. This feature guarantees the integrity of the conversion result and of the serial interface mode selection which is performed at the initial power-up. (See the 2-wire I/O sections in the Serial Interface Timing Modes section.)

When the V_{CC} voltage rises above this critical threshold, the converter creates an internal power-on-reset (POR) signal with duration of approximately 0.5ms. The POR signal clears all internal registers. Following the POR signal, the LTC2400 starts a normal conversion cycle and follows the normal succession of states described above. The first conversion result following POR is accurate within the specifications of the device.

Reference Voltage Range

The LTC2400 can accept a reference voltage from 0V to V_{CC}. The converter output noise is determined by the thermal noise of the front-end circuits, and as such, its value in microvolts is nearly constant with reference voltage. A decrease in reference voltage will not significantly improve the converter's effective resolution. On the other hand, a reduced reference voltage will improve the overall converter INL performance. The recommended range for the LTC2400 voltage reference is 100mV to V_{CC}.

Input Voltage Range

The converter is able to accommodate system level offset and gain errors as well as system level overrange situations due to its extended input range, see Figure 2. The LTC2400 converts input signals within the extended input range of $-0.125 \cdot V_{REF}$ to $1.125 \cdot V_{REF}$.

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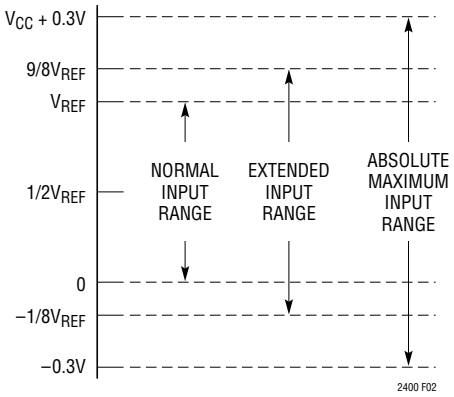

Figure 2. LTC2400 Input Range

For large values of V_{REF} this range is limited by the absolute maximum voltage range of –0.3V to (V_{CC} + 0.3V). Beyond this range the input ESD protection devices begin to turn on and the errors due to the input leakage current increase rapidly.

Input signals applied to V_{IN} may extend below ground by –300mV and above V_{CC} by 300mV. In order to limit any fault current, a resistor of up to 5k may be added in series with the V_{IN} pin without affecting the performance of the device. In the physical layout, it is important to maintain the parasitic capacitance of the connection between this series resistance and the V_{IN} pin as low as possible; therefore, the resistor should be located as close as practical to the V_{IN} pin. The effect of the series resistance on the converter accuracy can be evaluated from the curves presented in the Analog Input/Reference Current section. In addition a series resistor will introduce a temperature dependent offset error due to the input leakage current. A 1nA input leakage current will develop a 1ppm offset error on a 5k resistor if V_{REF} = 5V. This error has a very strong temperature dependency.

Output Data Format

The LTC2400 serial output data stream is 32 bits long. The first 4 bits represent status information indicating the sign, input range and conversion state. The next 24 bits are the conversion result, MSB first. The remaining 4 bits are sub LSBs beyond the 24-bit level that may be included in averaging or discarded without loss of resolution.

Bit 31 (first output bit) is the end of conversion ($\overline{EOC}$) indicator. This bit is available at the SDO pin during the conversion and sleep states whenever the $\overline{CS}$ pin is LOW. This bit is HIGH during the conversion and goes LOW when the conversion is complete.

Bit 30 (second output bit) is a dummy bit (DMY) and is always LOW.

Bit 29 (third output bit) is the conversion result sign indicator (SIG). If V_{IN} is >0, this bit is HIGH. If V_{IN} is <0, this bit is LOW. The sign bit changes state during the zero code.

Bit 28 (forth output bit) is the extended input range (EXR) indicator. If the input is within the normal input range $0 \le V_{IN} \le V_{REF}$, this bit is LOW. If the input is outside the normal input range, $V_{IN} > V_{REF}$ or $V_{IN} < 0$, this bit is HIGH.

The function of these bits is summarized in Table 1.

Table 1. LTC2400 Status Bits

Input Range	Bit 31 $\overline{EOC}$	Bit 30 DMY	Bit 29 SIG	Bit 28 EXR
$V_{IN} > V_{REF}$	0	0	1	1
$0 < V_{IN} \le V_{REF}$	0	0	1	0
$V_{IN} = 0^+/0^-$	0	0	1/0	0
$V_{IN} < 0$	0	0	0	1

Bit 27 (fifth output bit) is the most significant bit (MSB).

Bits 27-4 are the 24-bit conversion result MSB first.

Bit 4 is the least significant bit (LSB).

Bits 3-0 are sub LSBs below the 24-bit level. Bits 3-0 may be included in averaging or discarded without loss of resolution.

Data is shifted out of the SDO pin under control of the serial clock (SCK), see Figure 3. Whenever $\overline{CS}$ is HIGH, SDO remains high impedance and any SCK clock pulses are ignored by the internal data out shift register.

In order to shift the conversion result out of the device, $\overline{CS}$ must first be driven LOW. $\overline{EOC}$ is seen at the SDO pin of the device once $\overline{CS}$ is pulled LOW. $\overline{EOC}$ changes real time from HIGH to LOW at the completion of a conversion. This signal may be used as an interrupt for an external microcontroller. Bit 31 ($\overline{EOC}$) can be captured on the first rising edge of SCK. Bit 30 is shifted out of the device on the first falling edge of SCK. The final data bit (Bit 0) is shifted

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out on the falling edge of the 31st SCK and may be latched on the rising edge of the 32nd SCK pulse. On the falling edge of the 32nd SCK pulse, SDO goes HIGH indicating a new conversion cycle has been initiated. This bit serves as $\overline{EOC}$ (Bit 31) for the next conversion cycle. Table 2 summarizes the output data format.

As long as the voltage on the V_{IN} pin is maintained within the –0.3V to (V_{CC} + 0.3V) absolute maximum operating range, a conversion result is generated for any input value from –0.125 • V_{REF} to 1.125 • V_{REF}. For input voltages greater than 1.125 • V_{REF}, the conversion result is clamped to the value corresponding to 1.125 • V_{REF}. For input voltages below –0.125 • V_{REF}, the conversion result is clamped to the value corresponding to –0.125 • V_{REF}.

Frequency Rejection Selection (F_O Pin Connection)

The LTC2400 internal oscillator provides better than 110dB normal mode rejection at the line frequency and all its harmonics for 50Hz ±2% or 60Hz ±2%. For 60Hz rejection, F_O (Pin 8) should be connected to GND (Pin 4) while for 50Hz rejection the F_O pin should be connected to V_{CC} (Pin 1).

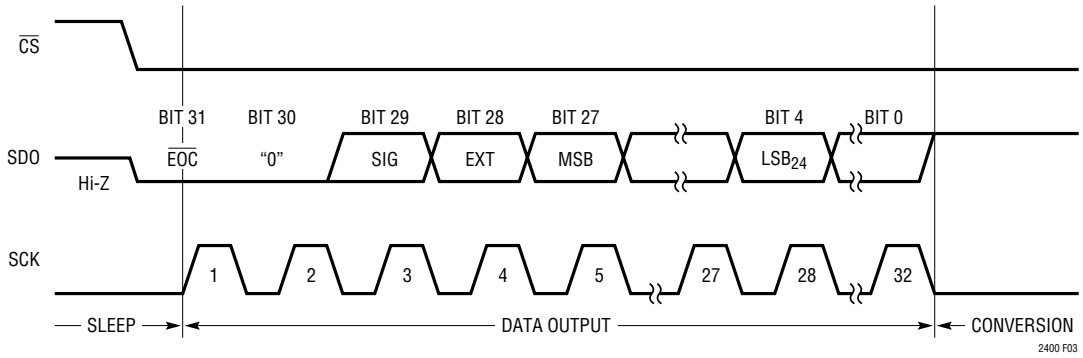

Figure 3. Output Data Timing

Table 2. LTC2400 Output Data Format

Input Voltage	Bit 31 $\overline{EOC}$	Bit 30 DMY	Bit 29 SIG	Bit 28 EXR	Bit 27 MSB	Bit 26	Bit 25	Bit 24	Bit 23	…	Bit 4 LSB	Bit 3-0 SUB LSBs*
V_{IN} > 9/8 • V_{REF}	0	0	1	1	0	0	0	1	1	...	1	X
9/8 • V_{REF}	0	0	1	1	0	0	0	1	1	...	1	X
V_{REF} + 1LSB	0	0	1	1	0	0	0	0	0	...	0	X
V_{REF}	0	0	1	0	1	1	1	1	1	...	1	X
3/4V_{REF} + 1LSB	0	0	1	0	1	1	0	0	0	...	0	X
3/4V_{REF}	0	0	1	0	1	0	1	1	1	...	1	X
1/2V_{REF} + 1LSB	0	0	1	0	1	0	0	0	0	...	0	X
1/2V_{REF}	0	0	1	0	0	1	1	1	1	...	1	X
1/4V_{REF} + 1LSB	0	0	1	0	0	1	0	0	0	...	0	X
1/4V_{REF}	0	0	1	0	0	0	1	1	1	...	1	X
$0^+/0^-$	0	0	1/0**	0	0	0	0	0	0	...	0	X
–1LSB	0	0	0	1	1	1	1	1	1	...	1	X
–1/8 • V_{REF}	0	0	0	1	1	1	1	0	0	...	0	X
V_{IN} < –1/8 • V_{REF}	0	0	0	1	1	1	1	0	0	...	0	X

*The sub LSBs are valid conversion results beyond the 24-bit level that may be included in averaging or discarded without loss of resolution.
**The sign bit changes state during the 0 code.

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The selection of 50Hz or 60Hz rejection can also be made by driving F_O to an appropriate logic level. A selection change during the sleep or data output states will not disturb the converter operation. If the selection is made during the conversion state, the result of the conversion in progress may be outside specifications but the following conversions will not be affected.

When a fundamental rejection frequency different from 50Hz or 60Hz is required or when the converter must be synchronized with an outside source, the LTC2400 can operate with an external conversion clock. The converter automatically detects the presence of an external clock signal at the F_O pin and turns off the internal oscillator. The frequency f_{EOSC} of the external signal must be at least 2560Hz (1Hz notch frequency) to be detected. The external clock signal duty cycle is not significant as long as the minimum and maximum specifications for the high and low periods t_{HEO} and t_{LEO} are observed.

While operating with an external conversion clock of a frequency f_{EOSC}, the LTC2400 provides better than 110dB normal mode rejection in a frequency range $f_{EOSC}/2560 \pm 4\%$ and its harmonics. The normal mode rejection as a function of the input frequency deviation from $f_{EOSC}/2560$ is shown in Figure 4.

Whenever an external clock is not present at the F_O pin, the converter automatically activates its internal oscillator and enters the Internal Conversion Clock mode. The LTC2400 operation will not be disturbed if the change of conversion clock source occurs during the sleep state or during the data output state while the converter uses an external serial clock. If the change occurs during the conversion state, the result of the conversion in progress may be outside specifications but the following conversions will not be affected. If the change occurs during the data output state and the converter is in the Internal SCK mode, the serial clock duty cycle may be affected but the serial data stream will remain valid.

Table 3 summarizes the duration of each state as a function of F_O.

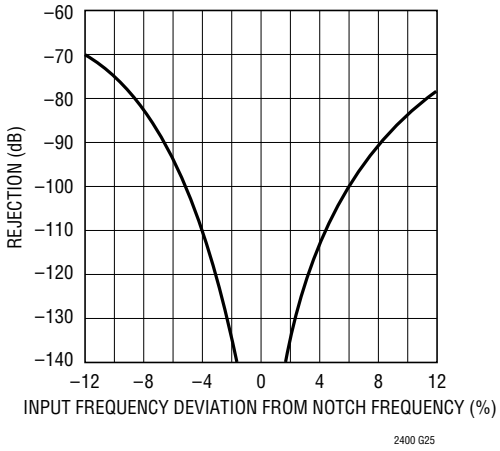

Figure 4. LTC2400 Normal Mode Rejection When Using an External Oscillator of Frequency f_{EOSC}

Table 3. LTC2400 State Duration

State	Operating Mode		Duration
CONVERT	Internal Oscillator	F_O = LOW (60Hz Rejection)	133ms
		F_O = HIGH (50Hz Rejection)	160ms
	External Oscillator	F_O = External Oscillator with Frequency f_{EOSC} kHz ($f_{EOSC}/2560$ Rejection)	$20480/f_{EOSC}$s
SLEEP			As Long As $\overline{CS}$ = HIGH Until $\overline{CS}$ = 0 and SCK ↓
DATA OUTPUT	Internal Serial Clock	F_O = LOW/HIGH (Internal Oscillator)	As Long As $\overline{CS}$ = LOW But Not Longer Than 1.67ms (32 SCK cycles)
		F_O = External Oscillator with Frequency f_{EOSC} kHz	As Long As $\overline{CS}$ = LOW But Not Longer Than $256/f_{EOSC}$ms (32 SCK cycles)
	External Serial Clock with Frequency f_{SCK} kHz		As Long As $\overline{CS}$ = LOW But Not Longer Than $32/f_{SCK}$ms (32 SCK cycles)

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SERIAL INTERFACE

The LTC2400 transmits the conversion results and receives the start of conversion command through a synchronous 3-wire interface. During the conversion and sleep states, this interface can be used to assess the converter status and during the data output state it is used to read the conversion result.

Serial Clock Input/Output (SCK)

The serial clock signal present on SCK (Pin 7) is used to synchronize the data transfer. Each bit of data is shifted out the SDO pin on the falling edge of the serial clock.

In the Internal SCK mode of operation, the SCK pin is an output and the LTC2400 creates its own serial clock by dividing the internal conversion clock by 8. In the External SCK mode of operation, the SCK pin is used as input. The internal or external SCK mode is selected on power-up and then reselected every time a HIGH-to-LOW transition is detected at the $\overline{CS}$ pin. If SCK is HIGH or floating at power-up or during this transition, the converter enters the internal SCK mode. If SCK is LOW at power-up or during this transition, the converter enters the external SCK mode.

Serial Data Output (SDO)

The serial data output pin, SDO (Pin 6), drives the serial data during the data output state. In addition, the SDO pin is used as an end of conversion indicator during the conversion and sleep states.

When $\overline{CS}$ (Pin 5) is HIGH, the SDO driver is switched to a high impedance state. This allows sharing the serial interface with other devices. If $\overline{CS}$ is LOW during the convert or sleep state, SDO will output $\overline{EOC}$. If $\overline{CS}$ is LOW during the conversion phase, the $\overline{EOC}$ bit appears HIGH on the SDO pin. Once the conversion is complete, $\overline{EOC}$ goes LOW. The device remains in the sleep state until the first rising edge of SCK occurs while $\overline{CS}$ = 0.

Chip Select Input ($\overline{CS}$)

The active LOW chip select, $\overline{CS}$ (Pin 5), is used to test the conversion status and to enable the data output transfer as described in the previous sections.

In addition, the $\overline{CS}$ signal can be used to trigger a new conversion cycle before the entire serial data transfer has been completed. The LTC2400 will abort any serial data transfer in progress and start a new conversion cycle anytime a LOW-to-HIGH transition is detected at the $\overline{CS}$ pin after the converter has entered the data output state (i.e., after the first rising edge of SCK occurs with $\overline{CS}$ = 0).

Finally, $\overline{CS}$ can be used to control the free-running modes of operation, see Serial Interface Timing Modes section. Grounding $\overline{CS}$ will force the ADC to continuously convert at the maximum output rate selected by F_O. Tying a capacitor to $\overline{CS}$ will reduce the output rate and power dissipation by a factor proportional to the capacitor's value, see Figures 12 to 14.

SERIAL INTERFACE TIMING MODES

The LTC2400's 3-wire interface is SPI and MICROWIRE compatible. This interface offers several flexible modes of operation. These include internal/external serial clock, 2- or 3-wire I/O, single cycle conversion and autostart. The following sections describe each of these serial interface timing modes in detail. In all these cases, the converter can use the internal oscillator (F_O = LOW or F_O = HIGH) or an external oscillator connected to the F_O pin. Refer to Table 4 for a summary.

Table 4. LTC2400 Interface Timing Modes

Configuration	SCK Source	Conversion Cycle Control	Data Output Control	Connection and Waveforms
External SCK, Single Cycle Conversion	External	$\overline{CS}$ and SCK	$\overline{CS}$ and SCK	Figures 5, 6
External SCK, 2-Wire I/O	External	SCK	SCK	Figure 7
Internal SCK, Single Cycle Conversion	Internal	$\overline{CS}$ ↓	$\overline{CS}$ ↓	Figures 8, 9
Internal SCK, 2-Wire I/O, Continuous Conversion	Internal	Continuous	Internal	Figure 10
Internal SCK, Autostart Conversion	Internal	C_{EXT}	Internal	Figure 11

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External Serial Clock, Single Cycle Operation (SPI/MICROWIRE Compatible)

This timing mode uses an external serial clock to shift out the conversion result and a $\overline{CS}$ signal to monitor and control the state of the conversion cycle, see Figure 5.

The serial clock mode is selected on the falling edge of $\overline{CS}$. To select the external serial clock mode, the serial clock pin (SCK) must be LOW during each $\overline{CS}$ falling edge.

The serial data output pin (SDO) is HI-Z as long as $\overline{CS}$ is HIGH. At any time during the conversion cycle, $\overline{CS}$ may be pulled LOW in order to monitor the state of the converter. While $\overline{CS}$ is pulled LOW, $\overline{EOC}$ is output to the SDO pin. $\overline{EOC}$ = 1 while a conversion is in progress and $\overline{EOC}$ = 0 if the device is in the sleep state. Independent of $\overline{CS}$, the device automatically enters the low power sleep state once the conversion is complete.

When the device is in the sleep state ($\overline{EOC}$ = 0), its conversion result is held in an internal static shift register. The device remains in the sleep state until the first rising edge of SCK is seen while $\overline{CS}$ is LOW. Data is shifted out the SDO pin on each falling edge of SCK. This enables external circuitry to latch the output on the rising edge of SCK. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 32nd rising edge of SCK. On the 32nd falling edge of SCK, the device begins a new conversion. SDO goes HIGH ($\overline{EOC}$ = 1) indicating a conversion is in progress.

At the conclusion of the data cycle, $\overline{CS}$ may remain LOW and $\overline{EOC}$ monitored as an end-of-conversion interrupt. Alternatively, $\overline{CS}$ may be driven HIGH setting SDO to HI-Z. As described above, $\overline{CS}$ may be pulled LOW at any time in order to monitor the conversion status.

Typically, $\overline{CS}$ remains LOW during the data output state. However, the data output state may be aborted by pulling $\overline{CS}$ HIGH anytime between the first rising edge and the 32nd falling edge of SCK, see Figure 6. On the rising edge of $\overline{CS}$, the device aborts the data output state and immediately initiates a new conversion. This is useful for systems not requiring all 32 bits of output data, aborting an invalid conversion cycle or synchronizing the start of a conversion.

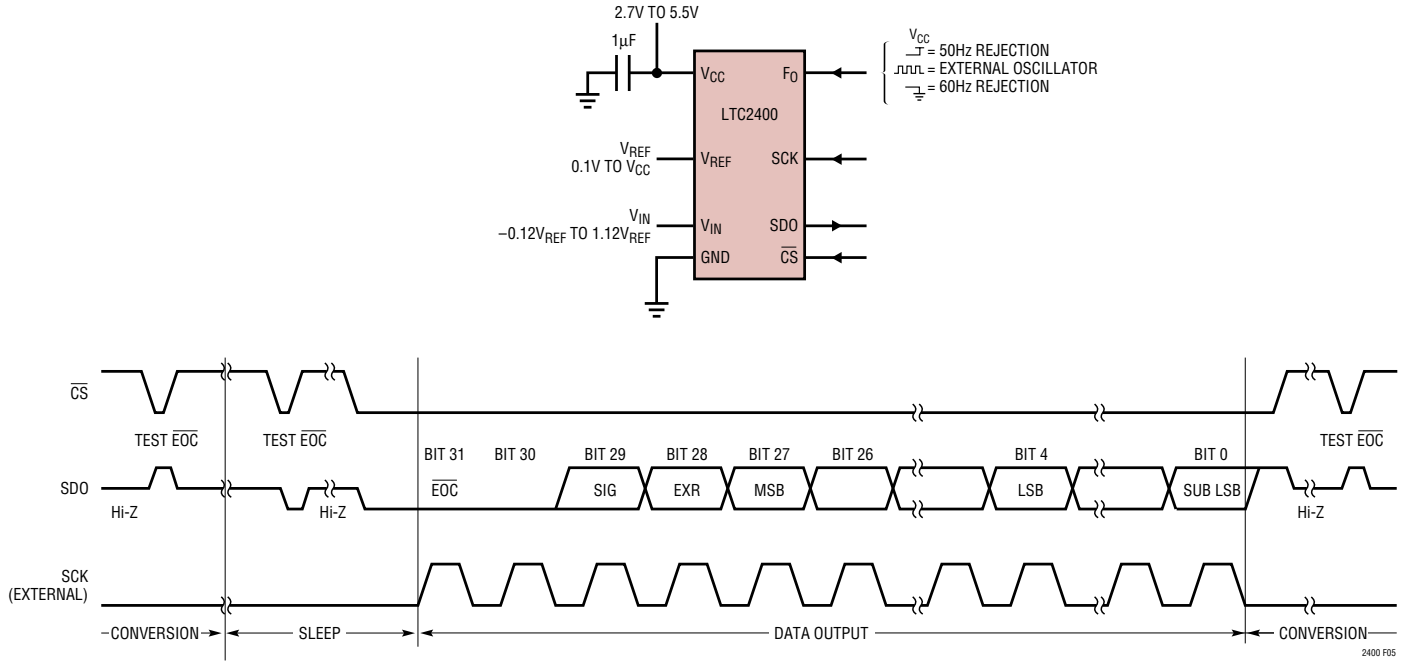

Figure 5. External Serial Clock, Single Cycle Operation

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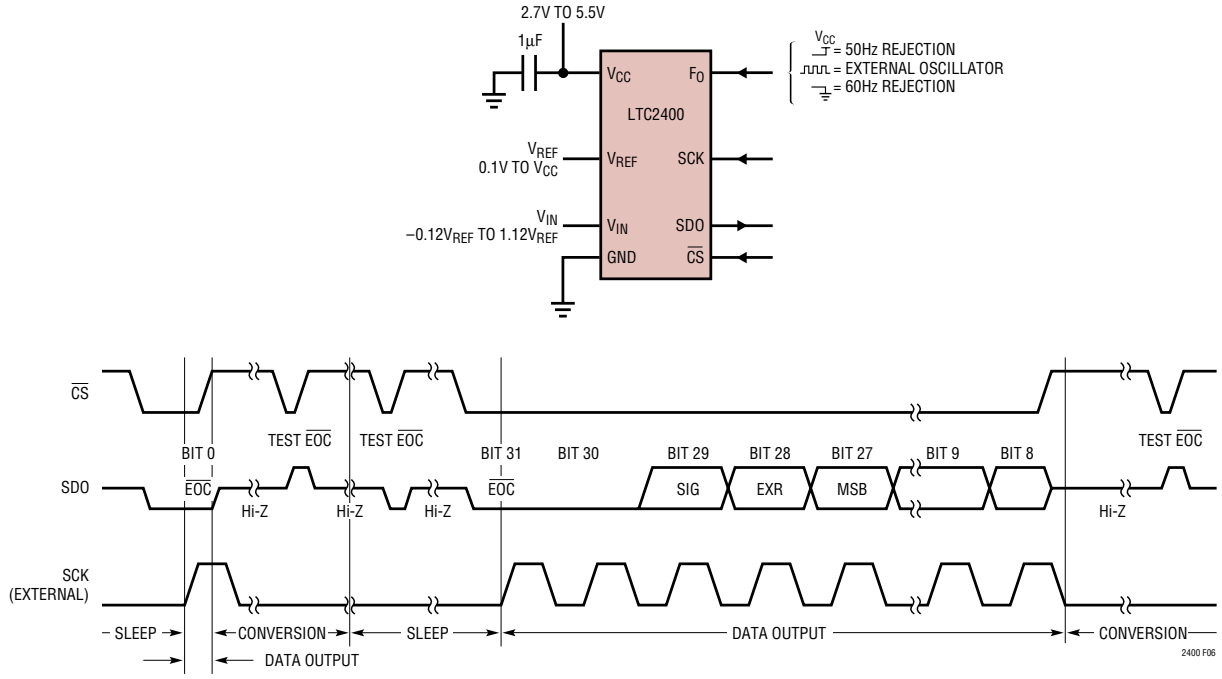

Figure 6. External Serial Clock, Reduced Data Output Length

External Serial Clock, 2-Wire I/O

This timing mode utilizes a 2-wire serial I/O interface. The conversion result is shifted out of the device by an externally generated serial clock (SCK) signal, see Figure 7. $\overline{CS}$ may be permanently tied to ground (Pin 4), simplifying the user interface or isolation barrier.

The external serial clock mode is selected at the end of the power-on reset (POR) cycle. The POR cycle is concluded approximately 0.5ms after V_{CC} exceeds 2.2V. The level applied to SCK at this time determines if SCK is internal or external. SCK must be driven LOW prior to the end of POR in order to enter the external serial clock timing mode.

Since $\overline{CS}$ is tied LOW, the end-of-conversion ($\overline{EOC}$) can be continuously monitored at the SDO pin during the convert and sleep states. $\overline{EOC}$ may be used as an interrupt to an external controller indicating the conversion result is ready. $\overline{EOC}$ = 1 while the conversion is in progress and $\overline{EOC}$ = 0 once the conversion enters the low power sleep state. On the falling edge of $\overline{EOC}$, the conversion result is loaded into an internal static shift register. The device remains in the sleep state until the first rising edge of SCK. Data is shifted out the SDO pin on each falling edge of SCK enabling external circuitry to latch data on the rising edge of SCK. $\overline{EOC}$ can be latched on the first rising edge of SCK. On the 32nd falling edge of SCK, SDO goes HIGH ($\overline{EOC}$ = 1) indicating a new conversion has begun.

Internal Serial Clock, Single Cycle Operation

This timing mode uses an internal serial clock to shift out the conversion result and a $\overline{CS}$ signal to monitor and control the state of the conversion cycle, see Figure 8.

In order to select the internal serial clock timing mode, the serial clock pin (SCK) must be floating (HI-Z) or pulled HIGH prior to the falling edge of $\overline{CS}$. The device will not enter the internal serial clock mode if SCK is driven LOW on the falling edge of $\overline{CS}$. An internal weak pull-up resistor is active on the SCK pin during the falling edge of $\overline{CS}$; therefore, the internal serial clock timing mode is automatically selected if SCK is not externally driven.

The serial data output pin (SDO) is HI-Z as long as $\overline{CS}$ is HIGH. At any time during the conversion cycle, $\overline{CS}$ may be pulled LOW in order to monitor the state of the converter.

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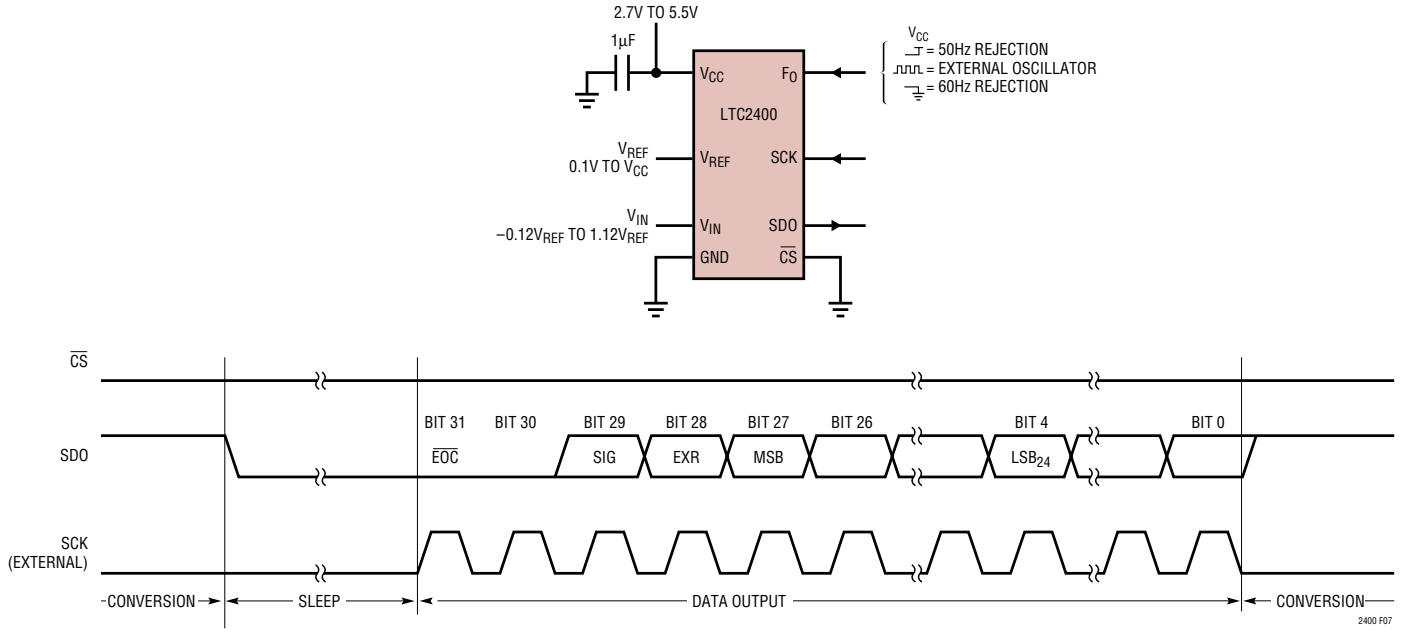

Figure 7. External Serial Clock, $\overline{CS}$ = 0 Operation

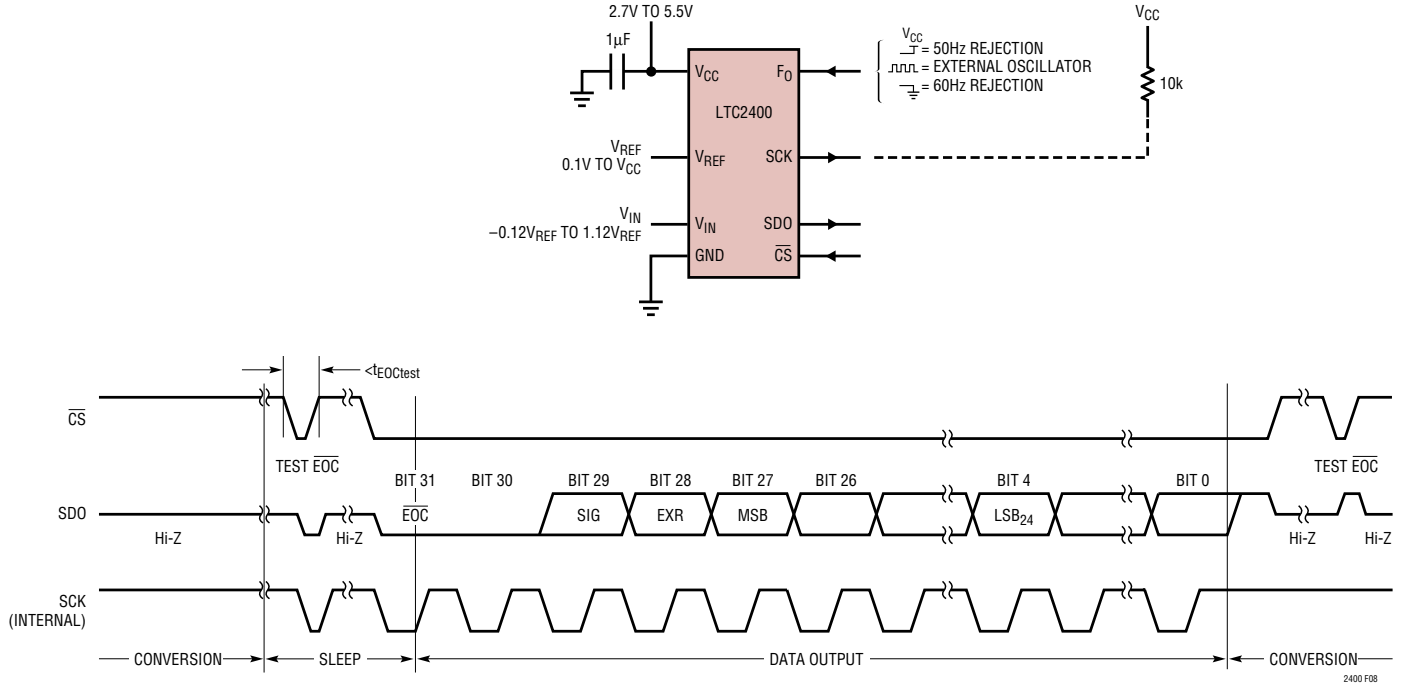

Figure 8. Internal Serial Clock, Single Cycle Operation

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Once $\overline{CS}$ is pulled LOW, SCK goes LOW and $\overline{EOC}$ is output to the SDO pin. $\overline{EOC}$ = 1 while a conversion is in progress and $\overline{EOC}$ = 0 if the device is in the sleep state.

When testing $\overline{EOC}$, if the conversion is complete ($\overline{EOC}$ = 0), the device will exit the sleep state and enter the data output state if $\overline{CS}$ remains LOW. In order to prevent the device from exiting the low power sleep state, $\overline{CS}$ must be pulled HIGH before the first rising edge of SCK. In the internal SCK timing mode, SCK goes HIGH and the device begins outputting data at time $t_{EOCtest}$ after the falling edge of $\overline{CS}$ (if $\overline{EOC}$ = 0) or $t_{EOCtest}$ after $\overline{EOC}$ goes LOW (if $\overline{CS}$ is LOW during the falling edge of $\overline{EOC}$). The value of $t_{EOCtest}$ is 23µs if the device is using its internal oscillator (F_O = logic LOW or HIGH). If F_O is driven by an external oscillator of frequency f_{EOSC}, then $t_{EOCtest}$ is $3.6/f_{EOSC}$. If $\overline{CS}$ is pulled HIGH before time $t_{EOCtest}$, the device remains in the sleep state. The conversion result is held in the internal static shift register.

If $\overline{CS}$ remains LOW longer than $t_{EOCtest}$, the first rising edge of SCK will occur and the conversion result is serially shifted out of the SDO pin. The data output cycle begins on this first rising edge of SCK and concludes after the 32nd rising edge. Data is shifted out the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the conversion result into external circuitry. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result on the 32nd rising edge of SCK. After the 32nd rising edge, SDO goes HIGH ($\overline{EOC}$ = 1), SCK stays HIGH, and a new conversion starts.

Typically, $\overline{CS}$ remains LOW during the data output state. However, the data output state may be aborted by pulling $\overline{CS}$ HIGH anytime between the first and 32nd rising edge of SCK, see Figure 9. On the rising edge of $\overline{CS}$, the device aborts the data output state and immediately initiates a new conversion. This is useful for systems not requiring all 32 bits of output data, aborting an invalid conversion cycle, or synchronizing the start of a conversion. If $\overline{CS}$ is pulled HIGH while the converter is driving SCK LOW, the internal pull-up is not available to restore SCK to a logic

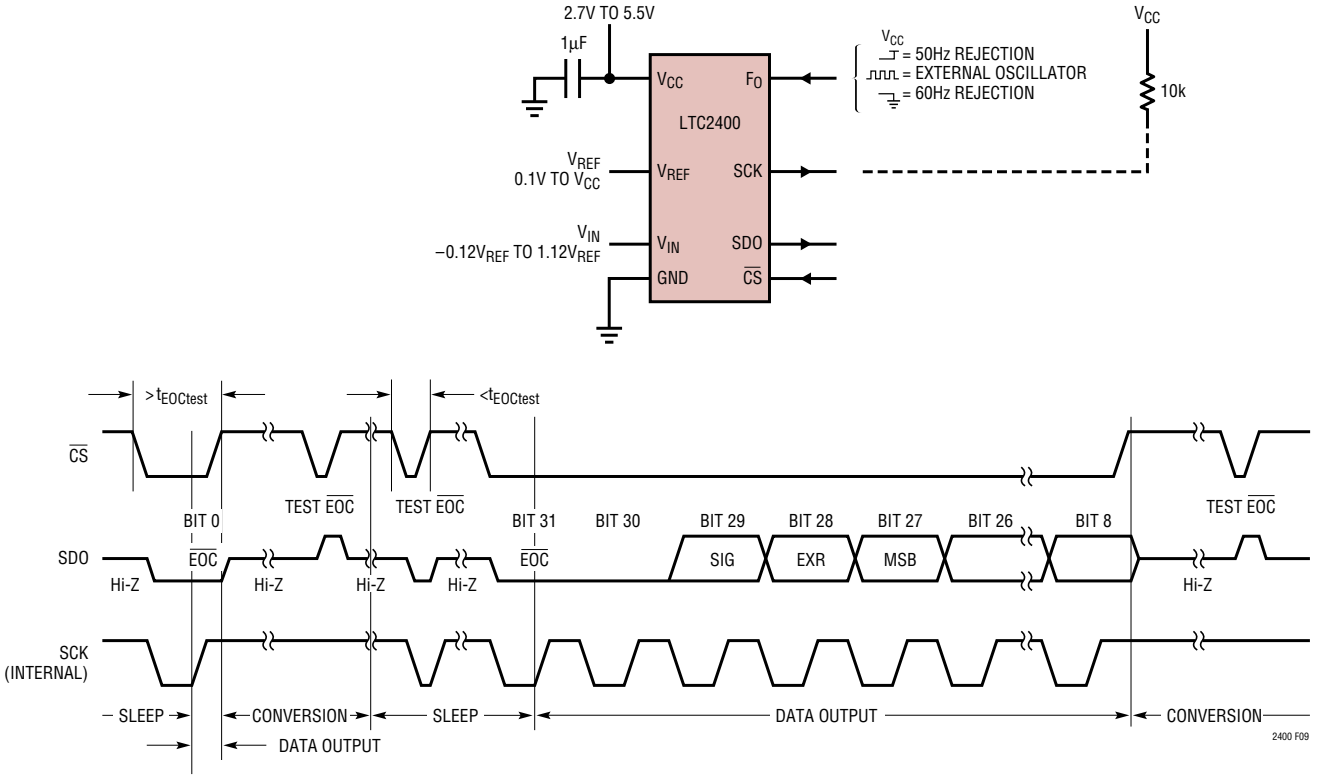

Figure 9. Internal Serial Clock, Reduced Data Output Length

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HIGH state. This will cause the device to exit the internal serial clock mode on the next falling edge of $\overline{CS}$. This can be avoided by adding an external 10k pull-up resistor to the SCK pin or by never pulling $\overline{CS}$ HIGH when SCK is LOW.

Whenever SCK is LOW, the LTC2400's internal pull-up at pin SCK is disabled. Normally, SCK is not externally driven if the device is in the internal SCK timing mode. However, certain applications may require an external driver on SCK. If this driver goes HI-Z after outputting a LOW signal, the LTC2400's internal pull-up remains disabled. Hence, SCK remains LOW. On the next falling edge of $\overline{CS}$, the device is switched to the external SCK timing mode. By adding an external 10k pull-up resistor to SCK, this pin goes HIGH once the external driver goes HI-Z. On the next $\overline{CS}$ falling edge, the device will remain in the internal SCK timing mode.

A similar situation may occur during the sleep state when $\overline{CS}$ is pulsed HIGH-LOW-HIGH in order to test the conversion status. If the device is in the sleep state ($\overline{EOC}$ = 0), SCK will go LOW. Once $\overline{CS}$ goes HIGH (within the time period defined above as $t_{EOCtest}$), the internal pull-up is activated. For a heavy capacitive load on the SCK pin, the internal pull-up may not be adequate to return SCK to a HIGH level before $\overline{CS}$ goes low again. This is not a concern under normal conditions where $\overline{CS}$ remains LOW after detecting $\overline{EOC}$ = 0. This situation is easily overcome by adding an external 10k pull-up resistor to the SCK pin.

Internal Serial Clock, 2-Wire I/O, Continuous Conversion

This timing mode uses a 2-wire, all output (SCK and SDO) interface. The conversion result is shifted out of the device by an internally generated serial clock (SCK) signal, see Figure 10. $\overline{CS}$ may be permanently tied to ground (Pin 4), simplifying the user interface or isolation barrier.

The internal serial clock mode is selected at the end of the power-on reset (POR) cycle. The POR cycle is concluded approximately 0.5ms after V_{CC} exceeds 2.2V. An internal weak pull-up is active during the POR cycle; therefore, the internal serial clock timing mode is automatically selected if SCK is not externally driven LOW (if SCK is loaded such that the internal pull-up cannot pull the pin HIGH, the external SCK mode will be selected).

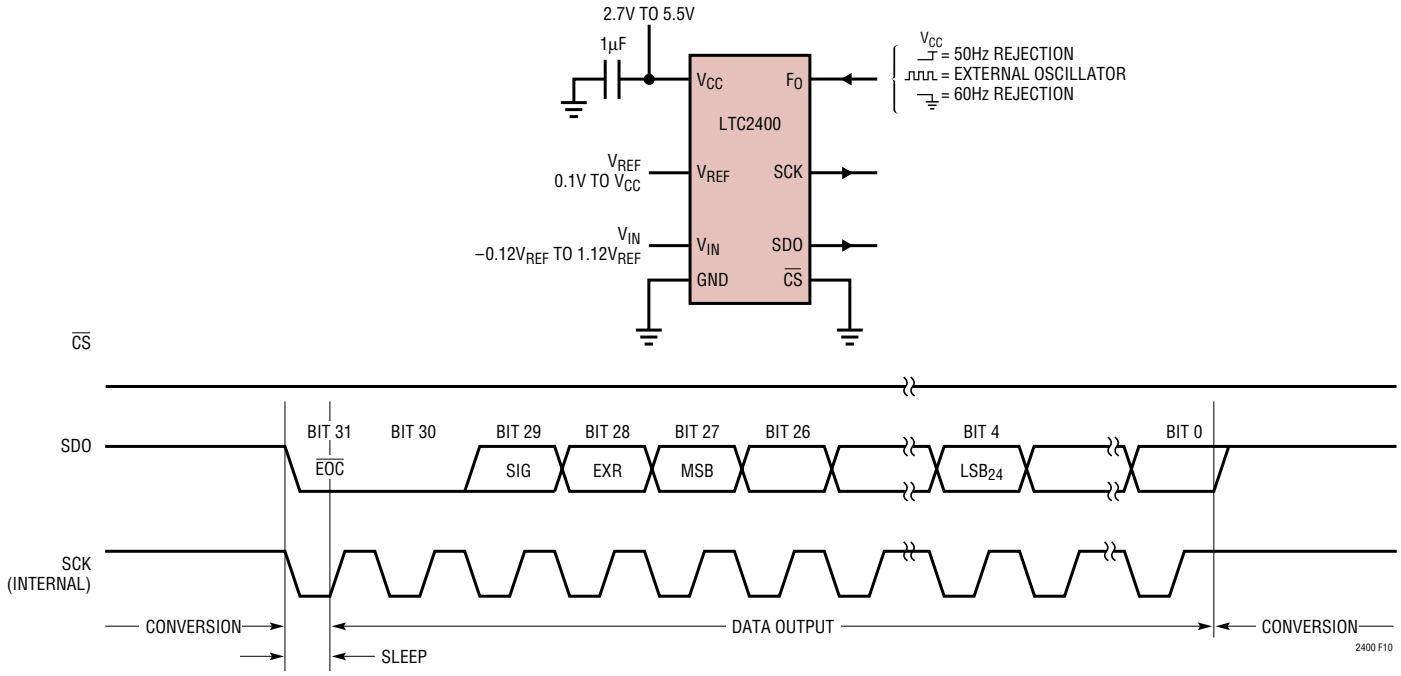

Figure 10. Internal Serial Clock, Continuous Operation

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During the conversion, the SCK and the serial data output pin (SDO) are HIGH ($\overline{EOC}$ = 1). Once the conversion is complete, SCK and SDO go LOW ($\overline{EOC}$ = 0) indicating the conversion has finished and the device has entered the low power sleep state. The part remains in the sleep state a minimum amount of time (1/2 the internal SCK period) then immediately begins outputting data. The data output cycle begins on the first rising edge of SCK and ends after the 32nd rising edge. Data is shifted out the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the conversion result into external circuitry. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 32nd rising edge of SCK. After the 32nd rising edge, SDO goes HIGH ($\overline{EOC}$ = 1) indicating a new conversion is in progress. SCK remains HIGH during the conversion.

Internal Serial Clock, Autostart Conversion

This timing mode is identical to the internal serial clock, 2-wire I/O described above with one additional feature. Instead of grounding $\overline{CS}$, an external timing capacitor is tied to $\overline{CS}$.

While the conversion is in progress, the $\overline{CS}$ pin is held HIGH by an internal weak pull-up. Once the conversion is complete, the device enters the low power sleep state and an internal 25nA current source begins discharging the capacitor tied to $\overline{CS}$, see Figure 11. The time the converter spends in the sleep state is determined by the value of the external timing capacitor, see Figures 12 and 13. Once the voltage at $\overline{CS}$ falls below an internal threshold (≈1.4V), the device automatically begins outputting data. The data output cycle begins on the first rising edge of SCK and ends on the 32nd rising edge. Data is shifted out the SDO

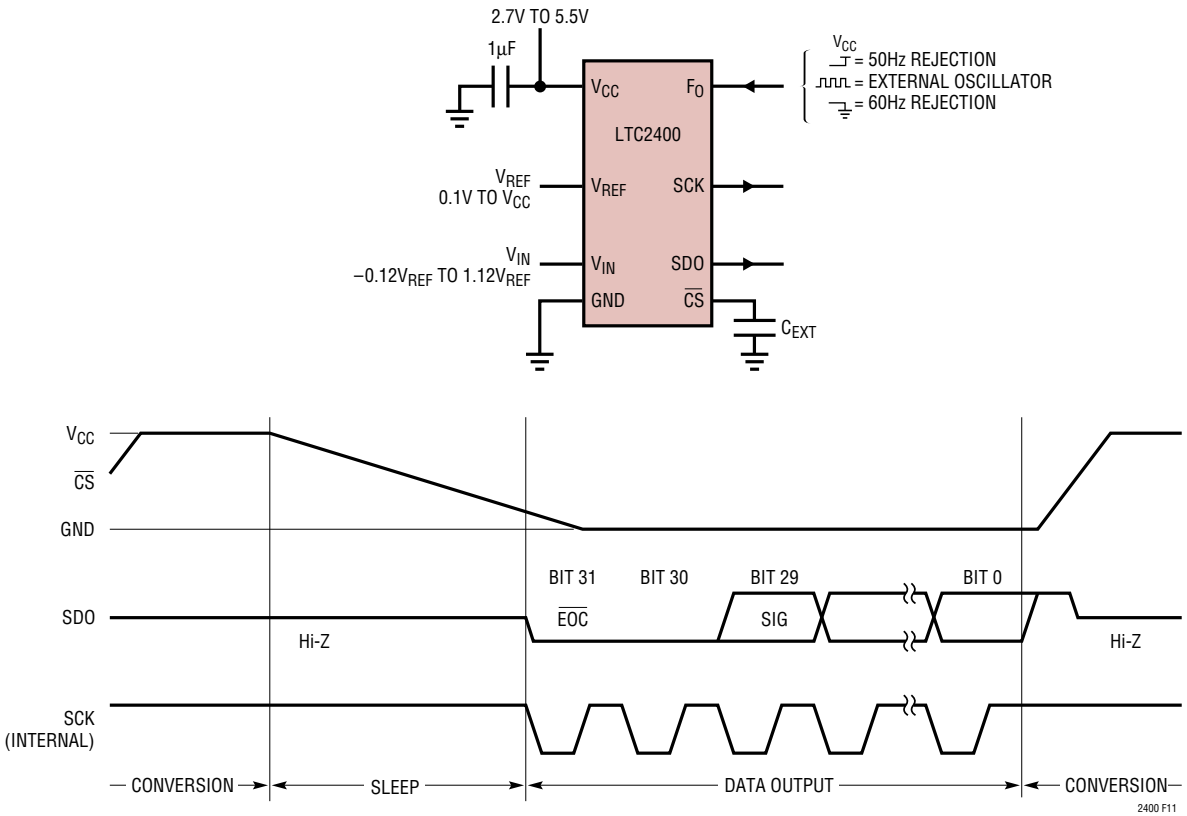

Figure 11. Internal Serial Clock, Autostart Operation

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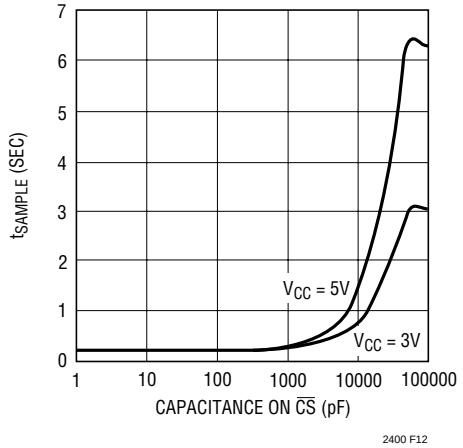

Figure 12. $\overline{CS}$ Capacitance vs t_{SAMPLE}

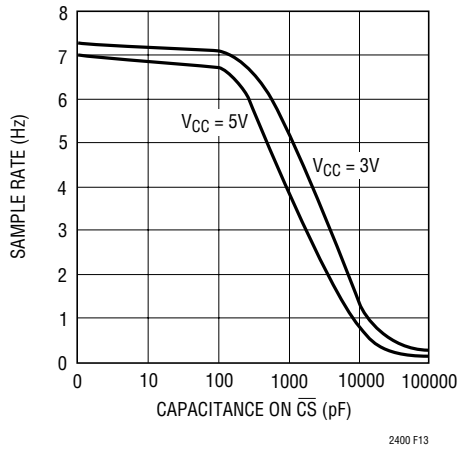

Figure 13. $\overline{CS}$ Capacitance vs Output Rate

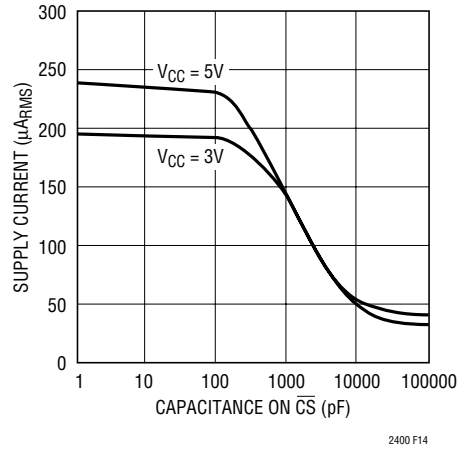

Figure 14. $\overline{CS}$ Capacitance vs Supply Current

pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the conversion result into external circuitry. After the 32nd rising edge, $\overline{CS}$ is pulled HIGH and a new conversion is immediately started. This is useful in applications requiring periodic monitoring and ultralow power. Figure 14 shows the average supply current as a function of capacitance on $\overline{CS}$.

It should be noticed that the external capacitor discharge current is kept very small in order to decrease the converter power dissipation in the sleep state. In the autostart mode the analog voltage on the $\overline{CS}$ pin cannot be observed without disturbing the converter operation using a regular oscilloscope probe. When using this configuration, it is important to minimize the external leakage current at the $\overline{CS}$ pin by using a low leakage external capacitor and properly cleaning the PCB surface.

The internal serial clock mode is selected every time the voltage on the $\overline{CS}$ pin crosses an internal threshold voltage. An internal weak pull-up at the SCK pin is active while $\overline{CS}$ is discharging; therefore, the internal serial clock timing mode is automatically selected if SCK is floating. It is important to ensure there are no external drivers pulling SCK LOW while $\overline{CS}$ is discharging.

DIGITAL SIGNAL LEVELS

The LTC2400's digital interface is easy to use. Its digital inputs (F_O, $\overline{CS}$ and SCK in External SCK mode of operation) accept standard TTL/CMOS logic levels and the internal hysteresis receivers can tolerate edge rates as slow as 100μs. However, some considerations are required to take advantage of exceptional accuracy and low supply current.

The digital output signals (SDO and SCK in Internal SCK mode of operation) are less of a concern because they are not generally active during the conversion state.

In order to preserve the LTC2400's accuracy, it is very important to minimize the ground path impedance which may appear in series with the input and/or reference signal and to reduce the current which may flow through this path. The GND pin should be connected to a low resistance ground plane through a minimum length trace. The use of multiple via holes is recommended to further reduce the

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connection resistance. The LTC2400's power supply current flowing through the 0.01Ω resistance of the common ground pin will develop a 2.5μV offset signal. For a reference voltage V_{REF} = 2.5V, this represents a 1ppm offset error.

In an alternative configuration, the GND pin of the converter can be the single-point-ground in a single point grounding system. The input signal ground, the reference signal ground, the digital drivers ground (usually the digital ground) and the power supply ground (the analog ground) should be connected in a star configuration with the common point located as close to the GND pin as possible.

The power supply current during the conversion state should be kept to a minimum. This is achieved by restricting the number of digital signal transitions occurring during this period.

While a digital input signal is in the range 0.5V to (V_{CC} – 0.5V), the CMOS input receiver draws additional current from the power supply. It should be noted that, when any one of the digital input signals (F_O, $\overline{CS}$ and SCK in External SCK mode of operation) is within this range, the LTC2400 power supply current may increase even if the signal in question is at a valid logic level. For micropower operation and in order to minimize the potential errors due to additional ground pin current, it is recommended to drive all digital input signals to full CMOS levels [V_{IL} < 0.4V and V_{OH} > (V_{CC} – 0.4V)].

Severe ground pin current disturbances can also occur due to the undershoot of fast digital input signals. Undershoot and overshoot can occur because of the impedance mismatch at the converter pin when the transition time of an external control signal is less than twice the propagation delay from the driver to LTC2400. For reference, on a regular FR-4 board, signal propagation velocity is approximately 183ps/inch for internal traces and 170ps/inch for surface traces. Thus, a driver generating a control signal with a minimum transition time of 1ns must be connected to the converter pin through a trace shorter than 2.5 inches. This problem becomes particularly difficult when shared control lines are used and multiple reflections may occur. The solution is to carefully terminate all transmission lines close to their characteristic impedance.

Parallel termination near the LTC2400 pin will eliminate this problem but will increase the driver power dissipation. A series resistor between 27Ω and 56Ω placed near the driver or near the LTC2400 pin will also eliminate this problem without additional power dissipation. The actual resistor value depends upon the trace impedance and connection topology.

Driving the Input and Reference

The analog input and reference of the typical delta-sigma analog-to-digital converter are applied to a switched capacitor network. This network consists of capacitors switching between the analog input (V_{IN}), ground (Pin 4) and the reference (V_{REF}). The result is small current spikes seen at both V_{IN} and V_{REF}. A simplified input equivalent circuit is shown in Figure 15.

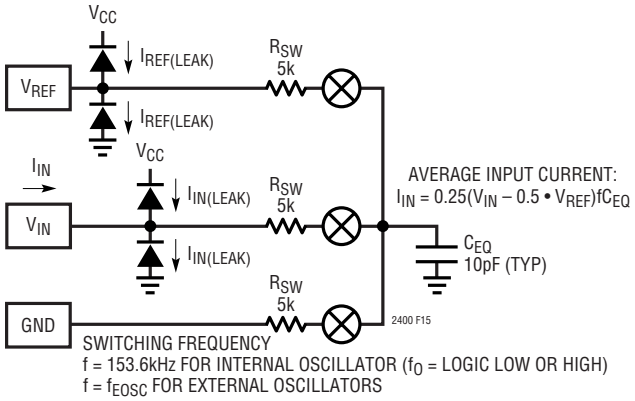

Figure 15. LTC2400 Equivalent Analog Input Circuit

The key to understanding the effects of this dynamic input current is based on a simple first order RC time constant model. Using the internal oscillator, the LTC2400's internal switched capacitor network is clocked at 153,600Hz corresponding to a 6.5μs sampling period. Fourteen time constants are required each time a capacitor is switched in order to achieve 1ppm settling accuracy.

Therefore, the equivalent time constant at V_{IN} and V_{REF} should be less than 6.5μs/14 = 460ns in order to achieve 1ppm accuracy.

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Input Current (V_{IN})

If complete settling occurs on the input, conversion results will be uneffected by the dynamic input current. If the settling is incomplete, it does not degrade the linearity performance of the device. It simply results in an offset/full-scale shift, see Figure 16. To simplify the analysis of input dynamic current, two separate cases are assumed: large capacitance at V_{IN} (C_{IN} > 0.01µF) and small capacitance at V_{IN} (C_{IN} < 0.01µF).

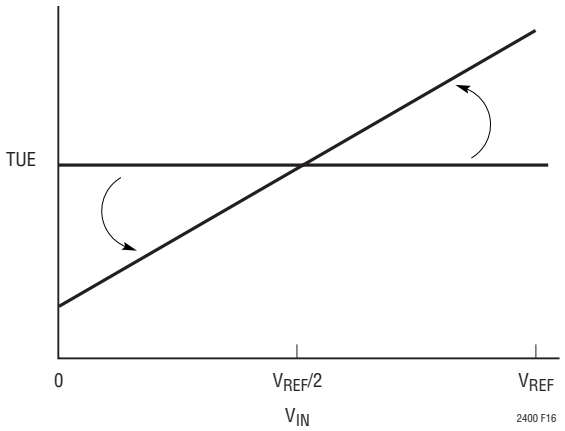

Figure 16. Offset/Full-Scale Shift

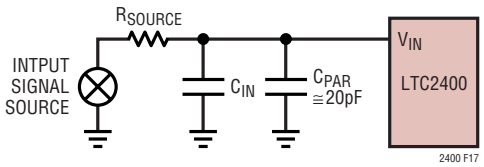

Figure 17. An RC Network at V_{IN}

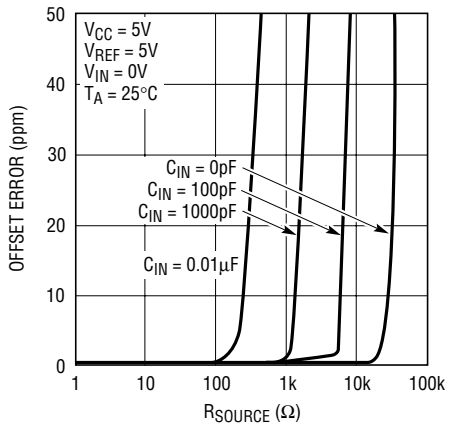

Figure 18. Offset vs R_{SOURCE} (Small C)

If the total capacitance at V_{IN} (see Figure 17) is small (<0.01µF), relatively large external source resistances (up to 20k for 20pF parasitic capacitance) can be tolerated without any offset/full-scale error. Figures 18 and 19 show a family of offset and full-scale error curves for various small valued input capacitors (C_{IN} < 0.01µF) as a function of input source resistance.

For large input capacitor values (C_{IN} > 0.01µF), the input spikes are averaged by the capacitor into a DC current. The gain shift becomes a linear function of input source resistance independent of input capacitance, see Figures 20 and 21. The equivalent input impedance is 1.66MΩ. This results in ±1.5µA of input dynamic current at the extreme values of V_{IN} (V_{IN} = 0V and V_{IN} = V_{REF}, when

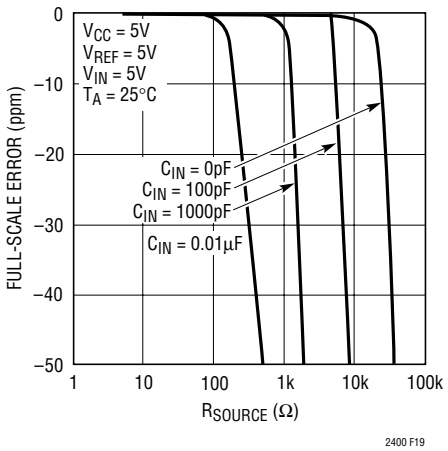

Figure 19. Full-Scale Error vs R_{SOURCE} (Small C)

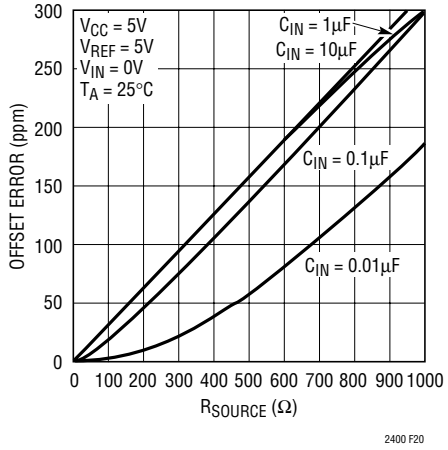

Figure 20. Offset vs R_{SOURCE} (Large C)

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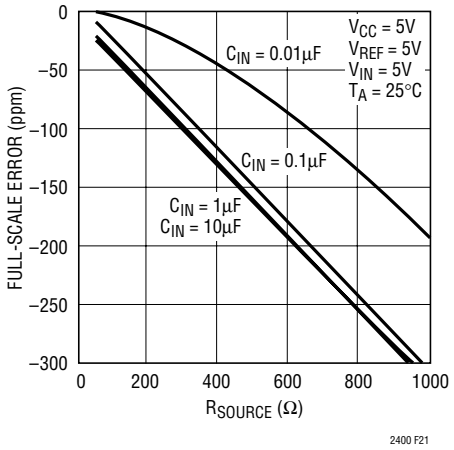

Figure 21. Full-Scale Error vs R_{SOURCE} (Large C)

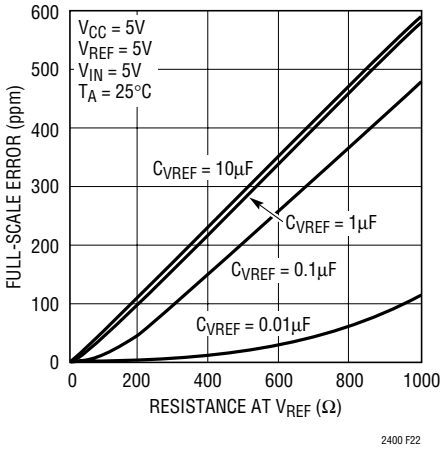

Figure 22. Full-Scale Error vs R_{VREF} (Large C)

V_{REF} = 5V). This corresponds to a 0.3ppm shift in offset and full-scale readings for every 1Ω of input source resistance.

In addition to the input current spikes, the input ESD protection diodes have a temperature dependent leakage current. This leakage current, nominally 1nA (±10nA max), results in a fixed offset shift of 10µV for a 10k source resistance.

Reference Current (V_{REF})

Similar to the analog input, the reference input has a dynamic input current. This current has negligible effect on the offset. However, the reference current at $V_{IN} = V_{REF}$ is similar to the input current at full-scale. For large values of reference capacitance (C_{VREF} > 0.01µF), the full-scale error shift is 0.3ppm/Ω of external reference resistance independent of the capacitance at V_{REF}, see Figure 22. If the capacitance tied to V_{REF} is small (C_{VREF} < 0.01µF), an input resistance of up to 20k (20pF parasitic capacitance at V_{REF}) may be tolerated, see Figure 23.

Unlike the analog input, the integral nonlinearity of the device can be degraded with excessive external RC time constants tied to the reference input. If the capacitance at node V_{REF} is small (C_{VREF} < 0.01µF), the reference input can tolerate large external resistances without reduction in INL, see Figure 24. If the external capacitance is large (C_{VREF} > 0.01µF), the linearity will be degraded by 0.15ppm/Ω independent of capacitance at V_{REF}, see Figure 25.

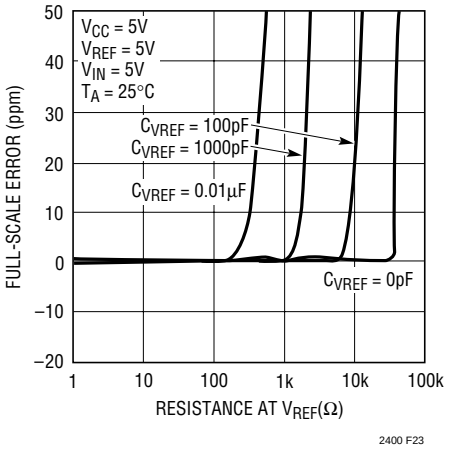

Figure 23. Full-Scale Error vs R_{VREF} (Small C)

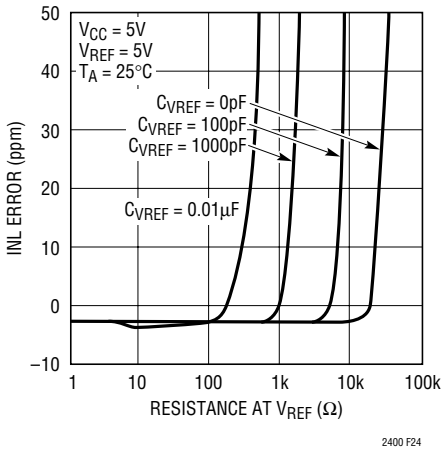

Figure 24. INL Error vs R_{VREF} (Small C)

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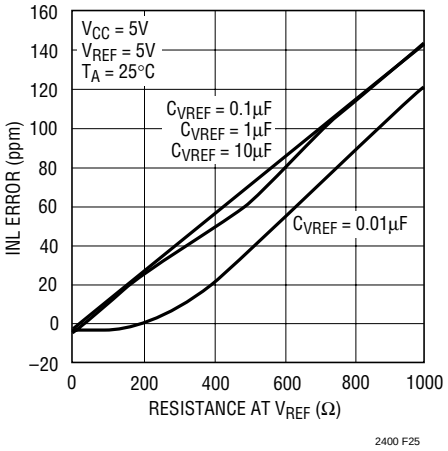


Figure 25. INL Error vs R_{VREF} (Large C)

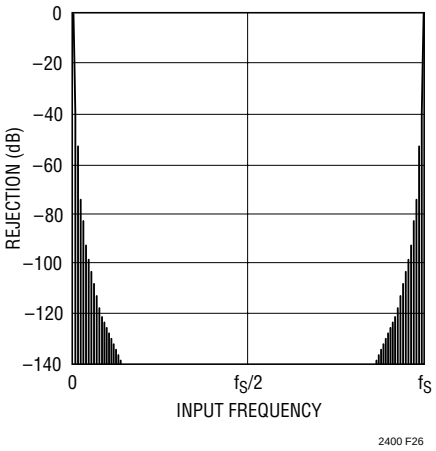


Figure 26. Sinc^4 Filter Rejection

In addition to the dynamic reference current, the V_{REF} ESD protection diodes have a temperature dependent leakage current. This leakage current, nominally 1nA (±10nA max), results in a fixed full-scale shift of 10µV for a 10k source resistance.

ANTIALIASING

One of the advantages delta-sigma ADCs offer over conventional ADCs is on-chip digital filtering. Combined with a large oversampling ratio, the LTC2400 significantly simplifies antialiasing filter requirements.

The digital filter provides very high rejection except at integer multiples of the modulator sampling frequency (f_S), see Figure 26. The modulator sampling frequency is 256 • F_O, where F_O is the notch frequency (typically 50Hz or 60Hz). The bandwidth of signals not rejected by the digital filter is narrow (≈0.2%) compared to the bandwidth of the frequencies rejected.

As a result of the oversampling ratio (256) and the digital filter, minimal (if any) antialias filtering is required in front of the LTC2400. If passive RC components are placed in front of the LTC2400 the input dynamic current should be considered (see Input Current section). In cases where large effective RC time constants are used, an external buffer amplifier may be required to minimize the effects of input dynamic current.

The modulator contained within the LTC2400 can handle large-signal level perturbations without saturating. Signal levels up to 40% of V_{REF} do not saturate the analog modulator. These signals are limited by the input ESD protection to 300mV below ground and 300mV above V_{CC}.

TYPICAL APPLICATIONS

SYNCHRONIZATION OF MULTIPLE LTC2400s

Since the LTC2400's absolute accuracy (total unadjusted error) is 10ppm, applications utilizing multiple matched ADCs are possible.

Simultaneous Sampling with Two LTC2400s

One such application is synchronizing multiple LTC2400s, see Figure 27. The start of conversion is synchronized to the rising edge of $\overline{CS}$. In order to synchronize multiple LTC2400s, $\overline{CS}$ is a common input to all the ADCs. To prevent the converters from autostarting a new conversion at the end of data output read, 31 or fewer SCK clock signals are applied to the LTC2400 instead of 32 (the 32nd falling edge would start a conversion). The exact timing and frequency for the SCK signal is not critical since it is only shifting out the data. In this case, two LTC2400's simultaneously start and end their conversion cycles under the external control of $\overline{CS}$.

Increasing the Output Rate Using Multiple LTC2400s

A second application uses multiple LTC2400s to increase the effective output rate by 4×, see Figure 28. In this case, four LTC2400s are interleaved under the control of separate $\overline{CS}$ signals. This increases the effective output rate from 7.5Hz to 30Hz (up to a maximum of 60Hz). Additionally, the one-shot output spectrum is unfolded allowing further digital signal processing of the conversion results. SCK and SDO may be common to all four LTC2400s. The four $\overline{CS}$ rising edges equally divide one LTC2400 conversion cycle (7.5Hz for 60Hz notch frequency). In order to synchronize the start of conversion to $\overline{CS}$, 31 or less SCK clock pulses must be applied to each ADC.

Both the synchronous and 4× output rate applications use the external serial clock and single cycle operation with reduced data output length (see Serial Interface Timing Modes section and Figure 6). An external oscillator clock is applied commonly to the F_O pin of each LTC2400 in order to synchronize the sampling times. Both circuits may be extended to include more LTC2400s.

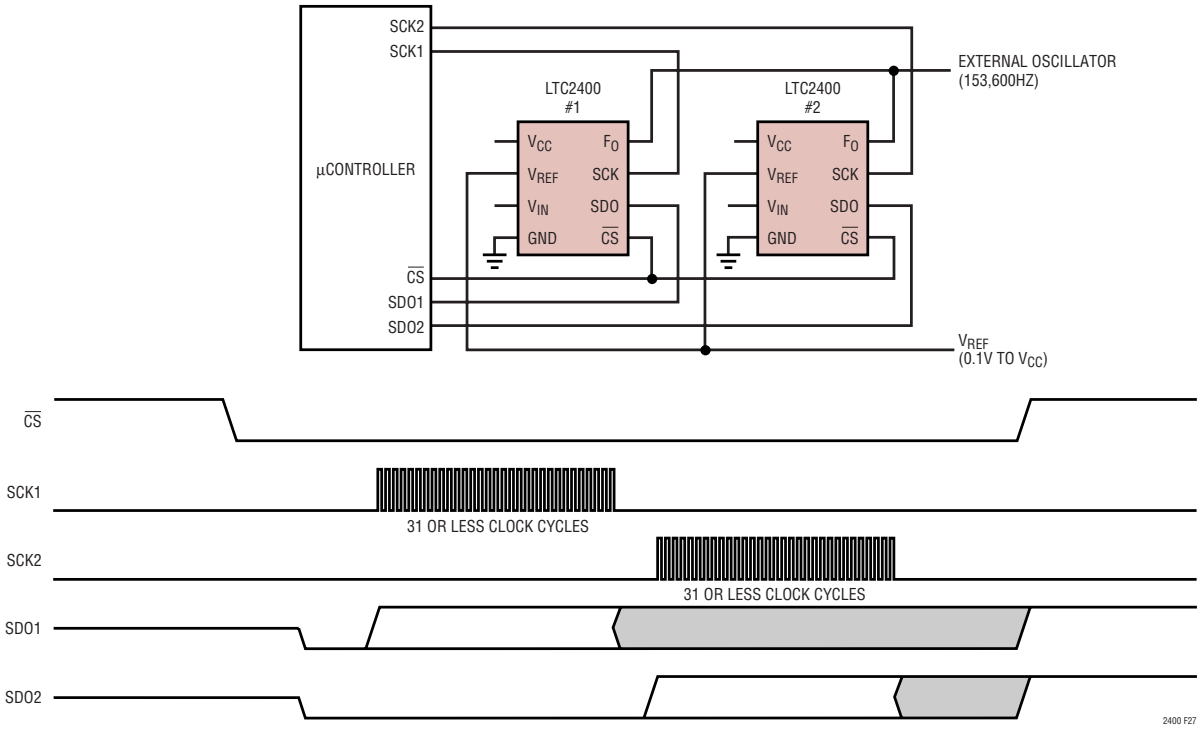


Figure 27. Synchronous Conversion—Extendable

TYPICAL APPLICATIONS

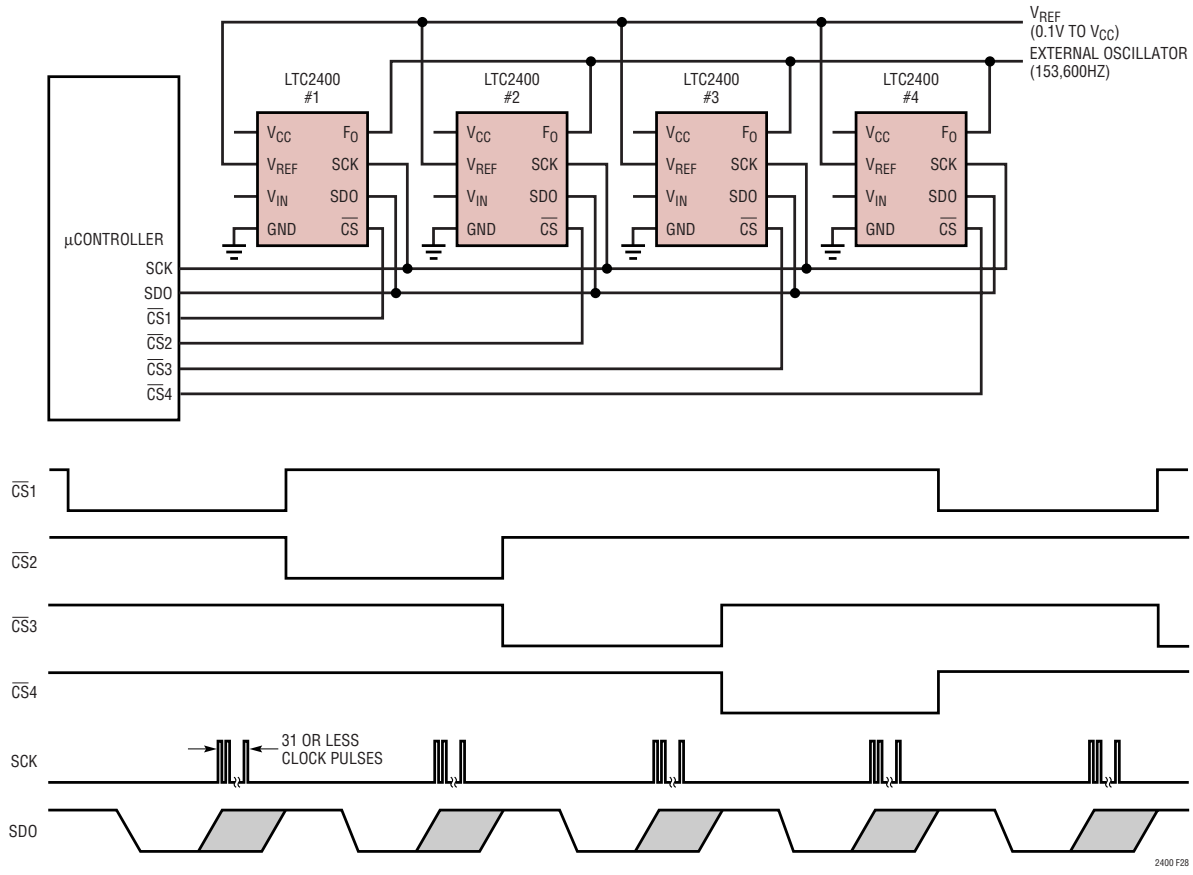


Figure 28. 4× Output Rate LTC2400 System

Differential to Single-Ended Analog Conditioning

The circuits in Figures 29 and 30 use the LTC1043 dual precision, switched capacitor building block. Each circuit uses one-half of an LTC1043 to perform a differential to single-ended conversion over an input common mode range that includes the power supplies. The LTC1043 samples a differential input voltage, holds it on C_S and transfers it to a ground-referenced capacitor C_H. The voltage on C_H is applied to the LTC2400's input and converted to a digital value.

The LTC1043 achieves its best differential to single-ended conversion when its internal switching frequency operates at a nominal 300Hz, as set by the 0.01µF capacitor C1, and when 1µF capacitors are used for C_S and C_H. C_S and C_H should be a film-type capacitor such as mylar or polypropylene.

Simple Differential Front-End for the LTC2400

The circuit in Figure 29 is ideal for wide dynamic range differential signals in applications where absolute accuracy is secondary to high resolution, have large signal swings, source impedances under 500Ω and use a 5V or ±5V supply.

The circuit achieves a nonlinearity of ±35ppm (a linearity accuracy of 14.5 bits), noise of 1.5µV_{RMS} and 21-bit resolution. The circuit exhibits a typical 2.75mV zero offset. However, this is not an offset that simply shifts the output code by a constant value. It is a gain error that alters the transfer function's slope. The gain error revolves around midscale (V_{REF}/2). This gain error can be corrected in software by measuring the error at 0V input and using the result to create a correction factor.

TYPICAL APPLICATIONS

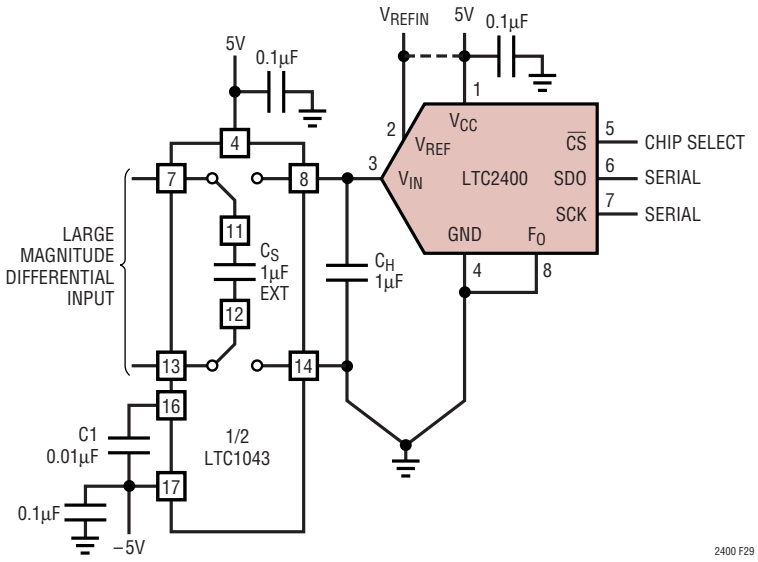


Figure 29. Simple Rail-to-Rail Circuit Converts Differential Signals to Single-Ended Signals

LTC2400 High Accuracy Differential to Single-Ended Converter for ±5V Supplies

The circuit in Figure 30 is ideal for low level differential signals in applications that have a ±5V supply and need high accuracy without calibration. The circuit combines an LTC1043 and LTC1050 as a differential to single-ended amplifier that has an input common mode range that includes the power supplies. Resistors R1 and R2 set the LTC1050's gain at 101.

The circuit schematic shows an optional resistor R_S. This resistor can be placed in series with the LTC2400's input to limit current if the input goes below –300mV. The resistor does not degrade the converter's performance as long as any capacitance, stray or otherwise, connected between the LTC2400's input and ground is less than 100pF. Higher capacitance will increase offset and full-scale errors (see Input Current section).

The circuit achieves a nonlinearity of ±1ppm, input referred noise of $0.05\mu V_{RMS}$ (averaging 64 samples), 19.6 bits resolution for a full-scale input of 40mV, and an overall accuracy of 20 bits when using an LTC1236-5 precision 5V reference.

Multiple Inputs

The simple circuit shown in Figure 31 takes advantage of the LTC2400's single conversion settling. The LTC1391 serially programmed multiplexer allows accurate conversions on each of its eight channels without introducing any offset, gain or linearity errors with its input signal between 0V and V_{REF}, as long as the total capacitance connected to the LTC2400's input is less than 1000pF. A small 2ppm (typ) error occurs when an active input channel's signal voltage reaches –300mV (typ). If the excursion below ground is above –200mV (typ), the error is less than the LTC2400's $0.3ppm_{RMS}$ noise. On the topside, the selected input signal's magnitude can go above the 5V supply with no linearity degradation or increased noise. Figure 31's circuit can tolerate overdrive on the unselected channel without conversion degradation as long as the overdrive is less than 250mV above the supply voltage or 250mV below ground. The linearity performance is similar to that shown in the Typical Performance Characteristics section.

Errors caused by channel-to-channel crosstalk are less than the LTC2400's typical input noise. This remains the case for a frequency range of 1Hz to 153.6kHz (the LTC2400's internal clock frequency or $10f_S$). When the frequency reaches 1.536MHz ($4V_{P-P}$), the RMS noise typically doubles and the linearity is degraded by 30ppm (typ).

TYPICAL APPLICATIONS

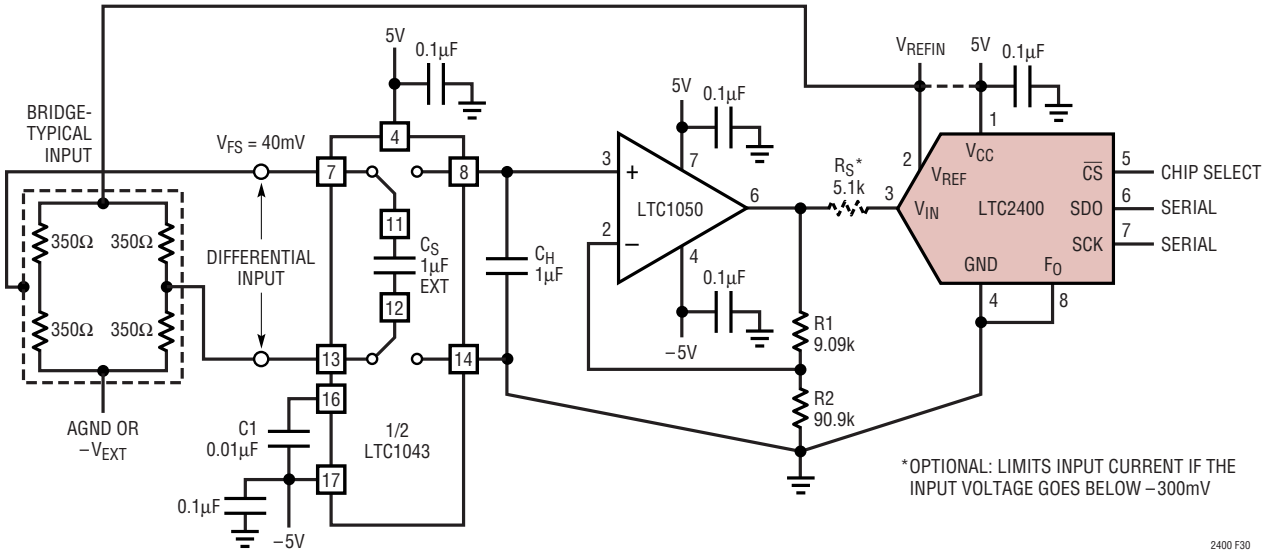


Figure 30. Differential to Single-Ended Converter for Low Level Inputs, Such as Bridges, Maintains the LTC2400's High Accuracy

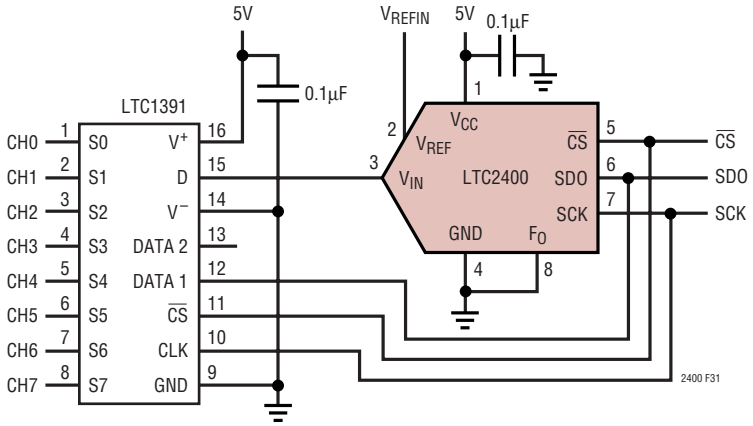


Figure 31. Multiplex 8-Signal Sources with the LTC1391 and Maintain the LTC2400's Conversion Accuracy

TYPICAL APPLICATIONS

Sample Driver for LTC2400 SPI Interface

The LTC2400 has a very simple serial interface that makes interfacing to microprocessors and microcontrollers very easy. Shown in Figures 32 and 34 are listings of sample source codes that can be used to initiate conversions and retrieve data from the LTC2400.

The listing in Figure 32 was created by Parallax, Inc. (916-624-8333), for the BASIC Stamp. This code uses individual port lines to control the LTC2400's conversion and retrieve the 32-bit result. A fourth port line is used to power the LTC2400, a vivid example of the converter's micropower operation. The program's main sequence activates the LTC2400's serial interface, uses a loop to retrieve the 32 conversion bits, and then places the converter's interface in a high impedance state and starting the next conversion. All bits are retained in variables ADlo and ADhi. The code can be found on their web site, www.parallaxinc.com.

```
'LTC2400        Sample Driver
'03/17/99       This program is an example showing how to access the
'               LTC2400 using the Basic Stamp2 from Parallax. Since
'               the BS2 is based on a 16-bit architecture, only the
'               upper 16 bits of the 24-bit result are displayed,
'               although all 24 bits are retrieved.

ADlo    var     word            'A/D result - lower 16 bits
ADhi    var     word            'A/D result - upper 8 bits
Ctr     var     byte            'loop counter
Temp    var     bit             'temporary bit used for shift

SDO     con     0               'Serial data connected to P0
SCK     con     1               'Serial clock connected to P1
CS      con     2               'Chip Select connected to P2
Pwr     con     3               'Stamp supplies power connected to P3
                                '(Uses only 0.3mA!)
Init
        dira = $E               'Set up data direction
                                'Pwr, CS, and SCK are outputs
                                'SDO is an input
        outa = $0               'Initialize outputs
                                'Pwr, CS, and SCK are low
        pause 100               'Wait 100mS for I/O to settle
        high Pwr                'Power up the LTC2400
        pause 1                 'Wait 1mS for power-on sequence
        high CS                 'Disable the device until we
Start                           'wish to read it.
        pause 125               'Eight times second
        low CS                  'Enable the LTC2400
        for Ctr = 0 to 31
        high SCK                'Cycle clock 32 times
        gosub ShiftL
```

TYPICAL APPLICATIONS

```
        ADlo.bit0 = in0                 'and sample data line
        low SCK
        next
        high CS                         'Disable the LTC2400
        ADhi = (ADhi<<4)+((ADlo&$F000)>>12)
        debug ?ADhi                     'Discard the lower eight bits
        goto Start                      'and display (debug command).
ShiftL
        Temp = ADlo.bit15               'This routine simply
        ADlo = ADlo<<1                  'performs a 1 bit
        ADhi = ADhi<<1                  'left shift on two
        ADhi.bit0 = Temp                '16 bit variables
        return
```

Figure 32. This BASIC Stamp Code is an Example of How Easy it is to Retrieve Data from the LTC2400

The listing in Figure 34 is a simple assembler routine for the 68HC11 microcontroller. It uses PORT D, configuring it for SPI data transfer between the controller and the LTC2400. Figure 33 shows the simple 3-wire SPI connection.

The code begins by declaring variables and allocating four memory locations to store the 32-bit conversion result. This is followed by initializing PORT D's SPI configuration. The program then enters the main sequence. It activates the LTC2400's serial interface by setting the $\overline{SS}$ output low, sending a logic low to $\overline{CS}$. It next waits in a loop for a logic low on the data line, signifying end-of-conversion. After the loop is satisfied, four SPI transfers are completed, retrieving the conversion. The main sequence ends by setting $\overline{SS}$ high. This places the LTC2400's serial interface in a high impedance state and initiates another conversion.

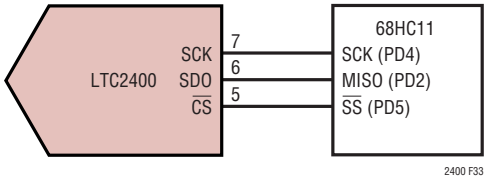


Figure 33. Connecting the LTC2400 to a 68HC11 MCU Using the SPI Serial Interface

```
**************************************************
* This example program transfers the LTC2400's 32-bit output    *
* conversion result into four consecutive 8-bit memory locations. *
**************************************************
*68HC11 register definition
PORTD   EQU     $1008   Port D data register
*                       " – , – , SS* ,CSK ;MOSI,MISO,TxD ,RxD"
DDRD    EQU     $1009   Port D data direction register
SPSR    EQU     $1028   SPI control register
*                       "SPIE,SPE ,DWOM,MSTR;SPOL,CPHA,SPR1,SPR0"
SPSR    EQU     $1029   SPI status register
*                       "SPIF,WCOL, – ,MODF; – , – , – , – "
SPDR    EQU     $102A   SPI data register; Read-Buffer; Write-Shifter
*
* RAM variables to hold the LTC2400's 32 conversion result
```

TYPICAL APPLICATIONS

```
*
DIN1    EQU     $00     This memory location holds the LTC2400's bits 31 - 24
DIN2    EQU     $01     This memory location holds the LTC2400's bits 23 - 16
DIN3    EQU     $02     This memory location holds the LTC2400's bits 15 - 08
DIN4    EQU     $03     This memory location holds the LTC2400's bits 07 - 00
*
**********************
* Start GETDATA Routine *
**********************
*
        ORG     $C000   Program start location
INIT1   LDS     #$CFFF  Top of C page RAM, beginning location of stack
        LDAA    #$2F    –,–,1,0;1,1,1,1
*                       –, –, SS*-Hi, SCK-Lo, MOSI-Hi, MISO-Hi, X, X
        STAA    PORTD   Keeps SS* a logic high when DDRD, bit 5 is set
        LDAA    #$38    –,–,1,1;1,0,0,0
        STAA    DDRD    SS*, SCK, MOSI are configured as Outputs
*                       MISO, TxD, RxD are configured as Inputs
*DDRD's bit 5 is a 1 so that port D's SS* pin is a general output
        LDAA    #$50
        STAA    SPCR    The SPI is configured as Master, CPHA = 0, CPOL = 0
*                       and the clock rate is E/2
*                       (This assumes an E-Clock frequency of 4MHz. For higher E-
*                       Clock frequencies, change the above value of $50 to a value
*                       that ensures the SCK frequency is 2MHz or less.)
GETDATA PSHX
        PSHY
        PSHA
        LDX     #$0     The X register is used as a pointer to the memory locations
*                       that hold the conversion data
        LDY     #$1000
        BCLR    PORTD, Y %00100000      This sets the SS* output bit to a logic
*                                       low, selecting the LTC2400
TRFLP1  LDAA    #$0     Load accumulator A with a null byte for SPI transfer
        STAA    SPDR    This writes the byte in the SPI data register and starts
*                       the transfer
WAIT1   LDAA    SPSR    This loop waits for the SPI to complete a serial
                        transfer/exchange by reading the SPI Status Register
        BPL     WAIT1   The SPIF (SPI transfer complete flag) bit is the SPSR's MSB
*                       and is set to one at the end of an SPI transfer. The branch
*                       will occur while SPIF is a zero.
        LDAA    SPDR    Load accumulator A with the current byte of LTC2400 data
                        that was just received
        STAA    0,X     Transfer the LTC2400's data to memory
        INX             Increment the pointer
        CPX     #DIN4+1 Has the last byte been transferred/exchanged?
        BNE     TRFLP1  If the last byte has not been reached, then proceed to the
*                       next byte for transfer/exchange
        BSET    PORTD,Y %00100000 This sets the SS* output bit to a logic high,
*                       de-selecting the LTC2400
        PULA            Restore the A register
        PULY            Restore the Y register
        PULX            Restore the X register
        RTS
```

Figure 34. This is an Example of 68HC11 Code That Captures the LTC2400's Conversion Results Over the SPI Serial Interface Shown in Figure 33

TYPICAL APPLICATIONS

Thermocouple Applications

Figure 35 shows a thermocouple interface circuit that demonstrates the practicality of direct connection to the LTC2400 using even the lowest output thermocouples (in this case, a type S thermocouple, with a full-scale output of 18mV).

This topology is the least costly solution for thermocouple sensing. As shown, it is capable of resolving approximately 0.25°C without averaging. Since the LTC2400 does not exhibit any easily discernible quantization effects, averaging can significantly extend the resolution for slow changing processes.

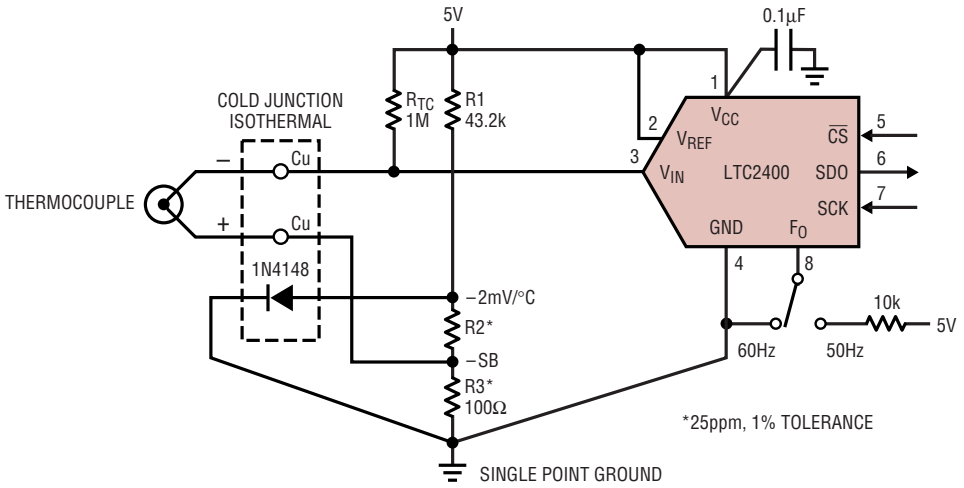
In this circuit, a 1N4148 diode provides cold junction compensation by producing, at the positive terminal of the thermocouple, an approximation of the average Seebeck coefficient for a type S thermocouple over the temperature range expected at the cold junction (0°C to 40°C). If the operating range is less, the coefficient can be adjusted to produce a better match for the range anticipated. This basic circuit can be used with other thermocouples by changing the divide ratio to suit the Seebeck coefficient of the type chosen (see table).

This circuit produces a DC offset at the cold junction reference point, of 1mV to 15mV, which must be nulled out in software. This DC offset, resulting from the forward voltage of the diode, is variable from device to device and must be calibrated for each unit.

Since the temperature coefficient of the 1N4148 diode is not guaranteed, a trim should be provided to accommodate a coefficient from 1.7mV/°C to 2.3mV/°C. Alternatively, a transistor can be used as a sensor with Omega Engineering thermocouple circuit board connectors that are available with TO-92 transistor retainer clips, placing the transistor in physical contact with the cold junction.

The 1M resistor R_{TC} shown is intended as an open-circuit detection scheme, producing full scale at the input of the LTC2400. Note that this resistor contributes to the offset and must have low TC, as should the resistors R2 and R3. Since R1 provides forward bias for the diode, its temperature coefficient is not as critical.

The circuit in Figure 35 uses only 12% of the LTC2400's input range and is able to accommodate the full-scale output of all thermocouple types. The commonly used



THERMOCOUPLE TYPE	SEEBECK COEFFICIENT*	R2
J	50.2µV/°C	3.83k
K	39.2µV/°C	4.99k
S	6.15µV/°C	32.4k

2400 F35

*20°C ≤ T_A ≤ 50°C

Figure 35. Diode Cold Junction Compensation

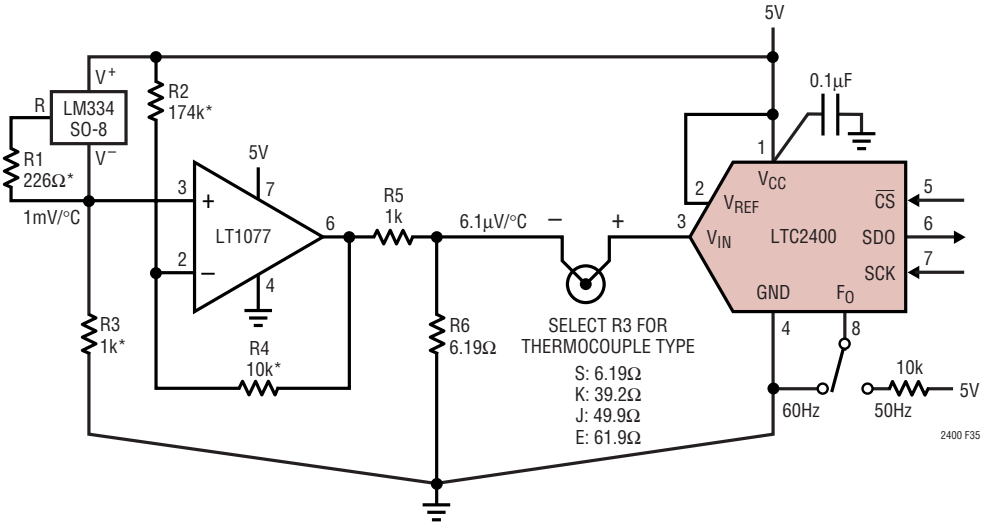
TYPICAL APPLICATIONS

thermocouple with the highest output is type E, at about 70mV. This circuit does not provide curvature correction for the Seebeck effect at the cold junction. If the application requires very high accuracy, the temperature of the cold junction should be determined via a separate input to the A/D, using an RTD for example. The cold junction compensation can be performed by implementing the thermocouple's NBS polynominal curvature correction in software. (The input to the LTC2400 can be multiplexed using the LTC1391 with little degradation.) If a separate temperature sensor is used to monitor the cold junction, the connection from the thermocouple to the LTC2400 can be direct. The junctions formed at the point where the thermocouple leads meet different metal (e.g., copper traces) must be equal in temperature, and the cold junction sensor must be mounted at that point. Any temperature differential between the leads, or any differential between the leads and the temperature sensor will introduce an error into the reading.

Figure 36 shows an inexpensive circuit with removal of the DC offset. The output of the LT®1077 is attenuated in order to produce the required coefficient, as well as reduce the noise and offset error contribution. If used with a thermistor, this circuit can be modified to produce curvature correction. The removal of the offset associated with diode forward voltage, or the 273°K overhead on some monolithic temperature sensors, simplifies the use of substantial gain after the thermocouple. Chopper amplifiers such as the LTC1050 can extend the noise floor of the LTC2400 by as much as a factor of 10 to 20. The use of a gain of 20 in front of the LTC2400 can extend the resolution of a thermocouple application to 0.02°C or better.

If absolute accuracy is not important, the use of a low noise bipolar amplifier, such as the LT1028, can extend the resolution an additional order of magnitude.

Note that achieving high accuracy in the circuit in Figure 36 requires a calibration sequence for circuit offset and gain correction.



*RECOMMENDED 0.1%, ±5ppm IRC AFD SERIES CHIP RESISTORS

Figure 36. Inexpensive Amplifier Improves Cold Junction Compensation

TYPICAL APPLICATIONS

A simpler, and potentially less expensive solution is the use of the LT1025 as shown in Figure 37.

The LT1025 incorporates the functions of temperature sensor, a precision divider chain required to produce the appropriate correction for five different types of thermocouples, as well as curvature correction. The LT1025 must be located at the cold junction. The use of a thermal mass around the cold junction, as well as protection from air currents, is advisable.

Simple Platinum RTD Interface

If high temperature resolution is required over a more limited range, Figure 38 can resolve approximately 0.01°C without additional amplification. The resistance of a platinum RTD changes by approximately 0.31Ω/°C at T_A = 25°C. The 100Ω to 300Ω source impedance of this circuit does not compromise the stability, accuracy or noise level of the LTC2400.

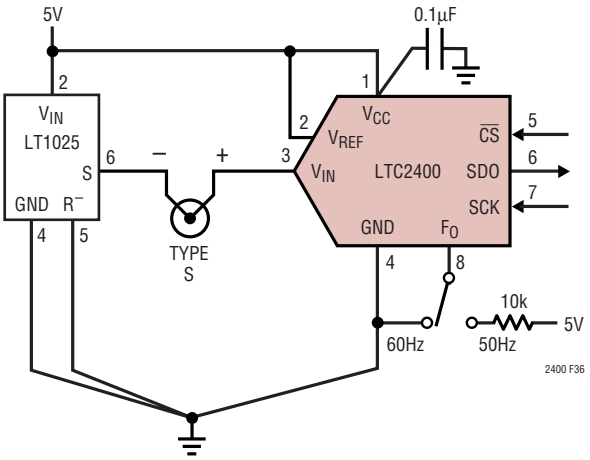


Figure 37. The LT1025 Complete Cold Junction Solution

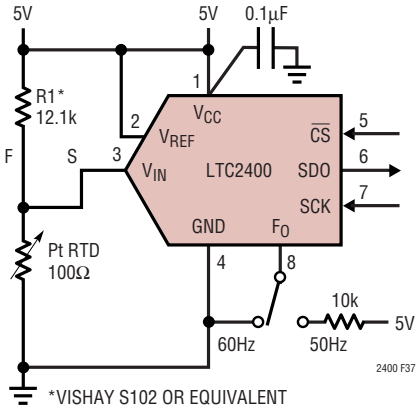


Figure 38. Simplest Platinum RTD Interface

TYPICAL APPLICATIONS

The 12.1k resistor should be a precision resistor such as a Vishay S102 series, or must be temperature stabilized. The excitation current is low enough for most sensors that the self-heating effect is near the noise floor of the LTC2400.

The use of a bipolar amplifier configuration shown in Figure 39 offers a potential resolution of 0.001°C

In order to achieve these results, the following effects must be considered. Variation in the self-heating of the RTD element due to air currents is the most difficult challenge. If the RTD is mounted in a sealed glass enclosure and painted black, the LTC2400 can detect the arrival of a person in the room. This is also true of infrared thermocouple sensors (thermopiles) that can also be used directly with the LTC2400. A variation of this circuit with two RTDs can detect small differential temperatures in order to determine heat inflow or outflow from a process. In order for this circuit to be practical, the ambient temperature of the amplifier and resistors must be controlled or the resistors must exhibit very low temperature coefficients. Precision resistor networks are always a good alternative and are available from Vishay or Caddock.

Half-Bridge Strain Gauge

The circuit in Figure 40 is a ratiometric half-bridge circuit with direct connection to the LTC2400. The use of two thin-film strain gauges in a half-bridge configuration can produce 2mV/V output and approximately 12-bit resolution. The 175Ω source impedance seen by the LTC2400 does not compromise operation.

The optional resistor shown can be up to 5k and will provide surge and transient protection for the LTC2400 if the strain gauges are located some distance from the LTC2400, or if the strain bearing member is not well grounded and may be subject to ESD discharge. Thin-film strain elements form coupling capacitance to the strain bearing member to which they are bonded. If noise

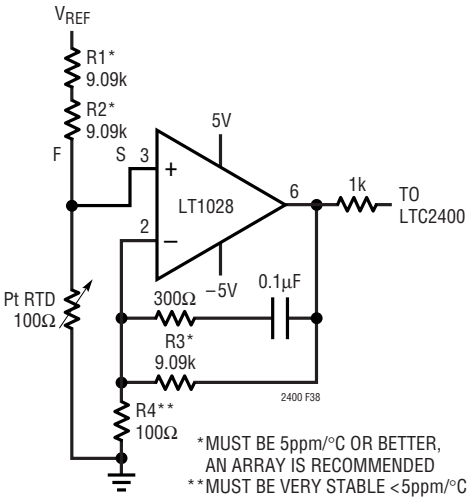


Figure 39. Extremely High Resolution RTD Interface

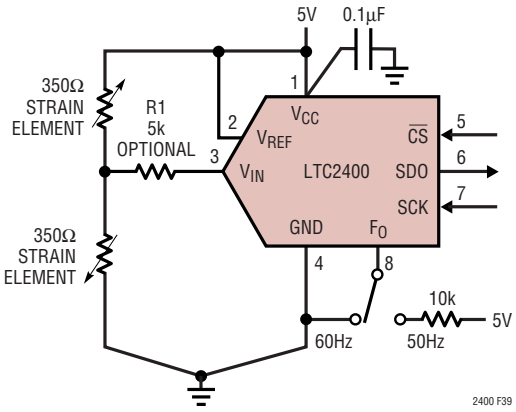


Figure 40. Half-Bridge Connection for Strain Gauges

TYPICAL APPLICATIONS

pick-up from the strain bearing member is largely 60Hz, the LTC2400 will reject it. If serious high frequency noise is present on the strain bearing member, it may be necessary to add buffering in order to allow the use of noise suppression.

Stable Relaxation Oscillator for External Clock

Applications that require that the notch produced by the LTC2400's sinc^4 filter be placed at some frequency other than 50Hz or 60Hz require an external clock. The frequency required is 2560× the required notch frequency. Simple relaxation oscillators built from logic gates with hysteresis such as the 74HC14 are not stable with temperature, supply voltage changes, or from device to device.

If for example, a remote weigh scale application requires rejection of a resonance at 11Hz, the frequency must be set to 28.16kHz. In many instances, these frequencies could be produced digitally with a phase lock loop or with digital dividers, but they are too low to be produced directly by a quartz oscillator. Quartz stability is generally not required, as the notches are wide enough that an oscillator with 0.1% to 1% stability is adequate.

In instances where digital generation of these frequencies is not practical due to power, space or cost limitations, and notches in the range of 4Hz to 120Hz are required, the circuit in Figure 41 can be used.

The frequency can be varied over this range by changing capacitor C1 over the range of 4000pf to 30pF. For the resistor values shown, the output frequency in kHz is approximately 9.5e-6 divided by C1 (C1 in pF). The circuit produces a controlled amount of hysteresis dependent only on resistor matching and self biases itself around the input threshold. All gates must be in the same package, and no loads should be driven from the outputs driving feedback paths. If there are spare gates, they can be used in parallel with gates B and D for improved drive of feedback paths.

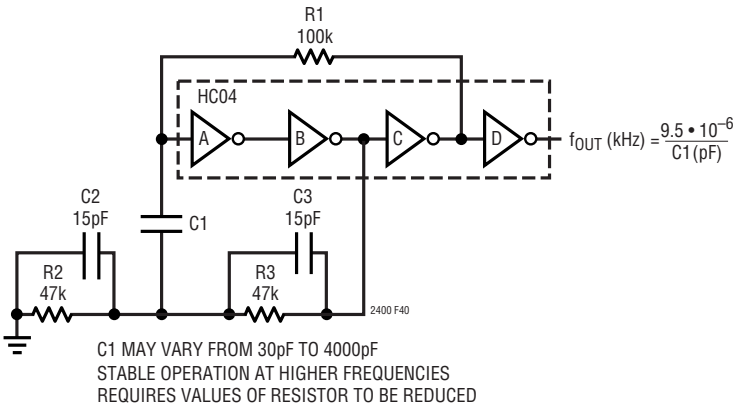


Figure 41. Stable Relaxation Low Power Oscillator for Notch Tuning

TYPICAL APPLICATIONS

The performance of the LTC2400 can be verified using the demonstration board DC228, see Figure 42 for the schematic. This circuit uses the computer's serial port to generate power and the SPI digital signals necessary for starting a conversion and reading the result. It includes a Labview application software program (see Figure 43) which graphically captures the conversion results. It can be used to determine noise performance, stability, and with an external source, linearity. As exemplified in the schematic, the LTC2400 is extremely easy to use. This demonstration board and associated software is available by contacting Linear Technology.

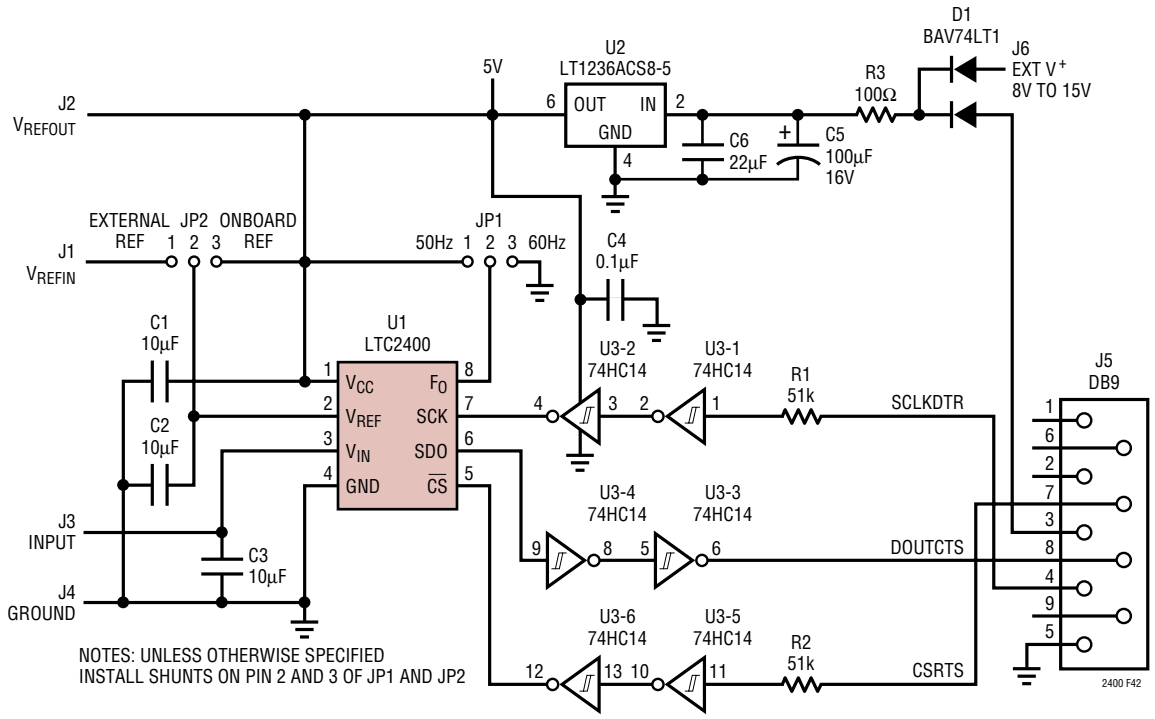


Figure 42. 24-Bit A/D Demo Board Schematic

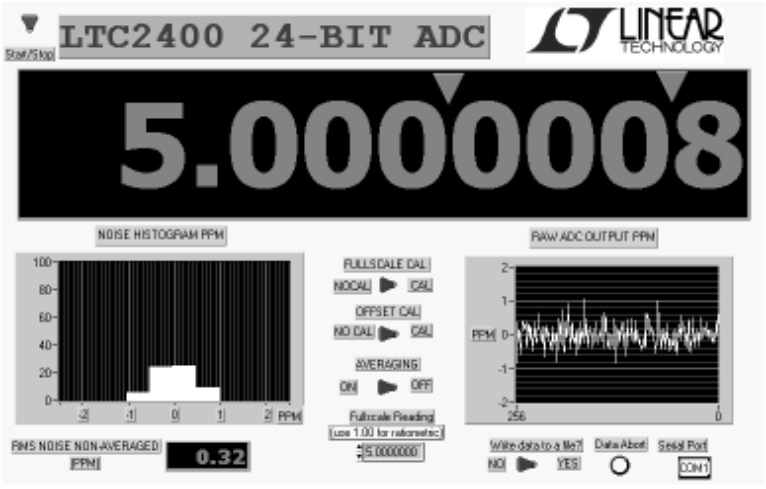
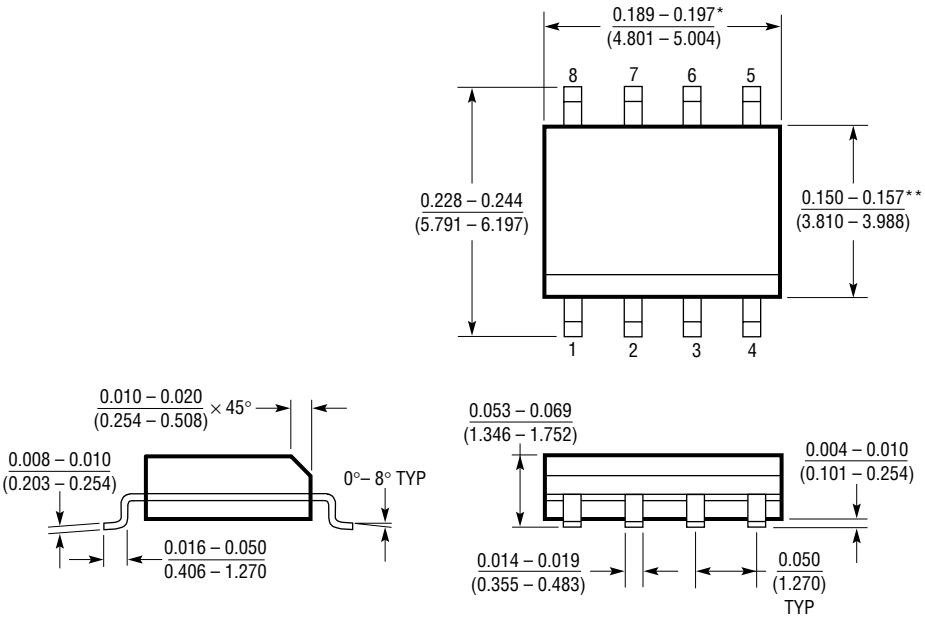


Figure 43. Display Graphic

PACKAGE INFORMATION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)

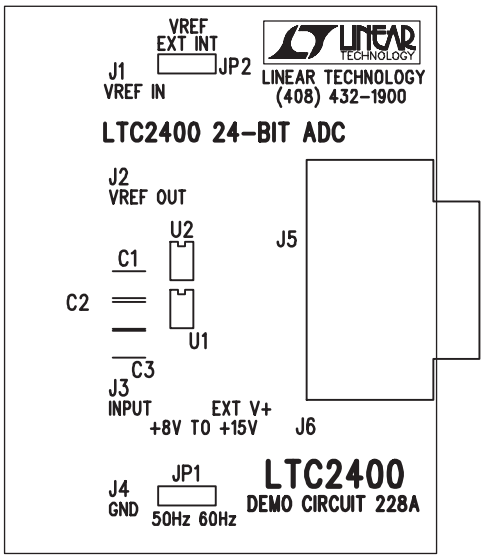


*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

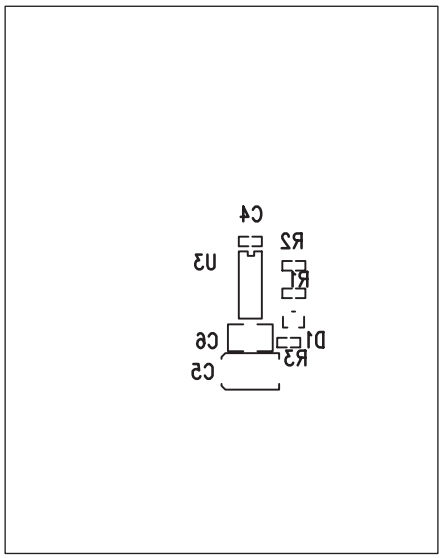
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S08 0996

PCB LAYOUT AND FILM

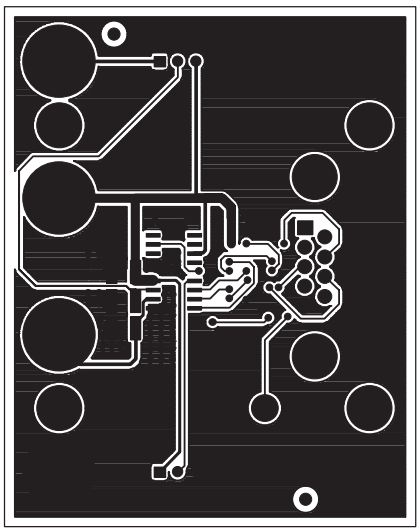


Component Side Silkscreen

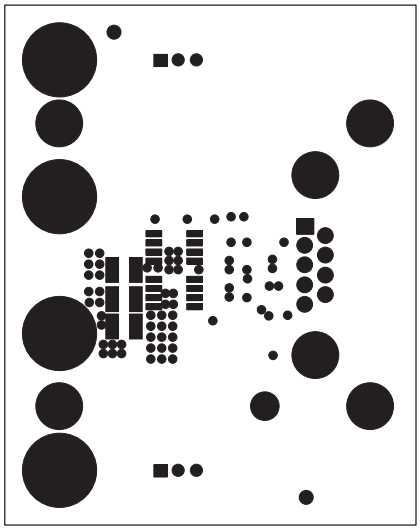


Solder Side Silkscreen

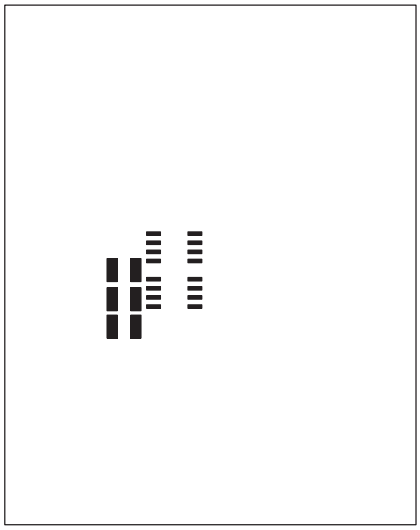
PCB LAYOUT AND FILM



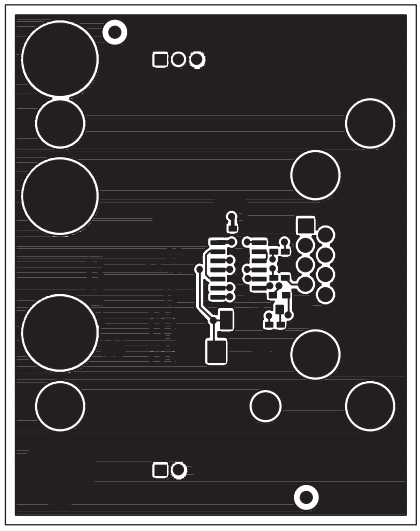
Component Side



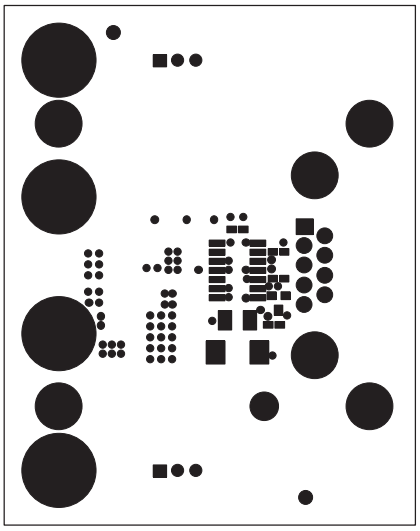
Component Side Solder Mask



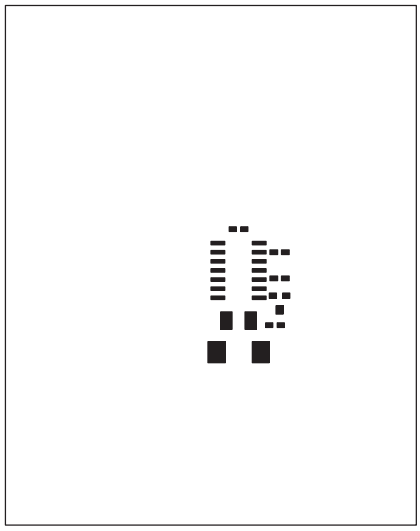
Component Side Paste Mask



Solder Side



Solder Side Solder Mask



Solder Side Paste Mask

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1019	Precision Bandgap Reference, 2.5V, 5V	3ppm/°C Drift, 0.05% Max
LT1025	Micropower Therocouple Cold Junction Compensator	
LTC1043	Dual Precision Instrumentation Switched Capacito Building Blockr	Precise Charge, Balanced Switching, Low Power
LTC1050	Precision Chopper Stabilized Op Amp	No External Components 5µV Offset, 1.6µV$_{P-P}$ Noise
LT1236A-5	Precision Bandgap Reference, 5V	0.05% Max, 5ppm/°C Drift
LT1460	Micropower Series Reference	0.075% Max, 10ppm/°C Max Drift, 2.5V, 5V and 10V Versions
LTC2401/LTC2402	1-/2-Channel 24-Bits ADCs	3µV Noise, 10-Pin MSOP Package, Ground Sensing
LTC2404/LTC2408	4-/8-Channel 24-Bit ADCs	Same Performance as LTC2400
LTC2420	20-Bit Micropower ADC	6µV Noise, Pin-Compatible with LTC2400

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